

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### General Description

DA7281 is a linear resonant actuator (LRA) and eccentric rotating mass (ERM) haptic driver offering automatic closed-loop LRA resonant frequency tracking. The feature guarantees consistency across LRA production tolerances, operating temperature, aging, and mechanical coupling. DA7281 offers wideband operation that fully utilizes the capabilities of newer wideband and multi-directional LRAs.

The differential output drive architecture and continuous actuator motion sensing enable efficient, calibration-free playback and minimize software complexity. Featuring wake-up on General Purpose Input (GPI) sequence trigger and/or I<sup>2</sup>C activity, DA7281 automatically returns to a low quiescent current state (typically 0.36  $\mu$ A) between playbacks. At only 20 % of the idle current of the nearest alternative solution, DA7281 significantly extends battery life in mobile systems.

To reduce system complexity, an integrated Waveform Memory allows haptic sequences to be pre-loaded to DA7281. Independent sequences can be triggered, with low-latency (0.75 ms), by the GPI pin without host interaction. Haptic sequences can also be streamed to DA7281 from an external source via I<sup>2</sup>C or pulse width modulated (PWM) signal.

DA7281 actively monitors the back electromotive force (BEMF) while continuously driving and applies closed-loop Active Acceleration and Rapid Stopping for sharper clicks and a higher fidelity user experience. This offers significant advantages over existing solutions that need to move into a high-impedance state during drive to measure the BEMF, which adds a considerable amount of inactive time to the sequence and lowers the effective click strength for a given LRA.

### Key Features

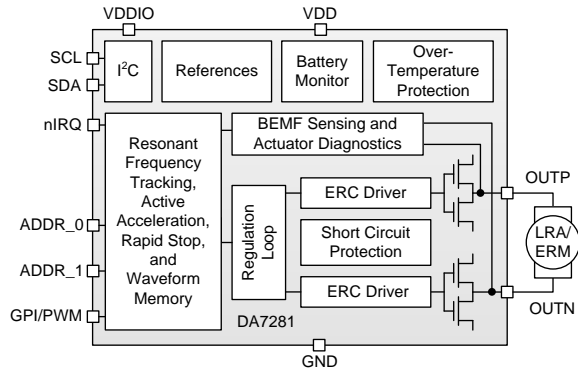
- LRA or ERM drive capability
- Automatic LRA resonant frequency tracking
- Wideband LRA support
- I<sup>2</sup>C and PWM input streaming
- Low latency (0.75 ms) I<sup>2</sup>C/GPI wake-up from low power consumption IDLE state,  $I_Q = 0.36 \mu\text{A}$
- Ultra-low latency (0.15 ms) wake-up from STANDBY state,  $I_Q = 0.8 \text{ mA}$
- GPI pin for triggering of up to two independent haptic sequences
- On-board Waveform Memory with amplitude, time, and frequency control
- Active Acceleration and Rapid Stop technology for high-fidelity haptic feedback
- Actuator diagnostics and fault handling
- Up to four I<sup>2</sup>C addresses via two address pins
- No software requirements with embedded operation
- Differential PWM output drive
- Current driven system to deliver constant actuator power
- Configurable EMI suppression
- Automatic short circuit protection
- Ultra-low power consumption,  $I_Q = 0.36 \mu\text{A}$ , with state retention in IDLE state
- Supply monitoring, reporting, and automatic output limiting
- Open- and closed-loop modes
- Custom wave drive support
- Small solution footprint requiring only one decoupling capacitor in both WLCSP and QFN

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### Applications

- Smartphones, wearables, and hearables
- Computer peripherals
- Gaming
- Automotive and industrial
- Virtual and augmented reality controllers



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### System Diagrams

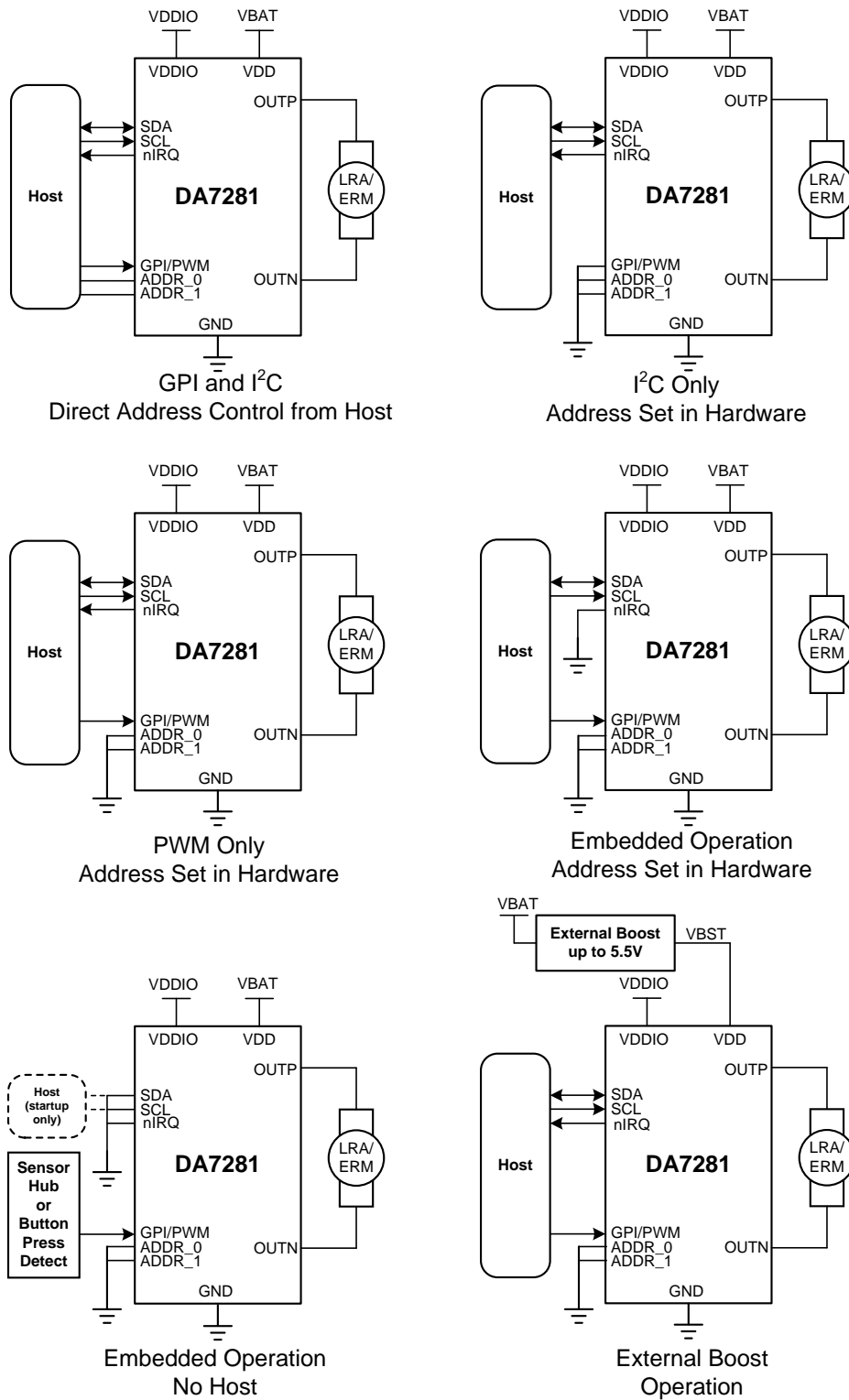


Figure 1: System Diagrams

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C  
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## Legal

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## Product Family

**Table 1: DA728x Feature Comparison**

Feature	DA7280	DA7281	DA7282	DA7283
OFF state via EN pin	No	No	Yes	Yes
OFF state current	N/A	N/A	5 nA	5 nA
IDLE state current	360 nA	360 nA	680 nA	680 nA
Number of GPI sequence trigger pins	3	1	3	3
I <sup>2</sup> C interface	Yes	Yes	Yes	No
Multiple I <sup>2</sup> C addressing	No	Yes	No	N/A
Operation without a host	No	No	No	Yes

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**
**1 Terms and Definitions**

BEMF	Back electromotive force
CDM	Charged device model
DMA	Dual mode actuator
DRO	Direct register override
EMI	Electromagnetic interference
ERC	Edge rate control
ERM	Eccentric rotating mass
ESD	Electrostatic discharge
ETWM	Edge triggered Waveform Memory
FET	Field-effect transistor
GND	Ground
GPI	General purpose input
Half-period	One half of the LRA resonant frequency period. For example, if $f_{LRA} = 200$ Hz, one half-period is 2.5 ms.
HBM	Human body model
IRQs	Interrupt requests
LRA	Linear resonant actuator
OTP	One time programmable
PCB	Printed circuit board
PID	Proportional-Integral-Derivative
PoR	Power-on reset
PWL	Piecewise linear
PWM	Pulse width modulated
QFN	Quad flat no leads
RC	Resistor-capacitor
RTWM	Register triggered Waveform Memory
WLCSP	Wafer level chip scale package



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### 2 Block Diagram

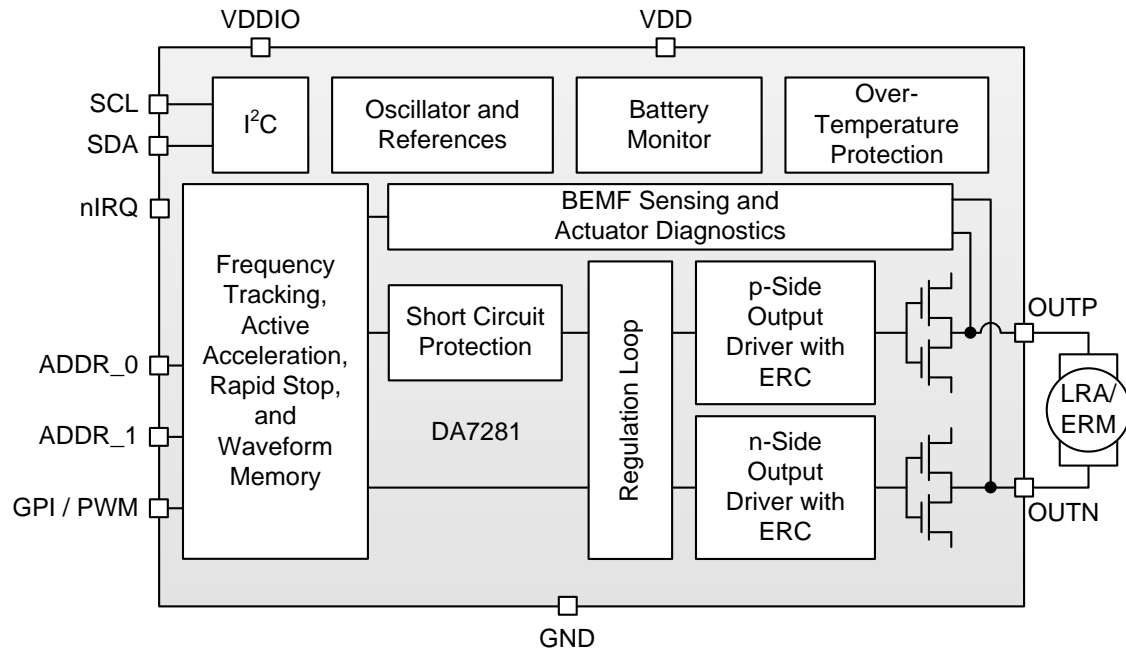


Figure 2: DA7281 Block Diagram

# DA7281

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 3 Pinout

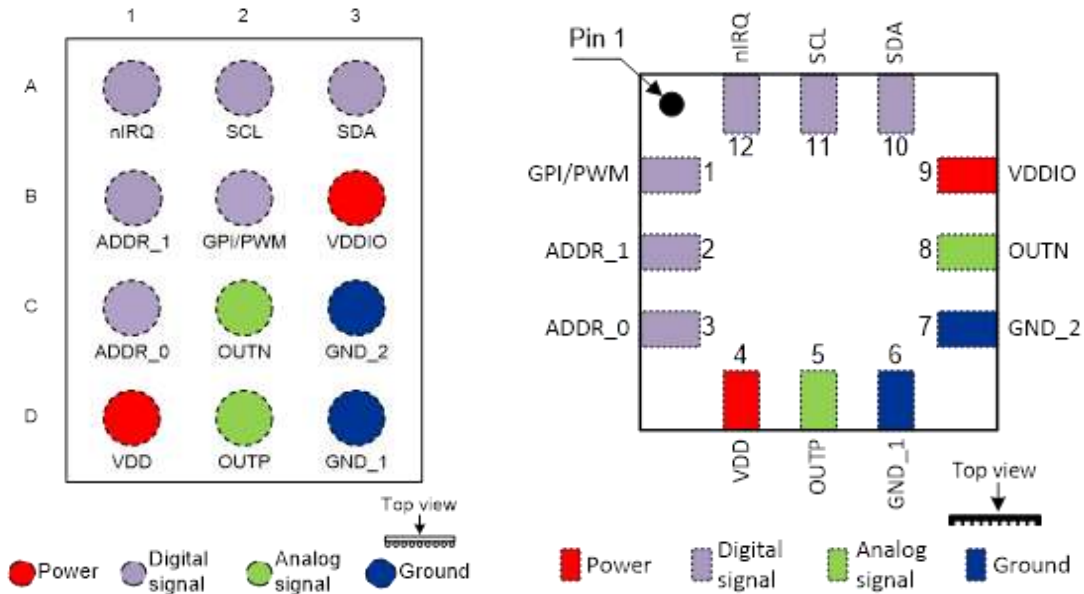


Figure 3: DA7281 Pinout Diagrams (Top View) for WLCSP (Left) and QFN (Right)

Table 2: Pin Description

Pin No. WLCSP	Pin No. QFN	Pin Name	Type (Table 3)	Description
A1	12	nIRQ	DO	Interrupt request line to host, open-drain, active low, connect to VDDIO via external pull-up resistor
A2	11	SCL	DI	I <sup>2</sup> C clock input
A3	10	SDA	DIO	I <sup>2</sup> C data input/output, open-drain, connect to VDDIO via external pull-up resistor
B1	2	ADDR_1	DI	I <sup>2</sup> C address 1
B2	1	GPI/PWM	DI	GPI sequence trigger, or PWM input
B3	9	VDDIO	PWR	Supply for digital I/O interfaces
C1	3	ADDR_0	DI	I <sup>2</sup> C address 0
C2	8	OUTN	AO	Haptic driver negative output
C3	7	GND_2	GND	Ground
D1	4	VDD	PWR	Haptics power supply; decouple to GND_1
D2	5	OUTP	AO	Haptic driver positive output
D3	6	GND_1	GND	Ground

Table 3: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AO	Analog output

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Pin Type	Description	Pin Type	Description
DO	Digital output	PWR	Power
DIO	Digital input/output	GND	Ground

## 4 Characteristics

### 4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 4: Absolute Maximum Ratings**

Parameter	Description	Conditions	Min	Max	Unit
V <sub>DD</sub>	Haptic power supply (battery or regulated rail)	Referenced to GND	-0.3	6	V
V <sub>DDIO</sub>	Digital IO supply		-0.3	6	V
V <sub>OUTN</sub>	Haptic driver negative output		-0.3	6	V
V <sub>OUTP</sub>	Haptic driver positive output		-0.3	6	V
V <sub>nIRQ</sub>	Interrupt request line to host		-0.3	6	V
V <sub>SCL</sub>	I <sup>2</sup> C clock input		-0.3	6	V
V <sub>SDA</sub>	I <sup>2</sup> C data input/output		-0.3	6	V
V <sub>GPI</sub>	General purpose input		-0.3	6	V
V <sub>ADDR_x</sub>	I <sup>2</sup> C address pins		-0.3	6	V
T <sub>A</sub>	Operating ambient temperature		-40	85	°C
T <sub>J</sub>	Operating junction temperature		-40	125	°C
T <sub>STG</sub>	Storage temperature		-65	150	°C
ESD <sub>HBM</sub>	ESD protection	Human Body Model (HBM) All non-exposed pins	4		kV
ESD <sub>CDM</sub>	ESD protection	Charged Device Model (CDM)	1		kV

### 4.2 Recommended Operating Conditions

Unless otherwise noted, the parameters listed in [Table 5](#) are valid for T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.8 V, and V<sub>DDIO</sub> = 1.8 V.

**Table 5: Recommended Operating Conditions**

Parameter	Description	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	Haptic power supply (battery or regulated rail)		2.8	3.8	5.5	V

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Parameter	Description	Conditions	Min	Typ	Max	Unit
V <sub>DDIO</sub>	Digital IO supply (Note 1)		1.35	1.8	5.5	V
Z <sub>LD</sub>	Nominal LRA DC impedance		4		50	Ω
C <sub>LD</sub>	Capacitance to ground on OUTP and OUTN				1	nF
f <sub>LRA</sub>	Nominal LRA resonant frequency	Frequency tracking enabled	50		300	Hz
f <sub>LRA_OL</sub>	Nominal LRA resonant frequency, open-loop	Frequency tracking disabled	25		100 0	Hz

**Note 1** During device operation V<sub>DDIO</sub> must be ≤ V<sub>DD</sub> if ADDR\_0, ADDR\_1, and GPI are not grounded.

### 4.3 Electrical Characteristics

Unless otherwise noted, the parameters listed in Table 6 and Table 7 are valid for T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.8 V, and V<sub>DDIO</sub> = 1.8 V.

**Table 6: Current Consumption**

Parameter	Description	Conditions	Min	Typ	Max	Unit
I <sub>Q_IDLE</sub>	System VDD current in IDLE state	System waiting for playback request		0.36	1	μA
I <sub>Q_VDDIO</sub>	VDDIO pin current	No I/O or nIRQ activity		0.13	0.5	μA
I <sub>Q_STANDBY</sub>	System VDD current in STANDBY state	System waiting for playback request		0.8	1	mA
I <sub>Q_NO_LD</sub>	System VDD current with no load	High-impedance load > 10 MΩ, H-bridge switching		1.35	1.5	mA

**Table 7: Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
I <sub>SHRT</sub>	Short circuit protection threshold	Short to GND or VDD	400	500	600	mA
I <sub>OUT_MAX</sub>	Maximum drive current			250	500 (Note 1)	mA
f <sub>TRCK_LRA</sub>	LRA frequency tracking range	Automatic tracking limits	50		300 (Note 2)	Hz
f <sub>TRCK_ACC_LRA</sub>	LRA frequency tracking accuracy	Frequency tracking accuracy during playback		0.5		Hz
f <sub>WIDEBAND</sub>	Wideband frequency range	User defined drive frequency	25		1000	Hz
f <sub>OUT_PWM</sub>	PWM output frequency	Differential OUTP and OUTN switching frequency	183	187.5	192	kHz
ERC	Programming range of output switching pins edge rate control	OUTP and OUTN slope	25	100	100	mV/ns

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

Parameter	Description	Conditions	Min	Typ	Max	Unit
f <sub>IN_PWM</sub>	PWM data input frequency		10		250	kHz
R <sub>D<sub>S</sub>_ON</sub>	H-bridge drain to source resistance when on	High side plus low side FETs		2		Ω
Z <sub>FLT_UZ</sub>	Actuator under-impedance threshold	Not applicable for coin ERM		4		Ω
Z <sub>FTL_OZ</sub>	Over-impedance threshold	Not applicable for coin ERM		50		Ω
Z <sub>OUT_OFF</sub>	Output impedance when H-bridge not switching	Pull-down enabled		15		kΩ
V <sub>DD_POR_FALL</sub>	V <sub>DD</sub> Power-on-Reset (PoR) falling threshold		2.4	2.55	2.7	V

**Note 1** For operation up to 500 mA (instead of 250 mA), see Section 5.7.12.

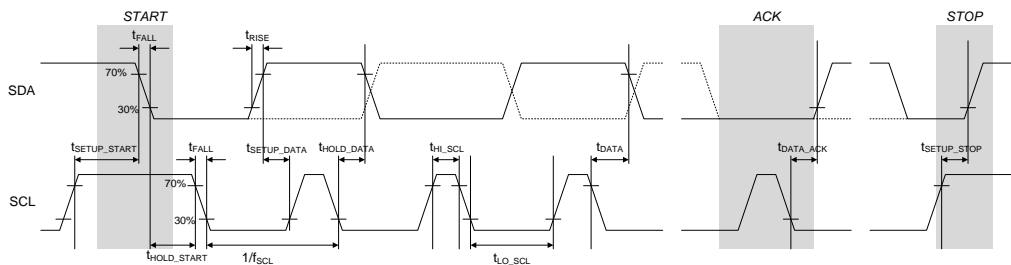
**Note 2** For operation outside this range, see Section 5.7.1.

**4.4 Timing Characteristics**

Unless otherwise noted, the parameters listed in Table 8 are valid for T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.8 V, and V<sub>DDIO</sub> = 1.8 V.

**Table 8: Timing Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
t <sub>ON</sub>	Cold boot to IDLE state time	V <sub>DD</sub> present and PoR released		1.2	1.5	ms
t <sub>OUT_IDLE</sub>	Time to output from IDLE state	From GPI or I <sup>2</sup> C trigger to output drive		0.75		ms
t <sub>OUT_STANDBY</sub>	Time to output from STANDBY state	From GPI or I <sup>2</sup> C trigger to output drive		0.15		ms



**Figure 4: I<sup>2</sup>C Interface Timing**

**Table 9: I<sup>2</sup>C Interface Timing Requirements**

Parameter	Description	Conditions	Min	Max	Unit
t <sub>BUF</sub>	Bus free time from STOP to START condition		0.5		μs
<b>Standard, Fast, and Fast-Plus Modes</b>					
C <sub>BUS</sub>	Bus line capacitive load			520	pF

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Parameter	Description	Conditions	Min	Max	Unit
f <sub>SCL</sub>	SCL clock frequency		0	1000 (Note 1)	kHz
t <sub>SETUP_START</sub>	Start condition setup time		0.26		μs
t <sub>HOLD_START</sub>	Start condition hold time		0.26		μs
t <sub>LO_SCL</sub>	SCL low time		0.5		μs
t <sub>HI_SCL</sub>	SCL high time		0.26		μs
t <sub>RISE</sub>	SCL and SDA rise time			120	ns
t <sub>FALL</sub>	SCL and SDA fall time			120	ns
t <sub>SETUP_DATA</sub>	Data setup time		50		ns
t <sub>HOLD_DATA</sub>	Data hold-time		0		ns
t <sub>SETUP_STOP</sub>	Stop condition setup time		0.26		μs
t <sub>DATA</sub>	Data valid time			0.45	μs
t <sub>DATA_ACK</sub>	Data valid acknowledge time			0.45	μs
t <sub>SPIKE</sub>	Spike suppression (SCL, SDA)	Fast/Fast+ mode		50	ns

**Note 1** f<sub>SCL</sub> maximum is 400 kHz at V<sub>DDIO</sub> ≤ 1.65 V and 1000 kHz at V<sub>DDIO</sub> > 1.65 V.

### 4.5 Thermal Characteristics

**Table 10: WLCSP Thermal Ratings**

Parameter	Description (Note 1)	Min	Typ	Max	Unit
R <sub>θJA</sub>	Junction-to-ambient thermal resistance		90.3		°C/W
R <sub>θJC_TOP</sub>	Junction-to-case (top) thermal resistance		43.6		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		49.0		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		6.4		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		45.8		°C/W

**Note 1** Multilayer JEDEC standard, still air, ambient temperature 25 °C, simulated value.

**Table 11: QFN Thermal Ratings**

Parameter	Description (Note 1)	Min	Typ	Max	Unit
R <sub>θJA</sub>	Junction-to-ambient thermal resistance		88.2		°C/W
R <sub>θJC_TOP</sub>	Junction-to-case (top) thermal resistance		54.6		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		39.3		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		3.4		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		50.0		°C/W

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**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C  
Addresses, Integrated Waveform Memory, and  
Wideband Support**

Parameter	Description (Note 1)	Min	Typ	Max	Unit
R <sub>θJC_BOTTOM</sub>	Junction-to-case (bottom) thermal resistance		4.4		°C/W

**Note 1** Multilayer JEDEC standard, still air, ambient temperature 25 °C, simulated value.

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 5 Functional Description

DA7281 is a haptic driver capable of driving both LRA and ERM actuators. The power-optimized architecture and advanced closed-loop digital algorithms achieve a very high-fidelity haptic drive. It features two I<sup>2</sup>C address pins, frequency control within an onboard Waveform Memory and a GPI input, for triggering up to two distinct sequences. This helps with emulating button pressing in many applications including gaming, mobile, and wearable devices.

The device controls the level of drive across the load and senses the movement of the actuator. The driven waveform is generated by a current regulated loop using a high-frequency PWM modulation. The differential output drive features a switching regulator architecture with H-bridge differential drive across the load at a frequency of 187.5 kHz. The drive level is based on the sequence from the data source selected by I<sup>2</sup>C interface, input PWM signal, or Waveform Memory.

DA7281 is capable of closed-loop actuator monitoring while driving to enable calibration-free playback, frequency tracking (LRA only), Active Acceleration, Rapid Stop, and actuator diagnostics.

Continuous resonant frequency tracking can be enabled while driving an LRA to track the mechanical resonance of the actuator through closed-loop control. This maximizes electrical to mechanical energy conversion efficiency for narrowband actuators and is especially useful in applications such as operating system notifications and alarms.

Resonant frequency tracking can be disabled to operate DA7281 in open-loop wideband frequency operation while driving LRAs with a wider bandwidth frequency response.

Active Acceleration and Rapid Stop features enable automated driving of both ERM and LRA loads (when frequency tracking is enabled). This reduces the time to reach the target acceleration level and the time for the actuator to come to a complete stop.

#### 5.1 Features Description

##### Driving LRA and ERM Actuators

DA7281 can drive both ERMs and LRAs depending on the register configuration, see Section 5.6.2.

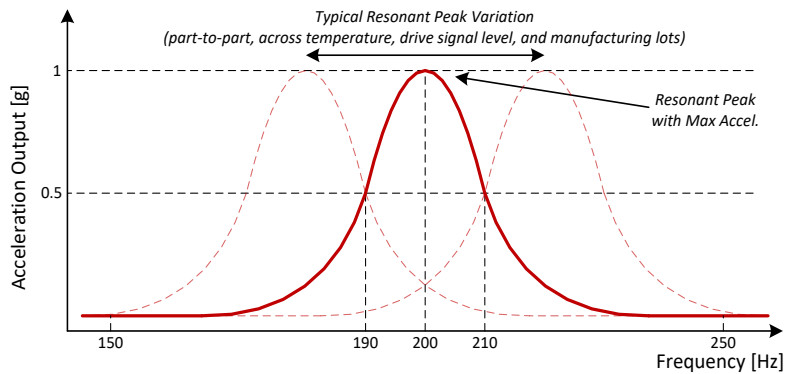
##### Automatic LRA Resonant Frequency Tracking

LRA resonant frequency shifts over time due to changing operating conditions, such as temperature or position, and manufacturing spread. LRAs are high-Q systems; if driven at a fixed frequency, the consequences are loss of electrical to mechanical energy conversion efficiency, weaker than nominal actuator acceleration output, and significant part-to-part variation in the end-product haptic feel.

Figure 5 illustrates that if the drive frequency is fixed, for example at 200 Hz, frequency variation in the resonant peak of only 10 Hz can result in a loss of 50 % of the output acceleration.



**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

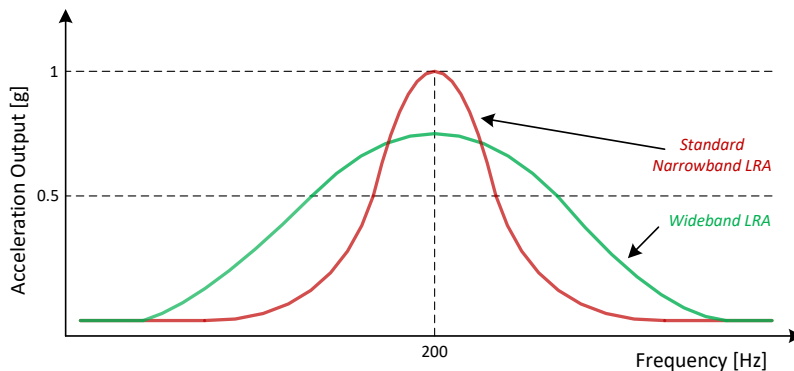


**Figure 5: LRA Output Acceleration Swept in Frequency with Constant Power Input Signal**

For a consistent user experience, DA7281 automatically locks onto and tracks the resonant frequency of the LRA through active BEMF sensing and closed-loop digital control. This ensures optimal output acceleration on every individual LRA throughout its lifetime and consistent part-to-part haptic feedback in the end product, see Section 5.3.

**Wideband LRA Support**

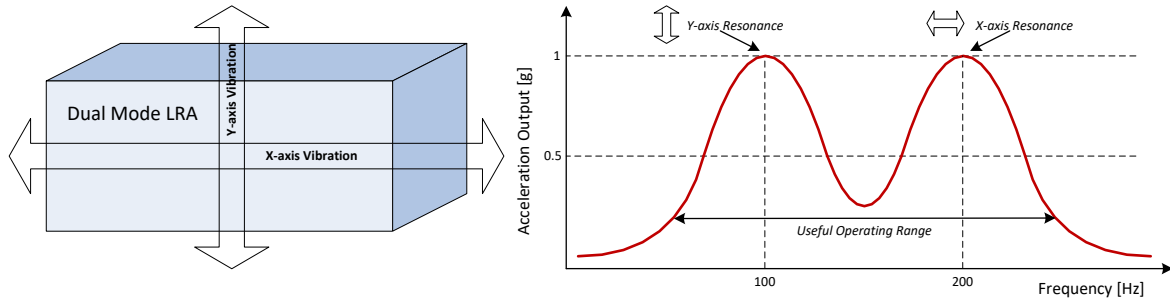
Wideband LRAs respond across a frequency range typically several times wider than narrowband ones, as demonstrated in Figure 6, and can be used in combination with DA7281 to create richer haptic feedback experience by utilizing the increased vibrational frequency range, see Section 5.5.



**Figure 6: Narrowband and Wideband LRA Response across Frequency**

Dual mode actuators (DMA) consist of two modes of vibration in different axes around different resonance points, depending on actuator construction. The two resonant points, wide response frequency, and different direction of vibration allow immersive gaming experience with multiple unique feedback effects. Figure 8 shows a typical DMA response, vibration in the y-axis occurs if the DMA is driven at 100 Hz and vibration in the x-axis occurs if the DMA is driven at 200 Hz.

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support



**Figure 7: Dual Mode LRA Response across Frequency**

The ability of DA7281 to control the frequency (25 Hz to 1000 Hz) and amplitude of the drive over time as well as the type of output wave allows the use of wideband sequences fully utilizing the capabilities of wideband and dual mode actuators for creating a richer user experience, see Section 5.7.5. Example use cases in DMAs are excitation of both resonant peaks simultaneously for maximum perceptible vibration or distinct single-frequency event-signaling clicks at different resonant frequencies and physical directions. Both DMAs and wideband LRAs can also be used to augment user audio experience by playing audio-derived haptic sequences over their useful frequency operating range.

DA7281 supports all of the above use cases and drives wideband LRAs via I<sup>2</sup>C or wideband Waveform Memory sequences triggered by I<sup>2</sup>C or GPI. The output drive can be configured as either square wave, sine wave, or custom wave to create different end effects, see Section 5.7.6.

Usually, LRA resonant frequency tracking is disabled during wideband operation. However, it can be enabled to either locate the resonant peak of wideband actuators, or to operate at a selected DMA resonance point and achieve the maximum possible actuator acceleration for a set input power, see Section 5.3 and Section 5.7.1.

### I<sup>2</sup>C and PWM Input Streaming

Haptic playback data can be streamed externally either via I<sup>2</sup>C direct register override or from a PWM data source, see Section 5.2.2. The external input data PWM frequency is independent of the output PWM signal frequency driven to the actuator. The input PWM signal is low-pass filtered to create a varying DC level that is the envelope for the drive across the actuator.

### Up to Four I<sup>2</sup>C Addresses via Two Address Pins

DA7281 has two dedicated address pins for setting the I<sup>2</sup>C base address. This allows up to four devices to work with the same I<sup>2</sup>C master by having different tie high and tie low settings on the pins. The I<sup>2</sup>C base address is also visible, which allows even more devices to be instantiated if the address pins are dynamically controlled, see Section 5.10.

### Low Latency I<sup>2</sup>C/GPI Wake-Up from IDLE State

The device supports low latency (0.75 ms) wake-up from IDLE state, which is the lowest power state (typically 0.36  $\mu$ A from  $V_{DD}$ ). Wake-up is triggered by either GPI or I<sup>2</sup>C activity. I<sup>2</sup>C is fully functional in all modes including IDLE state and DA7281 retains register settings in all modes, see Section 5.2.1.

### GPI Sequence Trigger for up to Two Independent Haptic Responses

The GPI input of DA7281 is used to trigger low-latency playback of up to two distinct sequences from IDLE state, see Section 5.2.7. Triggering is activated on events caused by rising or falling edges, or

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

both. The sequence playback is configurable with odd events trigger one sequence, and even events another.

### On-Board Waveform Memory with Amplitude, Time, and Frequency Control

DA7281 contains 100 bytes of highly optimized on-board Waveform Memory for user programmable haptic sequences, see Section 5.8. The Dialog Semiconductor specific format allows control of not only amplitude and time, but also frequency during the playback of a haptic sequence. This is specifically intended for use with wideband and dual mode actuators to create a richer user experience.

### Active Acceleration and Rapid Stop for High-Fidelity Haptic Feedback

By measuring and responding to the BEMF of the actuator, DA7281 supports Active Acceleration which improves actuator response both when increasing and decreasing drive amplitude by overdriving or underdriving relative to the desired drive level. Similarly, Rapid Stop minimizes the time needed for the actuator to come to a complete stop by driving against the direction of actuator movement. These two features enable a high-fidelity haptic response of the actuator and improve on its inherent physical performance and mechanical time constant, see Section 5.4.

### Continuous Actuator Diagnostics and Fault Handling

DA7281 monitors the actuator impedance at the start of each haptic sequence. The value of the impedance can be read back from a dedicated register, see Section 5.7.3. In addition, impedance, BEMF, and resonant frequency faults are flagged with automatic shutdown and notification via the nIRQ pin, see Section 5.6.6.

### No Software Requirements with Embedded Operation

The device can function in a stand-alone embedded operation where no host action is needed to clear generated faults and the device will attempt to drive on each request. This also allows operation in GPI trigger mode without the need for a host device or host communication, see Section 5.7.7. Note that initial download of sequences to the device is still required. Once loaded, the Waveform Memory is retained in all states as long as the supply does not drop below the PoR threshold.

### Differential Output Drive

DA7281 includes a full H-bridge differential output PWM drive that has the advantage of maximizing the power delivered to the LRA from a given supply and allows braking of DC motors by reversing voltage polarity. This doubles the voltage swing across the actuator and significantly increases system efficiency relative to a single transistor/LDO solution in legacy ERM or LRA applications.

### Current Driven System

The device outputs regulated current, rather than voltage, which allows BEMF tracking without the need to stop driving to sense the BEMF. This maximizes power delivery to the actuator per unit time when compared to voltage driven solutions, resulting in shorter and sharper haptic clicks. In addition, constant current drive provides constant force into an actuator independently of the BEMF amplitude.

### Configurable EMI Suppression

Switching node edge rate control (ERC) on the OUTP and OUTN pins reduces electromagnetic interference (EMI) and electrical interference via capacitive coupling in the end application, see Section 5.7.11. This eliminates any need for resistor-capacitor (RC) or ferrite bead filtering of the outputs, which offers a lower-cost bill of materials when using DA7281. Programmability of the ERC

## DA7281

### LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

also gives DA7281 a distinct advantage over competing solutions as it helps fine-tune a system without any PCB modifications.

#### Automatic Short Circuit Protection

Automatic low-latency short circuit protection detects shorts on the OOTP and OUTN pins to supply, ground, or between OOTP and OUTN, and protects DA7281 by forcing the H-bridge into a high-impedance state, see Section 5.6.6.

#### Ultra-Low Power Consumption with State Retention

In IDLE state, DA7281 has an ultra-low current consumption from the power supply at typically 0.36  $\mu$ A with a time to output of 0.75 ms. DA7281 returns automatically to IDLE after completing playback, keeps its internal state, and is available for I<sup>2</sup>C communications, see Section 5.2.1.

#### Ultra-Low Latency in STANDBY State

In STANDBY state, the time to output is 0.15 ms with current consumption of typically 0.8 mA, see Section 5.2.1.

#### Supply Monitoring, Reporting, and Automatic Output Limiting

DA7281 monitors the power supply voltage level and adjusts the drive voltage accordingly, so that the output does not clip to the supply voltage. This feature guarantees controlled output allowing continued resonant frequency tracking and Active Acceleration/Rapid Stop functionality even when the device is operating under low power supply conditions or heavy battery load. Supply voltage can be read back by the host from a dedicated register, see Section 5.7.13.

#### Open- and Closed-Loop Modes

DA7281 can be configured in either open- or closed-loop mode. In open-loop mode any actuator BEMF monitoring is disabled and the device works as a simple current based drive without any auto-adjustment on the drive period or amplitude. This is useful in wideband LRA playback. In closed-loop mode, the user can optionally turn on the frequency tracking, Active Acceleration, Rapid Stop, and amplitude control features, see Section 5.7.5 and Section 5.7.6.

#### Open-Loop Sine/Custom Wave Drive Support

In open-loop operation DA7281 can be configured to drive the actuator with a non-square wave signal. This improves the electrical efficiency, reduces audibility in some actuators, and allows simultaneous drive of multiple resonant points in DMAs. The exact shape of the output waveform can be configured via dedicated registers with the default set to a sine wave, see Section 5.7.6.

#### Small Solution Footprint

Available in an ultra-small 1.35 mm x 1.75 mm, 0.4 mm pitch, 0.545 mm height, 3 x 4 WLCSP, or a 3.0 mm x 3.0 mm, 0.65 mm pitch, 0.78 mm height, 12 lead QFN package, DA7281 minimizes the required PCB size and overall solution cost. In the typical application case, only a single 100 nF decoupling capacitor is required. See Section 9 and Section 10.

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### Additional Features

DA7281 also features:

- A temperature and supply stable ( $\pm 1.5\%$ ) internal oscillator which guarantees consistent haptic playback in the frequency domain over a wide range of operating conditions.
- Automatic over-temperature warning and shutdown capability.
- Low pad leakage current (typ.  $< 50\text{ nA}$ , for all pads combined).
- Low idle current from VDDIO (typ.  $130\text{ nA}$  at  $1.8\text{ V}$ ).
- I<sup>2</sup>C operation down to  $V_{\text{DDIO}} = 1.35\text{ V}$ .
- Output PWM frequency, at  $187.5\text{ kHz}$ , is  $167.5\text{ kHz}$  away from the audio band and at a non-audio sample rate multiple. This prevents audible fold back via supply disturbance common in near-audio-band switching haptic drivers.
- Easy to use Dialog **SmartCanvas™** GUI with a user tab for fast device setup without the need to directly interact with registers and an intuitive graphical environment for Waveform Memory editing and visualization.

## 5.2 Functional Modes

### 5.2.1 System States

DA7281 features IDLE and STANDBY states ensuring lowest power consumption and lowest start-up latency in different operating conditions. In addition, when any fault is detected, the device returns directly to the IDLE state. [Figure 8](#) shows the device states and the transitions into and out of each state.

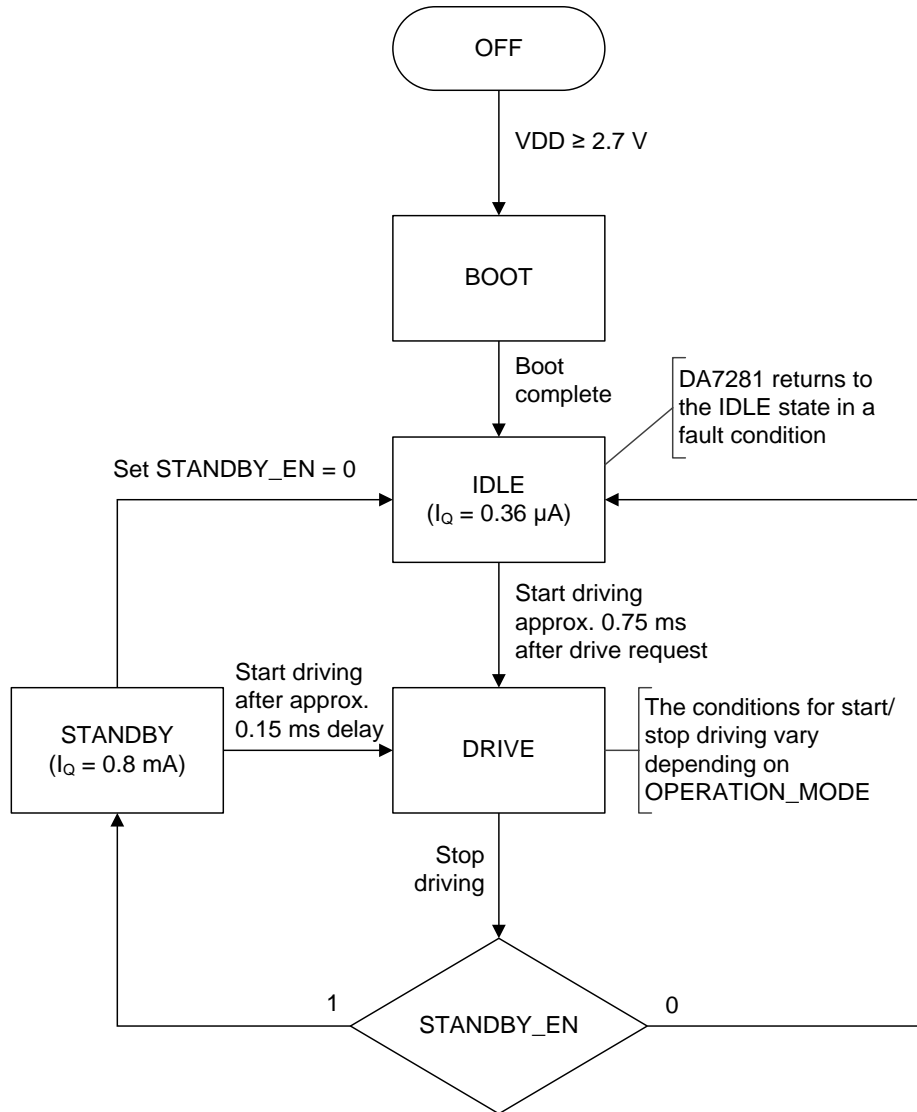
When a power supply is applied, DA7281 loads the register default settings. Once BOOT is complete, DA7281 remains in the IDLE state and awaits further I<sup>2</sup>C communication.

DA7281 enters the DRIVE state when playback of a haptic sequence begins. There are several different operating modes for playback, see [Section 5.2.2](#).

On completion of playback, DA7281 leaves DRIVE state and returns either to IDLE state (for low power consumption) or STANDBY state (for low latency-to-drive). This is configured using STANDBY\_EN.

If a fault condition occurs, DA7281 returns to the IDLE state, see [Section 5.6.6](#).

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**Figure 8: System State Diagram**

**5.2.2 Operating Modes**

DA7281 offers multiple operating modes for use in different applications and to minimize power consumption, see [Table 12](#).

**Table 12: Operating Modes**

Operating Mode	Description	OPERATION_MODE
Inactive	System waits in IDLE or STANDBY state based on STANDBY_EN setting	0
Direct register override (DRO)	Playback streaming via I <sup>2</sup> C; input written to OVERRIDE_VAL	1
Pulse width modulated (PWM)	Playback streaming from PWM data input source on pin GPI/PWM	2

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Operating Mode	Description	OPERATION_MODE
Register triggered waveform memory (RTWM)	Playback from Waveform Memory triggered only by I <sup>2</sup> C write to SEQ_START	3
Edge triggered waveform memory (ETWM)	Playback from Waveform Memory triggered by rising/falling edge on pin GPI/PWM or via I <sup>2</sup> C write to SEQ_START	4

### 5.2.3 Inactive Mode

DA7281 can be configured to automatically return to IDLE (for lower I<sub>Q</sub>) or STANDBY (for minimized latency) state after completion of playback, see Section 5.2.1. In both states the register contents are retained. DA7281 remains in Inactive mode until it receives a playback request via either the GPI/PWM pin or I<sup>2</sup>C (providing any faults in the fault registers have been cleared, see Section 5.6.6).

In the event of a fault the system will automatically return to the IDLE state, see Section 5.6.6.

### 5.2.4 Direct Register Override Mode

In DRO mode haptic sequences are streamed to DA7281 via I<sup>2</sup>C input. The drive level of the output is set via OVERRIDE\_VAL. For optimal start-up timing, update OVERRIDE\_VAL before setting OPERATION\_MODE = 1. OVERRIDE\_VAL is treated as a two's complement proportional value where:

If ACCELERATION\_EN = 1, the output drive level is equal to the value in OVERRIDE\_VAL multiplied by the voltage stored in ACTUATOR\_NOMMAX. OVERRIDE\_VAL is interpreted as a proportion between 0 % (0x00) and 100 % (0x7F). The range from 0xFF to 0x80 is not used, see Figure 30. If enabled, the automatic Active Acceleration and Rapid Stop features will take the output up to the voltage in ACTUATOR\_ABSMAX and/or reverse the drive level to be negative during level transitions, but in steady state the value will always scale to the voltage in ACTUATOR\_NOMMAX.

If ACCELERATION\_EN = 0, the output drive level is equal to the value in OVERRIDE\_VAL multiplied by the voltage stored in ACTUATOR\_ABSMAX. In this case OVERRIDE\_VAL is interpreted as a proportion between -100% (0x80) and 100% (0x7F), see Figure 31. When DA7281 is set up to drive an ERM, the negative value represents a change in drive voltage polarity, while for an LRA it represents a phase shift of 180° in the drive signal. Negative drive can be used to speed up output acceleration level changes without the use of the Active Acceleration and Rapid Stop. Note that in the ACCELERATION\_EN = 0 case Rapid Stop can still be enabled if an automatic stop to zero actuator acceleration is required.

**Note:** The output amplitude updates at twice the LRA frequency (when the differential voltage across the LRA crosses zero), therefore input changes more frequent than this are not required as sampling occurs only around a zero cross. Since the I<sup>2</sup>C is asynchronous to the output drive, updates to OVERRIDE\_VAL will have a one LRA half-period of uncertainty before propagating to the output. Synchronization of OVERRIDE\_VAL updates to the half period is possible via software by looking at the POLARITY register and updating the output drive level, see Section 5.7.8.

When driving a wideband LRA in DRO mode, resonant frequency tracking can be turned off. This enables wideband operation and two-dimensional effects using DMAs, see Sections 5.7.5 and 5.7.6.

During playback, if a value written to OVERRIDE\_VAL results in the output driving strength being maintained at 0 %, DA7281 will disable its output stage to save power. Drive is re-enabled automatically, with one LRA half-period delay, when a non-zero OVERRIDE\_VAL value I<sup>2</sup>C input is received.

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

**5.2.5 Pulse Width Modulation Mode**

PWM mode is used to stream haptic sequences to DA7281 via the GPI/PWM input pin where the output drive level is determined by the duty cycle of the PWM signal. For optimal start-up timing, the PWM input signal needs to be provided before setting OPERATION\_MODE = 2. The PWM duty cycle can be interpreted in two ways as follows:

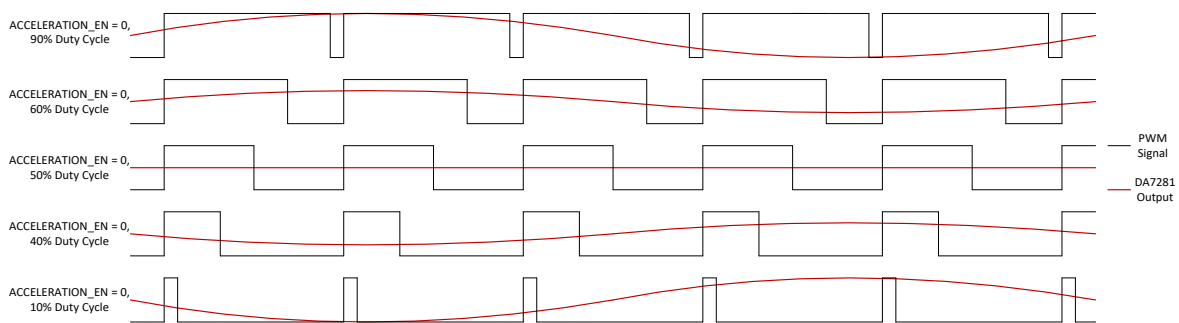
If ACCELERATION\_EN = 1, the output drive level is equal to the input signal duty cycle multiplied by the voltage stored in ACTUATOR\_NOMMAX. In this case the duty cycle is interpreted as a proportion between 0 % and 100 %, see Figure 30. The automatic Active Acceleration and Rapid Stop (if enabled) features will take the output up to the voltage in ACTUATOR\_ABSMAX and/or reverse the drive level to be negative during level transitions, but in steady state the final value will always scale to the voltage in ACTUATOR\_NOMMAX.

If ACCELERATION\_EN = 0, the output drive level is equal to the input signal duty cycle multiplied by the voltage stored in ACTUATOR\_ABSMAX. In this case the duty cycle is interpreted as a proportion between -100 % and 100 % where 50 % duty cycle is 0 %, see Figure 31. When DA7281 is set up to drive an ERM, the negative value represents a change in drive voltage polarity, while for an LRA it represents a phase shift of 180° in the drive signal. Negative drive can be used to speed up output acceleration level changes without the use of the Active Acceleration and Rapid Stop. Note that in the ACCELERATION\_EN = 0 case Rapid Stop can still be enabled if an automatic stop to zero actuator acceleration is required.

**Note:** The output PWM frequency is always independent of the PWM input frequency regardless of whether frequency tracking is enabled or disabled. To maximize accuracy and minimize power consumption and noise, it is best to keep the input PWM frequency as low as possible.

The PWM demodulator is rising edge sensitive. The minimum duty cycle that can be used to create the drive level can be configured in FULL\_BRAKE\_THR; any duty cycle below that value will produce a 0 % drive level.

During playback streaming in PWM mode, if a 0 % drive level is maintained by applying a 0 % (or 50 % if Active Acceleration is disabled) duty cycle PWM input, the DA7281 output stage is disabled to save power. Drive is re-enabled automatically, with one LRA half-period delay, when the duty cycle forces the drive level to be greater than 0 %.



**Figure 9: Example PWM Inputs with ACCELERATION\_EN = 0**

Note the 180° phase difference between driving > 50 % and < 50 %.

**5.2.6 Register Triggered Waveform Memory Mode**

If sequence consistency or I<sup>2</sup>C bus availability is a concern, register triggered waveform memory mode (RTWM) mode can be used to play back previously defined sequences from the Waveform Memory, see Section 5.8, via I<sup>2</sup>C register trigger only. Enter this mode by setting OPERATION\_MODE = 3.



## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 5.2.6.1 I<sup>2</sup>C Triggering and Sequence Looping

Sequence selection is done via PS\_SEQ\_ID with the additional option to loop the sequence up to 16 times using PS\_SEQ\_LOOP. To trigger a sequence, set SEQ\_START = 1. Once a sequence completes, the event is reported by dropping the nIRQ pin low and signaling via SEQ\_DONE\_M.

To repeat a sequence immediately following completion of playback, set SEQ\_CONTINUE = 1.

### 5.2.7 Edge Triggered Waveform Memory Mode

If there is no host available, or for minimal host interaction, edge triggered waveform memory mode (ETWM) mode can be used to play back a previously defined sequences from the Waveform Memory, see Section 5.8, via external GPI edge trigger or also via I<sup>2</sup>C trigger, as in RTWM mode. The ETWM is also useful if deterministic timing is required without reliance on the I<sup>2</sup>C bus.

The GPI/PWM pin can be configured and will react according to the setting in GPI\_POLARITY as follows:

- Rising edge trigger, GPI\_POLARITY = 0: only a rising GPI edge creates an event that triggers a pre-programmed sequence.
- Falling edge trigger, GPI\_POLARITY = 1: only a falling GPI edge creates an event that triggers a pre-programmed sequence.
- Rising and falling edge trigger, GPI\_POLARITY = 2: both edges create events that trigger a pre-programmed sequence.

Any event received during playback from pin GPI/PWM after the initial GPI trigger event will result in a sequence stop.

- There are two ways of reacting to a GPI event based on GPI\_MODE:
- Single sequence, GPI\_MODE = 0: no matter how many times the GPI is triggered, it will play the sequence located at GPI\_SEQUENCE\_ID.
- Multi-sequence, GPI\_MODE = 1: odd GPI events trigger the sequence at GPI\_SEQUENCE\_ID, while even GPI events trigger the sequence located at the value of GPI\_SEQUENCE\_ID + 1 bit.

In ETWM mode, a maximum of two different sequences can be configured when multi-sequence mode is enabled. The desired haptic sequence for the GPI must be set by programming GPI\_SEQUENCE\_ID.

Once a sequence has finished playing, a signal is sent via the nIRQ pin and DA7281 automatically returns to IDLE state, assuming STANDBY\_EN = 0, to await the next trigger event.

Sequence looping operates in the same way as RTWM mode, see Section 5.2.6.1.

## 5.3 Resonant Frequency Tracking

LRAs are high-Q systems that have to be driven exactly at resonance to achieve maximum possible output acceleration. DA7281 supports continuous resonant frequency tracking via BEMF sensing during playback to achieve optimum LRA acceleration output across manufacturing spread, operating temperature range, external damping, and actuator aging.

When the FREQ\_TRACK\_EN is high, a digital resonant frequency tracking loop locks onto the LRA resonant frequency in real time by adjusting the drive period. This ensures that the actuator is always driven at the optimum frequency for the highest efficiency electrical to mechanical energy conversion. The loop range of 50 Hz to 300 Hz covers existing narrowband LRAs; typical resonant frequency lock accuracy is 0.5 Hz.

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

To increase absolute accuracy of the lock during playback, DA7281 supports automatic scaling of the frequency tracking controller gain. The feature is enabled via `FREQ_TRACKING_AUTO_ADJ` and becomes active after the device has achieved initial lock, see Section 5.7.1.

The resonant frequency tracking algorithm is designed to converge to the correct value from up to 25 % offset between the initial nominal datasheet value and the actual resonant frequency. This range is conservative in order to prevent unwanted behavior. A fault will trigger if the actuator resonant frequency is outside the 50 Hz to 300 Hz range. To block these two features, set `FREQ_TRACKING_FORCE_ON = 1`, see Section 5.7.1.

**5.4 Active Acceleration and Rapid Stop**

Mechanical systems such as LRAs and ERMs accelerate and decelerate exponentially and the time between transitions (for example from stopping of the drive signal to the actuator coming to a complete rest) can be perceptibly slow for the user. DA7281 features Active Acceleration and Rapid Stop to overcome this latency, which enables stronger clicks and a higher fidelity playback in both LRAs and ERMs. This capability offers a distinct advantage over legacy systems, which do not sense BEMF, because it allows the use of cheaper, slower response time actuators while keeping haptic effects crisp.

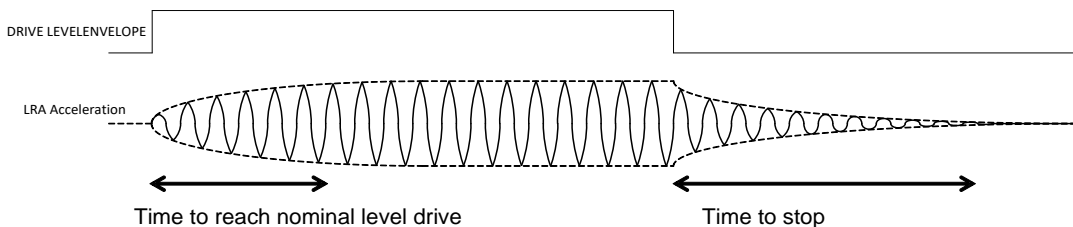
Active Acceleration employs relative drive architecture based on BEMF sensing, which enables temporary overdrive on all level changes reducing the time required to achieve a target drive level. The DA7281 Active Acceleration algorithm does not require dedicated calibration procedures and enables accurate overdrive and underdrive throughout the lifetime of an actuator. The feature removes the need for a separate calibration sequence to determine the correct overdrive duration, see Figure 10 and Figure 11.

Enabling Active Acceleration typically reduces the time to achieve the target drive level by a factor of two on sequence level changes. The Rapid Stop feature typically reduces the time to achieve a zero drive level by a factor of three when enabled. Figure 10 shows a drive sequence without the features enabled and Figure 11 illustrates the reduced time to target when Active Acceleration and Rapid Stop are enabled.

**Note:** The Active Acceleration and Rapid Stop features require frequency tracking to be enabled.

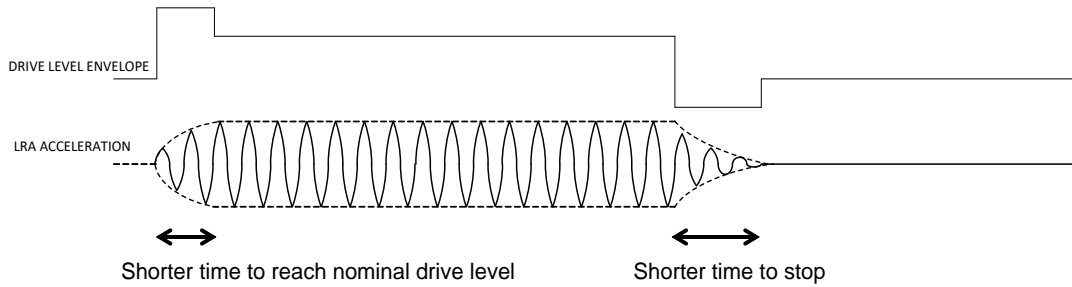
Figure 12 demonstrates the system with an actual LRA for an equivalent duration sequence without and with the Active Acceleration and Rapid Stop features. The nominal actuator acceleration is achieved faster and the stopping time is reduced by a factor of approximately eight.

Active Acceleration and Rapid Stop are enabled using `ACCELERATION_EN` and `RAPID_STOP_EN`.

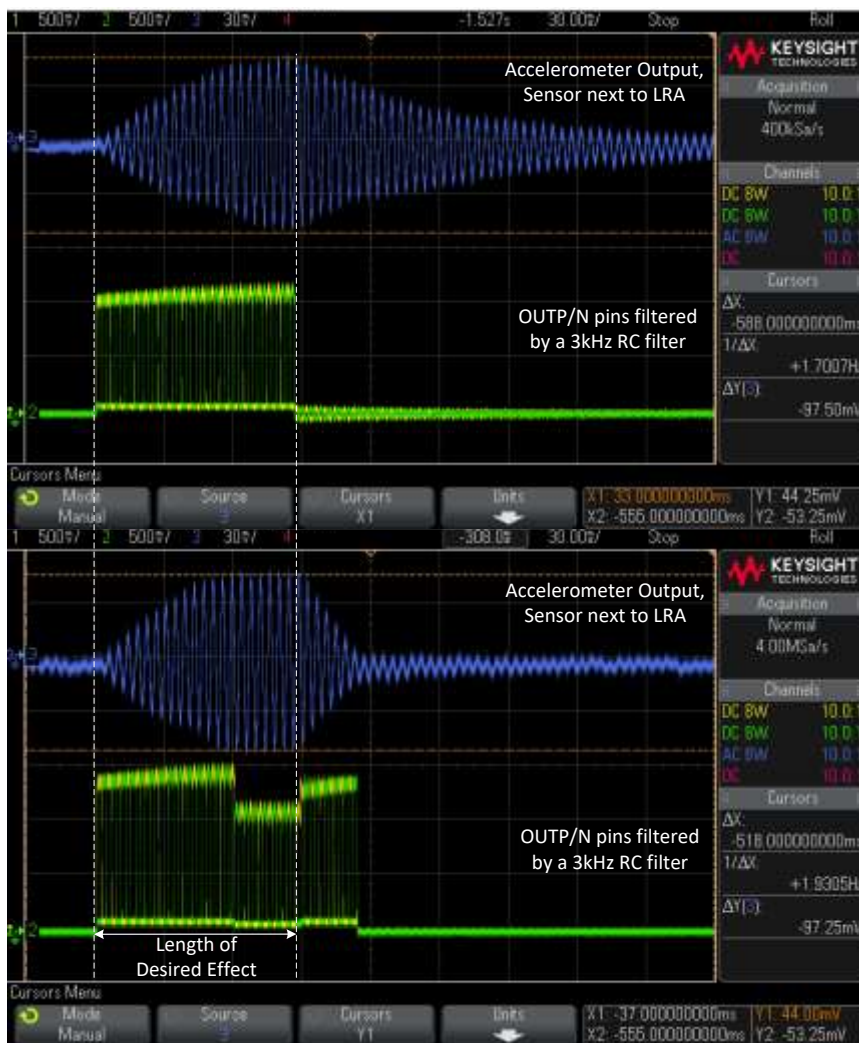


**Figure 10: LRA Single Step Drive without Acceleration and Rapid Stop**

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**



**Figure 11: LRA Single Step with Acceleration and Rapid Stop**



**Figure 12: Simple Drive (Top) versus Active Acceleration and Rapid Stop Enabled (Bottom)**

**5.5 Wideband Frequency Control**

DA7281 can be configured for wideband LRA support in DRO, RTWM, and ETWM modes. This allows an actuator to be driven outside of resonance to create a richer user experience. In this mode frequency tracking, Active Acceleration, and Rapid Stop features should be disabled. The accessible

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

frequency range becomes 25 Hz to 1000 Hz. After configuring the device, see Section 5.6, the following applies:

In DRO mode, streaming is as described in Section 5.2.4. To change output frequency, a new value is uploaded to LRA\_PER\_H and LRA\_PER\_L.

In RTWM or ETWM modes, the frequency information is encoded into the frames of a sequence, see Section 5.8.3. For information on sequence playback, see Section 5.6. If a repeatable frequency is required at the start of a sequence, the first frame of a sequence must contain frequency information.

### 5.6 Device Configuration and Playback

Minimal one-time setup is required to drive any given actuator. This consists of setting the chosen actuator type with its key parameters and selecting the drive mode. The Dialog [SmartCanvas](#) GUI automatically calculates the values required and sets the registers based on the entered actuator datasheet parameters. If the Dialog [SmartCanvas](#) GUI is not used, follow the steps outlined in this section.

#### 5.6.1 Boot

DA7281 comes out of reset when a power supply is provided to the device and boots for 1.5 ms. This is followed by entry to the Inactive mode where the device is kept in its lowest power state.

#### 5.6.2 Actuator Setup

The following setup procedure needs to be observed to program DA7281 to work with a specific actuator:

1. Choose the correct actuator type using ACTUATOR\_TYPE, 0 = LRA and 1 = ERM.
2. Choose the correct nominal maximum voltage across the actuator by checking the actuator datasheet for the maximum allowed RMS voltage and writing the value to ACTUATOR\_NOMMAX. The allowable range is between 0 V and 6 V in 23.4 mV steps. The ACTUATOR\_NOMMAX setting can be calculated using the following formula:

$$ACTUATOR\_NOMMAX[7:0] = \frac{V_{actuator\_nommax}}{23.4 \times 10^{-3}} \quad (1)$$

3. Choose the correct absolute maximum peak voltage across the actuator by checking the actuator datasheet and writing the value to ACTUATOR\_ABSMAX. The allowable range is between 0 V and 6 V in 23.4 mV steps. The ACTUATOR\_ABSMAX value can be calculated using the following formula:

$$ACTUATOR\_ABSMAX[7:0] = \frac{V_{actuator\_absmax}}{23.4 \times 10^{-3}} \quad (2)$$

4. Program the IMAX value (in units of mA) for the actuator using the following formula:

$$IMAX[4:0] = \frac{I_{max\_actuator\_mA} - 28.6}{7.2} \quad (3)$$

- where  $I_{max\_actuator\_mA}$  is the actuator max rated current in mA, as listed in its datasheet. Note that in general this should slightly exceed the ACTUATOR\_ABSMAX voltage divided by the actuator impedance.

5. Program the impedance of the actuator by checking the actuator datasheet and calculating the values for V2I\_FACTOR\_H and V2I\_FACTOR\_L using the following formulae:

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

$$V2I\_FACTOR[15:0] = \frac{Z \times (IMAX[4:0] + 4)}{1.6104} \quad (4)$$

$$V2I\_FACTOR\_H[7:0] = \frac{V2I\_FACTOR[15:0] - V2I\_FACTOR\_L[7:0]}{256} \quad (5)$$

$$V2I\_FACTOR\_L[7:0] = V2I\_FACTOR[15:0] - 256 \times V2I\_FACTOR\_H[7:0] \quad (6)$$

- Where V2I\_FACTOR[15:0] is the 16-bit concatenation of V2I\_FACTOR\_H[7:0] and V2I\_FACTOR\_L[7:0], Z is the impedance of the actuator in Ω (as read from its datasheet), and IMAX[4:0] is the 5-bit value of IMAX.

6. Program the LRA resonant frequency in terms of period by updating LRA\_PER\_H and LRA\_PER\_L based on the following formula:

$$LRA\_PER[14:0] = \frac{1}{LRA_{freq} \times 1333.32 \times 10^{-9}} \quad (7)$$

$$LRA\_PER\_H[7:0] = \frac{LRA\_PER[14:0] - LRA\_PER\_L[6:0]}{128} \quad (8)$$

$$LRA\_PER\_L[6:0] = LRA\_PER[14:0] - 128 \times LRA\_PER\_H[7:0] \quad (9)$$

- Where LRA<sub>req</sub> represents the LRA resonant frequency in Hz, as listed in the actuator datasheet.

**Note:** For ERM this value will signify the frequency of BEMF sensing; if more frequent updates are required, the value can be increased up to 300 Hz.

For driving coin ERMs, see Section 5.7.18.

### 5.6.3 Automatic Output Control

DA7281 has several automatic control loops and mechanisms to ensure excellent playback fidelity and easy actuator setup:

- Automatic frequency tracking - this feature allows resonant frequency tracking during playback and is enabled via `FREQ_TRACK_EN`. Frequency tracking must be enabled to use the Active Acceleration and Rapid Stop features. For fine-tuning the frequency tracking loop, see Section 5.7.1.
- Active Acceleration - this feature improves playback fidelity by overdriving and underdriving the actuator to allow faster transitions between acceleration levels. This improves on the inherent actuator mechanical time constant. To enable Active acceleration set `ACCELERATION_EN = 1`. Note that the input data is interpreted as either unsigned (`ACCELERATION_EN = 0`) or signed (`ACCELERATION_EN = 1`). For more detail on data formatting, see Section 5.9.
- Rapid Stop - this is a mechanism to allow the fastest possible stop to zero acceleration output for the actuator. DA7281 achieves this by driving in full reverse the actuator by applying a 180° phase shift in the case of an LRA or inverting the voltage across the actuator in the case of an ERM actuator. For fine-tuning the Rapid Stop feature, see Section 5.7.2.

### 5.6.4 Waveform Memory Setup

The Waveform Memory is initially empty. The user can create any set of haptic sequences by following the Waveform Memory format described in Section 5.8. For ease of use, the Dialog

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SmartCanvas GUI also provides a graphical tool to create sequences. The sequences can then be uploaded to the DA7281 Waveform Memory by going through the following steps:

1. Ensure that DA7281 is in Inactive mode (no playback ongoing and at least 1.5 ms have passed since cold boot).
2. Ensure the Waveform Memory is unlocked, set WAV\_MEM\_LOCK = 1.
3. Read back the location of SNP\_MEM\_0 by checking WAV\_MEM\_BASE\_ADDR.
4. Write the new contents of the Waveform Memory by starting from SNP\_MEM\_0.
5. If desired, re-lock the Waveform Memory, set WAV\_MEM\_LOCK = 0.

Once the DA7281 Waveform Memory is configured, it is retained until a power-on reset event. The host can update the Waveform Memory as many times as needed during the lifetime of the device.

### 5.6.5 Mode Configuration

Set OPERATION\_MODE according to the operating mode to be used. The device configuration flow is different for each operating mode. Sections 5.6.5.1 to 5.6.5.5 explain how to set up and operate the device in each of the operating modes.

#### 5.6.5.1 Inactive Mode

In Inactive mode, DA7281 waits in a low-power state in between playback events. For more details on power and latency trade-offs see Sections 5.2.1 and 5.2.3.

1. Set OPERATION\_MODE = 0 for DA7281 to go to Inactive mode.
2. Configure STANDBY\_EN to return to IDLE or STANDBY state after playback has finished.

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### 5.6.5.2 Direct Register Override (DRO) Mode

Figure 13 shows how to operate the device in DRO mode.

1. Starting from either the IDLE or STANDBY state, write the initial drive amplitude of the haptic sequence to `OVERRIDE_VAL`.
2. When ready to begin playback, set `OPERATION_MODE = 1`. The output will begin switching after approximately 0.75 ms.
3. While in the DRIVE state, write to `OVERRIDE_VAL` to drive a new amplitude and create the desired envelope of the haptic sequence. If `OVERRIDE_VAL = 0` during the DRIVE state, DA7281 will disable its output stage, but remain in a low latency-to-drive state and wait for further updates to `OVERRIDE_VAL`.
4. To stop driving set `OPERATION_MODE = 0`. DA7281 returns to either the IDLE or STANDBY state, depending on the value of `STANDBY_EN`.

**Note:** The allowable range of values written to `OVERRIDE_VAL` depends on whether `ACCELERATION_EN` is set to 1 or 0. If `ACCELERATION_EN = 1` then the usable range for `OVERRIDE_VAL` is 0x00 to 0x7F. If `ACCELERATION_EN = 0` then the usable range for `OVERRIDE_VAL` is 0x00 to 0xFF in two's complement. For further explanation, see Figure 30 and Figure 31.

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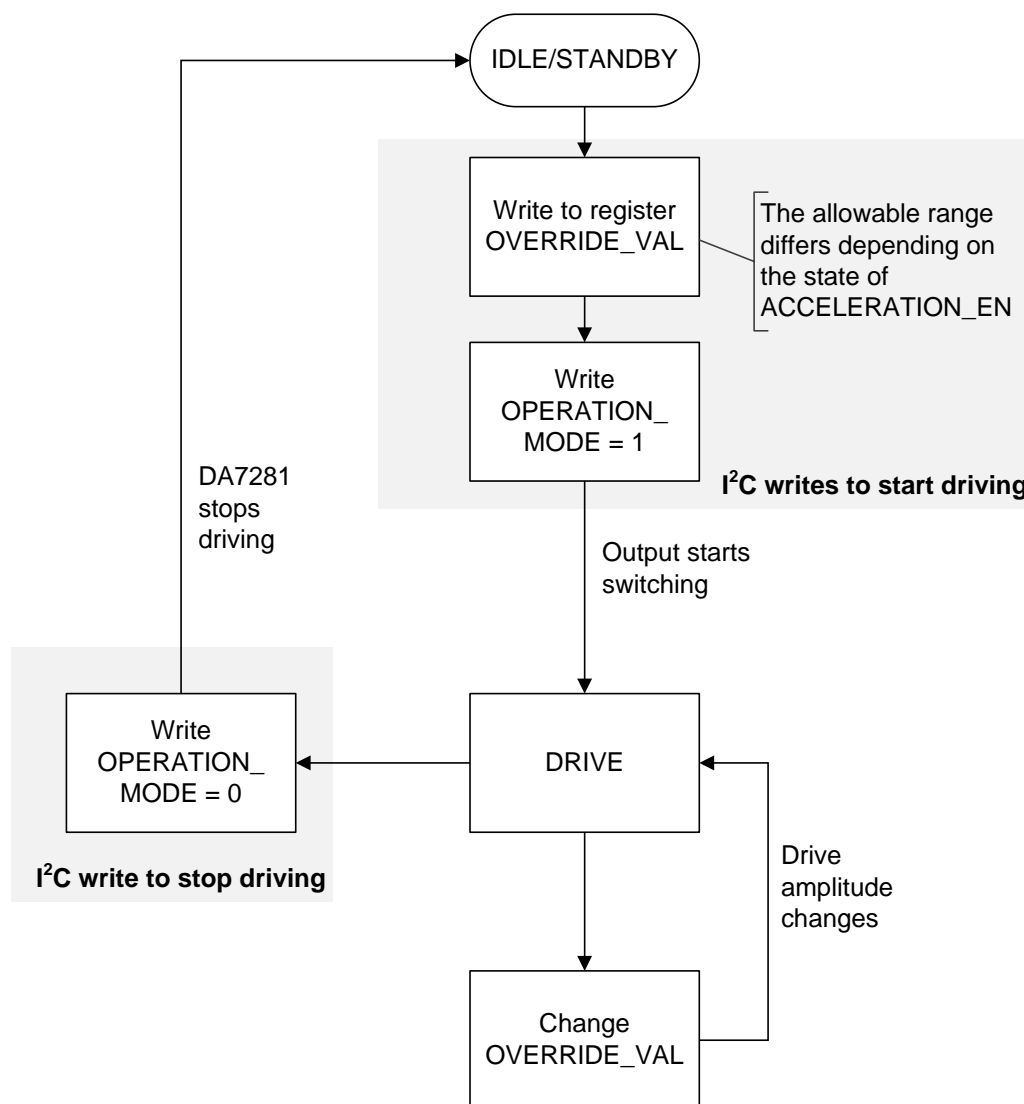


Figure 13: Operation in DRO Mode

### 5.6.5.3 PWM Mode

Figure 14 shows how to operate the device in PWM mode.

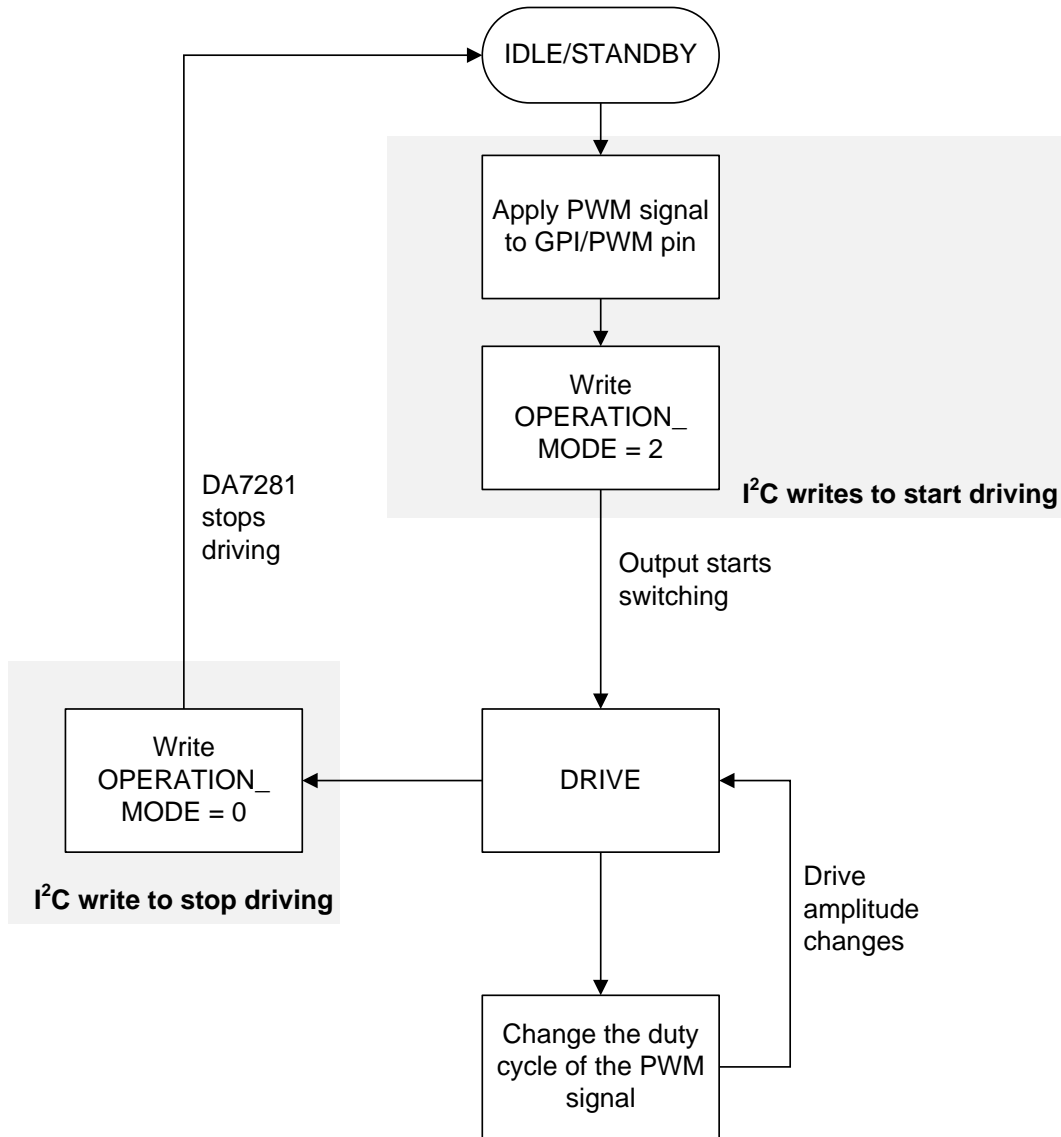
1. Starting from either the IDLE or STANDBY state, apply a PWM signal to the GPI/PWM pin.
2. When ready to begin playback, set OPERATION\_MODE = 2. The output will begin switching after approximately 0.75 ms with a drive amplitude proportional to the duty cycle of the incoming PWM signal.
3. While in the DRIVE state, update the duty cycle of the PWM signal to drive a new amplitude level and create the desired envelope of the haptic sequence. If the duty cycle of the PWM signal falls below the threshold set by FULL\_BRAKE\_THR, it is interpreted as a zero output drive level.
4. In order to stop driving, set OPERATION\_MODE = 0. DA7281 will return to either the IDLE or STANDBY state depending on the value of STANDBY\_EN.

**Note:** The duty cycle of the PWM signal is interpreted differently depending on the value of ACCELERATION\_EN. If ACCELERATION\_EN = 1, then zero drive corresponds to 50 % duty cycle  $\pm$



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FULL\_BRAKE\_THR. If ACCELERATION\_EN = 0, then zero drive corresponds to 0 % duty cycle + FULL\_BRAKE\_THR. For further explanation, see Figure 30 and Figure 31.



**Figure 14: Operation in PWM Mode**

**5.6.5.4 Register Triggered Waveform Memory (RTWM) Mode**

The following registers should be set up prior to operation in RTWM mode:

- Set `FREQ_WAVEFORM_TIMEBASE` according to the minimum or maximum sequence timebase required.
- Set `SNP_MEM_x` (where `x = 0 to 99`), see Section 5.8.
- If custom waveform sequences are required, see Section 5.7.5.
- Set `WAV_MEM_LOCK = 0` to prohibit access to the waveform memory if required.

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Figure 15 shows how to operate the device in RTWM mode.

1. While in the IDLE or STANDBY state, configure PS\_SEQ\_ID and PS\_SEQ\_LOOP to select the desired sequence from Waveform Memory.
2. For first-time playback, set OPERATION\_MODE = 3. On subsequent sequence playbacks, this step can be skipped (if OPERATION\_MODE = 3). The haptic sequence will not begin playing until a start event is created by setting SEQ\_START = 1.
3. While in the DRIVE state, set SEQ\_CONTINUE = 1 to repeat the sequence.
4. When the haptic sequence is completed, DA7281 will signal this by setting nIRQ = 0 and setting SEQ\_DONE\_M = 1. DA7281 will then return to IDLE or STANDBY state, depending on the value of STANDBY\_EN.
5. Clear the nIRQ and SEQ\_DONE\_M signals, set SEQ\_DONE\_M = 1.

At any time during operation in RTWM mode, set OPERATION\_MODE or SEQ\_START = 0 to return to the IDLE or STANDBY state.

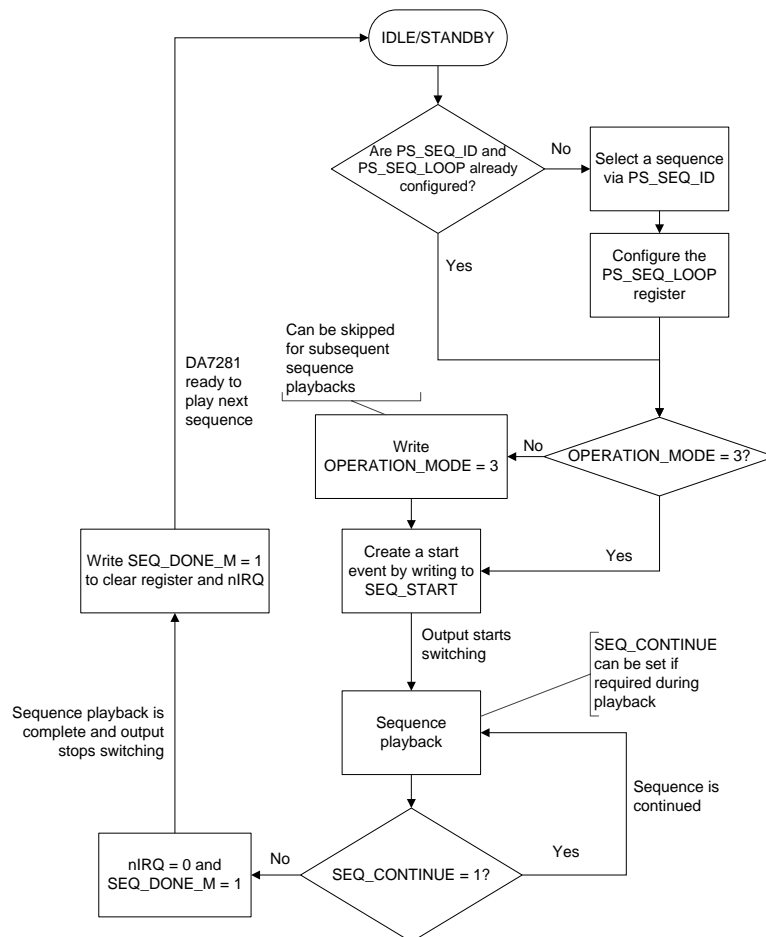


Figure 15: Operation in RTWM Mode

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### 5.6.5.5 Edge Triggered Waveform Memory (ETWM) Mode

The following registers should be set up prior to operation in ETWM mode:

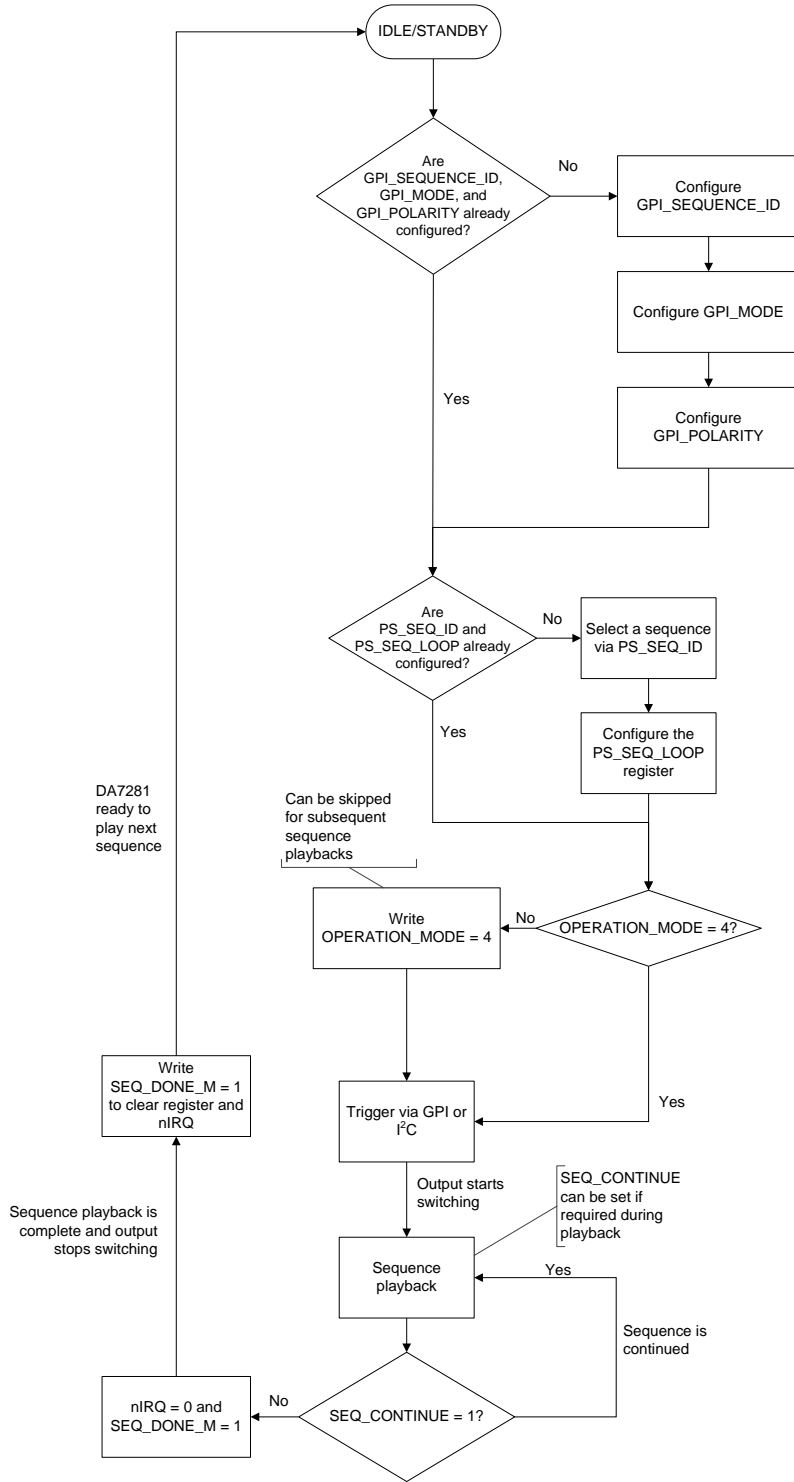
- Set SNP\_MEM\_x (where x = 0 to 99), see Section 5.8.
- Set FREQ\_WAVEFORM\_TIMEBASE according to the minimum or maximum sequence timebase required.
- If custom waveform sequences are required, see Section 5.7.5.
- Set WAV\_MEM\_LOCK = 0 to prohibit access to the waveform memory if required.

Figure 16 shows how to operate the device in ETWM mode.

1. Before first-time playback, set GPI\_SEQUENCE\_ID, GPI\_MODE, and GPI\_POLARITY, see Section 5.2.7. These bits determine which sequence the GPI/PWM pin points to, whether it triggers single or multiple sequences, and whether it reacts to rising, falling, or both edges.
2. Set PS\_SEQ\_ID and PS\_SEQ\_LOOP to select the sequence to play from Waveform Memory when a start event is created via writing to I<sup>2</sup>C (SEQ\_START). **Note:** If this has already been done, then this step can be skipped.
3. Set OPERATION\_MODE = 4. On subsequent sequence playbacks, this step can be skipped (if OPERATION\_MODE = 4). Haptic sequences will not begin playing until a start event is detected either by an edge on the GPI/PWM pin, or by setting SEQ\_START = 1 via I<sup>2</sup>C.
4. While in the DRIVE state, set SEQ\_CONTINUE = 1 to repeat the sequence.
5. When the haptic sequence is completed, DA7281 will signal this by setting nIRQ = 0 and setting SEQ\_DONE = 1. DA7281 will then return to IDLE or STANDBY state, depending on the value of the STANDBY\_EN.
6. Clear the nIRQ and SEQ\_DONE\_M signals by setting SEQ\_DONE\_M = 0 via I<sup>2</sup>C.

At any time during operation in ETWM mode, set OPERATION\_MODE or SEQ\_START = 0 to return to IDLE or STANDBY state.

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**Figure 16: Operation in ETWM Mode**

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### 5.6.6 Events and Diagnostics

DA7281 supports a comprehensive system for device, supply, and actuator diagnostics based on faults, warnings, and notifications. Faults return DA7281 to IDLE state and hold the system in IDLE until cleared, while warnings and notifications are used for host information only. If events are generated, the host is notified by the open-drain nIRQ pin pulling low.

A single IRQ\_EVENT1 byte containing all faults is presented to the host for simplified signaling. Warnings are reported via IRQ\_EVENT\_WARNING\_DIAG and input data faults via IRQ\_EVENT\_SEQ\_DIAG. [Table 13](#) provides a summary of the full array of faults:

**Table 13: Haptics Event Flag Descriptions**

Event Name	Description	Required Action
<b>Faults</b>		
E_OC_FAULT	Short circuit / over-current fault	Write 1 to clear
E_ACTUATOR_FAULT	An issue detected with the actuator impedance, BEMF amplitude, or resonant frequency	Write 1 to clear
E_SEQ_FAULT	Sequence ID, Waveform Memory, or PWM fault has occurred	Read IRQ_EVENT_SEQ_DIAG for diagnostic information
E_OVERTEMP_CRIT	Over-temperature event	Write 1 to clear
E_UVLO	Under-voltage fault	Write 1 to clear
<b>Notifications</b>		
E_SEQ_DONE	Memory sequence playback is complete	Write 1 to clear
E_SEQ_CONTINUE	Playback of a new sequence has started by the host setting SEQ_CONTINUE	Write 1 to clear
E_WARNING	A system warning is in effect	Read warnings in IRQ_EVENT_WARNING_DIAG
E_ADC_SAT	The input to the voltage sense ADC has saturated	Check if V2I_FACTOR_H/L is set correctly for the driven actuator
<b>Warnings</b>		
E_LIM_DRIVE	Playback is limited due to battery lower than sequence target	Reduce drive level if needed
E_LIM_DRIVE_ACC	Acceleration is limited due battery lower than overdrive level	Reduce drive level if needed
E_MEM_TYPE	Input memory data type does not match acceleration configuration	Check data format
<b>Input Data Faults</b>		
E_SEQ_ID_FAULT	Requested sequence ID does not exist	Reload PS_SEQ_ID and Waveform Memory
E_MEM_FAULT	Waveform Memory corruption (empty bytes, non-existent snippet ID, wrong frame parameter)	Reload Waveform Memory

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Event Name	Description	Required Action
E_PWM_FAULT	PWM timeout	Restart PWM interface and write 1 to E_SEQ_FAULT to clear

All events are write 1 to clear and can be masked using IRQ\_MASK1 and IRQ\_MASK2. Some of the sources generating E\_ACTUATOR\_FAULT can be disabled, for frequency tracking see Section 5.7.1 and for BEMF voltage amplitude see Section 5.7.14. For self-clearing of faults once in IDLE state, see Section 5.7.7.

### 5.7 Advanced Operation

DA7281 features several advanced modes of operation to fine-tune actuator haptic performance.

#### 5.7.1 Frequency Tracking

The closed-loop frequency tracking on DA7281 is implemented via a proportional-integral (PI) controller. The proportional coefficient (Kp) is stored in FRQ\_PID\_Kp\_H/L and the integral coefficient (Ki) in FRQ\_PID\_Ki\_H/L. The default values of the coefficients are optimized to cover a wide range of actuators with typical settling times of approximately 40 ms from a 20 % frequency offset. If further optimization is required to target a specific actuator the coefficients can be updated. The LRA tuning tool in the DA7281 SmartCanvas GUI provides an intuitive and graphical way to easily adjust the Kp and Ki coefficients.

To increase absolute accuracy of the lock during playback, DA7281 supports automatic scaling of the frequency tracking controller proportional coefficient. This feature is enabled via `FREQ_TRACKING_AUTO_ADJ` and becomes active after the device has achieved initial frequency lock. The `FRQ_LOCKED_LIM` value is used to determine the threshold for the initial lock and can be scaled up or down depending on system requirements. If optimizing `FRQ_PID_K<x>` coefficients with the `FREQ_TRACK_AUTO_ADJ` enabled in normal operation, ensure that the closed loop is stable for a step response when `FREQ_TRACK_AUTO_ADJ` is set at either 0 or 1.

The resonant frequency tracking algorithm converges to the correct value from up to 25 % offset between the initial nominal datasheet value and the actual resonant frequency. This range is conservative to prevent unwanted behavior. A fault triggers if the actuator resonant frequency is outside the 50 Hz to 300 Hz range. To block these checks, set `FREQ_TRACKING_FORCE_ON = 1`.

`FRQ_TRACK_BEMF_LIM` disables the frequency tracking if the BEMF signal becomes too low. It should always be set lower than the value in `RAPID_STOP_LIM`.

The instantaneous value of the resonant frequency period is updated every half-period and written to `LRA_PER_ACTUAL_H/L`. The values can be converted to period using the following formula:

$$LRA \text{ period (ms)} = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_ACTUAL\_H + LRA\_PER\_ACTUAL\_L) \quad (10)$$

If more accurate information is required (for example if a frequency tracking enabled sequence is played to determine the resonant frequency before entering wideband operation), the average resonant frequency information over the last four half-periods is written to `LRA_PER_AVERAGE_H/L`. The values can be converted to period using the following formula:

$$LRA \text{ period (ms)} = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_AVERAGE\_H + LRA\_PER\_AVERAGE\_L) \quad (11)$$

#### 5.7.2 Rapid Stop

The Rapid Stop algorithm relies on actuator BEMF sensing to detect actuator motion during a stop-to-zero LRA acceleration. The algorithm provides a stopping signal to the LRA until the actuator

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crosses the point of no acceleration. Since drive updates happen only at the zero cross point, this introduces latency that may cause the actuator to overshoot the stop position. Due to this, the Rapid Stop will also trigger at a pre-determined threshold set by `RAPID_STOP_LIM`. The default setup covers most actuators, but if Rapid Stop is too short (actuator not fully stopped), the register value should be decreased; and if Rapid Stop overshoots (actuator stopped and then reversed), the register value should be increased.

**Note:** The Rapid Stop algorithm can be triggered only for sequences longer than three half-periods.

### 5.7.3 Initial Impedance Update

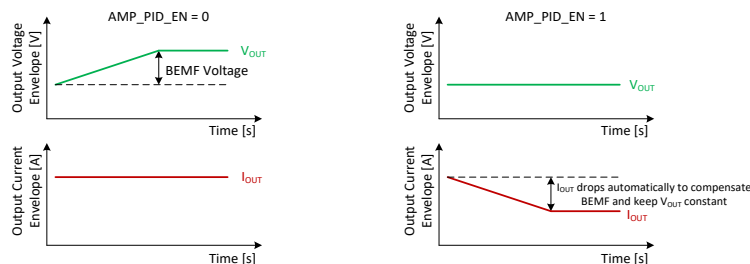
DA7281 performs an impedance measurement at the very first half-period of drive at the start of playback. This allows a one-shot update of `V2I_FACTOR_H/L` to take into account specific actuator variation for increased voltage accuracy of the drive. The result is reported to `IMPEDANCE_H/L`, which can be read by the host and converted to impedance using the following formula:

$$\text{Actuator Impedance}(R_{series}) = (\text{IMPEDANCE}_H \times 4 + \text{IMPEDANCE}_L) \times 0.0625\Omega \quad (12)$$

To disable this feature, set `V2I_FACTOR_FREEZE` and `CALIB_IMPEDANCE_DIS` = 1.

### 5.7.4 Amplitude PID

Some cylinder based ERMs generate excessively large-amplitude BEMF voltages. DA7281 can compensate for this by reducing the drive current level, set `AMP_PID_EN` = 1. The result is an improved haptic response. Figure 17 describes how the actuator voltage and current differs when `AMP_PID_EN` enabled or disabled.



**Figure 17: Output Voltage and Current for Different AMP\_PID\_EN Values**

**Note:** This is not usually required for LRAs as the amplitude of the BEMF is typically very low.

### 5.7.5 Wideband Operation

DA7281 natively supports wideband LRAs and allows continuous frequency updates to the output signal while driving. Amplitude and frequency data use parallel data paths, for configuration see Section 5.6.5. This section describes how to use the frequency component only.

For wideband operation, frequency tracking must be disabled, by setting `FREQ_TRACK_EN` = 0, because drive at frequencies different from the actuator resonant frequency is required. Rapid Stop and Active Acceleration also rely on frequency tracking so must be deactivated by setting

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ACCELERATION\_EN = 0 and RAPID\_STOP\_EN = 0. There are two ways to operate DA7281 during wideband operation:

- In the limited frequency range of 25 Hz to 300 Hz:
  - No further settings are required in RTWM and ETWM modes if the frequency information is already stored in the Waveform Memory frame data as described in Section 5.8.3. If the Waveform Memory does not contain frequency information, then each sequence can be played at a different frequency by setting LRA\_PER\_H and LRA\_PER\_L to the desired value via the formulae in Section 5.6.2 before triggering playback using the method described in Sections 5.6.5.4 and 5.6.5.5.
  - In the DRO and PWM modes, the frequency information can be updated via the LRA\_PER\_H and LRA\_PER\_L using the formulae in Section 5.6.2 either before triggering playback of each sequence, see Sections 5.6.5.2 and 5.6.5.3, or during the playback itself. As with amplitude, the one half-period uncertainty on the output frequency update also applies.
- In the full range of 25 Hz to 1024 Hz, the same procedures apply for all modes, but the following registers need to be set:
  - BEMF\_SENSE\_EN = 0
  - DELAY\_H = 0
  - DELAY\_SHIFT\_L = 0
  - DELAY\_FREEZE = 1

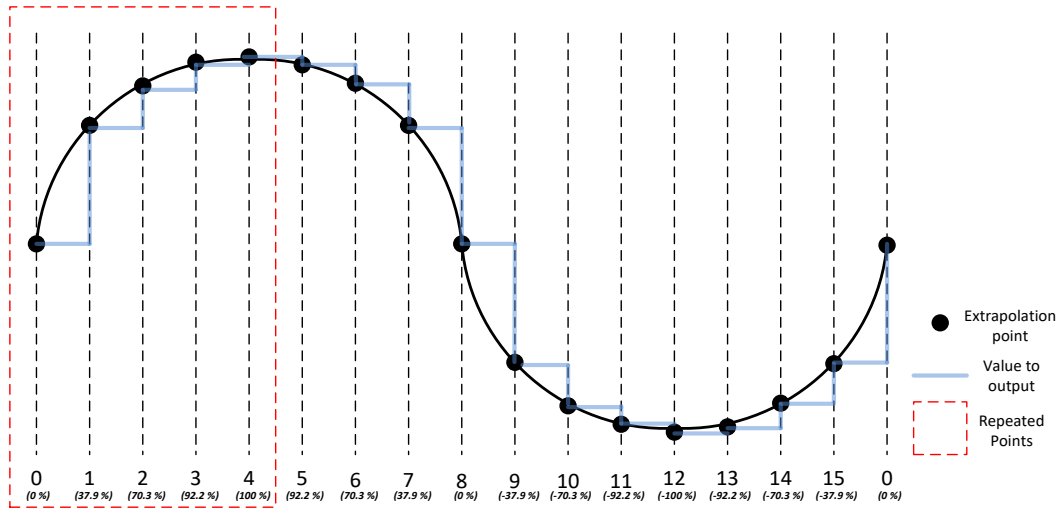
### 5.7.6 Custom Waveform Operation

With frequency tracking, Active Acceleration, and Rapid Stop disabled, and with the additional setup for wideband operation described in Section 5.7.5, DA7281 can be configured to drive a custom waveform to an LRA actuator. It is important to note that here the custom waveform denotes the actual output during a single LRA resonant period and not the overall amplitude envelope during drive events, which is controlled as previously described in Section 5.6.5. Amplitude and frequency data can be streamed as usual in DRO, PWM, RTWM, or ETWM modes.

The waveform output during a single resonant period comprises of 16 distinct points, see Figure 18, where points 0 to 4 are mirrored and repeated to create, by default, a sine wave (for example, point 3 and point 5, and point 2 and point 6 have the same amplitude).



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**Figure 18: Custom Wave Point Numbering**

Point 0 corresponds to an amplitude of 0 % of the value of IMAX, point 4 corresponds to an amplitude of 100 %, and points 1, 2, and 3 are scaled to the IMAX value by the unsigned CUSTOM\_WAVE\_GEN\_COEFF1, CUSTOM\_WAVE\_GEN\_COEFF2, and CUSTOM\_WAVE\_GEN\_COEFF3 coefficient values. The default coefficients are set to correspond to a sine wave but can be updated to recreate any required waveform that is built of four symmetrical sections, see Figure 18.

Table 14 contains a summary of the default coefficients and their settings.

**Table 14: Default CUSTOM\_WAVE\_GEN\_COEFFx Settings**

Point	% of IMAX[4:0]	Corresponding Bits
0	0	-
1	37.9	CUSTOM_WAVE_GEN_COEFF1
2	70.3	CUSTOM_WAVE_GEN_COEFF2
3	92.2	CUSTOM_WAVE_GEN_COEFF3
4	100	-

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Configure the following bits to enable custom waveform operation:

- BEMF\_SENSE\_EN = 0
- WAVEGEN\_MODE = 1
- V2I\_FACTOR\_FREEZE = 1
- DELAY\_H = 0
- DELAY\_SHIFT\_L = 0
- DELAY\_FREEZE = 1
- ACCELERATION\_EN = 0
- RAPID\_STOP\_EN = 0
- AMP\_PID\_EN = 0

After the above setup is executed, amplitude data can be streamed in any mode, see Section 5.6.5, and output frequency can be updated, see Section 5.7.6.

### 5.7.7 Embedded Operation

Should DA7281 be required to operate in a setup where no host is present or due to software limitations unable to communicate with the device during its required operation, DA7281 can operate in embedded operation by setting EMBEDDED\_MODE = 1. In this case DA7281 is configured to clear all system faults as it enters inactive mode when playback is finished or if a fault has been detected, see Section 5.6.6.

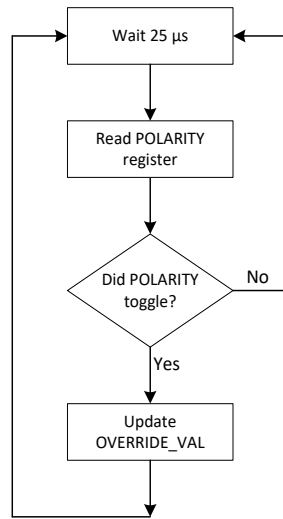
For example, if a short circuit occurs, the system will react in its usual way: stop driving, disable the current loop, and go to Inactive mode. Once in Inactive mode, the generated interrupt is automatically cleared and DA7281 will attempt to drive again on the next playback request without the host having to come in and clear faults.

### 5.7.8 Polarity Change Reporting for Half-Period Control in DRO Mode

For advanced sequence playback in DRO mode, the host may require DA7281 to update the output drive amplitude every half period. Since the I<sup>2</sup>C clock is asynchronous to the DA7281 internal clock and the exact timing of the half-period will change dynamically based on the frequency tracking loop, this is not a trivial operation.

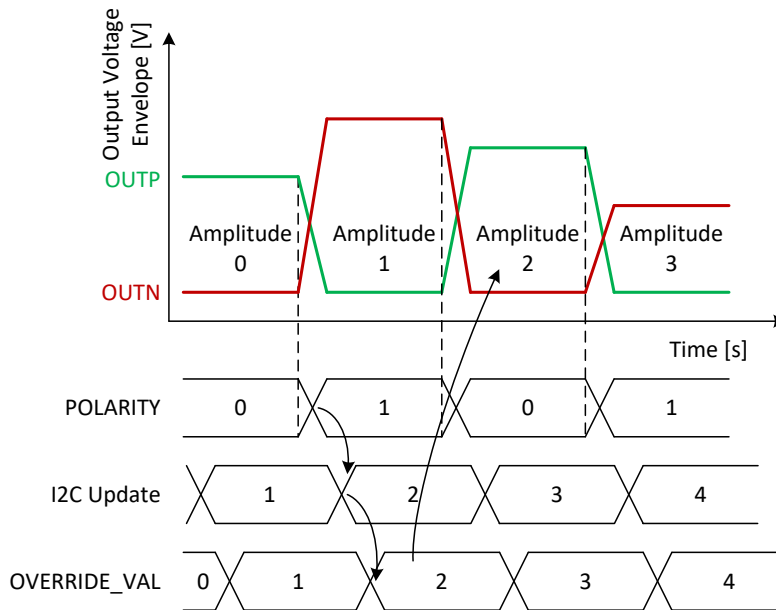
To overcome this limitation, the register POLARITY provides feedback. POLARITY toggles at the start of every half-period (so at a rate of 400 Hz for a 200 Hz resonant frequency actuator). This allows software synchronization of the updates to the OVERRIDE\_VAL, see Figure 19.

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**Figure 19: Half-Period Control in DRO Mode**

The timing of the sequence can be described as follows in [Figure 20](#) where Amplitude X denotes consecutive different output drive values:

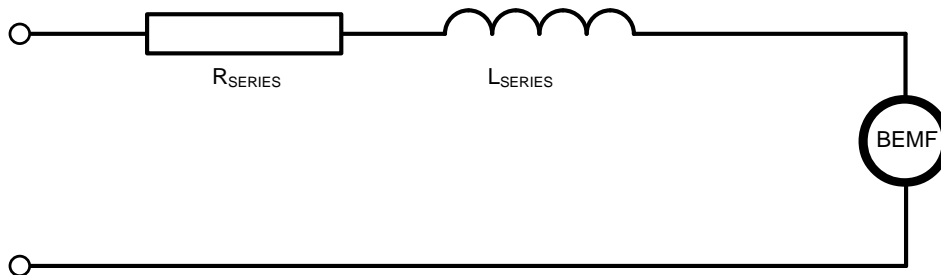


**Figure 20: Polarity Timing Relationship**

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**5.7.9 Loop Filter Configuration**

Haptic actuators (both ERM and LRA) can be modelled as a series combination of a resistor (Series R) and inductor (Series L) followed by a BEMF voltage source, see [Figure 21](#).



**Figure 21: Equivalent Electrical Model of an Actuator**

The usual variation of  $R_{SERIES}$  is from 8  $\Omega$  to 50  $\Omega$  and  $L_{SERIES}$  is from 20  $\mu\text{H}$  to either 2 mH or 3 mH. The current regulation loop in the output drive must be kept stable by applying the correct setting in the loop's filter. While the defaults cover the vast majority of available LRAs and ERMs further tuning is possible by adjusting LOOP\_FILTER\_CAP\_TRIM, LOOP\_FILTER\_RES\_TRIM, and LOOP\_FILTER\_LOW\_BW.

For LOOP\_FILTER\_CAP\_TRIM apply the settings in [Table 15](#).

**Table 15: LOOP\_FILTER\_CAP\_TRIM Register Trim Settings**

Register	Actuator Series Resistance ( $\Omega$ )			
	< 18	18 to 28	28 to 41	> 41
LOOP_FILTER_CAP_TRIM	3	2	1	0

For LOOP\_FILTER\_RES\_TRIM apply the settings in [Table 16](#).

**Table 16: LOOP\_FILTER\_RES\_TRIM Register Trim Settings**

$R_{series}$ ( $\Omega$ )	$L_{series}$ ( $\mu\text{H}$ )									
	25 or lower	50	75	100	125	150	175	200	225	250 or higher
4	2	2	3	3	3	3	3	3	3	3
6	1	2	2	3	3	3	3	3	3	3
8	1	2	2	2	3	3	3	3	3	3
10	0	1	2	2	2	3	3	3	3	3
12	0	1	2	2	2	2	3	3	3	3
14	0	1	1	2	2	2	2	3	3	3
16	0	1	1	2	2	2	2	2	3	3
18	0	0	1	1	2	2	2	2	2	3
20	0	1	1	2	2	2	3	3	3	3

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	L <sub>series</sub> (μH)									
22	0	1	1	2	2	2	2	3	3	3
24	0	1	1	2	2	2	2	3	3	3
26	0	1	1	2	2	2	2	2	3	3
28	0	1	2	2	2	3	3	3	3	3
30	0	1	2	2	2	3	3	3	3	3
32	0	1	2	2	2	2	3	3	3	3
34	0	1	1	2	2	2	3	3	3	3
36 to 40	0	1	1	2	2	2	2	3	3	3
42	0	1	2	2	3	3	3	3	3	3
44	0	1	2	2	3	3	3	3	3	3
46 to 50	0	1	2	2	2	3	3	3	3	3

Set LOOP\_FILT\_LOW\_BW high if the actuator inductance exceeds 1 mH.

#### 5.7.10 UVLO Threshold

The DA7281 UVLO has a default fall threshold of 2.8 V. This is adjustable in 100 mV steps via REF\_UVLO\_THRES. The full range is 2.7 V to 3.0 V.

#### 5.7.11 Edge Rate Control

DA7281 contains an advanced switching node ERC to minimize EMI and board disturbances. The slope of the ERC can be adjusted by changing the values of the HBRIDGE\_ERC\_LS\_TRIM (for low-side FET ERC) and HBRIDGE\_ERC\_HS\_TRIM (for high-side FET ERC). Default value is 100 mV/ns and the adjustable range is 25 mV/ns to 100 mV/ns in 25 mV/ns steps.

#### 5.7.12 Double Output Current Range

The nominal current rating for the DA7281 current regulation output is 250 mA. This range covers existing LRAs, however some LRA manufacturers allow significant actuator overdrive over short periods of time. DA7281 supports this by enabling LOOP\_IDAC\_DOUBLE\_RANGE, which doubles the maximum output current. When this is enabled, the following setup changes apply:

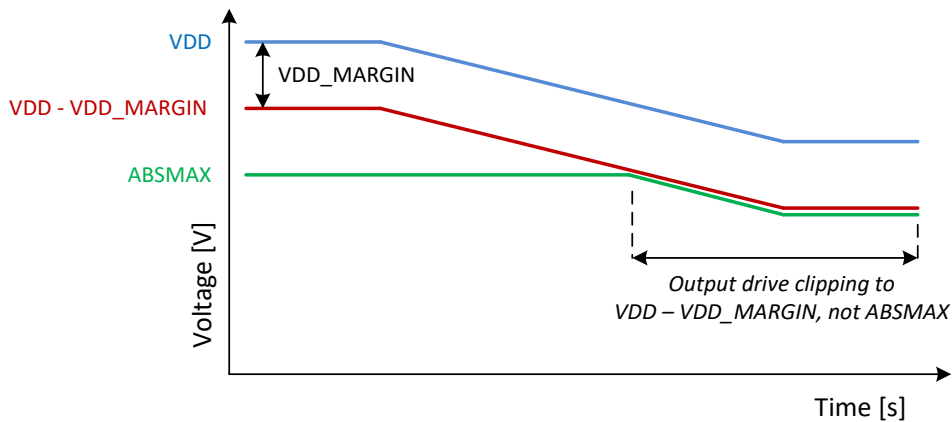
- IMAX now corresponds to twice the value computed by the formula in Section 5.6.2.
- When setting the impedance in V2I\_FACTOR\_H and V2I\_FACTOR\_L via the formula in Section 5.6.2, use  $Z_{\text{formula}} = 2 \cdot Z_{\text{real}}$ .
- When reading back from IMPEDANCE\_H and IMPEDANCE\_L, use an LSB of 0.03125 Ω.

#### 5.7.13 Supply Monitoring, Reporting, and Automatic Output Limiting

DA7281 monitors the level of the supply during playback and reports it via ADC\_VDD\_H and ADC\_VDD\_L. The two should be concatenated and read using the following formula:

$$VDD \text{ Supply Voltage} = (ADC\_VDD\_H \times 128 + ADC\_VDD\_L) \times 0.1831 \text{ mV} \quad (13)$$

DA7281 uses this information to prevent the device from clipping to supply by limiting the drive to a value determined by the VDD\_MARGIN register in 187.5 mV steps where 0x0 corresponds to no margin, see Figure 22.

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**Figure 22: Automatic Output Limiting**

The functionality is needed as DA7281 regulates current and if supply clipping occurs, the regulation stops and the BEMF information is lost. Furthermore, the VDD\_MARGIN register allows limiting of the power across the actuator for low supply values to prevent the battery from discharging too fast.

**5.7.14 BEMF Fault Limit**

To detect malfunctioning actuators that have stopped moving due to a mechanical fault, DA7281 can be configured to trigger an actuator fault if the BEMF voltage level falls below a threshold for long drive durations. The threshold for detection is set in BEMF\_FAULT\_LIM; a zero value of the register disables the fault checking.

**5.7.15 Increasing Impedance Detection Accuracy**

To increase the accuracy of the impedance reading in IMPEDANCE\_H and IMPEDANCE\_L, the register V2I\_FACTOR\_OFFSET\_EN could be set to 0. This removes an algorithmic offset utilized by the acceleration algorithm. Should V2I\_FACTOR\_OFFSET\_EN be equal to 0, ACCELERATION\_EN is recommended to be set to 0.

**5.7.16 Frequency Pause during Rapid Stop**

To address low mechanical time constant LRAs (start/stop times less than 20 ms) and improve the braking behavior, DA7281 has the option to pause frequency tracking during the execution of the Rapid Stop algorithm by setting FRQ\_PAUSE\_ON\_POLARITY\_CHANGE to 1.

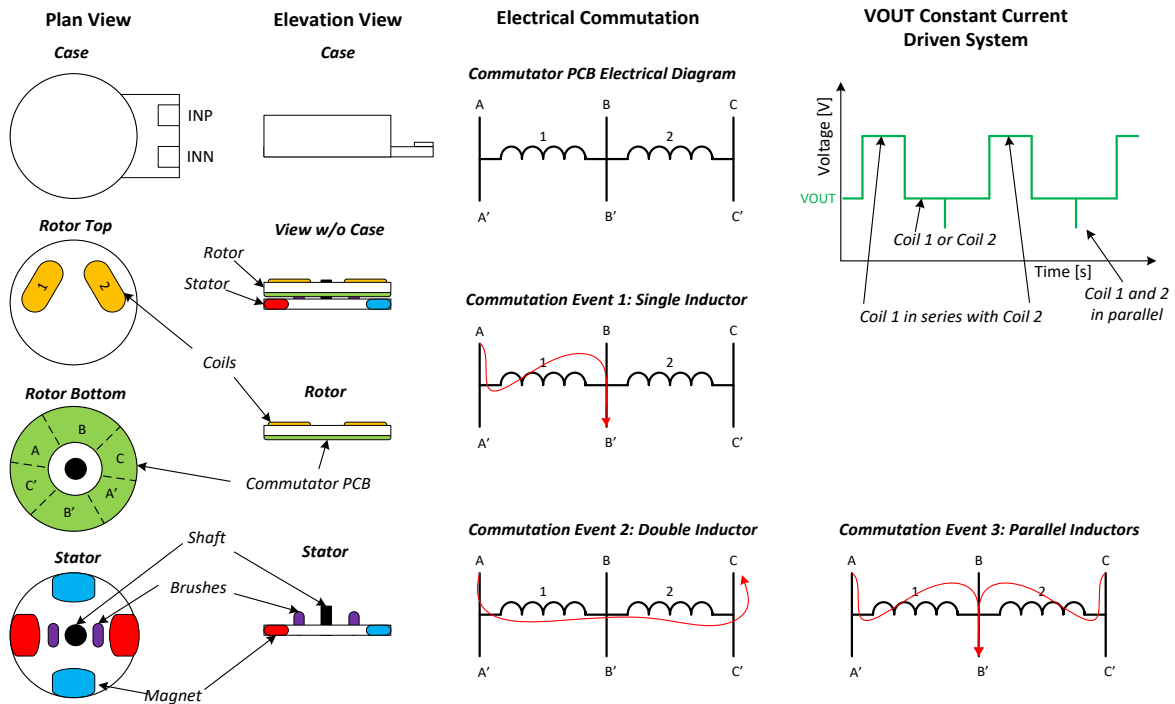
**5.7.17 Frequency Pause during Rapid Stop**

If DA7281 is used with LRAs that have significant BEMF voltage amplitude that can transiently exceed the IR drop across an actuator when reversing the phase of the drive signal, it is recommended to set DELAY\_BYPASS to 0.

**5.7.18 Coin ERM Operation**

The term coin ERM is used to describe an eccentric rotating mass actuator that is flat and has coin-like external appearance. The eccentric rotating mass is circular and contains two coil windings that are used for commutation, see [Figure 23](#).

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**Figure 23: Coin ERM Physical and Electrical Summary**

Due to the commutation of the motor, the impedance varies between one coil, two coils in series, and for very short periods two coils in parallel. Due to this behavior, DA7281 cannot extract the BEMF and actuator motion is not detectable for coin ERM actuators. Therefore, Active Acceleration and Rapid Stop features are not available. Manual overdrive or underdrive of the coin ERM to speed up the transition between two levels of acceleration is possible and recommended for better user experience. Note that due to the varying impedance and the constant current drive of DA7281, the output voltage will vary, with no effect on the performance of the DA7281, see [Figure 23](#).

Recommended setup specific for a coin ERM, in addition to generic ERM setup described in Section 5.6.2:

- ACCELERATION\_EN = 0
- RAPID\_STOP\_EN = 0
- AMP\_PID\_EN = 0
- V2I\_FACTOR\_FREEZE = 1
- CALIB\_IMPEDANCE\_DIS = 1
- BEMF\_FAULT\_LIM = 0
- Set the V2I factor using the single winding impedance, see Section 5.6.2
- Set IMAX using the maximum start-up current, see Section 5.6.2

### 5.8 Waveform Memory

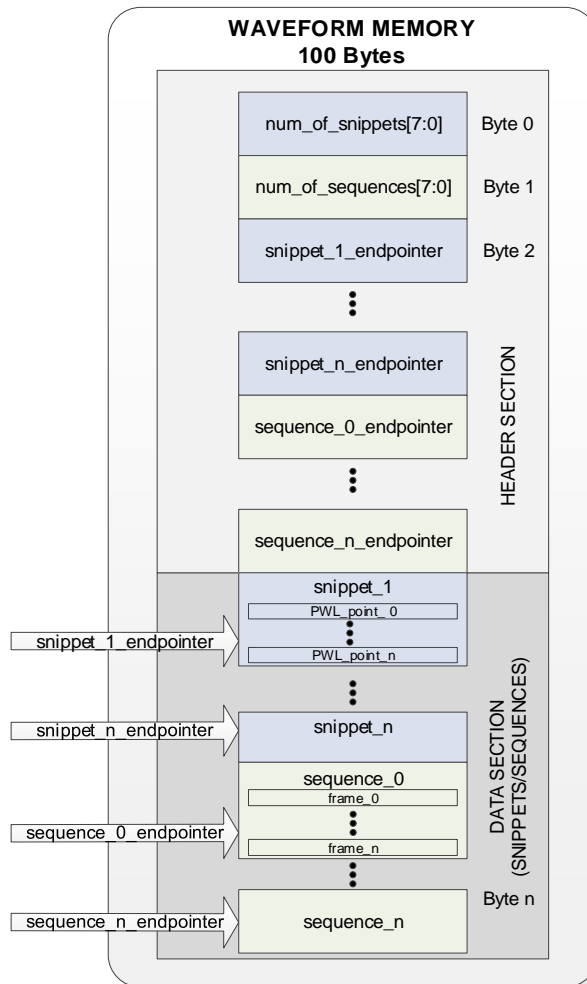
The Waveform Memory stores haptic drive sequences. A single haptic effect is called a sequence and each sequence is formed by one or more frames that address one or more snippets stored in memory. The overall Waveform Memory structure is described in detail in Section 5.8.1; Sections 5.8.2 to 5.8.4 provide definitions for snippets, frames, and sequences.

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

**NOTE**  
 It is recommended that the Dialog [SmartCanvas](#) GUI is used to construct sequences and upload them to the Waveform Memory. The easy to use GUI provides intuitive visualization of the sequences in the Waveform Memory and requires only basic knowledge of the overall memory format.

**5.8.1 Waveform Memory Structure**

The waveform memory structure has a 100-byte capacity for storing snippets, frames, and sequences. Sequences reference the snippets using frames to allow complex haptic sequences to be created in a memory efficient manner. The overall structure of the Waveform Memory can be seen in [Figure 24](#). For Waveform Memory programming, see [Section 5.6.4](#).



**Figure 24: Waveform Memory Structure**



## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 5.8.1.1 Header Section

The three sections constituting the header for the Waveform Memory are:

- Byte 0: Defines the number of snippets stored.
- Byte 1: Defines the number of sequences stored.
- Byte 2 and onwards: The snippet(s) and sequence(s) end address pointer(s) are stored. Each pointer address occupies one byte. Up to 15 snippets can be addressed in addition to snippet 0, which is the silence snippet, see [Note 1](#). Up to 16 sequences can be addressed. A snippet or sequence pointer points to the location in the waveform memory where the last byte of the respective snippet or sequence resides.

### 5.8.1.2 Data Section

The upper memory section contains the PWL data describing the snippets, see [Table 17](#). The lower part of the memory contains the pre-stored sequences.

Snippet IDs are determined by the order in which they are listed, starting from SNP\_ID = 1. Sequence IDs are determined by the order in which they are listed, starting from 0.

## 5.8.2 Snippet Definition

Snippets are formed by storing a series of one or more piecewise linear (PWL) amplitude and time pairs. Snippets represent the basic building blocks used in the Waveform Memory.

**Table 17: PWL Byte Structure**

Bit	7	6	5	4	3	2	1	0
Description	RMP	TIME[6:4]			AMP[3:0]			

A byte is allocated for each amplitude and time pair in the Waveform Memory, see [Table 17](#). A snippet consists of one or more bytes containing RMP, TIME and AMP data.

- RMP defines whether a ramp (RMP = 1) or a step (RMP = 0) is required between consecutive time and amplitude pairs.
- TIME contains the unitless time information (number of timebases) with the minimum being 1 timebase. Consequently, TIME = 0 signifies time base of 1, TIME = 1 signifies time base of 2, and so on, with the longest duration at 8 timebases for TIME = 7.
- AMP contains the amplitude information of the snippet. If ACCELERATION\_EN = 1, AMP is unsigned and scales between 0 and 15, where 0 represents silence and 15 represents 100 % drive. If ACCELERATION\_EN = 0, AMP is in two's complement and scales between 7 and -7 where 7 represents 100 % full scale and -7 represents -100 % (full scale 180° reversed polarity). To maintain symmetry, -8 is interpreted as -7.

### LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

For example, assuming ACCELERATION\_EN = 1, the snippet shown in Figure 25 creates a waveform that ramps from zero to an amplitude of 1111 over a period of two timebases, then step from 1111 to 1000, and remains there for four timebases. The length (in milliseconds) of a timebase is specified using the TIMEBASE frame bits, see Section 5.8.3.

Description	RMP	TIME[6:4]			AMP[3:0]			
Ramp	1	0	1	0	1	1	1	1
Step	0	1	0	0	1	0	0	0

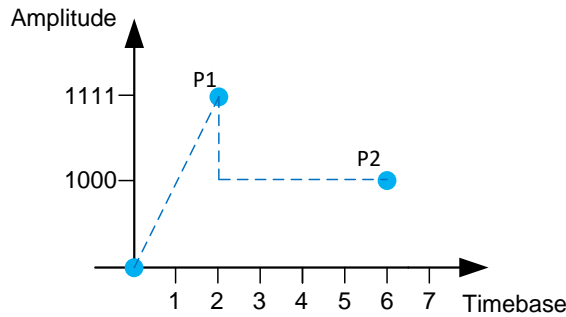


Figure 25: Snippet Ramp and Step with ACCELERATION\_EN = 1

If a constant drive level of longer than 8 timebases is required, set RMP = 0 for subsequent PWL points.

Figure 26 shows a generic example of a snippet, where P<sub>n</sub> represents the PWL pair located at amplitude A<sub>n</sub> and with time step T<sub>n</sub>, where n represents the PWL pair number. Note that a snippet played at the start of a non-looped sequence will start from a default point P<sub>0</sub> set at zero amplitude; however, if the snippet is not at the start of a sequence or is read during the looping of a sequence, the starting point will be the last played PWL point.

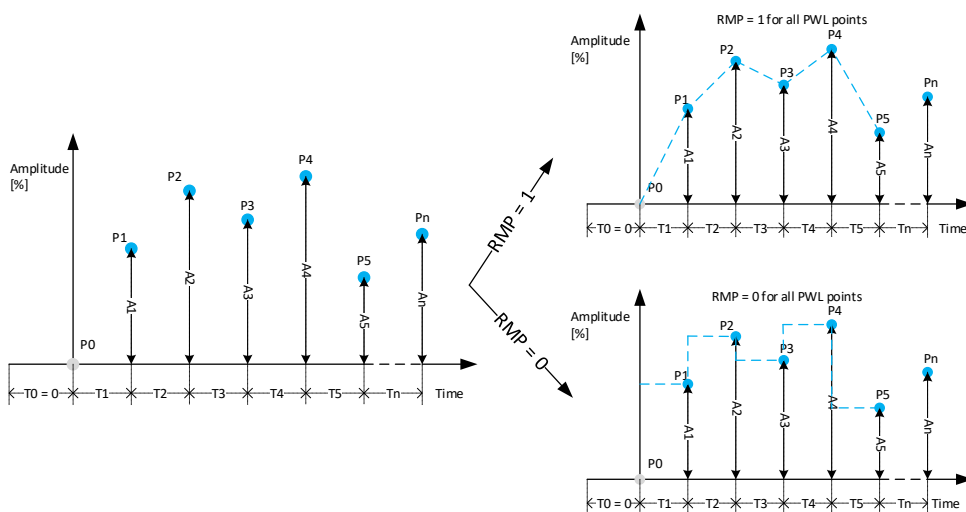


Figure 26: Snippet Example

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**Note 1** A built-in snippet containing a single silent PWL point (amplitude = 0) is available by setting SNP\_ID = 0. The duration is set to two timebases. Because of the existence of this snippet, customer defined snippets start at SNP\_ID = 1. The snippet is inherent to the decoding and is not actually stored in the waveform memory. The number of snippets (byte 0) does not include snippet 0 and there is no end pointer for snippet 0 stored in the waveform memory.

### 5.8.3 Frame Definition

A frame consists of a collection of parameters used to define the playback of a snippet with differing gain, time base, carrier frequency, and number of repetitions. A frame consists of up to three bytes, its structure is shown in [Figure 27](#). The frame parameters can be easily set up using the Dialog SmartCanvas GUI.

- Byte 1 is mandatory. For byte 1, always set COMMAND\_TYPE = 0. If set incorrectly, the device will generate an interrupt of the type E\_MEM\_FAULT.
- Byte 2 is optional. When used, set COMMAND\_TYPE = 1 in Byte 2.
- Byte 3 is optional, for use in wideband sequences only, and contains the frame frequency's eight LSBs.

If COMMAND\_TYPE of frame Byte 2 is set to 1 and FREQ\_CMD = 1, then the Byte 3 contains drive frequency data to enable wideband LRA support.

All frame parameters except COMMAND\_TYPE, SNP\_ID\_L, GAIN, and TIMEBASE are optional. For a full description, see [Table 18](#).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1 =>	COMMAND_TYPE = 0	GAIN [1:0]		TIMEBASE[1:0]		SNP_ID_L[2:0]		
Byte 2 =>	COMMAND_TYPE = 1	SNP_ID_LOOP[3:0]				FREQ_CMD	FREQ[8]	SNP_ID_H
Byte 3 =>	FREQ[7:0]							

**Figure 27: Command Structure for a Single Frame**

**Table 18: Bit Definitions for Frame Parameters**

Byte Number	Register Bit Definitions	Description
1 and/or 2	COMMAND_TYPE	COMMAND_TYPE labels the byte and tells the system how to interpret the following seven LSBs. COMMAND_TYPE = 0 in Byte 1 COMMAND_TYPE = 1 signifies Byte 2 is present followed by Byte 1
1	GAIN[1:0]	Gain applied to the snippet identified by SNP_ID_L/H: 00 = 0 dB 01 = -6 dB 10 = -12 dB 11 = -18 dB
1	TIMEBASE[1:0]	The timebase length of the snippet pointed to by the snippet ID. This register is interpreted differently depending on FREQ_WAVEFORM_TIMEBASE:

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Byte Number	Register Bit Definitions	Description
		If <code>FREQ_WAVEFORM_TIMEBASE = 0 (default)</code> : 00 = 5.44 ms 01 = 21.76 ms 10 = 43.52 ms 11 = 87.04 ms If <code>FREQ_WAVEFORM_TIMEBASE = 1</code> : 00 = 1.36 ms 01 = 5.44 ms 10 = 21.76 ms 11 = 43.52 ms
1	<code>SNP_ID_L[2:0]</code>	<code>SNP_ID_L</code> is mandatory and contains the LSBs of the snippet ID ( <code>SNP_ID</code> ). Up to eight snippets can be addressed.
2	<code>SNP_ID_LOOP[3:0]</code>	<code>SNP_ID_LOOP</code> is the loop multiplier of the snippet identified by <code>SNP_ID_L/H</code> and shows how many times a snippet is looped. If not present, the loop multiplier is 1. The number of loop iterations is equal to <code>SNP_ID_LOOP + 1</code> (that is, 0 = 1 iteration, 15 = 16 iterations). When the loop multiplier is > 1, playback begins from P1 instead of P0, see <a href="#">Figure 26</a> , after the first playback loop is complete.
2	<code>FREQ_CMD</code>	If <code>FREQ_CMD = 1</code> , the frame is a 3-byte command with frequency information. The frequency information is stored in <code>FREQ[7:0]</code> .
2	<code>FREQ[8]</code>	Drive frequency MSB. The total frequency range is represented by the 9-bit concatenation of <code>FREQ[8]</code> and <code>FREQ[7:0]</code> (possible values: 0 to 511), which corresponds to the range 1 Hz to 1024 Hz. The LSB step size is 2 Hz and values below 25 Hz are interpreted as 25 Hz. The result is also converted from frequency to period and stored in the <code>FRQ_LRA_PER_ACT_x</code> registers for read-back.
2	<code>SNP_ID_H</code>	<code>SNP_ID_H</code> is the MSB of the snippet ID ( <code>SNP_ID</code> ). This can be used to increase the range of addressable snippets from 8 to 16. This bit is optional and if not present <code>SNP_ID_H = 0</code> .
3	<code>FREQ[7:0]</code>	Drive frequency LSBs. The total frequency range is represented by the 9-bit concatenation of <code>FREQ[8]</code> and <code>FREQ[7:0]</code> (possible values: 0 to 511), which corresponds to the range 1 Hz to 1024 Hz. The LSB step size is 2 Hz and values below 25 Hz are interpreted as 25 Hz. The result is also converted from frequency to period and stored in the <code>FRQ_LRA_PER_ACT_x</code> registers for read-back.

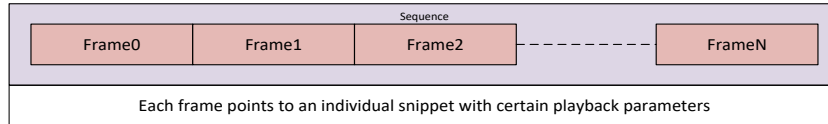
**Note:** The frequency command should be used only when `FREQ_TRACK_EN = 0`, otherwise the frequency tracking loop will update the frequency away from the set one.

**Note:** The If `FREQ_TRACK_EN = 0` and a frequency update containing frame is played, the new frequency will be maintained for all subsequent frames or sequences until a new frame with a new frequency command is played. Assume that Sequence 0 contains no frames with frequency commands, Sequence 1 has a frame with command setting the frequency at 150 Hz, and Sequence 2 has one at 200 Hz. If Sequence 0 is played after Sequence 1, it will be played at 150 Hz. If Sequence 0 is played after Sequence 2, it will be played at 200 Hz.

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**5.8.4 Sequence Definition**

A sequence is built up of one or more frames, see [Figure 28](#), and written to memory using the format described in Section [5.8.1](#).



**Figure 28: Sequence Structure**

**Note:** Only sequences can be played. It is not possible to point directly to a snippet (although a sequence can be created which contains only one snippet).

**Note:** If a sequence ends on a non-zero value, zero is assumed to follow and the device will end the haptic playback at the end of the sequence.

**Note:** The starting amplitude at the beginning of a frame or snippet is dependent on the ending amplitude of the previous frame or snippet. The starting amplitude at the start of a sequence is zero. See [Figure 26](#) for more details.

**5.8.4.1 Pre-Stored Waveform Memory Example**

[Figure 29](#) shows an example of a typical Waveform Memory operation with all features enabled.

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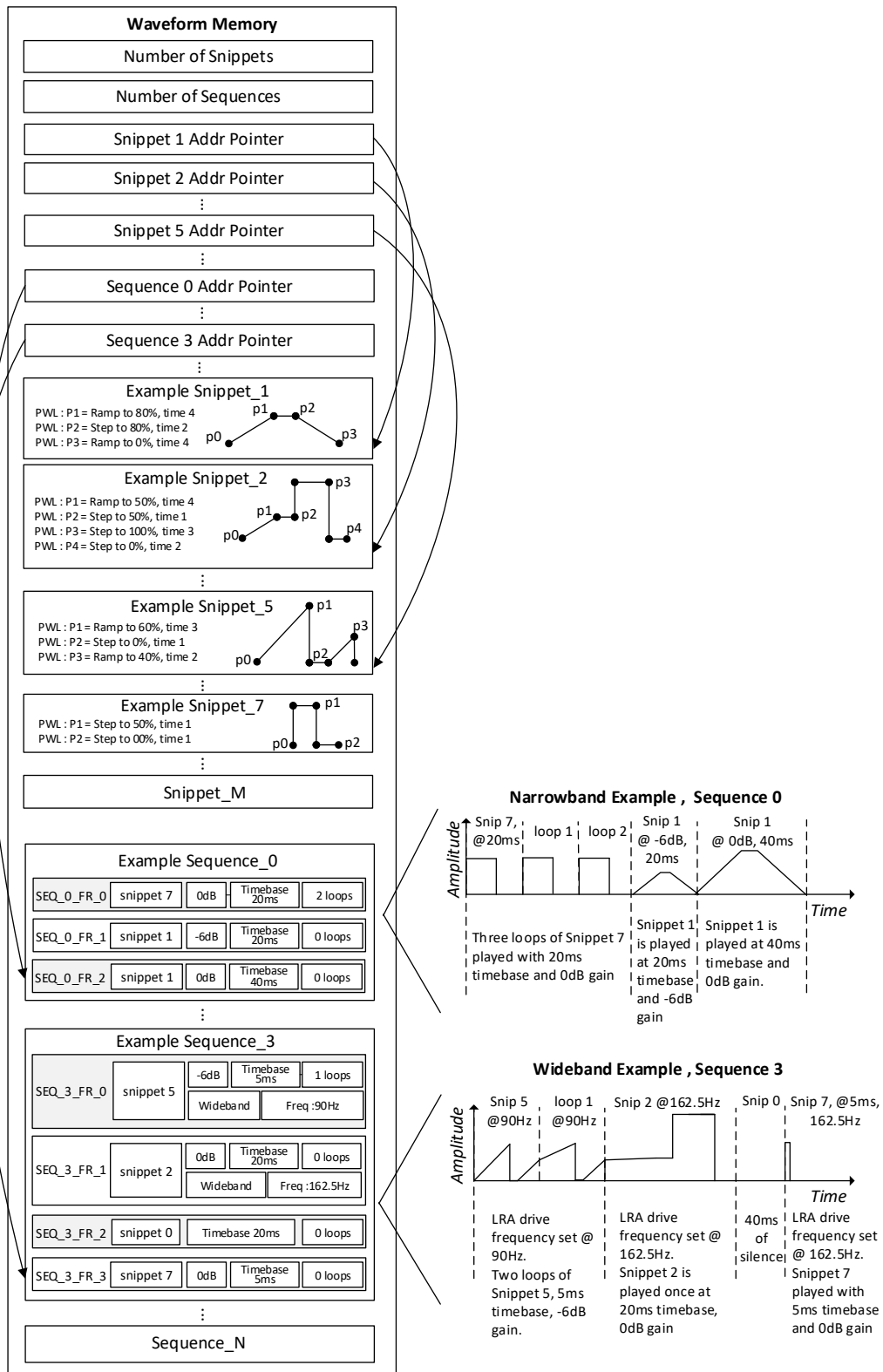
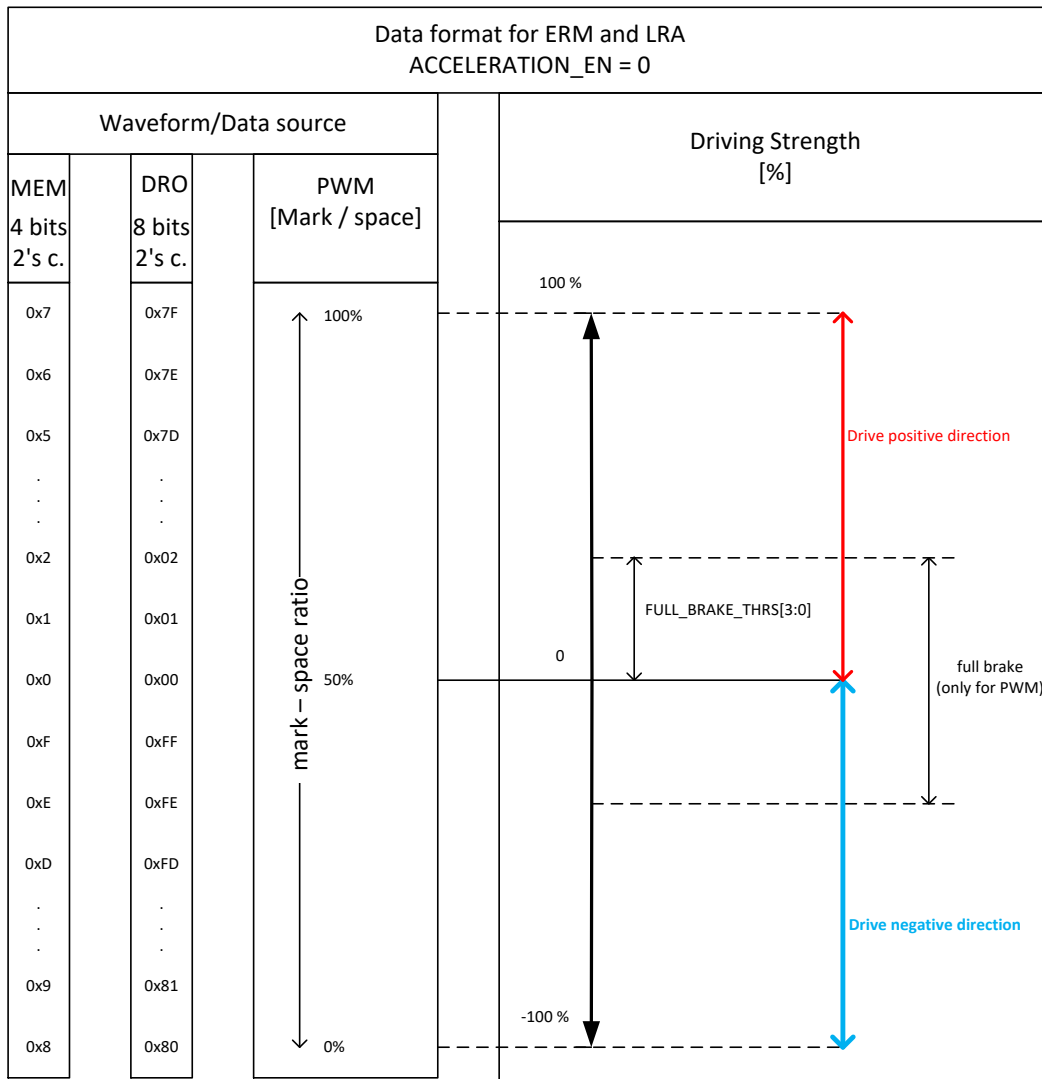


Figure 29: Waveform Memory Example

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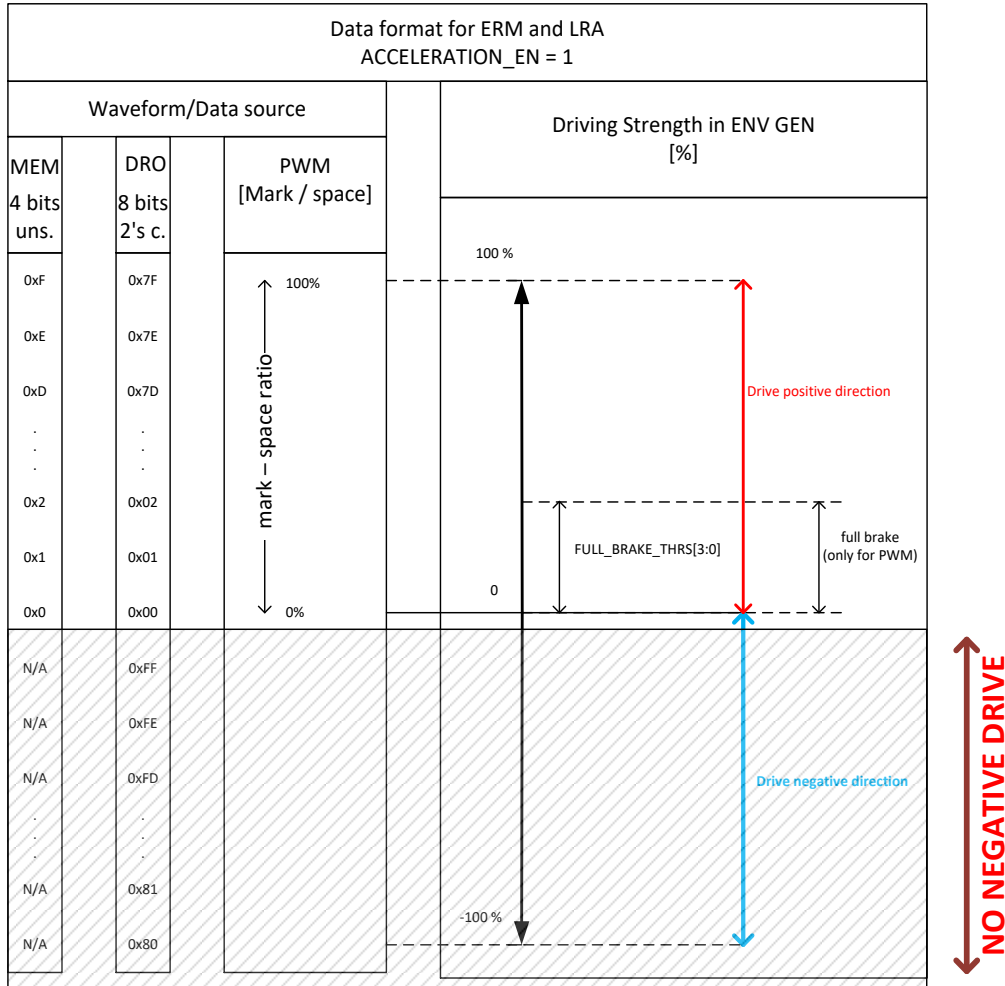
**5.9 General Data Format**

This section describes the data format used by the three different data input sources (DRO, PWM, and Waveform Memory). Four bits are used for storing the envelope value of snippets in Waveform Memory. Interpretation of the data is different depending on ACCELERATION\_EN. For an overview of the data interpretation with and without Active Acceleration enabled, see [Figure 30](#) and [Figure 31](#).



**Figure 30: Overview of Data Formats with Acceleration Disabled**

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**Figure 31: Overview of Data Formats with Acceleration Enabled**

**5.9.1 DRO Mode**

DRO data is supplied from I<sup>2</sup>C and is interpreted as 8-bit two's complement signed number.

- For ACCELERATION\_EN = 0:
  - The most negative value corresponds to -100 % driving strength.
  - The most positive value corresponds to +100 % driving strength.
  - A zero value corresponds to no drive.
  - The full range is between 127 (100 %) and -127 (-100 %), with -128 interpreted as -127 to keep the ranges symmetrical
- For ACCELERATION\_EN = 1:
  - Negative values are omitted and substituted with zero.
  - The most positive value corresponds to +100 % driving strength.
  - Zero value corresponds to no drive.



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### 5.9.2 PWM Mode

PWM provides mark / space ratio between 0 % and 100 %. The interpretation of duty cycle depends on the state of ACCELERATION\_EN.

- For ACCELERATION\_EN = 0:
  - A 0 % duty cycle corresponds to -100 % driving strength.
  - A 50 % duty cycle corresponds to no drive.
  - A 100 % duty cycle corresponds to +100 % driving strength.
  - FULL\_BRAKE\_THR defines a lower threshold for driving strength, below this threshold, drive is interpreted as zero.
- For ACCELERATION\_EN = 1:
  - A 0 % duty cycle corresponds to no drive.
  - A 50 % duty cycle corresponds to +50 % driving strength.
  - A 100 % duty cycle corresponds to +100 % driving strength.
  - Negative drive is not possible.
  - FULL\_BRAKE\_THR defines a lower threshold for driving strength, below this threshold, drive is interpreted as zero.

The encoded value of PWM data is converted to 8-bit two's complement data using the DRO format and is written to OVERRIDE\_VAL so it can be read back.

### 5.9.3 RTWM and ETWM Modes

- For ACCELERATION\_EN = 0:
  - The 4 bits of the amplitude value are interpreted as a two's complement signed value.
  - The most negative value corresponds to -100 % driving strength.
  - The most positive value corresponds to +100 % driving strength.
  - A zero value corresponds to no drive.
- The full range is between 7 (100 %) and -7 (-100 %), with -8 interpreted as -7 to keep the ranges symmetrical. ACCELERATION\_EN = 1
  - The 4 bits of the amplitude value are interpreted as an unsigned value.
  - The most positive value corresponds to +100 % driving strength.
  - Negative drive is not possible.
  - A zero value corresponds to no drive.

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 5.10 I<sup>2</sup>C Control Interface

DA7281 is software controlled from the host by registers accessed via an I<sup>2</sup>C compatible serial control interface. Data is shifted into or out of the DA7281 under the control of the host processor, which also provides the serial clock.

The DA7281 7-bit I<sup>2</sup>C default slave address is stored in register CIF\_I2C2, bits IF\_BASE\_ADDR and has a value of 0x4A (1001010 binary), which is equivalent to 0x94 (8-bit) for writing and 0x95 (8-bit) for reading. However, the two LSBs of the slave address are directly controlled by the ADDR\_1 and ADDR\_0 pins. The control is dynamic, which means that any change of the ADDR\_x pins during operation (VDD and VDDIO present) will result in the I<sup>2</sup>C base address changing to the new one presented by the ADDR\_x combination. The relationship between ADDR\_1 and ADDR\_0 to the default base address is summarized in [Table 19](#).

**Table 19: Relationship between ADDR\_x Pins and I<sup>2</sup>C Base and Effective Addresses**

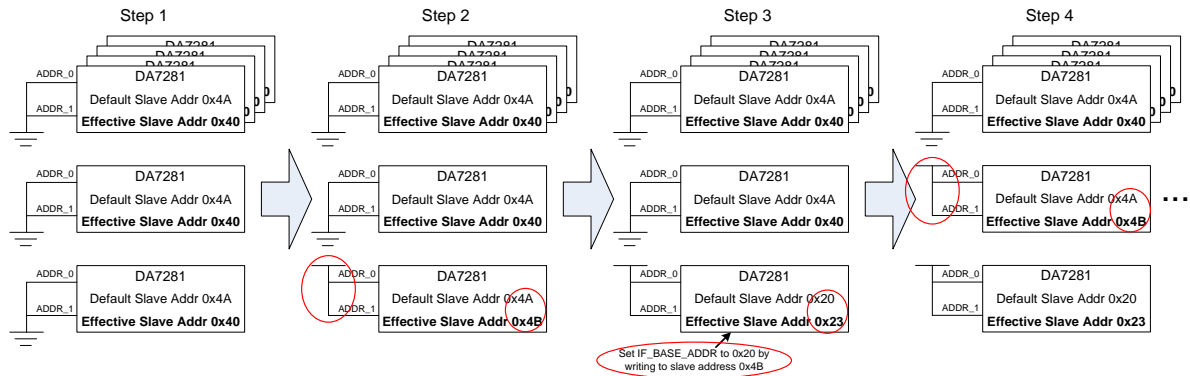
Default I <sup>2</sup> C Base Address (Stored in IF_BASE_ADDR) Hex / Binary	ADDR_1	ADDR_0	Effective I <sup>2</sup> C Base Address Hex / Binary
0x4A / 1001010	0 / GND	0 / GND	0x48 / 1001000
0x4A / 1001010	0 / GND	1 / VDDIO	0x49 / 1001001
0x4A / 1001010	1 / VDDIO	0 / GND	0x4A / 1001010
0x4A / 1001010	1 / VDDIO	1 / VDDIO	0x4B / 1001011

Up to four devices can be present in a system with a single I<sup>2</sup>C master by connecting the ADDR\_x pins to VDDIO or GND, see [Table 19](#). If more devices need to be instantiated, this could be done by modifying the base address register on some of them in the following procedure (GPI settings are for illustrative purposes, others can be used):

1. Power up VDD and VDDIO for all DA7281s present. Control ADDR\_x pins on each device individually with separate GPIOs on the host side. Keep all ADDR\_x pins connected to GND. Effective slave address for all devices is 0x48 (modified from the default 0x4A due to ADDR\_0 and ADDR\_1 being at GND).
2. On a single DA7281, change ADDR\_0 and ADDR\_1 to VDDIO and wait for 50  $\mu$ s. This is now the only device with an effective I<sup>2</sup>C address of 0x4B.
3. Change that device IF\_BASE\_ADDR bits to 0x20 via an I<sup>2</sup>C write to device address 0x4B. The effective address is 0x23 (due to ADDR\_0 and 1).
4. Repeat steps 2 to 3 as many times as need to activate all devices with unique I<sup>2</sup>C base addresses.

This procedure is shown in [Figure 32](#):

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

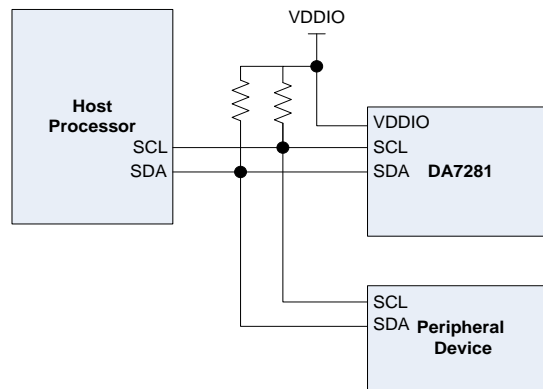


**Figure 32: Instantiating More than Four DA7281s in the Same System**

The I<sup>2</sup>C clock is supplied by the SCL line and the bidirectional I<sup>2</sup>C data is carried by the SDA line. The I<sup>2</sup>C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (1 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. This means that two devices cannot conflict if they drive the bus simultaneously.

DA7281 supports Standard-mode, Fast-mode, and Fast-mode Plus, with the highest frequency of the bus at 1 MHz in Fast-mode Plus. The exact frequency can be determined by the application and does not have any relation to the DA7281 internal clock signals. DA7281 will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow-down.

Communication on the I<sup>2</sup>C bus always takes place between two devices, one acting as the master and the other as the slave. The DA7281 will only operate as a slave.



**Figure 33: Schematic of the I<sup>2</sup>C Control Interface Bus**

All data is transmitted across the I<sup>2</sup>C bus in groups of eight bits. To send a bit the SDA line is driven to the intended state while the SCL is LOW (a LOW on SCL indicates a zero bit). Once the SDA has settled, the SCL line is brought HIGH and then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte for data. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master while the bus is in the Idle mode (the bus is free). It is initiated by a HIGH to LOW transition on the SDA line while the SCL is in the HIGH state (a STOP condition is indicated by a LOW to HIGH transition on the SDA line while the SCL line is in the HIGH state).

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support



**Figure 34: I<sup>2</sup>C START and STOP Conditions**

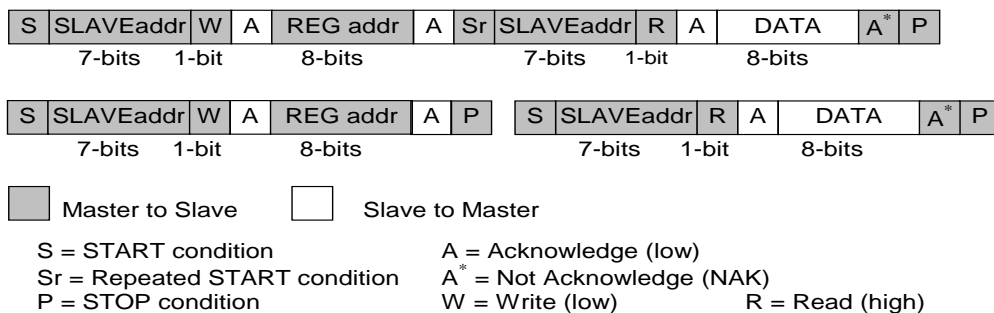
The I<sup>2</sup>C bus is monitored by DA7281 for a valid slave address whenever the interface is enabled. It responds with an Acknowledge immediately when it receives its own slave address. The Acknowledge is done by pulling the SDA line LOW during the following clock cycle (white blocks marked with A in Figure 35 to Figure 39).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (DA7281 responds to all bytes with Acknowledge), see Figure 35.



**Figure 35: I<sup>2</sup>C Byte Write (SDA line)**

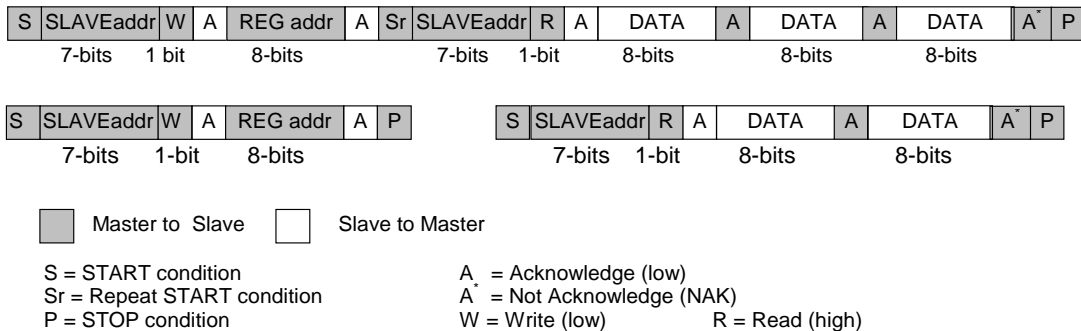
When the host reads data from a register it first has to write access DA7281 with the target register address and then read access DA7281 with a repeated START, or alternatively a second START condition. After receiving the data the host sends a Not Acknowledge (NAK) and terminates the transmission with a STOP condition:



**Figure 36: Examples of the I<sup>2</sup>C Byte Read (SDA line)**

Consecutive (Page) Read-Out mode, I2C\_WR\_MODE (register CIF\_I2C1) = 0, is initiated from the master by sending an Acknowledge instead of Not Acknowledge (NAK) after receipt of the data word. The I<sup>2</sup>C control block then increments the address pointer to the next I<sup>2</sup>C address and sends the data to the master. This enables an unlimited read of data bytes until the master sends an NAK directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent I<sup>2</sup>C address is read out, the DA7281 will return code zero.

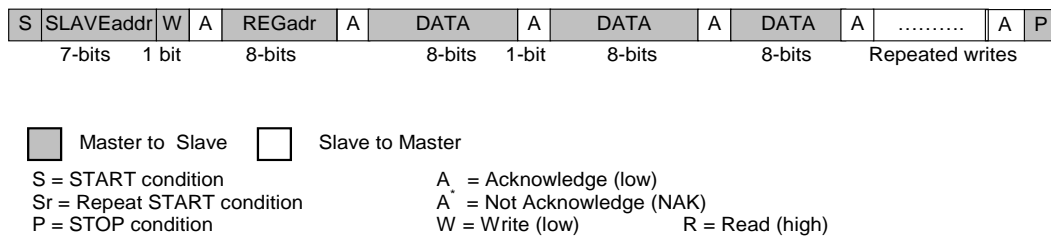
## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support



**Figure 37: Examples of I<sup>2</sup>C Page Read (SDA line)**

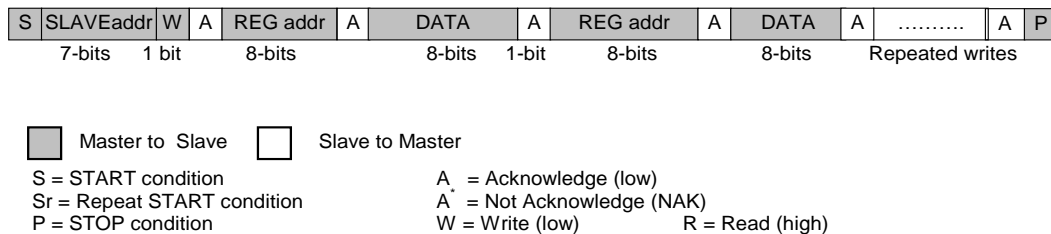
In Page mode the slave address after Sr (Repeated START condition) must be the same as the previous slave address.

Consecutive (Page) Write mode, I2C\_WR\_MODE = 0, is supported if the master sends several data bytes following a slave register address. The I<sup>2</sup>C control block then increments the address pointer to the next I<sup>2</sup>C address, stores the received data and sends an Acknowledge until the master sends the STOP condition.



**Figure 38: I<sup>2</sup>C Page Write (SDA line)**

An alternative Repeated-Write mode that uses non-consecutive slave register addresses is available using the CIF\_I2C1 register. In this Repeat Mode, I2C\_WR\_MODE = 1, the slave can be configured to support a host's repeated write operations into several non-consecutive registers. Data is stored at the previously received register address. If a new START or STOP condition occurs within a message, the bus returns to Idle mode. This is illustrated in Figure 39.



**Figure 39: I<sup>2</sup>C Repeated Write (SDA line)**

In Page mode, I2C\_WR\_MODE = 0, both Page mode reads and writes using auto-incremented addresses, and Repeat mode reads and writes using non auto-incremented addresses, are supported. In Repeat mode, I2C\_WR\_MODE = 1, however, only Repeat mode reads and writes are supported.

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 6 Register Overview

#### 6.1 Register Map

All register bits classed as Reserved are Read-Only and can be ignored.

**Table 20: Register Map**

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x00	CHIP_REV	CHIP_REV_MINOR<3:0>			CHIP_REV_MAJOR<3:0>					0xCA
0x03	IRQ_EVENT1	E_OC_FAULT	E_ACTUATOR_FAULT	E_WARNING	E_SEQ_FAULT	E_OVERTEMP_CRIT	E_SEQ_DONE	E_UVLO	E_SEQ_CONTINUE	0x00
0x04	IRQ_EVENT_WARNING_DIAG	E_LIM_DRIVE	E_LIM_DRIVE_AC	Reserved	E_MEM_TYPE	E_OVERTEMP_WARN	Reserved	Reserved	Reserved	0x00
0x05	IRQ_EVENT_SEQ_DIAG	E_SEQ_ID_FAULT	E_MEM_FAULT	E_PWM_FAULT	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x06	IRQ_STATUS1	STA_OC	STA_ACTUATOR	STA_WARNING	STA_SEQ_FAULT	STA_OVERTEMP_CRIT	STA_SEQ_DONE	STA_UVLO_VBAT_OK	STA_SEQ_CONTINUE	0x00
0x07	IRQ_MASK1	OC_M	ACTUATOR_M	WARNING_M	SEQ_FAULT_M	OVERTEMP_CRIT_M	SEQ_DONE_M	E_UVLO_M	SEQ_CONTINUE_M	0x00
0x08	CIF_I2C1	I2C_WRMODE	I2C_TO_ENABLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x40
0x09	CIF_I2C2	Reserved	IF_BASE_ADDR<6:0>							0x4A
0x0A	FRQ_LRA_PER_H	LRA_PER_H<7:0>								0x21
0x0B	FRQ_LRA_PER_L	Reserved	LRA_PER_L<6:0>							0x4F
0x0C	ACTUATOR1	ACTUATOR_NOMMAX<7:0>								0x5A
0x0D	ACTUATOR2	ACTUATOR_ABSMAX<7:0>								0x78
0x0E	ACTUATOR3	Reserved	Reserved	Reserved	IMAX<4:0>					0x17
0x0F	CALIB_V2I_H	V2I_FACTOR_H<7:0>								0x01
0x10	CALIB_V2I_L	V2I_FACTOR_L<7:0>								0x0D
0x11	CALIB_IMP_H	IMPEDANCE_H<7:0>								0x00
0x12	CALIB_IMP_L	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IMPEDANCE_L<1:0>		0x00
0x13	TOP_CFG1	EMBEDDED_MODE	Reserved	ACTUATOR_TYPE	BEMF_SENSITIVE	FREQ_TRACK_ENABLE	ACCELERATION_ENABLE	RAPID_STOP_ENABLE	AMP_PID_ENABLE	0x1E
0x14	TOP_CFG2	Reserved	Reserved	Reserved	MEM_DATA_SIGNED	FULL_BRAKE_THR<3:0>				0x01
0x15	TOP_CFG3	Reserved	Reserved	Reserved	Reserved	VDD_MARGIN<3:0>				0x03
0x16	TOP_CFG4	V2I_FACTOR_FR	CALIB_IMPEDANCE_DIS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x40
0x17	TOP_INT_CFG1	FRQ_LOCKED_LIM<5:0>						BEMF_FAULT_LIM<1:0>		0x81

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x1C	TOP_INT_CF G6_H	FRQ_PID_Kp_H<7:0>								0x0E
0x1D	TOP_INT_CF G6_L	FRQ_PID_Kp_L<7:0>								0x20
0x1E	TOP_INT_CF G7_H	FRQ_PID_Ki_H<7:0>								0x03
0x1F	TOP_INT_CF G7_L	FRQ_PID_Ki_L<7:0>								0x20
0x20	TOP_INT_CF G8	Reserved 0	RAPID_STOP_LIM<2:0>			FRQ_TRACK_BEMF_LIM<3:0>				0x43
0x22	TOP_CTL1	Reserved	Reserved	Reserved	SEQ_ST ART	STANDB Y_EN	OPERATION_MODE<2:0>			0x00
0x23	TOP_CTL2	OVERRIDE_VAL<7:0>								0x00
0x24	SEQ_CTL1	Reserved	Reserved	Reserved	Reserved	Reserved	FREQ_W AVEFOR M_TIME BASE	WAVEG EN_MOD E	SEQ_CO NTINUE	0x08
0x25	SWG_C1	CUSTOM_WAVE_GEN_COEFF1<7:0>								0x61
0x26	SWG_C2	CUSTOM_WAVE_GEN_COEFF2<7:0>								0xB4
0x27	SWG_C3	CUSTOM_WAVE_GEN_COEFF3<7:0>								0xEC
0x28	SEQ_CTL2	PS_SEQ_LOOP<3:0>				PS_SEQ_ID<3:0>				0x00
0x2B	GPI_CTL	Reserved	GPI_SEQUENCE_ID<3:0>				GPI_MO DE	GPI_POLARITY<1:0>		0x10
0x2C	MEM_CTL1	WAV_MEM_BASE_ADDR <7:0>								0x84
0x2D	MEM_CTL2	WAV_ME M_LOCK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserve d	0x80
0x2E	ADC_DATA_ H1	ADC_VDD_H<7:0>								0xFF
0x2F	ADC_DATA_ L1	Reserved	ADC_VDD_L<6:0>							0x7F
0x43	POLARITY	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	POLARI TY	0x00
0x44	LRA_AVR_H	LRA_PER_AVERAGE_H<7:0>								0x00
0x45	LRA_AVR_L	Reserved	LRA_PER_AVERAGE_L<6:0>							0x00
0x46	FRQ_LRA_P ER_ACT_H	LRA_PER_ACTUAL_H<7:0>								0x21
0x47	FRQ_LRA_P ER_ACT_L	Reserved	LRA_PER_ACTUAL_L<6:0>							0x4F
0x48	FRQ_PHASE _H	DELAY_H<7:0>								0x25
0x49	FRQ_PHASE _L	DELAY_ FREEZE	Reserved	Reserved	Reserved	Reserved	DELAY_SHIFT_L<2:0>			0x05
0x4C	FRQ_CTL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserve d	FREQ_T RACKIN G_AUTO _ADJ	FREQ_T RACKIN G_FORC E_ON	0x02
0x5F	TRIM3	Reserved	LOOP_ID AC_DOU BLE_RA NGE	LOOP_FI LT_LOW _BW	REF_UVLO_THRES		Reserve d	Reserved	Reserve d	0x0E
0x60	TRIM4	Reserved	Reserved	Reserved	Reserved	LOOP_FILT_CAP_TRI M<1:0>		LOOP_FILT_RES_TRI M<1:0>		0x9C

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x62	TRIM6	Reserved	Reserved	Reserved	Reserved	HBRIDGE_ERC_LS_TRIM<1:0>		HBRIDGE_ERC_HS_TRIM<1:0>		0x5F
0x6E	TOP_CFG5	Reserved	Reserved	Reserved	Reserved	Reserved	DELAY_BYPASS	FRQ_PAUSE_ON_POLARITY_CHANGE	V2I_FACTOR_OF_FSET_EN	0x01
0x81	IRQ_EVENT_ACTUATOR_FAULT	Reserved	E_TEST_ADC_STAT_FAULT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x82	IRQ_STATUS2	STA_ADC_STAT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x83	IRQ_MASK2	ADC_STAT_M	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x84 to 0xE7	SNP_MEM_x	SNP_MEM_x<7:0> where x = 0 to 99								0x00

## 6.2 Register Descriptions

**Table 21: CHIP\_REV (0x0000)**

Bit	Mode	Symbol	Description	Reset
[7:4]	RO	CHIP_REV_MINOR	Device revision code (minor)	0xC
[3:0]	RO	CHIP_REV_MAJOR	Device revision code (major)	0xA

**Table 22: IRQ\_EVENT1 (0x0003)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	E_OC_FAULT	Over-current / short-circuit fault on the OUTP or OUTN pin (write 1 to clear)	0x0
[6]	RW	E_ACTUATOR_FAULT	Actuator fault, see Section 5.6.6 (write 1 to clear)	0x0
[5]	RW	E_WARNING	System warnings Read IRQ_EVENT_WARNING_DIAG for warning diagnostic (write 1 to clear)	0x0
[4]	RW	E_SEQ_FAULT	Sequence faults: SEQ_ID_FAULT, memory fault or PWM fault Read IRQ_EVENT_SEQ_DIAG for diagnostic information (write 1 to clear)	0x0
[3]	RW	E_OVERTEMP_CRIT	Critical chip temperature event, chip temperature has exceeded the critical limit of 125 °C (write 1 to clear)	0x0
[2]	RW	E_SEQ_DONE	IRQ indicating that sequence playback from waveform memory is complete (write 1 to clear)	0x0



## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Bit	Mode	Symbol	Description	Reset
[1]	RW	E_UVLO	Under-voltage fault, supply below the UVLO threshold Clear to attempt restart (write 1 to clear)	0x0
[0]	RW	E_SEQ_CONTINUE	IRQ indicating that playback of a new sequence has occurred because SEQ_CONTINUE is set to 1 (write 1 to clear)	0x0

**Table 23: IRQ\_EVENT\_WARNING\_DIAG (0x0004)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	E_LIM_DRIVE	IRQ indicating that playback is limited because the power supply level is lower than the sequence target (write 1 to E_WARNING to clear)	0x0
[6]	RW	E_LIM_DRIVE_ACC	IRQ indicating that acceleration is limited because the power supply level is lower than required for the acceleration target (write 1 to E_WARNING to clear)	0x0
[4]	RW	E_MEM_TYPE	Indicates that the memory data type configured in register MEM_DATA_SIGNED does not match the acceleration configuration (ACCELERATION_EN). MEM_DATA_SIGNED = 1 for ACCELERATION_EN = 0 MEM_DATA_SIGNED = 0 for ACCELERATION_EN = 1 (write 1 to E_WARNING to clear)	0x0
[3]	RW	E_OVERTEMP_WARN	Over-temperature warning, chip temperature has exceeded the warning limit of 105 °C (write 1 to E_WARNING to clear)	0x0

**Table 24: IRQ\_EVENT\_SEQ\_DIAG (0x0005)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	E_SEQ_ID_FAULT	IRQ indicating that requested sequence ID configured in PS_SEQ_ID is not valid (write 1 to E_SEQ_FAULT to clear)	0x0
[6]	RW	E_MEM_FAULT	Indicates that the Waveform Memory is corrupted (empty, invalid snippet ID, invalid frame structure) (write 1 to E_SEQ_FAULT to clear)	0x0
[5]	RW	E_PWM_FAULT	IRQ indicating that the PWM input signal has timed out (write 1 to E_SEQ_FAULT to clear)	0x0

**Table 25: IRQ\_STATUS1 (0x0006)**

Bit	Mode	Symbol	Description	Reset
[7]	RO	STA_OC	Over-current / short circuit fault status	0x0
[6]	RO	STA_ACTUATOR	Actuator fault status	0x0
[5]	RO	STA_WARNING	System warnings status	0x0
[4]	RO	STA_PAT_FAULT	Sequence faults status	0x0

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Bit	Mode	Symbol	Description	Reset
[3]	RO	STA_OVERTEMP_CRIT	Over-temperature status	0x0
[2]	RO	STA_PAT_DONE	Memory based sequence status	0x0
[1]	RO	STA_UVLO_VBAT_OK	UVLO output status: 0 during normal operation; 1 if there is a UVLO event	0x0
[0]	RO	STA_SEQ_CONTINUE	Continuous sequence status	0x0

**Table 26: IRQ\_MASK1 (0x0007)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	OC_M	Over-current / short circuit fault mask	0x0
[6]	RW	ACTUATOR_M	Actuator fault mask	0x0
[5]	RW	WARNING_M	System warnings mask	0x0
[4]	RW	SEQ_FAULT_M	Sequence faults mask	0x0
[3]	RW	OVERTEMP_CRIT_M	Over-temperature fault mask	0x0
[2]	RW	SEQ_DONE_M	Memory based sequence interrupt mask	0x0
[1]	RW	E_UVLO_M	Soft shutdown fault mask	0x0
[0]	RW	SEQ_CONTINUE_M	Continuous sequence interrupt mask	0x0

**Table 27: CIF\_I2C1 (0x0008)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	I2C_WR_MODE	I <sup>2</sup> C write mode <b>0x0 = Auto-increment (addr, data, data, data,...)</b> <b>0x1 = Repeat (addr, data, addr, data,...)</b>	0x0
[6]	RW	I2C_TO_ENABLE	I <sup>2</sup> C timeout enable. If there are no negative edges on SCL for approx. 35 ms, the slave resets. <b>0x0 = Disabled</b> <b>0x1 = Enabled</b>	0x1

**Table 28: CIF\_I2C2 (0x0009)**

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	I2C_BASE_ADDR	I <sup>2</sup> C base address	0x4A

**Table 29: FRQ\_LRA\_PER\_H (0x000A)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	LRA_PER_H	Used for specifying the LRA drive frequency. MS-bits of the initial LRA resonant frequency period.  $LRA\_PER[14:0] = \frac{1}{LRA_{freq} \times 1333.32 \times 10^{-9}}$	0x21

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Bit	Mode	Symbol	Description	Reset
			$\begin{aligned} &LRA\_PER\_H[7:0] \\ &= \frac{LRA\_PER[14:0] - LRA\_PER\_L[6:0]}{128} \\ \\ &LRA\_PER\_L[6:0] \\ &= LRA\_PER[14:0] \\ &\quad - 128 \times LRA\_PER\_H[7:0] \end{aligned}$ <p>Where <math>LRA_{freq}</math> represents the LRA resonant frequency (in Hz) as listed in the actuator datasheet. See Section 5.6.2.  <b>Default corresponds to 174 Hz.</b></p>	

**Table 30: FRQ\_LRA\_PER\_L (0x000B)**

Bit	Mode	Symbol	Description	Reset
[6:0]	RW	LRA_PER_L	<p>Used for specifying the LRA drive frequency. LS-bits of the initial LRA resonant frequency period.</p> $LRA\_PER[14:0] = \frac{1}{LRA_{freq} \times 1333.32 \times 10^{-9}}$ $LRA\_PER\_H[7:0] = \frac{LRA\_PER[14:0] - LRA\_PER\_L[6:0]}{128}$ $LRA\_PER\_L[6:0] = LRA\_PER[14:0] - 128 \times LRA\_PER\_H[7:0]$ <p>Where <math>LRA_{freq}</math> represents the LRA resonant frequency in Hz as listed in the actuator datasheet. See Section 5.6.2.  <b>Default corresponds to 174 Hz.</b></p>	0x4F

**Table 31: ACTUATOR1 (0x000C)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	ACTUATOR_NO MMAX	<p>Nominal actuator voltage rating, unsigned, see Section 5.6.2  Sets full-scale of unsigned haptic waveform when acceleration enabled (ACCELERATION_EN = 1)</p> $ACTUATOR\_NOMMAX = \frac{V_{actuator\_nommax}}{23.4 \times 10^{-3}}$ <p><b>Default: 0x5A = 2.106 V</b></p>	0x5A

**Table 32: ACTUATOR2 (0x000D)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	ACTUATOR_AB SMAX	<p>Absolute actuator maximum voltage rating, see Section 5.6.2.  Overdrive is limited to this value when acceleration enabled (ACCELERATION_EN = 1)</p>	0x78

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Bit	Mode	Symbol	Description	Reset
			Sets full-scale of unsigned haptic waveform when acceleration disabled  $ACTUATOR\_ABSMAX = \frac{V_{actuator\_absmax}}{23.4 \times 10^{-3}}$ <b>Default: 0x78 = 2.808 V</b>	

**Table 33: ACTUATOR3 (0x000E)**

Bit	Mode	Symbol	Description	Reset
[4:0]	RW	IMAX	Actuator max current rating  $IMAX = \frac{I_{max\_actuator\_mA} - 28.6}{7.2}$ where $I_{max\_actuator\_mA}$ is the actuator max rated current in mA, as listed in its datasheet, see Section 5.6.2. <b>Default: 0x17 = 194 mA</b>	0x17

**Table 34: CALIB\_V2I\_H (0x000F)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	V2I_FACTOR_H	MS-bits for translating actuator impedance to output voltage drive level  $V2I\_FACTOR[15:0] = \frac{Z \times (IMAX[4:0] + 4)}{1.6104}$ $V2I\_FACTOR\_H[7:0] = \frac{V2I\_FACTOR[15:0] - V2I\_FACTOR\_L[7:0]}{256}$ $V2I\_FACTOR\_L[7:0] = V2I\_FACTOR[15:0] - 256 \times V2I\_FACTOR\_H[7:0]$ Where $V2I\_FACTOR[15:0]$ is the 16-bit concatenation of $V2I\_FACTOR\_H[7:0]$ and $V2I\_FACTOR\_L[7:0]$ , Z is the impedance of the actuator in $\Omega$ (as read from its datasheet), and $IMAX[4:0]$ is the 5-bit value of IMAX, see Section 5.6.2.	0x01

**Table 35: CALIB\_V2I\_L (0x0010)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	V2I_FACTOR_L	LS-bits for translating actuator impedance to output voltage drive level  $V2I\_FACTOR[15:0] = \frac{Z \times (IMAX[4:0] + 4)}{1.6104}$	0x0D

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Bit	Mode	Symbol	Description	Reset
			$V2I\_FACTOR\_H[7:0] = \frac{V2I\_FACTOR[15:0] - V2I\_FACTOR\_L[7:0]}{256}$ $V2I\_FACTOR\_L[7:0] = V2I\_FACTOR[15:0] - 256 \times V2I\_FACTOR\_H[7:0]$ <p>Where V2I_FACTOR[15:0] is the 16-bit concatenation of V2I_FACTOR_H[7:0] and V2I_FACTOR_L[7:0], Z is the impedance of the actuator in <math>\Omega</math> (as read from its datasheet), and IMAX[4:0] is the 5-bit value of IMAX, see Section 5.6.2.</p>	

**Table 36: CALIB\_IMP\_H (0x0011)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	IMPEDANCE_H	MS-bits of calculated impedance ( <b>default 22 <math>\Omega</math></b> ), see Section 5.7.3. $Impedance (\Omega) = 4 \times 62.5 \times 10^{-3} \times IMPEDANCE\_H + 62.5 \times 10^{-3} \times IMPEDANCE\_L$	0x00

**Table 37: CALIB\_IMP\_L (0x0012)**

Bit	Mode	Symbol	Description	Reset
[1:0]	RO	IMPEDANCE_L	LS-bits of calculated impedance ( <b>default 22 <math>\Omega</math></b> ), see Section 5.7.3. $Impedance (\Omega) = 4 \times 62.5 \times 10^{-3} \times IMPEDANCE\_H + 62.5 \times 10^{-3} \times IMPEDANCE\_L$	0x0

**Table 38: TOP\_CFG1 (0x0013)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	EMBEDDED_M ODE	Embedded operation enable (self-clearing IRQs), see Section 5.7.7. <b>0x0 = Faults cleared by host</b> 0x1 = DA7281 clears faults automatically	0x0
[5]	RW	ACTUATOR_TY PE	Specifies actuator type: LRA or ERM, see Section 5.6.2. <b>0x0 = LRA</b> 0x1 = ERM	0x0
[4]	RW	BEMF_SENSE_ EN	Enable internal loop computations; should be disabled only in custom waveform and wideband operation, see Sections 5.7.5 and 5.7.6. 0x0 = Custom Waveform Operation <b>0x1 = Standard Operation</b>	0x1

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Bit	Mode	Symbol	Description	Reset
[3]	RW	FREQ_TRACK_EN	Enable resonant frequency tracking; ignored in ERM mode, see Section 5.3. 0x0 = frequency tracking disabled <b>0x1 = frequency tracking enabled</b>	0x1
[2]	RW	ACCELERATION_EN	Enable Active Acceleration, see Section 5.4. 0x0 = Active Acceleration disabled <b>0x1 = Active Acceleration enabled</b>	0x1
[1]	RW	RAPID_STOP_EN	Enable Rapid Stop, see Section 5.4. 0x0 = Rapid Stop disabled <b>0x1 = Rapid Stop enabled</b>	0x1
[0]	RW	AMP_PID_EN	Enable Amplitude PID, see Section 5.4. <b>0x0 = Amplitude PID disabled</b> 0x1 = Amplitude PID enabled	0x0

Table 39: TOP\_CFG2 (0x0014)

Bit	Mode	Symbol	Description	Reset
[4]	RW	MEM_DATA_SIGNED	Memory data format; set according to the value of ACCELERATION_EN: <b>0x0 = unsigned (for ACCELERATION_EN = 1)</b> 0x1 = signed (for ACCELERATION_EN = 0)	0x0
[3:0]	RW	FULL_BRAKE_THR	Full-brake threshold for PWM mode with step size 6.66%, see Section 5.2.5. 0x0 = brake threshold disabled <b>0x1 = 6.66 % of ACTUATOR_NOMMAX</b> 0x2 = 13.33 % of ACTUATOR_NOMMAX ... ~6.66% steps... 0x15 = 100 % of ACTUATOR_NOMMAX	0x1

Table 40: TOP\_CFG3 (0x0015)

Bit	Mode	Symbol	Description	Reset
[3:0]	RW	VDD_MARGIN	V <sub>DD</sub> margin setting. Target voltage needs to be below V <sub>DD</sub> - VDD_MARGIN, otherwise voltage is clamped to V <sub>DD</sub> - VDD_MARGIN and a LIM_DRIVE IRQ is generated. See Section 5.7.13 for further details. 0x0 = 0 mV 0x1 = 187.5 mV 0x2 = 375 mV <b>0x3 = 562.5 mV</b> ... 187.5 mV steps... 0xF = 2.8125 V	0x3

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**Table 41: TOP\_CFG4 (0x0016)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	V2I_FACTOR_FREEZE	Stop automatic updates to V2I_FACTOR_x, see Section 5.7.3. <b>0x0 = updates enabled</b> 0x1 = updates disabled	0x0
[6]	RW	CALIB_IMPEDANCE_DIS	Stop automatic updates to V2I_FACTOR_x during playback, see Section 5.7.3. 0x0 = updates enabled <b>0x1 = updates disabled</b>	0x1

**Table 42: TOP\_INT\_CFG1 (0x0017)**

Bit	Mode	Symbol	Description	Reset
[7:2]	RW	FRQ_LOCKED_LIM	Limit for generating frequency locked signal that enabled scaling of the frequency tracking PID gain, see Section 5.7.1. If error is below the FRQ_LOCKED_LIM*4 frequency is locked	0x20
[1:0]	RW	BEMF_FAULT_LIM	Limit for BEMF fault generation. If voltage is below the threshold BEMF, a fault is generated, see Section 5.7.14. 0x0 = BEMF fault disabled <b>0x1 = 4.9 mV</b> 0x2 = 27.9 mV 0x3 = 49.9 mV	0x1

**Table 43: TOP\_INT\_CFG6\_H (0x001C)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Kp_H	MS-bits of the frequency tracking loop PID Kp proportional coefficient, see Section 5.7.1 for details	0x0E

**Table 44: TOP\_INT\_CFG6\_L (0x001D)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Kp_L	LS-bits of the frequency tracking loop PID Kp proportional coefficient, see Section 5.7.1 for details	0x20

**Table 45: TOP\_INT\_CFG7\_H (0x001E)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Ki_H	MS-bits of the frequency tracking loop PID Ki integral coefficient, see Section 5.7.1 for details	0x03

**Table 46: TOP\_INT\_CFG7\_L (0x001F)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	FRQ_PID_Ki_L	LS-bits of the frequency tracking loop PID Ki integral coefficient, see Section 5.7.1 for details	0x20

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**Table 47: TOP\_INT\_CFG8 (0x0020)**

Bit	Mode	Symbol	Description	Reset
[6:4]	RW	RAPID_STOP_LIM	Selects the Rapid Stop threshold at which DA7281 stops driving while braking, see Section 5.7.2	0x4
[3:0]	RW	FRQ_TRACK_BEMF_LIM	Selects the frequency tracking threshold at which DA7281 pauses frequency tracking, see Section 5.7.1	0x3

**Table 48: TOP\_CTL1 (0x0022)**

Bit	Mode	Symbol	Description	Reset
[4]	RW	SEQ_START	Start/stop control of Waveform Memory sequence playback <b>0x0 = Stop playback and return to IDLE state</b> 0x1 = Start playback	0x0
[3]	RW	STANDBY_EN	Sets the state DA7281 returns to after completion of playback, see Section 5.2.1. <b>0x0 = Return to IDLE state after playback</b> 0x1 = Return to STANDBY state after playback	0x0
[2:0]	RW	OPERATION_MODE	Haptic operation mode, see Section 5.2. <b>0x0 = Inactive mode</b> 0x1 = Direct register override (DRO) mode 0x2 = Playback from PWM data source (PWM) mode 0x3 = Register triggered waveform memory (RTWM) mode 0x4 = Edge triggered waveform memory (ETWM) mode	0x0

**Table 49: TOP\_CTL2 (0x0023)**

Bit	Mode	Symbol	Description	Reset																											
[7:0]	RW	OVERRIDE_VAL	Used to set the output drive level in DRO mode. Scales the contents of ACTUATOR_ABSMAX and/or ACTUATOR_NOMMAX, depending on whether Active Acceleration is enabled. See Section 5.2.4. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">OVERRIDE_VAL Value</th> <th style="width: 25%;">Scaling factor when ACCELERATION_EN = 0</th> <th style="width: 25%;">Scaling factor when ACCELERATION_EN = 1</th> </tr> </thead> <tbody> <tr> <td>0x7F</td> <td>1</td> <td>1</td> </tr> <tr> <td>0x7E</td> <td>0.992</td> <td>0.992</td> </tr> <tr> <td>...</td> <td>...step of 0.008...</td> <td>...step of 0.008...</td> </tr> <tr> <td>0x01</td> <td>0.0079</td> <td>0.0079</td> </tr> <tr> <td>0x00</td> <td>0</td> <td>0</td> </tr> <tr> <td>0xFF</td> <td>-0.0079</td> <td>0</td> </tr> <tr> <td>...</td> <td>...step of 0.008...</td> <td>...step of 0.008...</td> </tr> <tr> <td>0x81</td> <td>-1</td> <td>0</td> </tr> </tbody> </table>	OVERRIDE_VAL Value	Scaling factor when ACCELERATION_EN = 0	Scaling factor when ACCELERATION_EN = 1	0x7F	1	1	0x7E	0.992	0.992	...	...step of 0.008...	...step of 0.008...	0x01	0.0079	0.0079	0x00	0	0	0xFF	-0.0079	0	...	...step of 0.008...	...step of 0.008...	0x81	-1	0	0x0
OVERRIDE_VAL Value	Scaling factor when ACCELERATION_EN = 0	Scaling factor when ACCELERATION_EN = 1																													
0x7F	1	1																													
0x7E	0.992	0.992																													
...	...step of 0.008...	...step of 0.008...																													
0x01	0.0079	0.0079																													
0x00	0	0																													
0xFF	-0.0079	0																													
...	...step of 0.008...	...step of 0.008...																													
0x81	-1	0																													



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Bit	Mode	Symbol	Description	Reset
			0x80      -1      0	

**Table 50: SEQ\_CTL1 (0x0024)**

Bit	Mode	Symbol	Description	Reset
[2]	RW	FREQ_WAVEFORM_TIMEBASE	Frequency waveform timebase setting for waveform memory frames. See Section 5.8.3. <b>0x0    5.44, 21.76, 43.52, 87.04 ms</b> 0x1    1.36, 5.44, 21.76, 43.52 ms	0x0
[1]	RW	WAVEGEN_MODE	Enable bit for custom waveform operation, see Section 5.7.5. <ul style="list-style-type: none"> <li>• If WAVEGEN_MODE = 0, then set BEMF_SENSE_EN = 1</li> <li>• If WAVEGEN_MODE = 1, then set BEMF_SENSE_EN = 0</li> </ul> <b>0x0 = Normal wave mode (step/ramp sequences)</b> 0x1 = Custom wave mode (sinewave sequences)	0x0
[0]	RW	SEQ_CONTINUE	Control for back-to-back Waveform Memory sequence playback during RTWM and ETWM modes. If SEQ_CONTINUE = 1, new sequence playback starts at end of current sequence. Register is self-cleared when the next sequence is started, see Section 5.6.5.	0x0

**Table 51: SWG\_C1 (0x0025)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	CUSTOM_WAVE_GEN_COEFF1	Coefficient1 for custom wave generation, represents a proportion of the set IMAX, see Section 5.7.5. Default corresponds to a sine wave. 0x00 = 0 % 0x01 = 0.4 % ...      ...steps of approx. 0.4 % <b>0x61 = 37.9 %</b> ...      ...steps of approx. 0.4 % 0xFF = 100 %	0x61

**Table 52: SWG\_C2 (0x0026)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	CUSTOM_WAVE_GEN_COEFF2	Coefficient2 for custom wave generation, represents a proportion of the set IMAX, see Section 5.7.5. Default corresponds to a sine wave. 0x00 = 0 % 0x01 = 0.4 % ...      ...steps of approx. 0.4 % <b>0xB4 = 70.3 %</b> ...      ...steps of approx. 0.4 % 0xFF = 100 %	0xB4

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**Table 53: SWG\_C3 (0x0027)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	CUSTOM_WAVE_GEN_COEFF3	Coefficient1 for custom wave generation, represents a proportion of the set IMAX, see Section 5.7.5. Default corresponds to a sine wave. 0x00 = 0 % 0x01 = 0.4 % ... ..steps of approx. 0.4 % <b>0xEC = 92.2 %</b> ... ..steps of approx. 0.4 % 0xFF = 100 %	0xEC

**Table 54: SEQ\_CTL2 (0x0028)**

Bit	Mode	Symbol	Description	Reset
[7:4]	RW	PS_SEQ_LOOP	Number of times the pre-stored sequence (pointed to by PS_SEQ_ID) is repeated, see Section 5.6.5. <b>0x0 = No repetition (sequence played once)</b> 0x1 = 1 repetition (sequence played twice) ... ..step of 1... 0xF = 15 repetitions (sequence played 16 times)	0x0
[3:0]	RW	PS_SEQ_ID	ID of pre-stored and read-back of GPI triggered sequence, see Section 5.6.5.4.	0x0

**Table 55: GPI\_CTL (0x002B)**

Bit	Mode	Symbol	Description	Reset
[6:3]	RW	GPI_SEQUENCE_ID	GPI mode of operation, see Section 5.2.7.	0x2
[2]	RW	GPI_MODE	GPI mode of operation, see Section 5.2.7. <b>0x0 = Single sequence</b> 0x1 = Multi-sequence	0x0
[1:0]	RW	GPI_POLARITY	Selection which GPI edge triggers an event: <b>0x0 = Rising edge</b> 0x1 = Falling edge 0x2 = Both edges	0x0

**Table 56: MEM\_CTL1 (0x002C)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	WAV_MEM_BASE_ADDR	Snippet memory start address, see Section 5.8.	0x84

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Table 57: MEM\_CTL2 (0x002D)

Bit	Mode	Symbol	Description	Reset
[7]	RW	WAV_MEM_LOCK	Lock bit for preventing access to Waveform Memory, see Section 5.6.4. 0x0 = Locked <b>0x1 = Unlocked</b>	0x1

Table 58: ADC\_DATA\_H1 (0x002E)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	ADC_VDD_H	Unsigned VDD measurement, see Section 5.7.13 <i>VDD Supply Voltage</i> $= (ADC\_VDD\_H \times 128 + ADC\_VDD\_L) \times 0.1831mV$	0xFF

Table 59: ADC\_DATA\_L1 (0x002F)

Bit	Mode	Symbol	Description	Reset
[6:0]	RO	ADC_VDD_L	Unsigned VDD measurement, see Section 5.7.13 <i>VDD Supply Voltage</i> $= (ADC\_VDD\_H \times 128 + ADC\_VDD\_L) \times 0.1831mV$	0x7F

Table 60: POLARITY (0x0043)

Bit	Mode	Symbol	Description	Reset
[0]	RO	POLARITY	Current polarity read-back, see Section 5.7.8	0x0

Table 61: LRA\_AVR\_H (0x0044)

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	LRA_PER_AVERAGE_H	MS-bits of the average LRA resonant period based on the last four half-periods, see Section 5.7.1. The following formula describes the output: <i>LRA period (ms)</i> $= 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_AVERAGE\_H + LRA\_PER\_AVERAGE\_L)$	0x0

Table 62: LRA\_AVR\_L (0x0045)

Bit	Mode	Symbol	Description	Reset
[6:0]	RO	LRA_PER_AVERAGE_L	LS-bits of the average LRA resonant period based on the last four half-periods, see Section 5.7.1. The following formula describes the output:	0x0

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Bit	Mode	Symbol	Description	Reset
			$LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_AVERAGE\_H + LRA\_PER\_AVERAGE\_L)$	

**Table 63: FRQ\_LRA\_PER\_ACT\_H (0x0046)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RO	LRA_PER_ACTUAL_H	MS-bits of the actual LRA resonant period based on half-period, see Section 5.5. The following formula describes the output: $LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_ACTUAL\_H + LRA\_PER\_ACTUAL\_L)$	0x21

**Table 64: FRQ\_LRA\_PER\_ACT\_L (0x0047)**

Bit	Mode	Symbol	Description	Reset
[6:0]	RO	LRA_PER_ACTUAL_L	LSBs of the actual LRA resonant period based on half-period, see Section 5.5. The following formula describes the output: $LRA\ period\ (ms) = 1333.32 \times 10^{-9} \times (128 \times LRA\_PER\_ACTUAL\_H + LRA\_PER\_ACTUAL\_L)$	0x4F

**Table 65: FRQ\_PHASE\_H (0x0048)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	DELAY_H	Used during custom waveform operation, see Section 5.7.5. Only use the following settings, all other settings are reserved: 0x0 = Setting for wideband mode <b>0x25 = Setting for closed-loop frequency tracking mode</b>	0x25

**Table 66: FRQ\_PHASE\_L (0x0049)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	DELAY_FREEZE	Used during custom waveform operation. Set to 1 only in wideband mode with frequency tracking disabled, see Section 5.7.5 <b>0x0 = Setting for closed-loop frequency tracking mode</b> 0x1 = Setting for wideband mode	0x0

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

Bit	Mode	Symbol	Description	Reset
[2:0]	RW	DELAY_SHIFT_L	Used during custom waveform operation, see Section 5.7.5. Only use the following settings, all other settings are reserved: 0x0 = Setting for wideband mode <b>0x5 = Setting for closed-loop frequency tracking mode</b>	0x5

Table 67: FRQ\_CTL (0x004C)

Bit	Mode	Symbol	Description	Reset
[1]	RW	FREQ_TRACKING_AUTO_ADJ	Enables the auto-scaling of the frequency tracking proportional coefficient, see Section 5.7.1. 0x0 = No auto-scaling <b>0x1 = Auto-scaling</b>	0x1
[0]	RW	FREQ_TRACKING_FORCE_ON	Force the tracking on when the error exceeds 25 % of initial guess, see Section 5.7.1. <b>0x0 = Off</b> 0x1 = On	0x0

Table 68: TRIM3 (0x005F)

Bit	Mode	Symbol	Description	Reset
[6]	RW	LOOP_IDAC_DOUBLE_RANGE	Loop IDAC double range control, see Section 5.7.12	0x0
[5]	RW	LOOP_FILTER_LOW_BANDWIDTH	Loop filter low bandwidth, see Section 5.7.9	0x0
[4:3]	RW	REF_UVLO_THRESH	UVLO threshold, see Section 5.7.10 00 = 2.7 V <b>01 = 2.8 V</b> 10 = 2.9 V 11 = 3.0 V	0x1

Table 69: TRIM4 (0x0060)

Bit	Mode	Symbol	Description	Reset
[3:2]	RW	LOOP_FILTER_CAP_TRIM	Loop capacitor trim, see Section 5.7.9	0x3
[1:0]	RW	LOOP_FILTER_RES_TRIM	Loop resistance trim, see Section 5.7.9	0x0

Table 70: TRIM6 0x(0062)

Bit	Mode	Symbol	Description	Reset
[3:2]	RW	HBRIDGE_EDGE_RATE_CONTROL_SETTING_TRIM	Low side edge rate control setting, see Section 5.7.11. 00 = 25 mV/ns 01 = 50 mV/ns	0x3

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

Bit	Mode	Symbol	Description	Reset
			10 = 75 mV/ns <b>11 = 100 mV/ns</b>	
[1:0]	RW	HBRIDGE_ERC_HS_TRIM	High side edge rate control setting, see Section 5.7.11 00 = 25 mV/ns 01 = 50 mV/ns 10 = 75 mV/ns <b>11 = 100 mV/ns</b>	0x3

**Table 71: D2602\_TOP\_CFG5 (0x006E)**

Bit	Mode	Symbol	Description	Reset
[2]	RW	DELAY_BYPASS	Delay comparator bypass enable	0x0
[1]	RW	FRQ_PAUSE_ON_POLARITY_CHANGE	Pause the frequency update when the drive polarity changes (during rapid stop, negative acceleration, negative DRO value) <b>0x0 = Pause disabled</b> 0x1 = Pause enabled	0x0
[0]	RW	V2I_FACTOR_OFFSET_EN	Apply a 50 mV offset to the V2I factor calculation 0x0 = No offset applied <b>0x1 = 50 mV offset applied</b>	0x1

**Table 72: IRQ\_EVENT\_ACTUATOR\_FAULT (0x0081)**

Bit	Mode	Symbol	Description	Reset
[2]	RO	ADC_SAT_FAULT	ADC produced saturated result, which is not expected to happen (write 1 to E_ACTUATOR to clear)	0x0

**Table 73: IRQ\_STATUS2 (0x0082)**

Bit	Mode	Symbol	Description	Reset
[7]	RO	STA_ADC_SAT	Status of ADC saturation fault: ADC_SAT_FAULT	0x0

**Table 74: IRQ\_MASK2 (0x0083)**

Bit	Mode	Symbol	Description	Reset
[7]	RW	ADC_SAT_M	Masking for ADC saturation fault: ADC_SAT_FAULT	0x0

**Register SNP\_MEM\_xx**

Table 75 shows the first, intermediary, and last snippet memory registers.

- The snippet register addresses increment by 1 for each snippet.
- The Bit ([7:0]), Mode (RW), and Reset (0x0) are identical for each snippet register.
- For further details on the Waveform Memory, see Section 5.8.

**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support**

**Table 75: SNP\_MEM\_xx (0x0084 to 0x00E7)**

Bit	Mode	Symbol	Description	Reset
[7:0]	RW	SNP_MEM_00	Snippet memory byte 0	0x0
[7:0]	RW	SNP_MEM_xx	Snippet memory byte x	0x0
[7:0]	RW	SNP_MEM_99	Snippet memory byte 99	0x0

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7 Package Information

7.1 WLCSP Package Outline

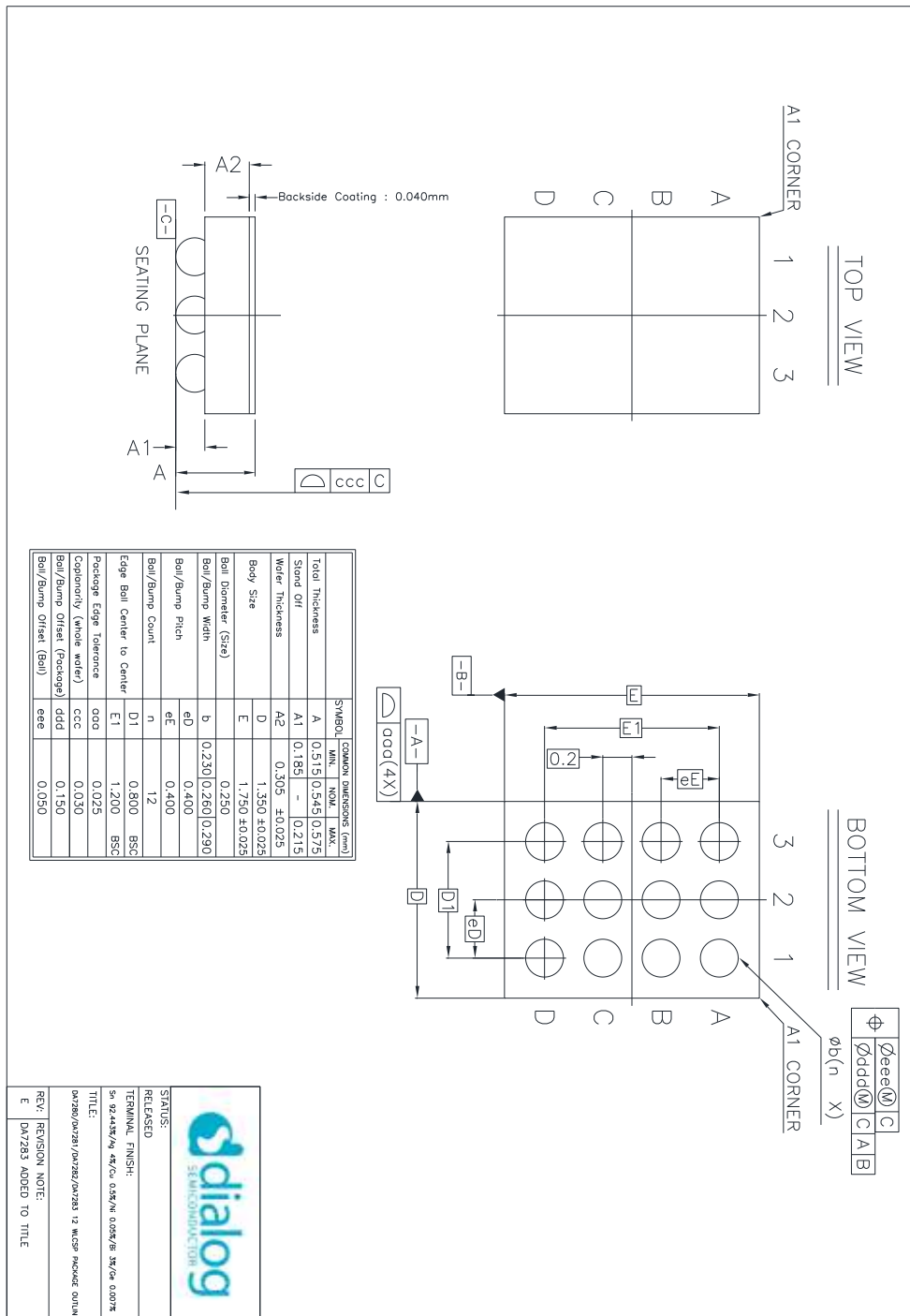


Figure 40: WLCSP Package Outline Drawing



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### LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

#### 7.2 QFN Package Outline

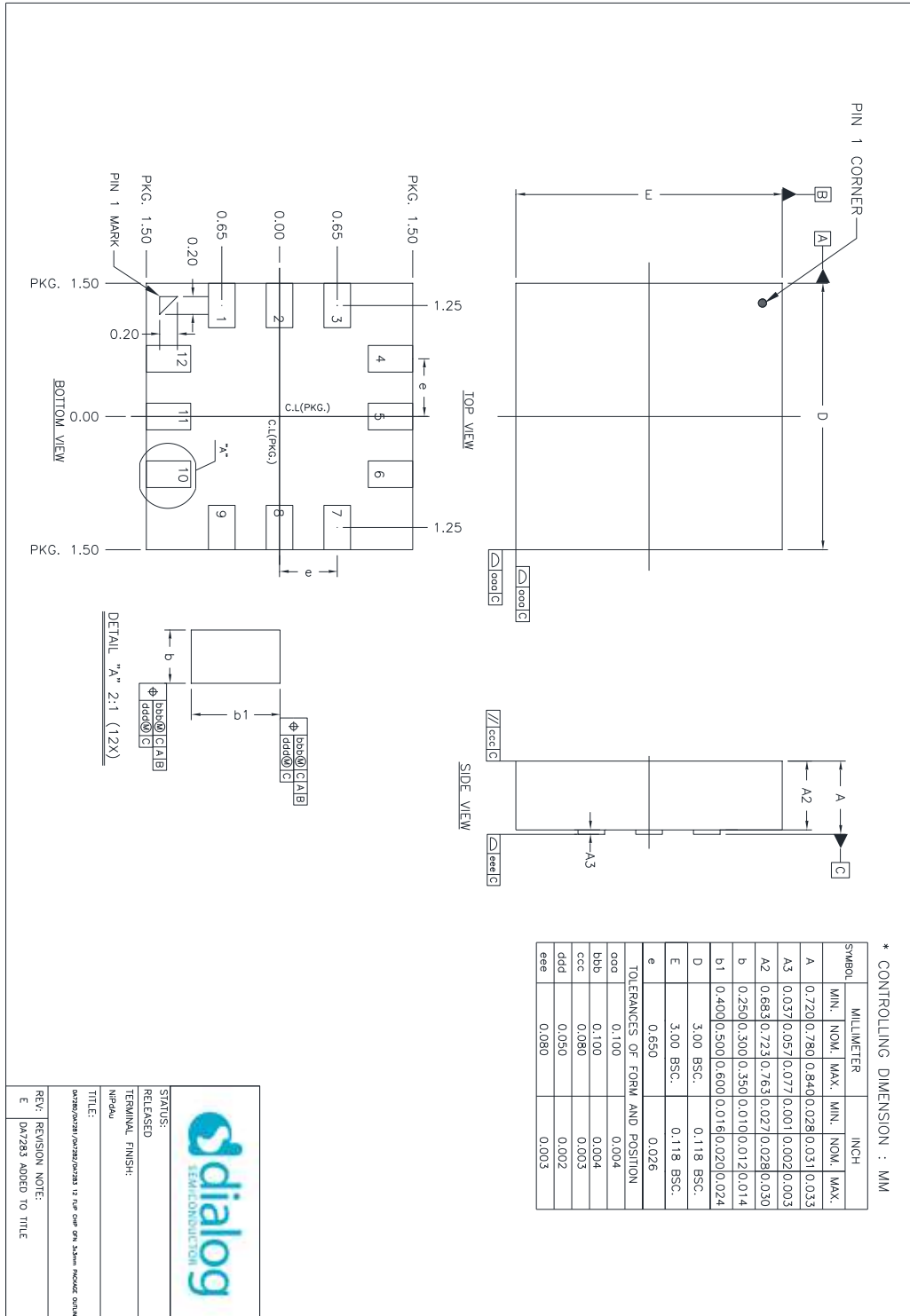


Figure 41: QFN Package Outline Drawing

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 7.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in [Table 76](#).

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

The WLCSP package is qualified for MSL 1.

The QFN package is qualified for MSL 3.

**Table 76: MSL Classification**

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

### 7.4 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore, a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

### 7.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

# DA7281

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### 8 Ordering Information

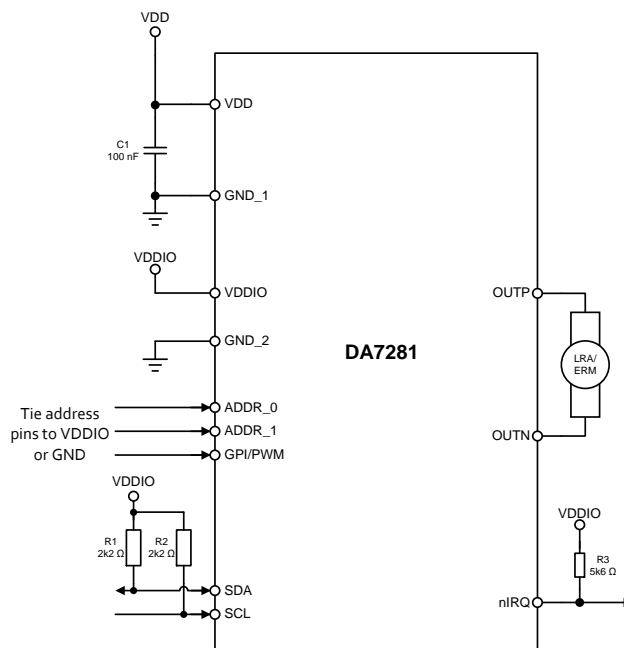
The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor’s [customer support portal](#) or your local sales representative.

**Table 77: Ordering Information**

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA7281-00V42	WLCSP	1.35 x 1.75	Tape and reel	4500
DA7281-00V4C	WLCSP	1.35 x 1.75	Tape and reel	250
DA7281-00FV2	QFN	3.0 x 3.0	Tape and reel	6000
DA7281-00FVC	QFN	3.0 x 3.0	Tape and reel	250

### 9 Application Information

The Dialog [SmartCanvas](#) GUI enables easy access to the device and can be used to accelerate product development time. For further information, contact your Dialog Semiconductor representative.



**Figure 42: External Components Diagram**

**Note:** Drive the GPI and ADDR pins at the same voltage level as the VDDIO pin.

**Note:** Ground any unused GPI pins.

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

**Note:** The C1 capacitor should be placed as close as possible to, and between, VDD and GND\_1. It removes high-frequency noise only; ensure additional decoupling (typ. 10  $\mu$ F) is included elsewhere in the system.

### 10 Layout Guidelines

For optimal layout, place the 100 nF capacitor as close to VDD and GND\_1 pins as possible. It is also advisable to use solid a ground plane under the device.

The QFN can be routed out on a single layer. It is recommended to connect GND\_1 and GND\_2 to a local ground plane on the top layer with a low-impedance via connection to the main ground plane, see [Figure 44](#).

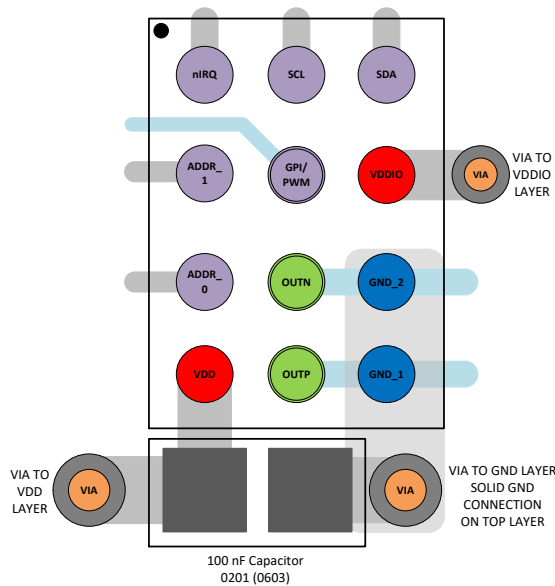


Figure 43: WLCSP Example PCB Layout

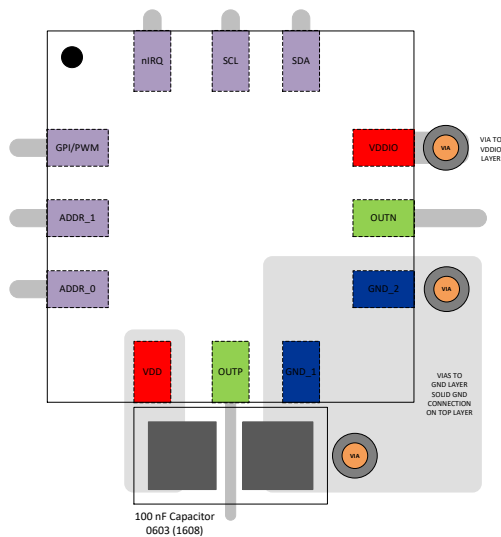


Figure 44: QFN Example PCB Layout

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### Revision History

Revision	Date	Description
3.1	10-Feb-2022	Updated logo, disclaimer, copyright.
3.0	30-Jul-2019	Final datasheet

**Change details:**

- Front page, minor rewording to better describe part
- [Table 1](#): Updated Product Family to include DA7283
- [Section 2: Pinout](#)
  - Formatting changes to merge tables and use space better
- [Section 3.3 Electrical Characteristics](#)
  - Table 7 Added parameter V<sub>DD\_POR\_FALL</sub>
- [Section 5.1 Features Description](#)
  - Minor rewording to better describe part
- [Section 5.7.1: Frequency Tracking](#)
  - Added sentence regarding use of SmartCanvas GUI to adjust Kp and Ki coefficients
  - Added sentence regarding checking stability of closed loop to step response when optimizing Kp and Ki coefficients with `FREQ_TRACK_AUTO_ADJ` enabled
- [Section 5.8: Waveform Memory](#)
  - Added note recommending SmartCanvas GUI is used to construct and upload WM sequences
- [Section 5.8.1: Waveform Memory Structure](#)
  - Figure 26: Replaced Sequence 1 with Sequence 0
  - Clarification of explanation of Figure 25
- [Section 5.8.2: Snippet Definition](#)
  - Clarification of TIME and AMP definitions
  - Added note to explain snippet 0
- [Section 5.8.3: Frame Definition](#)
  - Clarified Byte 1 and Byte 2 definitions
  - Clarified `SNP_ID_LOOP [3:0]` definition
  - Added notes explaining updating of frequencies
- [Section 5.8.4: Sequence Definition](#)
  - Further clarification of sequences
  - Figure 30: Replaced Sequence 1 with Sequence 0
- [Section 5.9.1 DRO Mode](#)
  - Clarification of full range
- [Section 5.9.3 RTWM and ETWM Modes](#)
  - Clarification of full range
- [Section 6: Register Overview](#)
  - Reset values (and associated descriptions) updates for the following addresses: 0x00, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F, 0x10, 0x11, 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x2C, 0x46, 0x47, and 0x5F
- [Section 7 Package Information](#)
  - WLCSP and QFN updated to rev E (only change is to title)
- [Section 7.3 Moisture Sensitivity Level](#)
  - Added QFN Package MSL level of 3
- [Section 9: Application Information](#)
  - Added Notes to clarify external components recommended

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**LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C  
Addresses, Integrated Waveform Memory, and  
Wideband Support**

Revision	Date	Description
○ Back page: Updated disclaimer		
1.0	30-Jul-2018	Initial version (Target datasheet)

## LRA/ERM Haptic Driver with Multiple I<sup>2</sup>C Addresses, Integrated Waveform Memory, and Wideband Support

### Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via <a href="http://www.dialog-semiconductor.com">www.dialog-semiconductor.com</a> .
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

### RoHS Compliance

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