KAF-16801

4096 (H) x 4096 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−16801 is a high performance area CCD (charge-coupled device) image sensor with 4096 (H) × 4096 (V) photo active pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD
Pixel Count	4096 (H) × 4096 (V)
Pixel Size	9.0 μm (H) × 9.0 μm (V)
Active Image Size	36.88 mm (H) × 36.88 mm (V) 52.1 mm (Diagonal) 645 1.3x Optical Format
Chip Size	38.60 mm (H) × 37.76 mm (V)
Optical Fill Factor	100%
Saturation Signal	100,000 electrons
Output Sensitivity	13 μV/e⁻
Dark Current (Accumulation Model)	< 10 pA/cm^2
Dark Current Doubling Rate	6°C
Dynamic Range (Saturation Signal/Dark Noise)	76 dB
Quantum Efficiency (450, 550, 650 nm)	40%, 52%, 65%
Maximum Date Rate	10 MHz
Package	CERDIP Package (Sidebrazed)
Cover Glass	Clear

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.

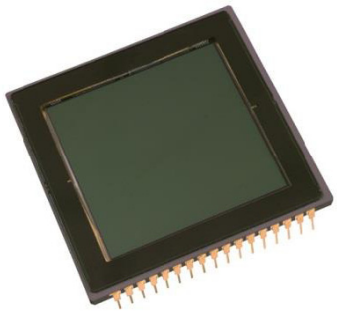


Figure 1. KAF−16801 Full Frame CCD Image Sensor

Features

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for High Sensitivity
- Low Dark Current
- High Output Sensitivity

Application

- Scientific Imaging

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAF−16801 IMAGE SENSOR

Part Number	Description	Marking Code
KAF−16801−AAA−DP−B1	Monochrome, No Microlens, CERDIP Package (Sidebrazed, CuW), Taped Clear Cover Glass (No Coatings), Grade 1	KAF−16801−AAA Serial Number
KAF−16801−AAA−DP−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed, CuW), Taped Clear Cover Glass (No Coatings), Grade 2	
KAF−16801−AAA−DP−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed, CuW), Taped Clear Cover Glass (No Coatings), Engineering Sample	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KEK−4H0082−KAF−160801−12−5	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

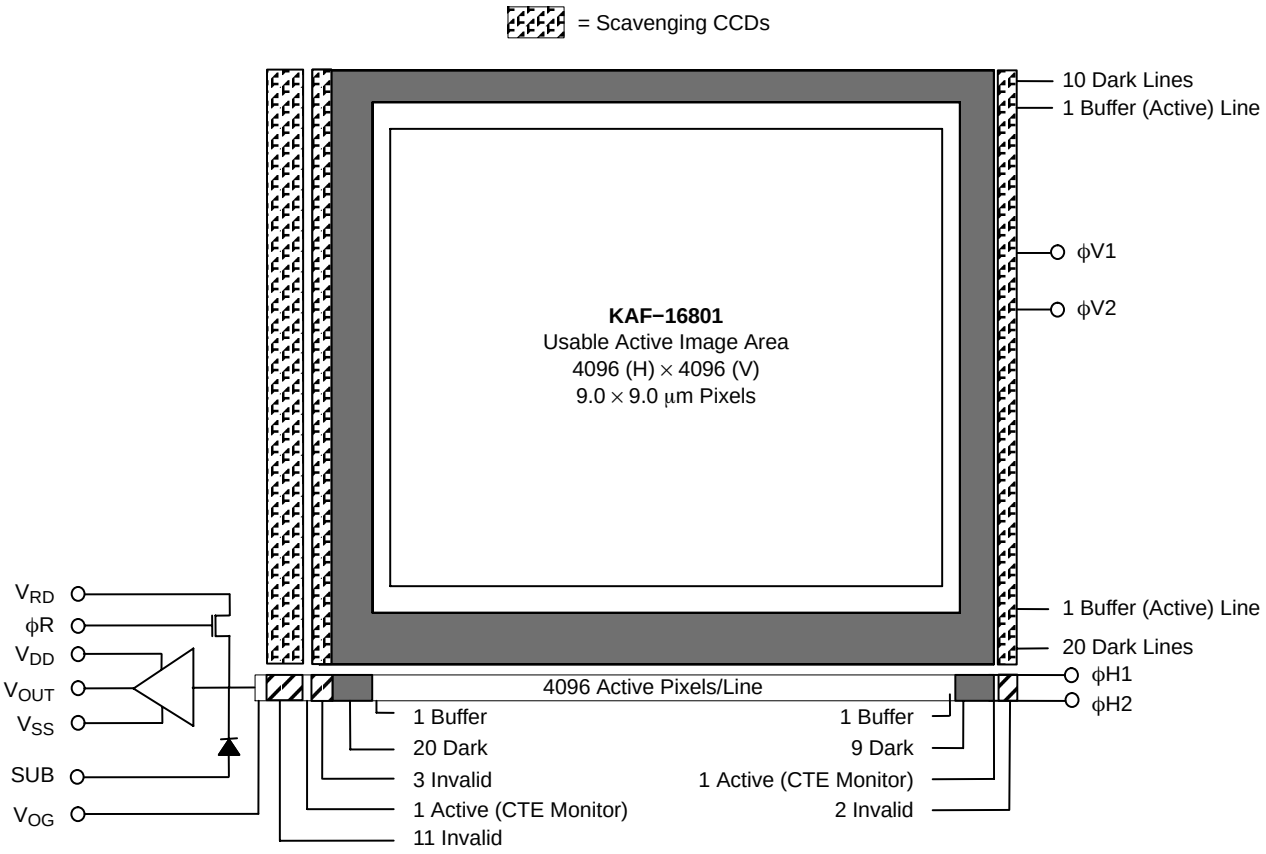


Figure 2. Block Diagram

The sensor consists of 4,127 parallel (vertical) CCD shift registers each 4,128 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 4096 × 4096 photosensitive array surrounded by a light shielded dark reference of 29 columns and 30 rows. There is a buffer region of one photosensitive pixel surrounding the photosensitive region (one column at the beginning of a line, one column at the end of a line, one row at the beginning of a frame, and one row at the end of a frame). The parallel (vertical) CCD registers transfer the image one line at a time into a single 4,145 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a three-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels. This includes 20 leading and 10 trailing pixels on every line excluding the inactive and photosensitive buffer pixels. There are also 20 full dark lines at the start of every frame and 10 full dark lines at the end of each frame. Under normal circumstances, these dark reference pixels do not respond to light. However, the pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on

FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and FD is reset to the potential applied by V_{RD}. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the VOUT pin of the device – see Figure 3.

Transfer Efficiency Test Pixels and Dummy Pixels

At the beginning of each line and at the end of each line are extra horizontal CCD pixels. These are a combination of pixels that are not associated with any vertical CCD register and two that are associated with extra photo active vertical CCDs. The two extra photo active vertical CCDs are provided to give an accurate photo generated signal that can be used to monitor the charge transfer efficiency in the serial (horizontal) register.

They are arranged as follows beginning with the first pixel in each line:

- 11 Dark, Inactive Pixels
- 1 Photoactive Test Pixel
- 3 Inactive Pixels
- 20 Dark Reference Pixels
- 1 Active Buffer Pixel
- 4,096 Photoactive Pixels
- 1 Active Buffer Pixel
- 9 Dark Reference Pixels
- 1 Photoactive Test Pixel
- 2 Inactive Pixels

Image Acquisition

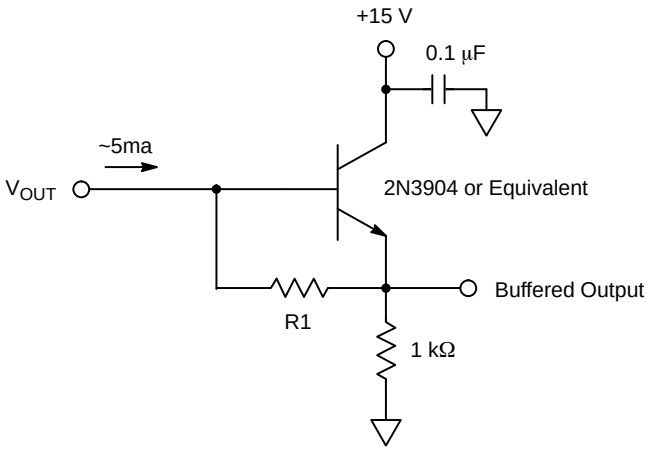
An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level. See Figure 8.

Charge Transport

Referring again to Figure 8 − Timing Diagrams, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV1 while ϕH2 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH1 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Horizontal Register

Output Structure



Notes:

1. For operation of up to 10 MHz.
2. The value of R1 depends on the desired output current according the following formula: R1 = 0.7 / I_{OUT}.
3. The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5 mA is recommended for capacitance of 12 pF and pixel rates up to 20 MHz.

Figure 3. Output Structure Load Diagram

Physical Description

Pin Description and Device Orientation

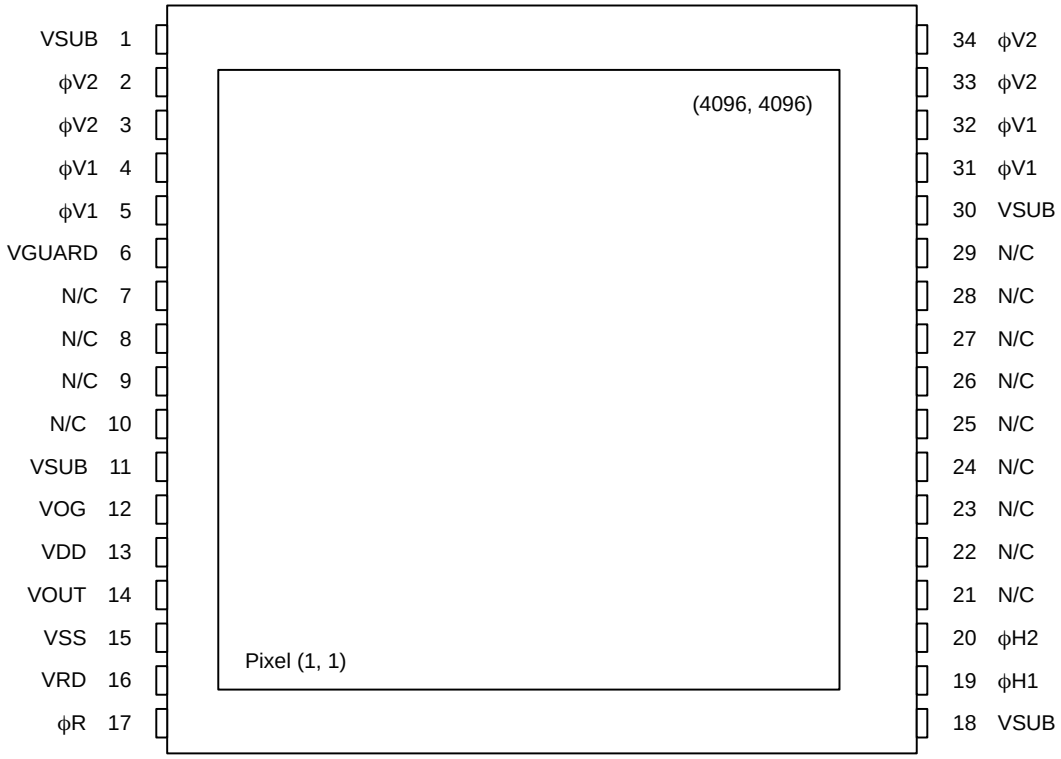


Figure 4. Pinout Diagram

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	VSUB	Substrate (Ground)
2	ϕV2	Vertical CCD Clock − Phase 2
3	ϕV2	Vertical CCD Clock − Phase 2
4	ϕV1	Vertical CCD Clock − Phase 1
5	ϕV1	Vertical CCD Clock − Phase 1
6	VGUARD	Guard Ring
7	N/C	No Connection (Open Pin)
8	N/C	No Connection (Open Pin)
9	N/C	No Connection (Open Pin)
10	N/C	No Connection (Open Pin)
11	VSUB	Substrate (Ground)
12	VOG	Output Gate
13	VDD	Amplified Supply
14	VOUT	Video Output
15	VSS	Amplifier Supply Returen
16	VRD	Reset Drain
17	ϕR	Reset Clock

Pin	Name	Description
18	VSUB	Substrate (Ground)
19	ϕH1	Horizontal CCD Clock − Phase 1
20	ϕH2	Horizontal CCD Clock − Phase 2
21	N/C	No Connection (Open Pin)
22	N/C	No Connection (Open Pin)
23	N/C	No Connection (Open Pin)
24	N/C	No Connection (Open Pin)
25	N/C	No Connection (Open Pin)
26	N/C	No Connection (Open Pin)
27	N/C	No Connection (Open Pin)
28	N/C	No Connection (Open Pin)
29	N/C	No Connection (Open Pin)
30	VSUB	Substrate (Ground)
31	ϕV1	Vertical CCD Clock − Phase 1
32	ϕV1	Vertical CCD Clock − Phase 1
33	ϕV2	Vertical CCD Clock − Phase 2
34	ϕV2	Vertical CCD Clock − Phase 2

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATIONAL CONDITIONS

(All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.)

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal Vertical CCD Capacity Horizontal CCD Capacity Output Node Capacity	N_{SAT}	 – 90,000 –	 100,000 200,000 180,000	 100,000 – 250,000	e^-/pix	1	Design[12]
Photoresponse Non-Linearity	PRNL	–	1	2	%	2	Design[12]
Photoresponse Non-Uniformity	PRNU	–	1	3	%	3, 10	Die[11]
Dark Signal	J_{DARK}	– –	18 3.5	50 10	e^-/pix/sec pA/cm^2	4	Die[11]
Dark Signal Doubling Temperature		5	6.3	7.5	°C		Design[12]
Dark Signal Non-Uniformity	DSNU	–	18	50	e^-/pix/sec	5, 10	Die[11]
Dynamic Range	DR	73	76	–	dB	6	Design[12]
Charge Transfer Efficiency	CTE	0.99997	0.99999	–			Die[11]
Output Amplifier DC Offset	V_{ODC}	V_{RD} − 3.0	V_{RD} − 2.5	V_{RD} − 2.0	V	7	Die[11]
Output Amplifier Bandwidth	f_{-3dB}	–	140	–	MHz	8	Design[12]
Output Amplifier Sensitivity	V_{OUT}/N_e^-	12.5	13	14	$\mu V/e^-$		Design[12]
Output Amplifier Output Impedance	Z_{OUT}	–	130	–	Ω		Design[12]
Noise Floor	n_e^-	–	15	20	electrons	9	Die[11]

1. For pixel binning applications, electron capacity up to 270,000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst case deviation from straight line fit, between 1% and 90% of V_{SAT}.
3. One Sigma deviation of a 128 × 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of 32 × 32 blocks within the sensor (each block is 128 × 128 pixels).
6. 20log (N_{SAT} / n_e^-) at nominal operating frequency and 25°C.
7. Video level offset with respect to ground.
8. Assumes 10 pF off-chip load.
9. Output amplifier noise at 25°C, operating at pixel frequency up to 2 MHz, bandwidth = 20 MHz, t_{INT} = 0, and no dark current shot noise.
10. Specification excludes region [1, 1, 400, 400]. See Dark Current Non-uniformity.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

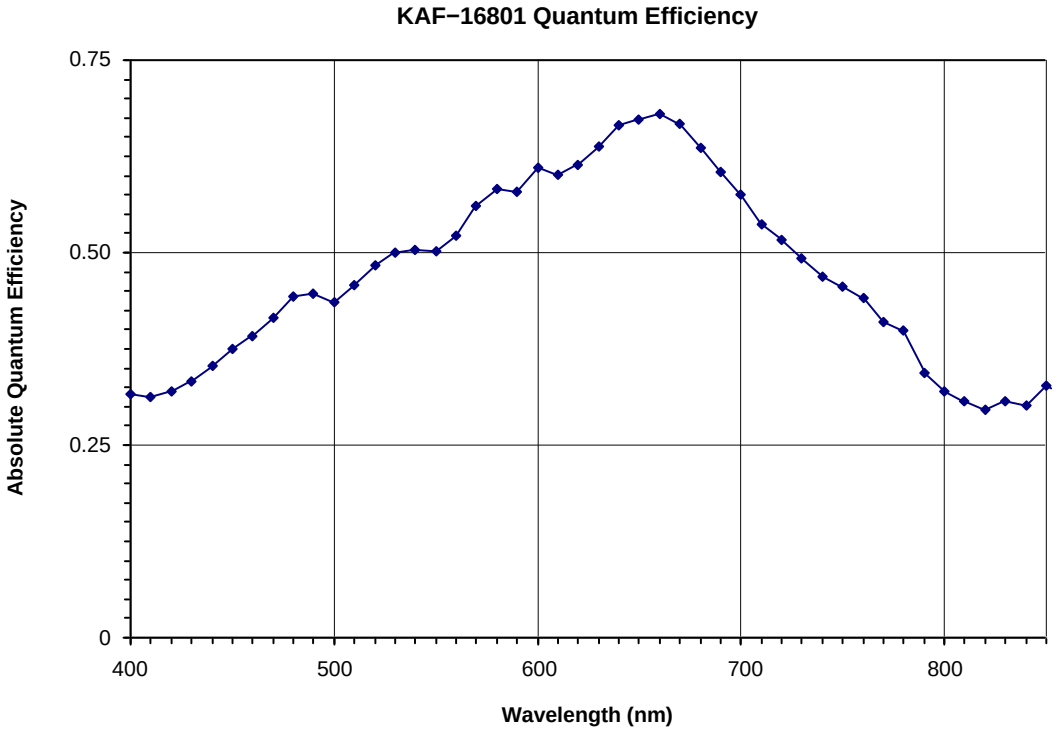


Figure 5. Typical Spectral Response

Dark Current Non-Uniformity

The photoresponse non-uniformity specification and the dark signal non-uniformity specification of the sensor both exclude the region that is [1, 1, 400, 400]. The reason for this exclusion is that when the sensor is running with V_{DD} always on, and the integration times are greater than 100 msec, a non-uniformity will become evident surrounding the first pixel. This non-uniformity is a result of the output amplifier emitting light into the photoactive area (see Figure 9). The elevated dark signal in this region typically ranges from 30 e^-/pix/sec to 100 e^-/pix/sec, depending on the part, and is independent of temperature. If V_{DD} is switched to 0 V at least 10 μsec after the last pixel is read out, and switched back to full value 10 μsec before the first pixel of the next frame, the effect of the amplifier glow will be eliminated (see Figure 10).

DEFECT DEFINITIONS

Table 6. SPECIFICATIONS (All defect tests performed at T = 25°C)

Classification	Point Defects	Cluster Defects	Maximum Cluster Size	Column Defects	Maximum Column Width
C1	≤ 60	≤ 8	8	4	1
C2	≤ 120	≤ 16	8	10	1
C3	≤ 240	≤ 32	15	20	2

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation.

Bright: A pixel with a dark current > 7,000 e^-/pixel/sec at 25°C.

Cluster Defect

A grouping of not more than 5 adjacent point defects.

Column Defect

A grouping of > 5 contiguous point defects along a single column.

A column containing a pixel with dark current > 20,000 e^-/pixel/sec.

A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 ke^-.

A column which contains a pixel that loses > 250 e^- under 2 ke^- illumination.

Neighboring Pixels

The surrounding 128 × 128 pixels or ±64 columns/rows.

Defect Separation

Column and cluster defects are separated by no less than 2 pixels in any direction (excluding single pixel defects).

Defect Region Exclusion

Defect region excludes the outer 2 rows and columns at each side/end of the sensor.

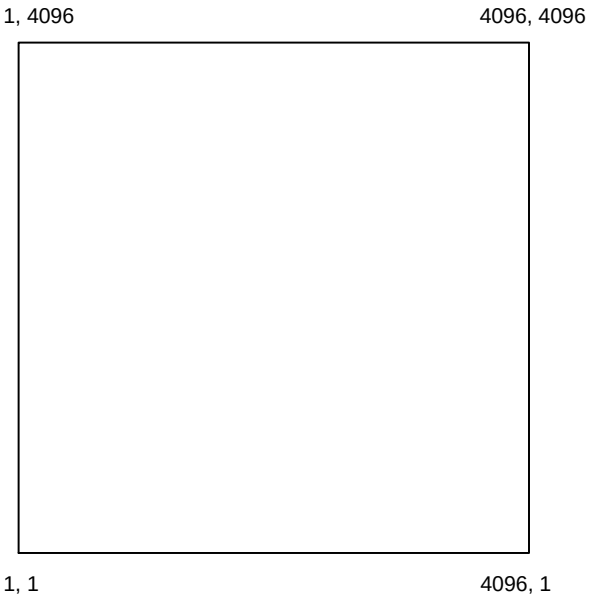


Figure 6. Active Pixel Region

OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{DIODE}	0	20	V	13, 14
Gate Pin Voltages − Type 1	V_{GATE1}	−16	16	V	13, 15
Gate Pin Voltages − Type 2	V_{GATE2}	0	16	V	13, 16
Inter-Gate Voltages	$V_{G−G}$	−	16	V	17
Output Bias Current	I_{OUT}	−	−10	mA	18
Output Load Capacitance	C_{LOAD}	−	15	pF	18
Storage Temperature	T	−50	70	°C	
Humidity	RH	5	90	%	19

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
13. Referenced to pin VSUB.
14. Includes pins: VRD, VDD, VSS, VOUT, VGUARD.
15. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
16. Includes pins: ϕR, VOG.
17. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕV1 to ϕH2, ϕH1 to V_{OG}.
18. Avoid shorting output pins to ground or any low impedance source during operation.
19. T = 25°C. Excessive humidity will degrade MTF.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	11.0	12.0	12.25	V	0.01	
Output Amplifier Return	V_{SS}	1.5	2.0	2.5	V	0.45	
Output Amplifier Supply	V_{DD}	14.5	15.0	17.0	V	I_{OUT}	
Substrate	V_{SUB}	0	0	0	V	0.01	
Output Gate	V_{OG}	4.5	5.0	5.2	V	0.01	
Guard Ring	V_{LG}	9.0	10.0	12.0	V	0.01	
Video Output Current	I_{OUT}	−3.5	−5.0	−10.0	mA		20

20. An output load sink must be applied to V_{OUT} to activate output amplifier − see Figure 3.

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock − Phase 1	ϕV1	Low	−9.0	−8.5	−8.3	V	250 nF (All ϕV1 Pins)
Vertical CCD Clock − Phase 1	ϕV1	High	ϕV1 Low + 10.5	2.0	ϕV1 Low + 10.5	V	250 nF (All ϕV1 Pins)
Vertical CCD Clock − Phase 2	ϕV2	Low	−9.0	−8.5	−8.3	V	250 nF (All ϕV2 Pins)
Vertical CCD Clock − Phase 2	ϕV2	High	ϕV2 Low + 10.5	2.0	ϕV2 Low + 10.5	V	250 nF (All ϕV2 Pins)
Horizontal CCD Clock − Phase 1	ϕH1	Low	−2.5	−2.5	−1.8	V	500 pF
Horizontal CCD Clock − Phase 1	ϕH1	High	ϕH1 Low + 10.5	8.0	ϕH1 Low + 10.5	V	500 pF
Horizontal CCD Clock − Phase 2	ϕH2	Low	−2.5	−2.5	−1.8	V	300 pF
Horizontal CCD Clock − Phase 2	ϕH2	High	ϕH2 Low + 10.5	8.0	ϕH2 Low + 10.5	V	300 pF
Reset Clock	ϕR	Low	3.0	5.0	5.5	V	10 pF
Reset Clock	ϕR	High	9.5	10.0	10.5	V	10 pF

21. All pins draw less than 10 μA DC current.
22. Capacitance include gate to V_{SUB} and gate to gate (ϕV1−ϕV2, ϕH1−ϕH2).

TIMING

Table 10. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H	−	8	15	MHz	23, 24, 25
ϕV1, ϕV2 Clock Frequency	F_V	−	25	25	MHz	23, 24, 25
Pixel Period (1 Count)	t_e	67	125	−	ns	
ϕH1, ϕH2 Set-up Time	$t_{\phi HS}$	0.5	1	−	μs	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	40	40	−	μs	24
ϕV1, ϕV2 Clock Pulse Overlap	t_{OVRLP}	20	20	−	μs	
Reset Clock Width	$t_{\phi R}$	10	20	−	ns	26
Readout Time	$t_{READOUT}$	1,398	2,390	−	ms	27
Integration Time	t_{INT}	−	−	−		28
Line Time	t_{LINE}	338.7	580	−	μs	29

23. 50% duty cycle values.
24. CTE may degrade above the nominal frequency.
25. Rise and fall times (10/90% levels) should be limited to 5−10% of clock period. Cross-over of register clocks should be between 40−60% of amplitude.
26. ϕR should be clocked continuously.
27. $t_{READOUT} = (4128 \cdot t_{LINE})$
28. Integration time is user specified. Longer integration times will degrade noise performance.
29. $t_{LINE} = (2 \cdot t_{\phi V}) - t_{OVRLP} + t_{\phi HS} + (4145 \cdot t_e) + t_e$.

Frame Timing

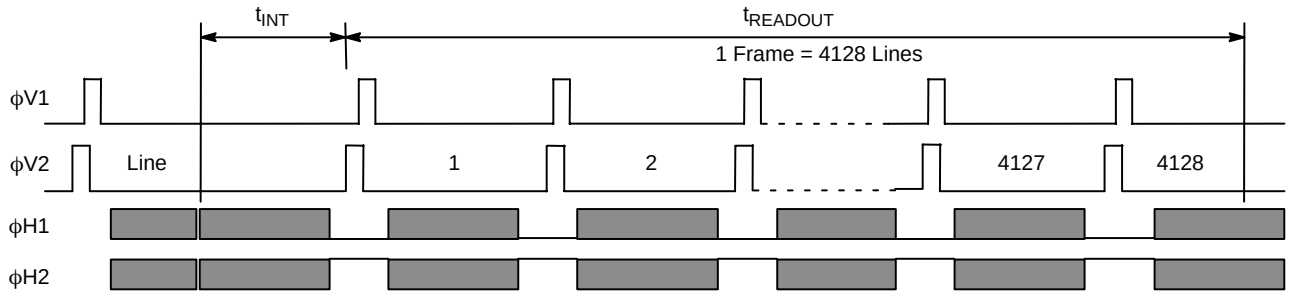
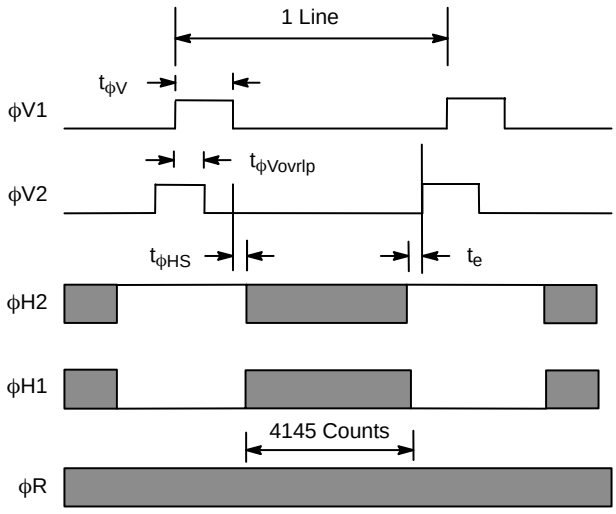


Figure 7. Frame Timing Diagram

Line Timing and Pixel Timing

Line Timing Detail



Pixel Timing Detail

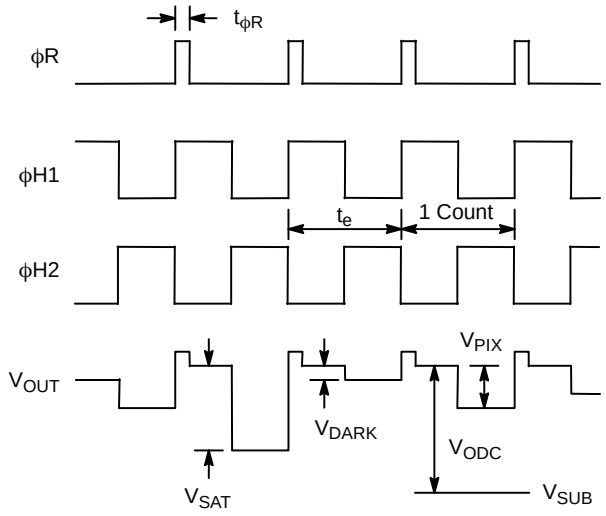


Figure 8. Line Timing and Pixel Timing

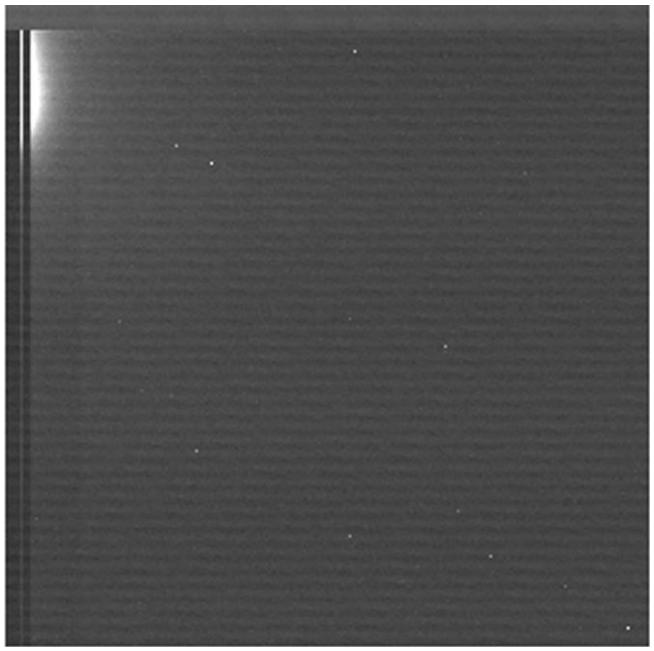


Figure 9. Amplifier Glow − S11LE @-20C with 20 sec Integration @1 MHz V_{DD} always ON (+15)

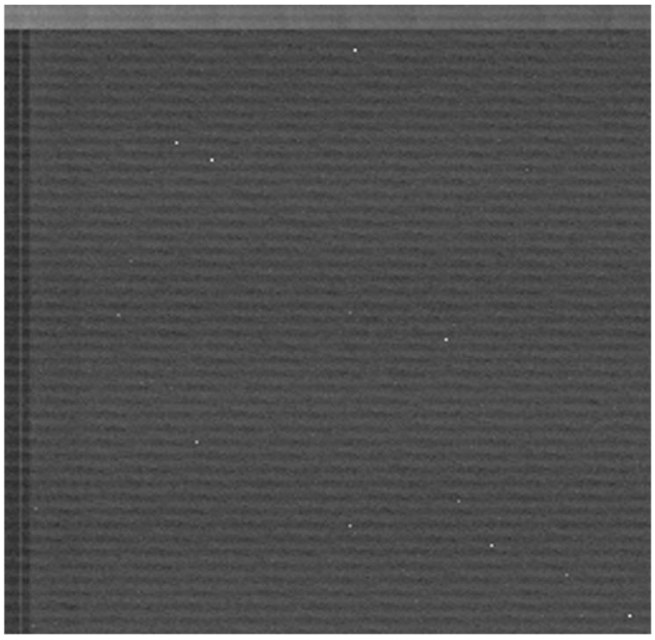


Figure 10. Amplifier Glow − S11LE @-20C with 20 sec Integration @1 MHz V_{DD} OFF during Integration

NOTE: Amplifier glow is suppressed by switching V_{DD} to 0 V during integration.

STORAGE AND HANDLING

Table 11. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	−20	100	°C	30
Operating Temperature	T_{OP}	−60	60	°C	

30. Storage toward the maximum temperature will accelerate microlens degradation.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

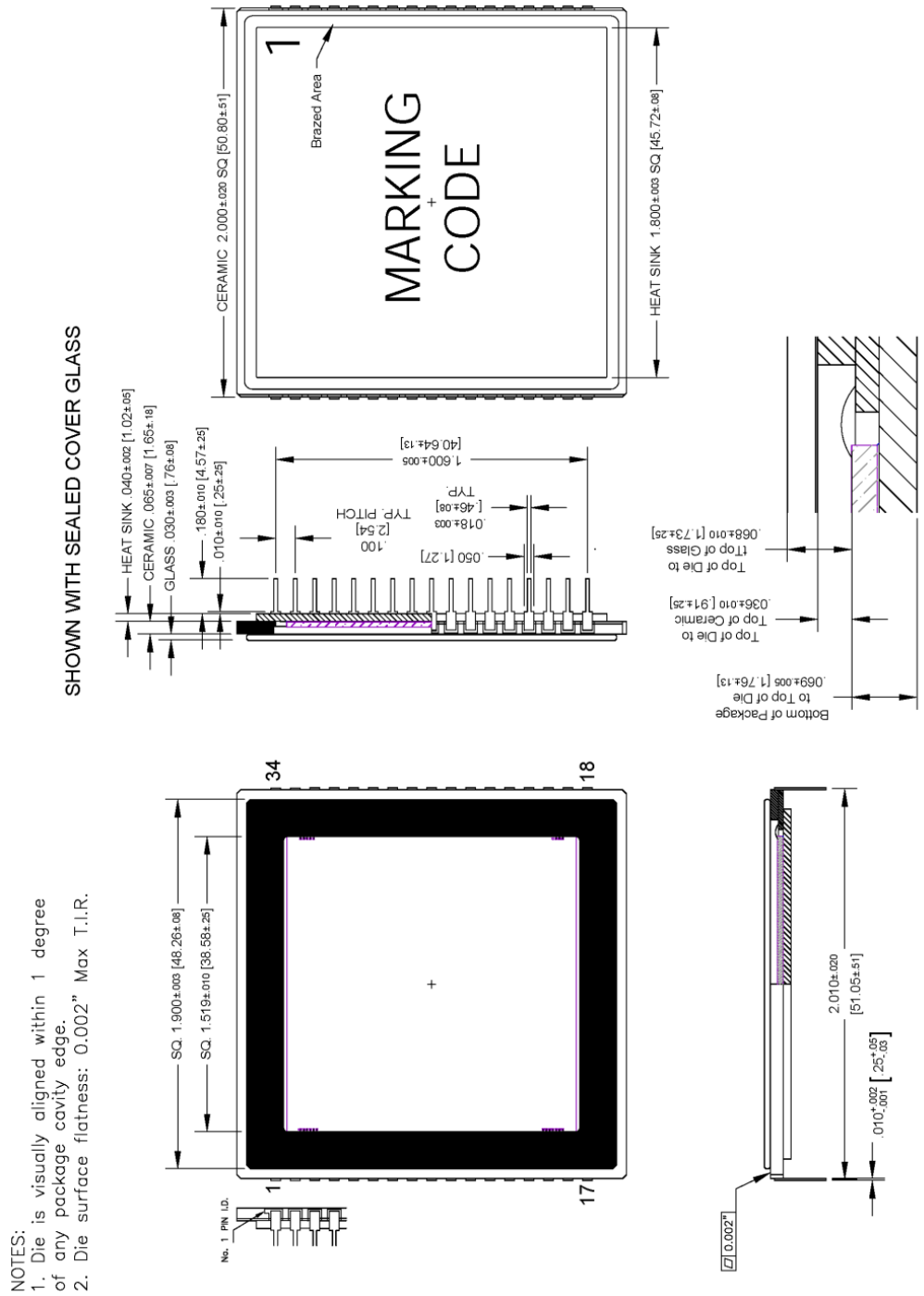


Figure 11. Completed Assembly (1 of 2)

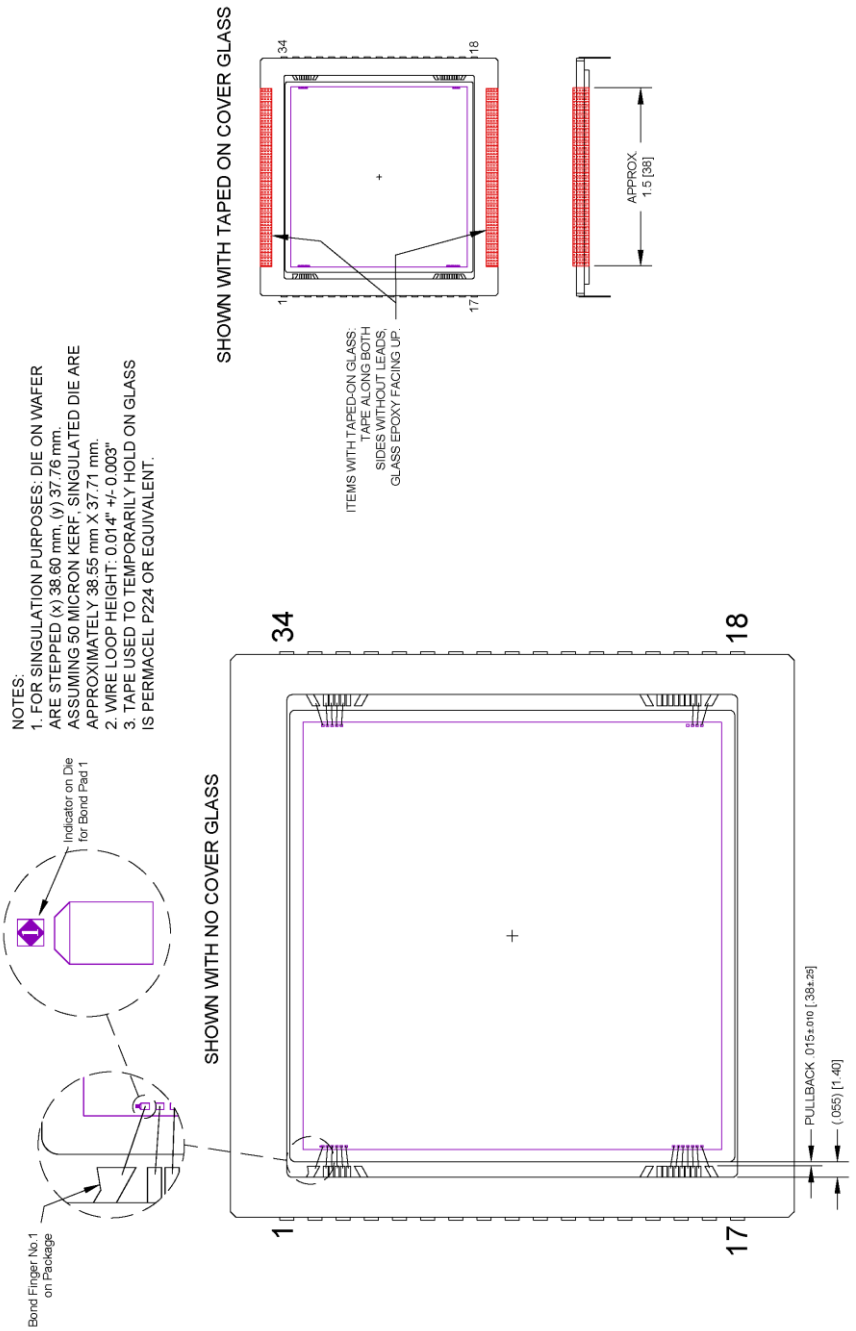


Figure 12. Completed Assembly (2 of 2)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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