Evaluating the ADuM4146 11 A High Voltage Isolated Bipolar Gate Driver with Fault Detection, Miller Clamp

FEATURES

- 11 A peak short-circuit current
- Desaturation protection circuitry
- Integrated Miller clamp
- CMOS input logic levels
- 12 V to 30 V output drive
- Supports TO-220 and TO-247 switch footprints

SUPPORTED *i*COUPLER MODELS

- ADuM4146ARWZ
- ADuM4146BRWZ
- ADuM4146CRWZ

EVALUATION BOARD PICTURE

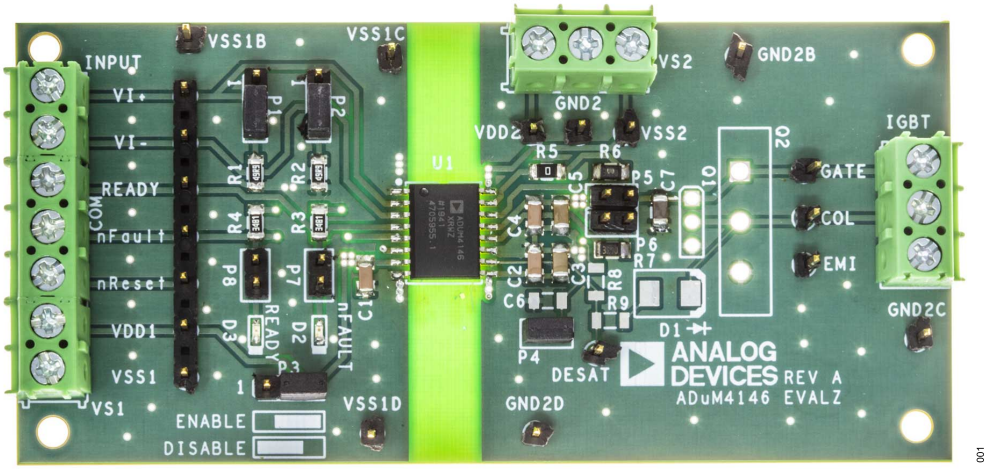

Figure 1.

GENERAL DESCRIPTION

The EVAL-ADuM4146EBZ supports the ADuM4146 advanced isolated gate driver. The EVAL-ADuM4146EBZ comes populated with the ADuM4146BRWZ grade of the model but is compatible with all three grades. Because the evaluation board has footprints for insulated gate bipolar transistors (IGBTs) and metal-oxide semiconductor field effect transistors (MOSFETs) in TO-247, TO-220, and 0.100" spaced lead packages, the ADuM4146 can be evaluated with many different power devices. The EVAL-ADuM4146EBZ comes with footprints to facilitate evaluating the desaturation detection, as well as Miller clamp operation.

For full details on the ADuM4146, see the ADuM4146 data sheet, which should be consulted in conjunction with this user guide when using this evaluation board.

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REVISION HISTORY

4/2022—Revision 0: Initial Version

SETTING UP THE EVAL-ADUM4146EBZ

INITIAL CONFIGURATION

Before the first use, certain things must be completed to prepare the EVAL-ADuM4146EBZ for operation. In the stock configuration, the R1 to R5 resistors are not placed. These are the location of the series external resistors for the charging and discharging paths to V_{OUT_ON} and V_{OUT_OFF}. It is recommended to use 1206 surface-mount resistors with values between approximately 1 Ω and 10 Ω, depending on the load being driven. Calculate the expected power dissipation within the external series gate resistors. The EVAL-ADuM4146EBZ was not designed with full power operation as the main goal. However, this evaluation board was designed to simply showcase the different functions of the ADuM4146. As such, the layout is not as tight as an actual application requires, and in an actual application, many external series gate resistors can be placed in parallel with one another to increase the allowable power dissipation.

An actual IGBT or MOSFET can be placed in the provided landing patterns to the right of P5 and P6. P5 and P6 allow shorting across the series external resistors to observe overshoot and/or to probe the voltage to quantify peak currents.

In the stock configuration, the DESAT circuitry is left open. Before the first use, if DESAT functionality is not used, it is recommended to short the DESAT pin to ground, either by placing a 0.1" jumper on P4 or by placing a 0 Ω resistor in the C6 component pad. Failure to do so results in a DESAT fault being observed on the first rising edge of the output.

If the DESAT circuitry is tested, an IGBT or MOSFET must be added to the circuit to allow for the DESAT pin to be pulled down during on times, preventing the DESAT fault. Additionally, C6, R9, and D1 must have appropriate components placed. For details about sizing, refer to the ADuM4146 data sheet. R8 is provided to allow extra DESAT blanking current by means of an external pull-up resistor. If U1 is replaced with either the A grade or C grade of the ADuM4146, R8 is required as there is no internal current source on these grades.

R3 and R4 come with 3.48 kΩ resistors in place. These resistors provide pull ups to the READY and $\overline{\text{FAULT}}$ pins. LED indicators can be activated by placing jumpers on P7 and/or P8. When in place, D2 and D3 illuminate to give the status of the $\overline{\text{FAULT}}$ and READY pins, but the voltages on $\overline{\text{FAULT}}$ and READY are clamped to the forward voltage of the light emitting diodes (LEDs). As such, it is not recommended to drive a CMOS input with the $\overline{\text{FAULT}}$ and READY pins if the indicator LEDs are used.

P3 allows for easy enabling and disabling of the ADuM4146 by means of jumper pins. A silkscreen reminder is included to show which pins to short to enable or disable the ADuM4146.

Pins accompany the screw terminals. It is left to the user to decide which connection mechanism to use. Do not leave V_{SS2} floating because it must always be at or less than the potential of GND_2. Shorting V_{SS2} and GND_2 is a valid operating point.

During operation, if a fault is seen, the $\overline{\text{FAULT}}$ pin is brought low. In this case, the ADuM4146 can be reset by either powering down V_{DD1} to V_{SS1} and powering back up, or by bringing the $\overline{\text{RESET}}$ pin low then high again. The easiest way to toggle $\overline{\text{RESET}}$ is to remove the jumper on P3 from Pin 2 and Pin 3 and then replace them. An internal pull-down resistor brings $\overline{\text{RESET}}$ low on its own.

PAD LAYOUT FOR THE DEVICE UNDER TEST (DUT)

Figure 3 shows the top layer artwork for the dual gate driver circuit and the following components:

- U1 is the footprint for the ADuM4146.
- C1, C2, and C4 are 0.1 µF bypass capacitors, and C3 and C5 are 10 µF bypass capacitors.
- R6 and R7 are gate resistors that control the edges of the outputs. By default, no resistors are installed; these resistors must be populated with low value 1206 resistors, generally in the 1 Ω to 10 Ω range.

POWER CONNECTIONS

Follow these steps to connect the EVAL-ADuM4146EBZ to the power supply:

1. Connect the 5 V or 3.3 V input supply with the positive terminal on V_{DD1} and the ground on V_{SS1}.
2. Connect the ADuM4146 V_{DD2} supply voltage (12 V to 30 V) to the V_{DD2} pin and its return to the V_{SS2} pin.

Note that V_{SS1} and V_{SS2} are functionally isolated. The emitter and source of the IGBT or the MOSFET are tied to GND_2.

INPUT AND OUTPUT CONNECTIONS

The V_I+ and V_I− pins are CMOS inputs. P1 and P2 allow for easy placement of 49.9 Ω terminating resistors by placing a 0.1" jumper in Position 2 and Position 3 of P1 and/or P2. This also allows for dc state testing of the V_I+ and V_I− pins. In Position 1 and Position 2, a jumper pulls the input pin high. If no jumper is placed, the V_I+ and V_I− pins and screw terminals are high-Z inputs.

The EVAL-ADuM4146EBZ comes with screw terminals for both the input and output connections. These terminals help facilitate connection options but are not the best option for high performance transient testing. The best measurements performed on the load, whether it is an IGBT, a MOSFET or a load capacitor, come from small loop measurements performed right at the load. Using the screw terminals as either the sensing node or for the connection of the load often results in overshoot being observed during measurement.

EVALUATION BOARD SCHEMATIC

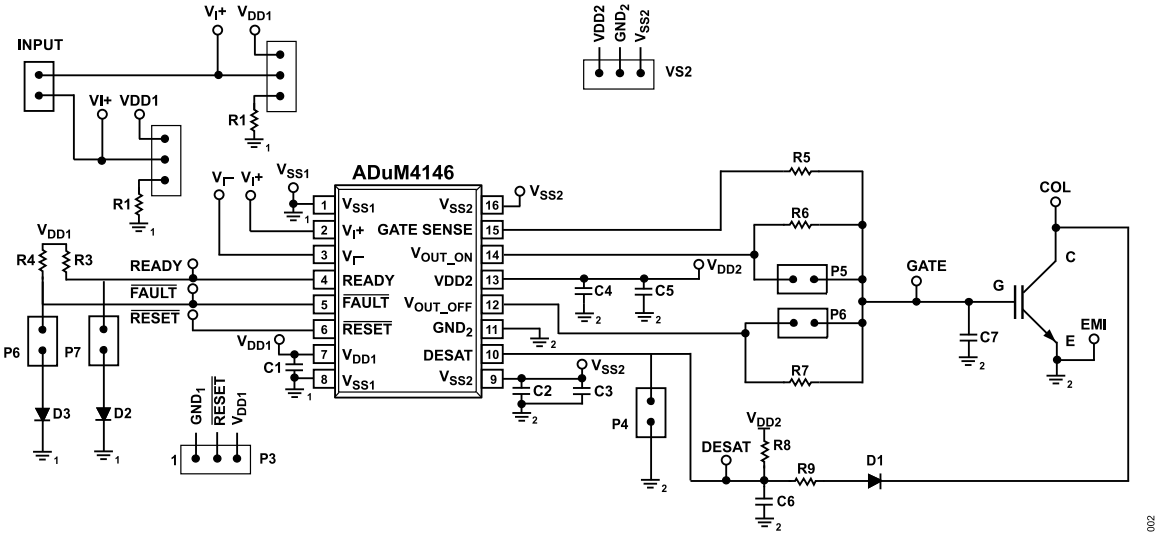

Figure 2. EVAL-ADuM4146EBZ Evaluation Board Schematic

EVALUATION BOARD LAYOUT

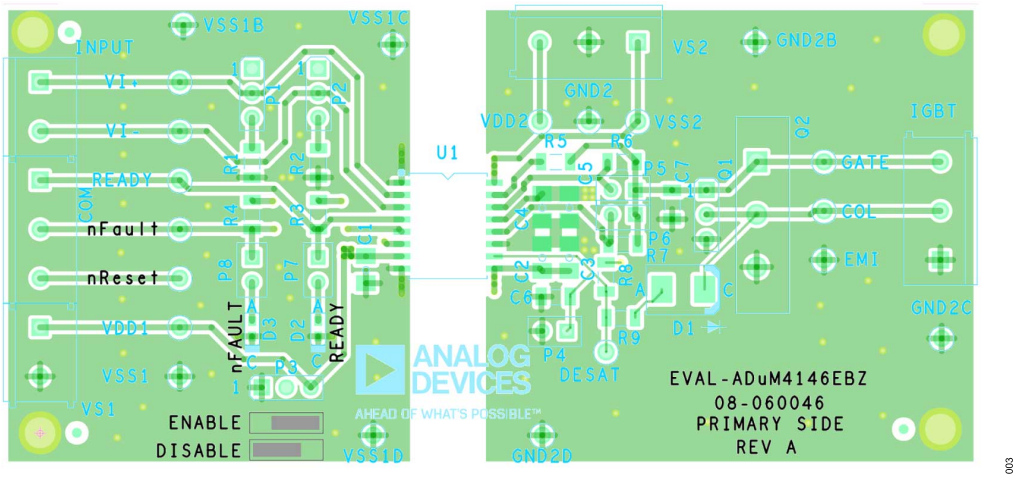

Figure 3. EVAL-ADuM4146EBZ Evaluation Board Top Layer

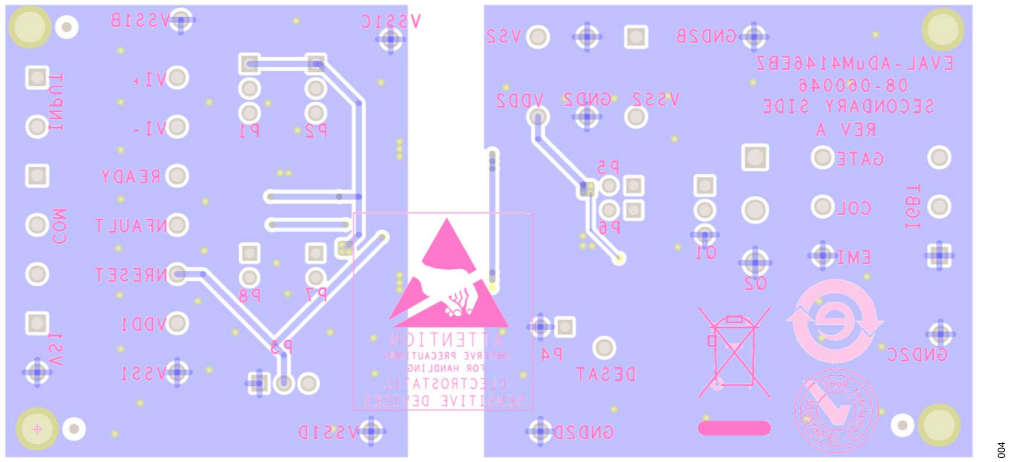

Figure 4. EVAL-ADuM4146EBZ Evaluation Board Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description
1	U1	ADuM4146BRWZ 11 A high voltage isolated bipolar gate driver with fault detection, Miller clamp
3	C1, C2, C4	Capacitors, 0.1 µF, 50 V, 10%, 1206
2	C3, C5	Capacitors, 10 µF, 50 V, 10%, 1206
1	D2	LTST-C190GKT, green LED, 0603
1	D3	LTST-C190CKT, red LED, 0603
2	R1, R2	Resistors, 49.9 Ω, ¼ W, 1206
2	R3, R4	Resistors, 3.48 kΩ, ¼ W, 1206
1	R5	Resistor, 0 Ω, ¼ W, 1206
5	P4 to P8	2 position, 0.1" male header
3	P1 to P3	3 position, 0.1" male header
Not applicable	C6, C7, D1, Q1, Q2, R6 to R9	Not installed

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.