MMA053AA

Datasheet

DC–8 GHz 1 W GaAs MMIC pHEMT Distributed Power Amplifier

Released

May 2017

Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

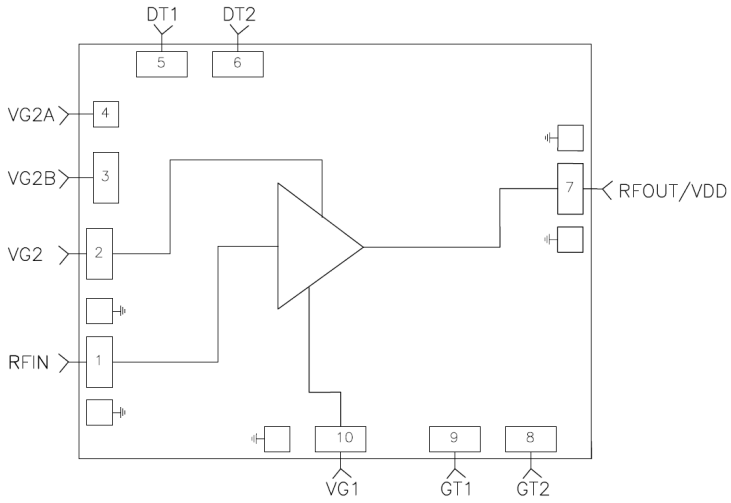
Revision 1.0 was published in May 2017. It was the first publication of this document.

2 Product Overview

MMA053AA is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pHEMT distributed power amplifier die that operates between DC and 8 GHz. The amplifier provides 17 dB of gain, +43 dBm output IP3, and +31 dBm of output power at 3 dB compression, while requiring only 410 mA from a 11 V supply. Gain flatness over the DC to 8 GHz frequency range varies by only ±0.5 dB, making the MMA053AA die ideal for EW, ECM, radar, and test equipment applications. The MMA053AA amplifier features compact die size and I/Os that are internally matched to 50 Ω, facilitating easy integration into multi-chip modules (MCMs).

The following figure is a functional block diagram for the MMA053AA device.

Figure 1 • Functional Block Diagram



2.1 Applications

The MMA053AA device is designed for the following applications:

- Test instrumentation
- Telecom infrastructure
- Microwave radio and VSAT
- Microwave communications

2.2 Key Features

The following are key features of the MMA053AA device:

- Frequency range: DC to 8 GHz
- High P3dB output power: 31 dBm
- Gain: 17 dB
- High OIP3: 43 dBm
- Bias V_{DD} = 11 V/ 410 mA, V_G = –0.7 V
- 50 Ω matched I/O
- Compact die size: 3 mm × 2.25 mm × 0.07 mm

3 Electrical Specifications

This section details the electrical specifications of the MMA053AA device.

3.1 Absolute Maximum Ratings

This following table shows the absolute maximum ratings of the MMA053AA device.

Table 1 • Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 °C to 150 °C
Operating temperature	–55 °C to 85 °C
Drain bias voltage, (V_D)	+12 V
Gate bias voltages, (V_{G1})	0 V
Gate bias voltages, (V_{G2})	+4 V
RF input power (7 dB compression)	TBD
DC power dissipation (T = 85 °C)	5.6 W
Channel temperature	175 °C
Thermal impedance	TBD
ESD sensitivity (HBM)	TBD

3.2 Specified Electrical Performance

The following table shows the specified electrical performance of the MMA053AA device at 25 °C, where V_{DD} is 11 V and I_{DD} is 410 mA. V_{G1} = –0.7 V and V_{G2} is not used.

Table 2 • Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		DC		8	GHz
Gain	DC–8 GHz		17		dB
Gain flatness	DC–8 GHz		±0.5		dB
Noise figure	2 GHz–8 GHz		3		dB
Input return loss	DC–8 GHz		–17		dB
Output return loss	DC–8 GHz		–15		dBm
P1dB	DC–8 GHz		29		dBm
Psat	DC–8 GHz		31		dBm
OIP3	DC–8 GHz		43		dBm
V_{DD} (drain voltage supply)			11		V
I_{DD} (drain current)			410		mA
V_{G1} (gate voltage supply)			0.7		V

3.3 Typical Performance Curves

The following graphs show the typical electrical performance curves of the MMA053AA device at 25 °C, where V_{DD} is 11 V and there is an on-chip V_{G2} bias.

Figure 2 • Gain and Return Loss vs. Frequency

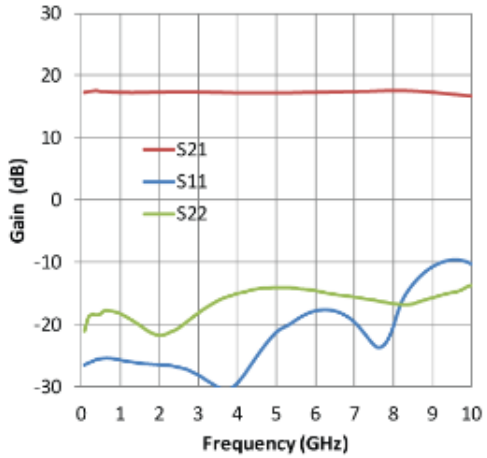


Figure 3 • Gain vs. Temperature

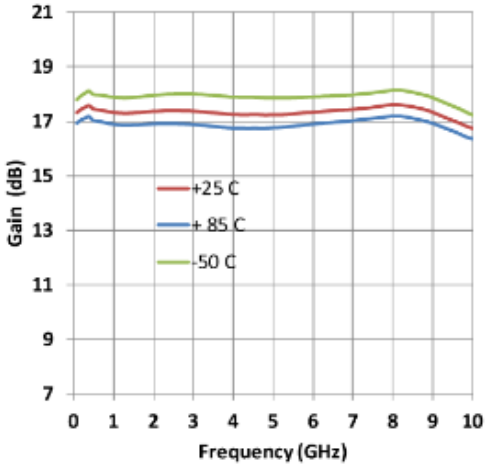


Figure 4 • Input Return Loss vs. Frequency

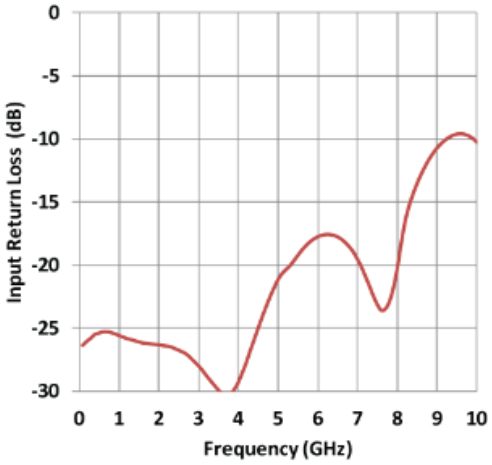


Figure 5 • Input Return Loss vs. Temperature

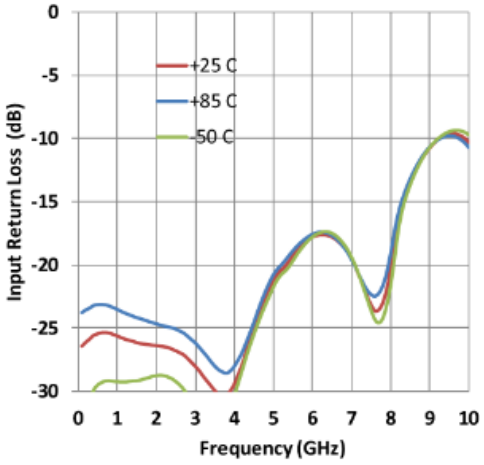


Figure 6 • Noise Figure vs. Frequency

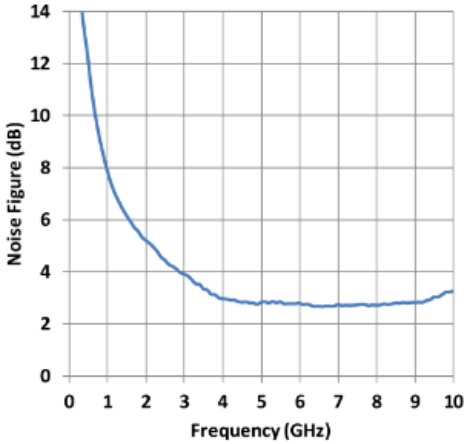


Figure 7 • Noise Figure vs. Temperature

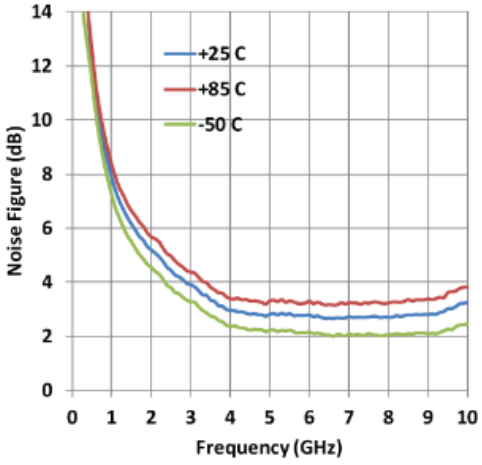


Figure 8 • Output Return Loss vs. Frequency

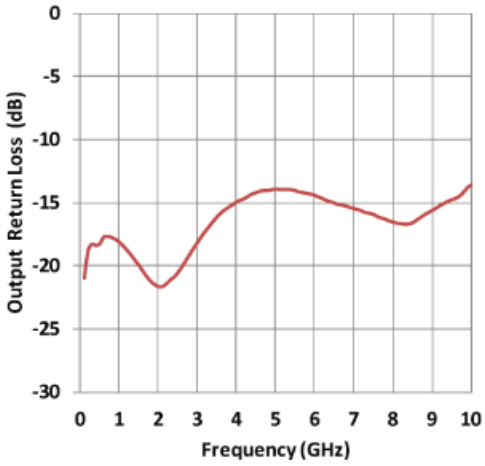


Figure 9 • Output Return Loss vs. Temperature

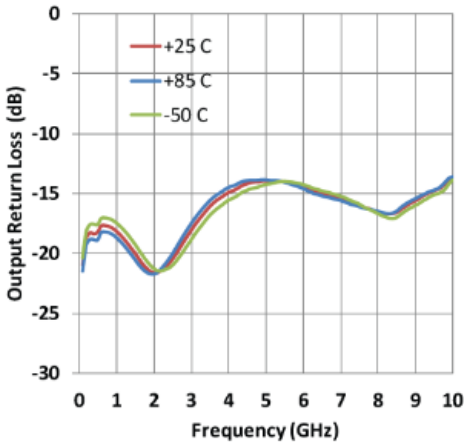


Figure 10 • Isolation vs. Frequency

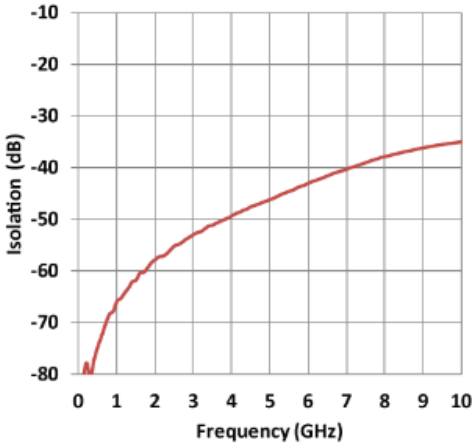


Figure 11 • Isolation vs. Temperature

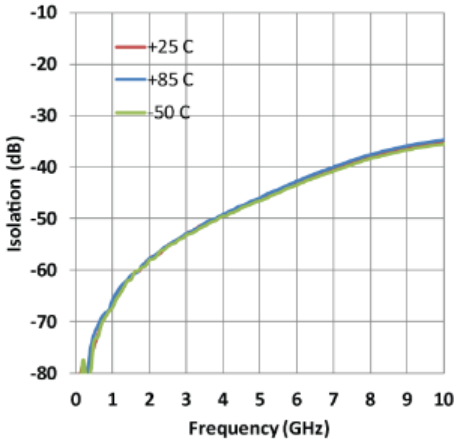


Figure 12 • OIP3 vs. Frequency

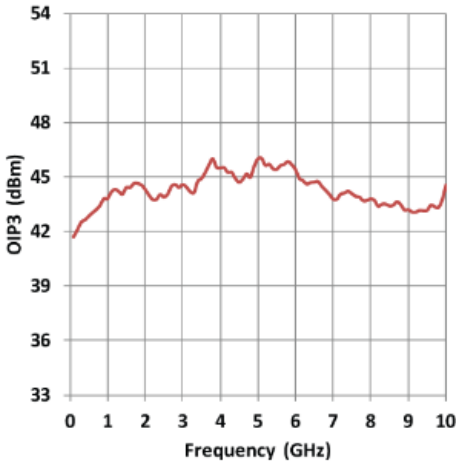


Figure 13 • OIP3 vs. Temperature

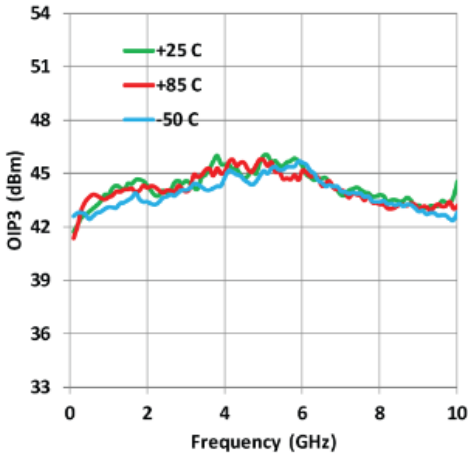


Figure 14 • P1dB vs. Frequency

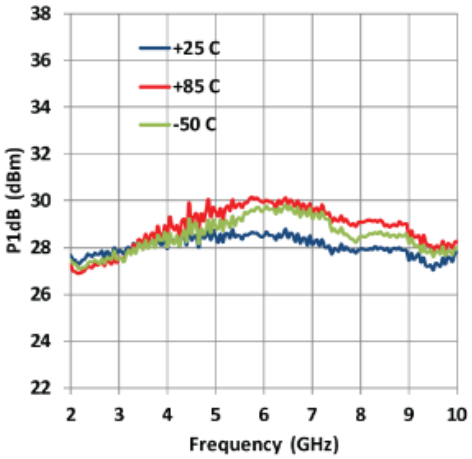
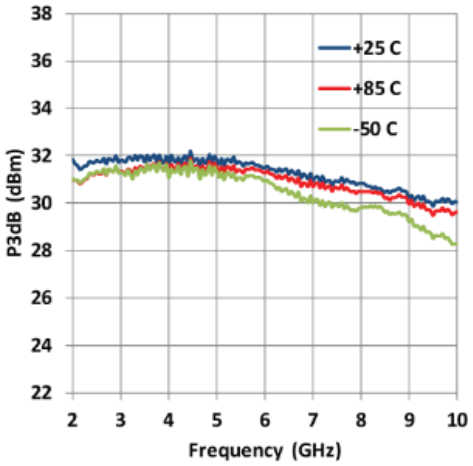


Figure 15 • P3dB vs. Frequency



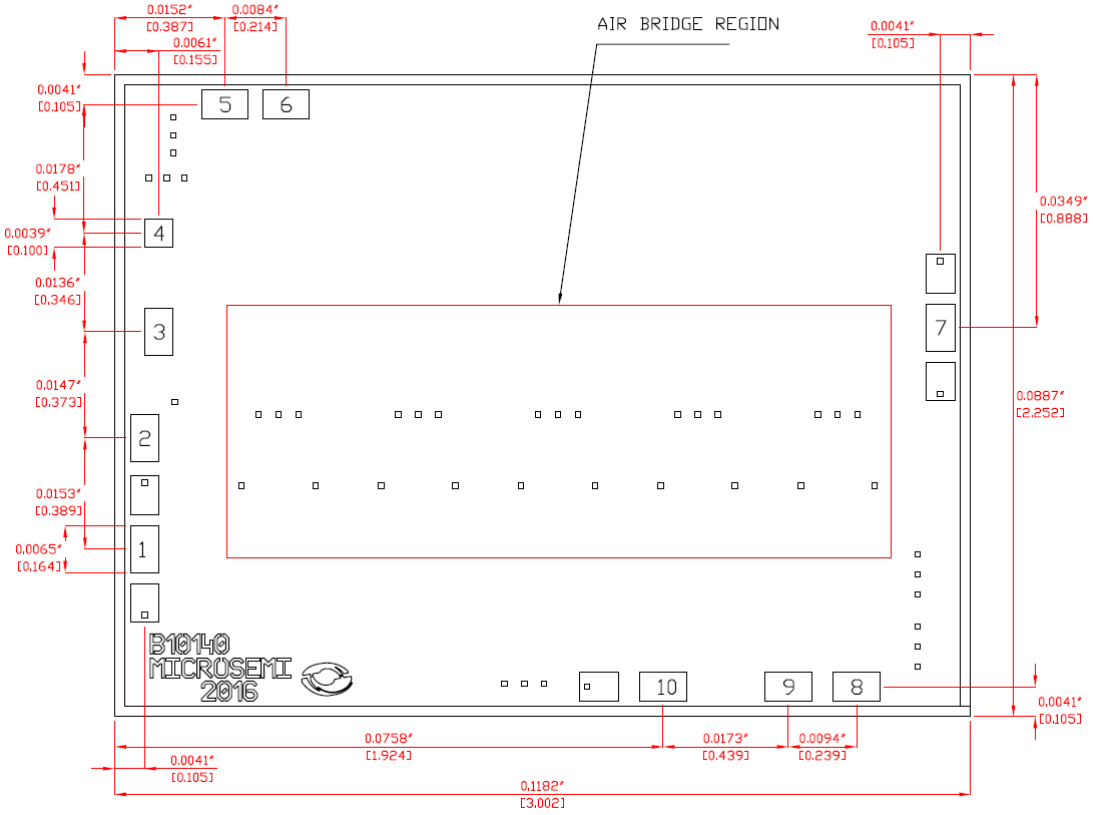
4 Chip Outline Specification

This section details the chip outline specifications of the MMA053AA device.

4.1 Chip Outline Drawing

The following illustration shows the package outline of the MMA053AA device. Dimensions are in millimeters [inches].

Figure 16 • Chip Outline Drawing



4.2 Die Packaging Information

The following table lists the die package information of the MMA053AA device. Contact your Microsemi sales representative for additional packaging information

Standard Format	Optimal Format
Waffle pack	Gel pack
50–100 pieces per pack	50 pieces per pack

4.3 Bond Pad Information

The following table lists the bond pad information of the MMA053AA device.

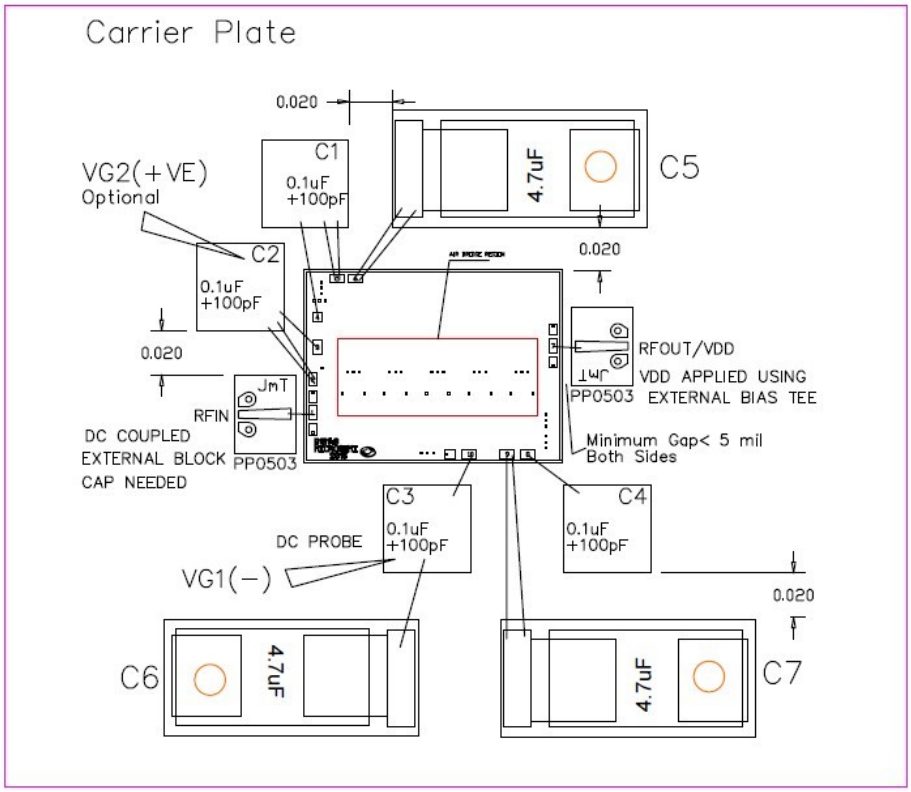
Table 3 • Bond Pad Information

Bond Pad Number	Bond Pad Name	Description
1	RFIN	This pad is AC/DC-coupled and matched to 50 Ω. External large DC blocking capacitor is required to extend performance to very low-frequencies.
2	VG2	External positive Gate 2 control (Optional) for amplifier. Please follow “MMIC Amplifier Biasing Procedure” application note. See application circuit/assembly for required external components.
3	VG2B	DC output for on-chip VG2 bias network. Must be connected to VG2 if on-chip VG2 bias network is to be used, otherwise no connection is required.
4	VG2A	DC input for on-chip VG2 bias network. Must be connected to DT1 if on-chip VG2 bias network is to be used, otherwise no connection is required.
5,6	DT1, DT2	Low-frequency drain termination. Attach external bypass capacitors as per application circuit.
7	RFOUT/VDD	This pad is AC/DC-coupled and matched to 50 Ω. External V_{DD} bias network is required to provide I_{DD} as per the application circuit
8,9	GT2, GT1	Low-frequency gate termination. Attach external bypass capacitors as per application circuit.
10	VG1	Negative Gate 1 control for amplifier. Please follow “MMIC Amplifier Biasing Procedure” application note. See application circuit/assembly for required external components.
Die Bottom	RF/DC ground	Die bottom must be connected to external RF/DC ground on carrier.

4.4 Assembly Diagram

The following illustration shows the assembly diagram of the MMA053AA device. The carrier plate is gold plated. It is necessary to attach components using conductive epoxy. The bypass chip caps are ceramic and must be assembled within 10 mils of the die. Use 1 mil Au bond wires.

Figure 17 • Assembly Diagram RF Probing With On-Chip VG2 Bias Configuration



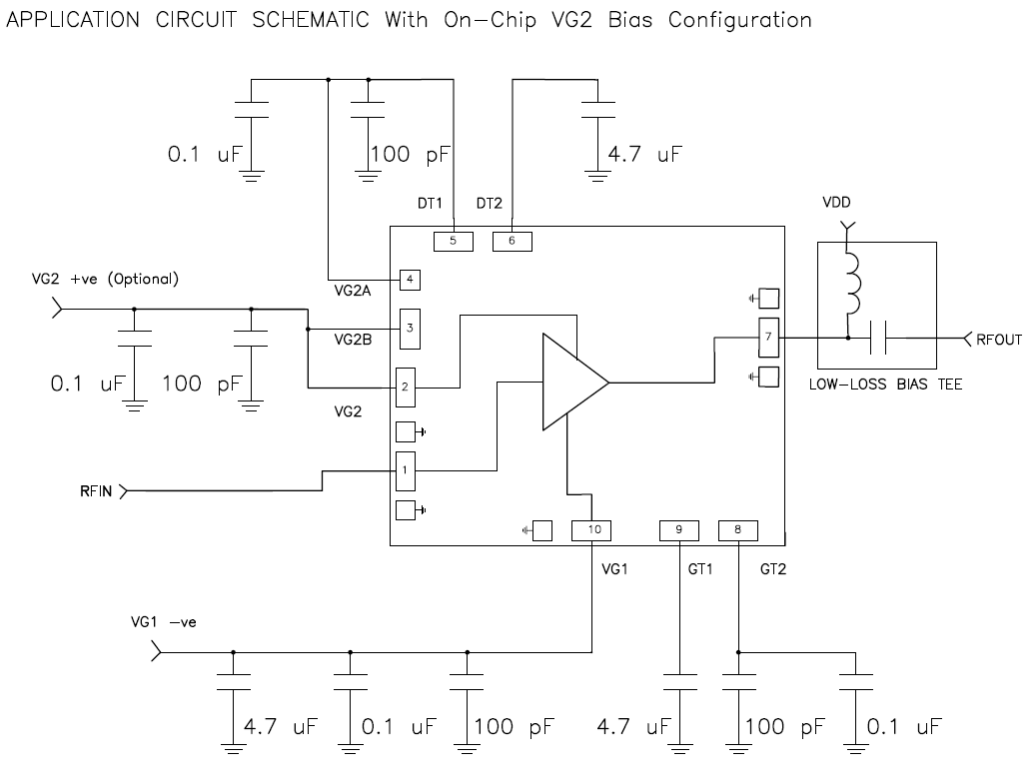
Notes:

1. Attach components on carrier plate using conductive epoxy.
2. VG2A connected to DT1 and VG2B connected to VG2 for on-chip VG2 bias. Disconnect to apply external VG2 bias.
3. Use 1 mil Au bond wires.
4. C1, C2, C3, C4: Presidio VB series dual cap P/N: MVB4040X104MEK5C1B
   C5, C6, C7: 4.7 µF on PCB insert.

4.5 Applications Information

The following illustration shows applications information for the MMA053AA device

Figure 18 • Application Circuit Schematic



5 Handling and Die Attachment Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01 GaAs MMIC Handling and Die Attach Recommendations.

6 Ordering Information

The following table lists the ordering information for the MMA053AA device.

Table 4 • Ordering Information

Part Number	Package
MMA053AA	Die in waffle or GEL pack

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One Enterprise, Aliso Viejo,
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