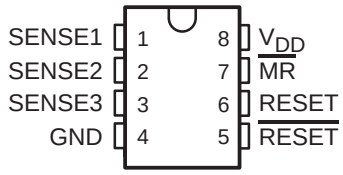
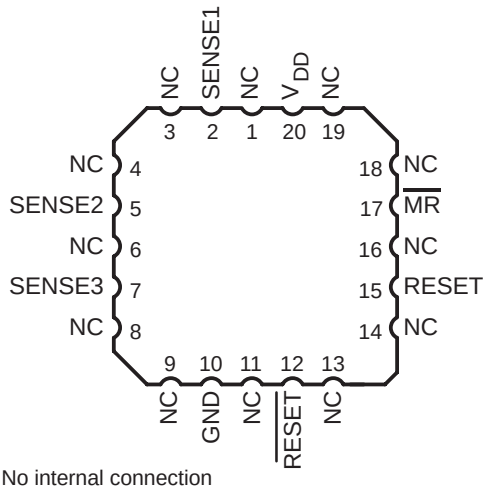
- **Qualified for Military Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Triple Supervisory Circuits for DSP and Processor-Based Systems**
- **Power-On Reset Generator with Fixed Delay Time of 200 ms, No External Capacitor Needed**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40 μA**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1.1$ V**
- **CDIP-8 and LCCC-20 Packages**
- **Temperature Range . . . −55°C to 125°C**

**JG PACKAGE**
**(TOP VIEW)**



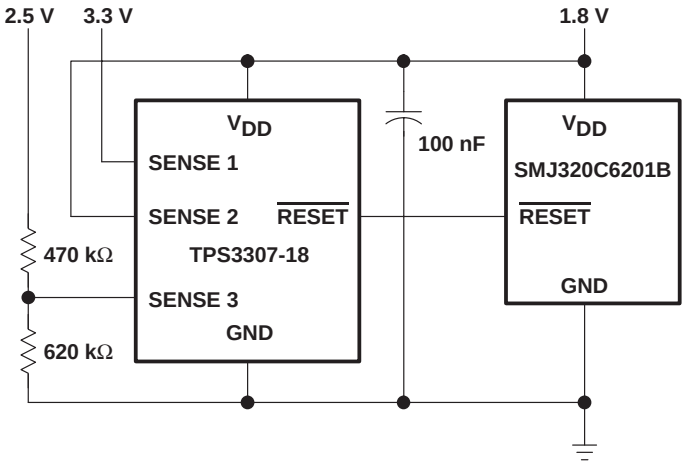

**FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307−18 and SMJ320C6201B.




- **Military applications using DSPs, Microcontrollers or Microprocessors**
- **Industrial Equipment**
- **Programmable Controls**

**Figure 1. Applications Using the TPS3307-18**

## description

The TPS3307-18 is a micropower supply voltage supervisor designed for circuit initialization primarily in automotive DSP and processor-based systems, which require more than one supply voltage.

The TPS3307-18 is designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj,. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## description (continued)

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

**SUPPLY VOLTAGE MONITORING**

| DEVICE | NOMINAL SUPERVISED VOLTAGE | | | THRESHOLD VOLTAGE (TYP) | | |
|---|---|---|---|---|---|---|
| | SENSE1 | SENSE2 | SENSE3 | SENSE1 | SENSE2 | SENSE3 |
| TPS3307-18 | 3.3 V | 1.8 V | User defined | 2.93 V | 1.68 V | 1.25 V† |

† The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage $V_{DD}$ becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps $\overline{\text{RESET}}$ active as long as SENSEn remain below the threshold voltage $V_{IT+}$.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\,typ}$ = 200 ms, starts after all SENSEn inputs have risen above the threshold voltage $V_{IT+}$. When the voltage at any SENSE input drops below the threshold voltage $V_{IT-}$, the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-18 incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-18 includes an active-high RESET output.

## ORDERING INFORMATION

| $T_A$ | PACKAGE‡ | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| −55°C to 125°C | Ceramic Dual In Line (JG) | TPS3307-18MJGB | TPS3307-18MJGB |
| | Leadless Ceramic Chip Carrier (FK) | TPS3307-18MFKB | TPS3307-18MFKB |

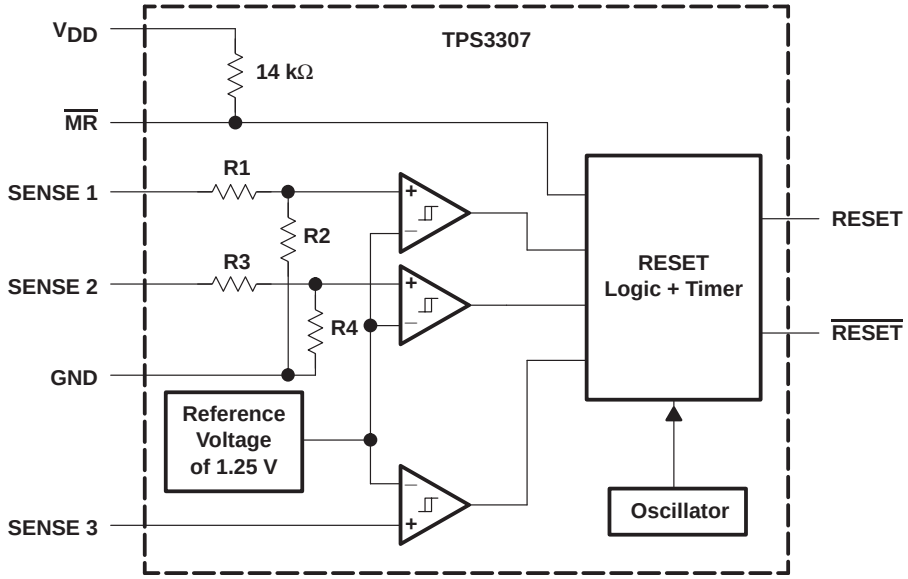
‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION/TRUTH TABLES**

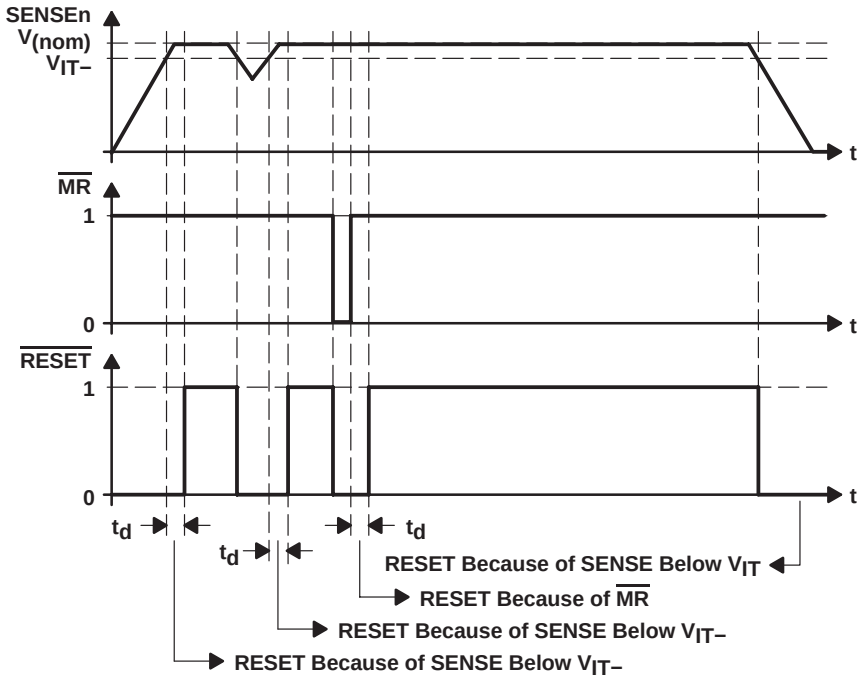
| $\overline{\text{MR}}$ | SENSE1>$V_{IT1}$ | SENSE2>$V_{IT2}$ | SENSE3>$V_{IT3}$ | $\overline{\text{RESET}}$ | RESET |
|---|---|---|---|---|---|
| L | X | X | X | L | H |
| H | 0 | 0 | 0 | L | H |
| H | 0 | 0 | 1 | L | H |
| H | 0 | 1 | 0 | L | H |
| H | 0 | 1 | 1 | L | H |
| H | 1 | 0 | 0 | L | H |
| H | 1 | 0 | 1 | L | H |
| H | 1 | 1 | 0 | L | H |
| H | 1 | 1 | 1 | H | L |

X = Don't care

## functional block diagram




## timing diagram



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note1) . . . . . 7 V
All other pins (see Note 1) . . . . . −0.3 V to 7 V
Maximum low output current, $I_{OL}$ . . . . . 5 mA
Maximum high output current, $I_{OH}$ . . . . . −5 mA
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$ . . . . . −55°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000 h continuously.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| JG | 1 W | 6.25 mW/°C | 719 mW | 625 mW | 375 mW |
| FK | 1.39 W | 11.58 mW/°C | 869 mW | 695 mW | 232 mW |

## recommended operating conditions at specified temperature range

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{DD}$ | 2 | 6 | V |
| Input voltage at $\overline{MR}$ and SENSE3, $V_I$ | 0 | $V_{DD}$+0.3 | V |
| Input voltage at SENSE1 and SENSE2, $V_I$ | 0 | $(V_{DD}+0.3)V_{IT}/1.25V$ | V |
| High-level input voltage at $\overline{MR}$, $V_{IH}$ | $0.7xV_{DD}$ | | V |
| Low-level input voltage at $\overline{MR}$, $V_{IL}$ | | $0.3\times V_{DD}$ | V |
| Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$ | | 50 | ns/V |
| Operating free-air temperature range, $T_A$ | −55 | 125 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $V_{DD}$ = 2 V to 6 V, $I_{OH}$ = −20 µA | $V_{DD}$ − 0.2V | | | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OH}$ = −2 mA | $V_{DD}$ − 0.4V | | | |
| | | | $V_{DD}$ = 6 V, $I_{OH}$ = −3 mA | $V_{DD}$ − 0.4V | | | |
| $V_{OL}$ | Low-level output voltage | | $V_{DD}$ = 2 V to 6 V, $I_{OL}$ = 20 µA | | | 0.2 | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OL}$ = 2 mA | | | 0.4 | |
| | | | $V_{DD}$ = 6 V, $I_{OL}$ = 3 mA | | | 0.4 | |
| | Power-up reset voltage (see Note 2) | | $V_{DD} \geq$ 1.1 V, $I_{OL}$ = 20 µA | | | 0.4 | V |
| $V_{IT-}$ | Negative-going input threshold voltage (see Note 3) | VSENSE3 | $V_{DD}$ = 2 V to 6 V | 1.22 | 1.25 | 1.29 | V |
| | | VSENSE2 | | 1.64 | 1.68 | 1.73 | V |
| | | VSENSE1 | | 2.86 | 2.93 | 3.02 | |
| $V_{hys}$ | Hysteresis at VSENSEn input | | $V_{IT-}$ = 1.25 V | 2 | 10 | 30 | mV |
| | | | $V_{IT-}$ = 1.68 V | 2 | 15 | 40 | |
| | | | $V_{IT-}$ = 2.93 V | 3 | 30 | 60 | |
| $I_H$ | High-level input current | $\overline{MR}$ | $\overline{MR}$ = 0.7 × $V_{DD}$, $V_{DD}$ = 6 V | | −130 | −180 | µA |
| | | SENSE1 | VSENSE1 = $V_{DD}$ = 6 V | | 5 | 8 | |
| | | SENSE2 | VSENSE2 = $V_{DD}$ = 6 V | | 6 | 9 | |
| | | SENSE3 | VSENSE3 = $V_{DD}$ | −25 | | 25 | nA |
| $I_L$ | Low-level input current | $\overline{MR}$ | $\overline{MR}$ = 0 V, $V_{DD}$ = 6 V | | −430 | −600 | µA |
| | | SENSEn | VSENSE1,2,3 = 0 V | −1 | | 1 | |
| $I_{DD}$ | Supply current | | | | | 40 | µA |
| $C_i$ | Input capacitance | | $V_I$ = 0 V to $V_{DD}$ | | 10 | | pF |

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_r$, $V_{DD} \geq$ 15 µs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 µF) should be placed close to the supply terminals.

## timing requirements at $V_{DD}$ = 2 V to 6 V, $R_L$ = 1 MΩ, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_w$ | Pulse width | SENSEn | $V_{SENSEnL} = V_{IT-} - 0.2$ V, $V_{SENSEnH} = V_{IT+} + 0.2$ V | 6 | 10 | | µs |
| | | $\overline{MR}$ | $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$ | 100 | 150 | | ns |

## switching characteristics at $V_{DD}$ = 2 V to 6 V, $R_L$ = 1 MΩ, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time | | $V_{I(SENSEn)} \geq V_{IT+} + 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$, See timing diagram | 140 | 200 | 280 | ms |
| $t_{PHL}$ | Propagation (delay) time, high-to-low level output | $\overline{MR}$ to $\overline{RESET}$<br>$\overline{MR}$ to RESET | $V_{I(SENSEn)} \geq V_{IT+} + 0.2$ V, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$ | | 200 | 600 | ns |
| $t_{PLH}$ | Propagation (delay) time, low-to-high level output | $\overline{MR}$ to $\overline{RESET}$<br>$\overline{MR}$ to RESET | | | | | |
| $t_{PHL}$ | Propagation (delay) time, high-to-low level output | SENSEn to $\overline{RESET}$ | $V_{IH} = V_{IT+} + 0.2$ V, $V_{IL} = V_{IT-} - 0.2$ V, $\overline{MR} \geq 0.7 \times V_{DD}$ | | 1 | 5 | µs |
| $t_{PLH}$ | Propagation (delay) time, low-to-high level output | SENSEn to RESET | | | | | |

## TYPICAL CHARACTERISTICS

**NORMALIZED SENSE THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT $V_{DD}$**

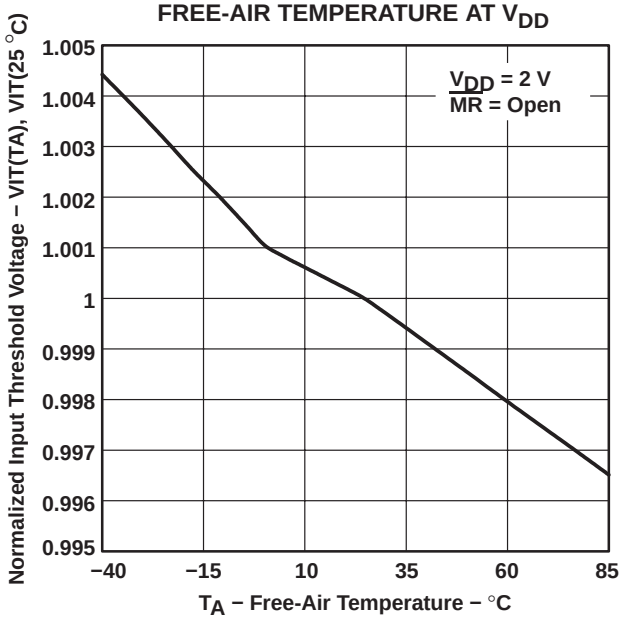



Figure 2

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

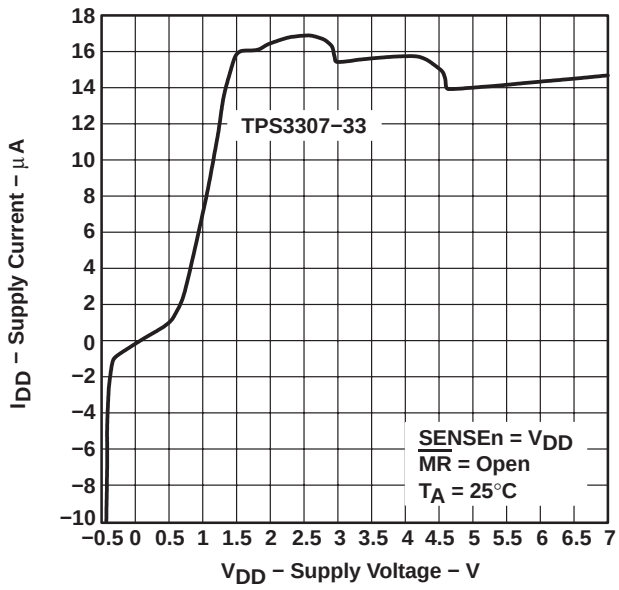



Figure 3

**INPUT CURRENT vs INPUT VOLTAGE AT $\overline{MR}$**

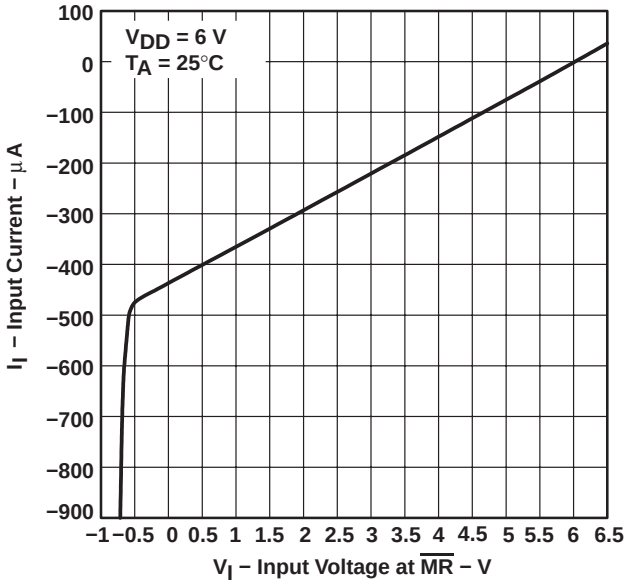



Figure 4

**MINIMUM PULSE DURATION AT SENSE vs THRESHOLD OVERDRIVE**

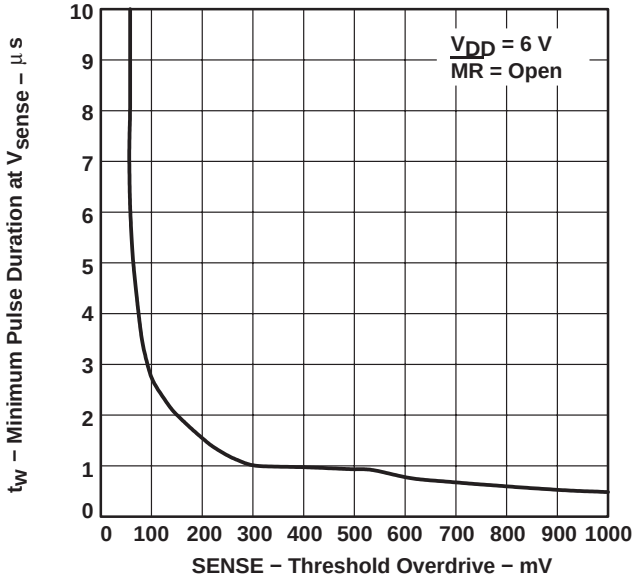



Figure 5

## TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

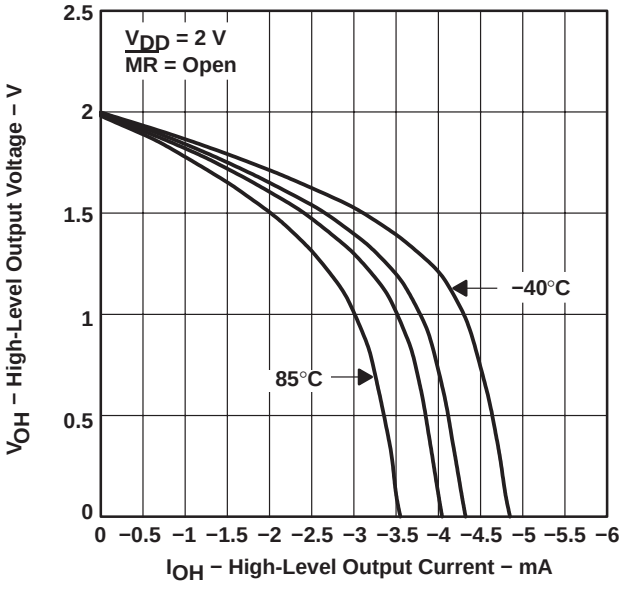



Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

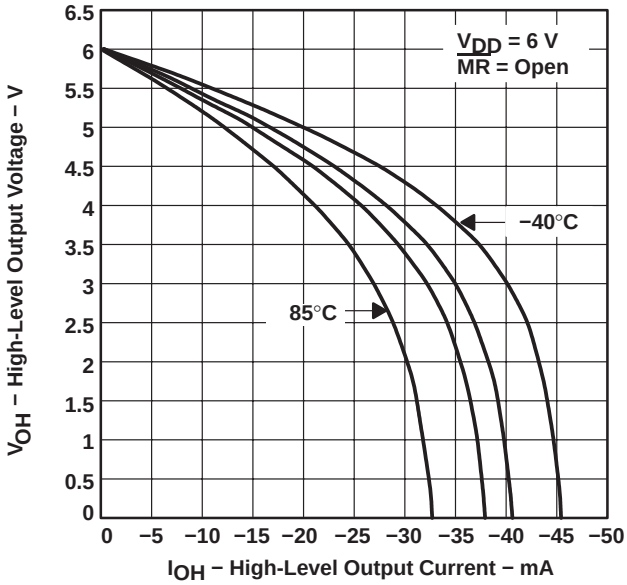



Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

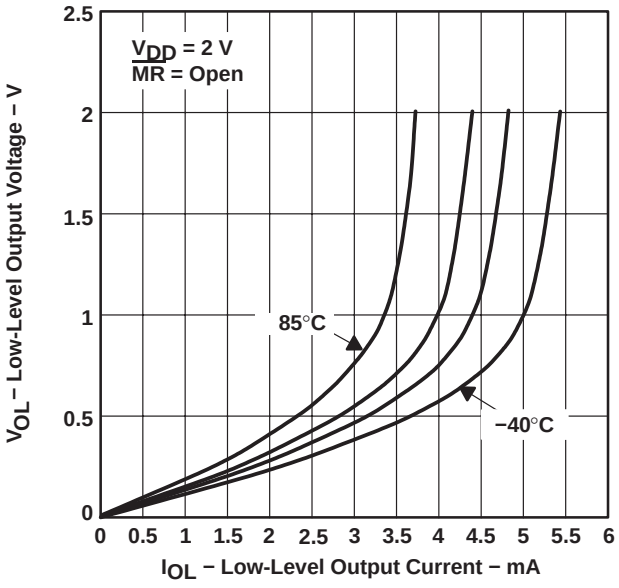



Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

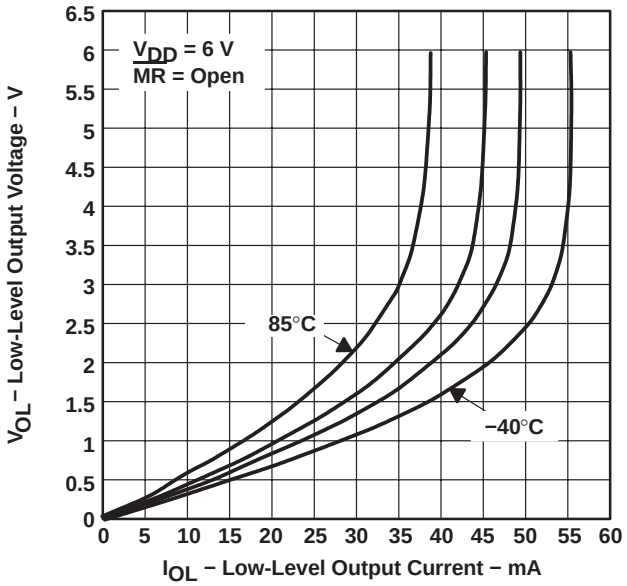



Figure 9

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9959101Q2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9959101Q2A TPS3307-18MFKB | Samples |
| 5962-9959101QPA | ACTIVE | CDIP | JG | 8 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9959101QPA TPS3307-18M | Samples |
| TPS3307-18MFKB | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9959101Q2A TPS3307-18MFKB | Samples |
| TPS3307-18MJGB | ACTIVE | CDIP | JG | 8 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 9959101QPA TPS3307-18M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



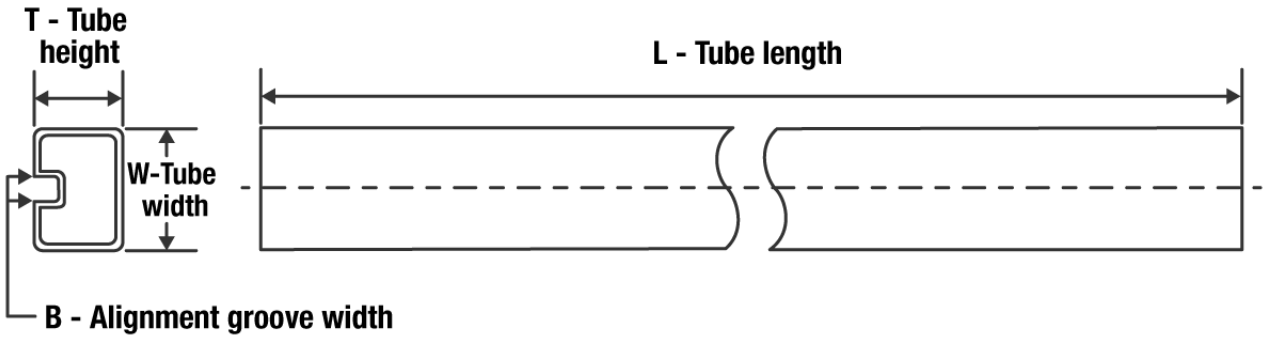
**OTHER QUALIFIED VERSIONS OF TPS3307-18M :**

- Automotive : TPS3307-18-Q1
- Enhanced Product : TPS3307-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9959101Q2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| TPS3307-18MFKB | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |

# GENERIC PACKAGE VIEW

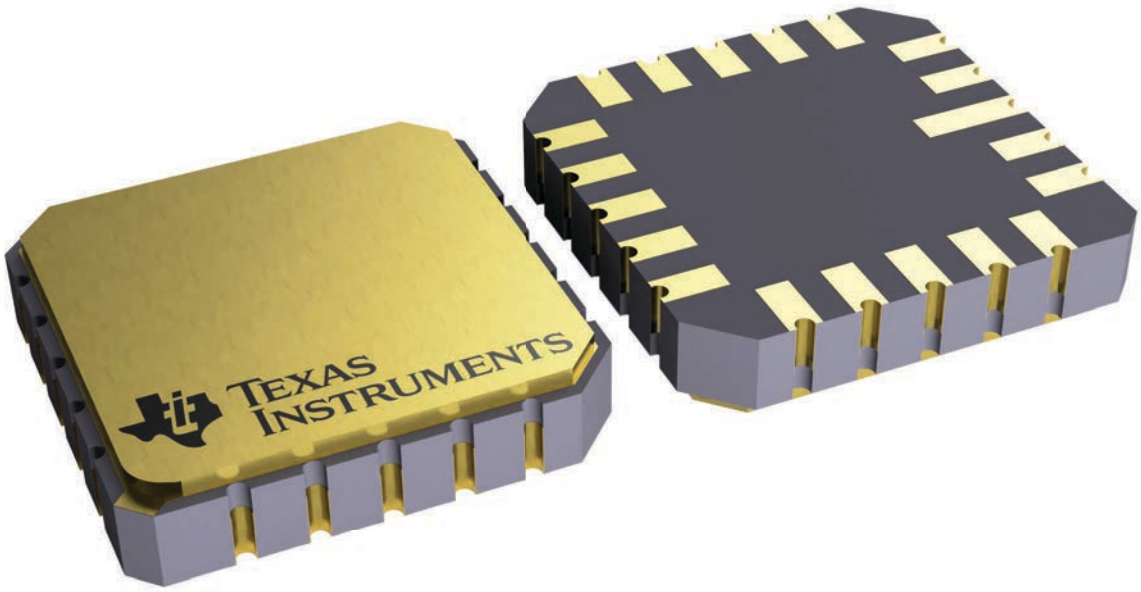
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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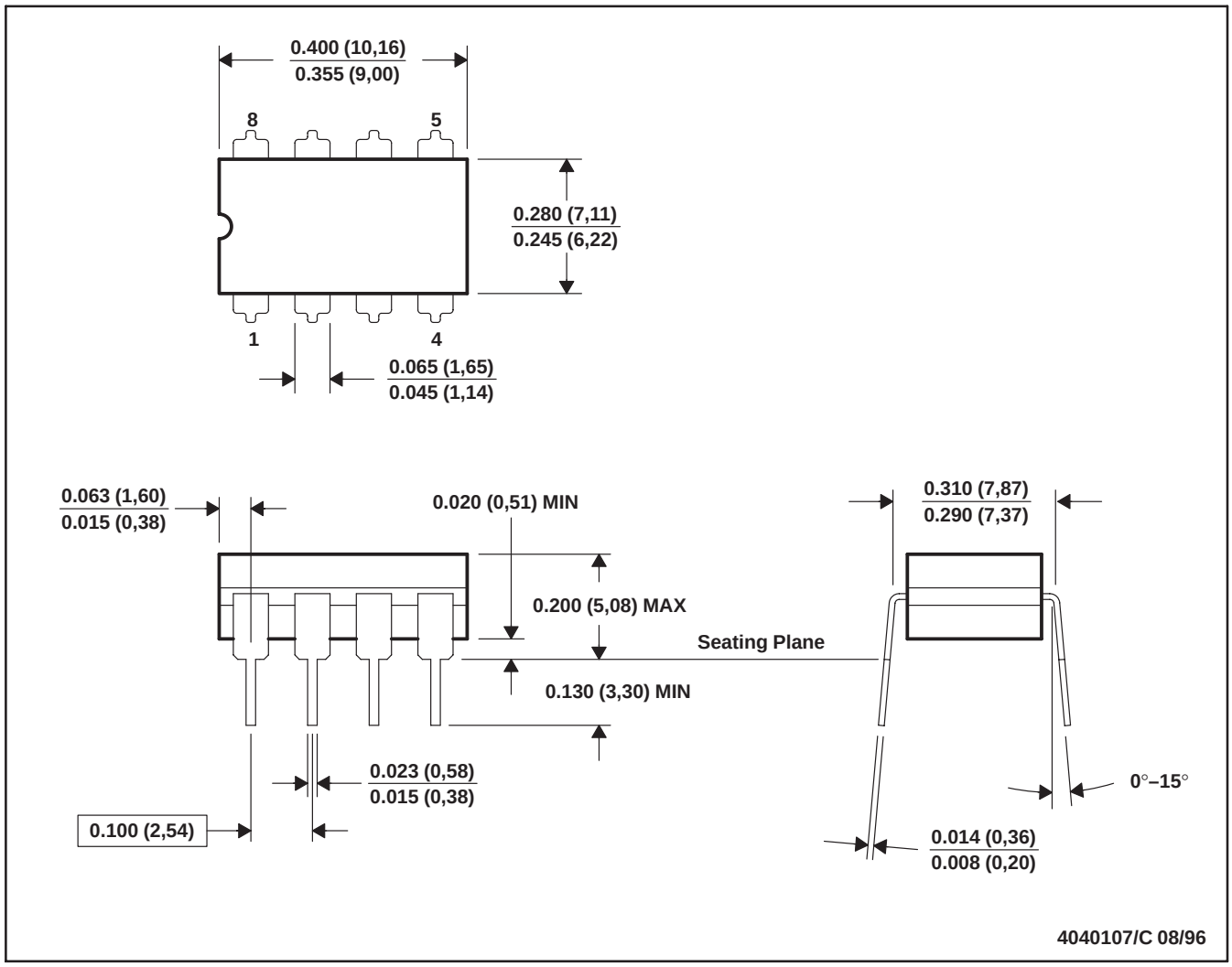
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

**JG (R-GDIP-T8)** **CERAMIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

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