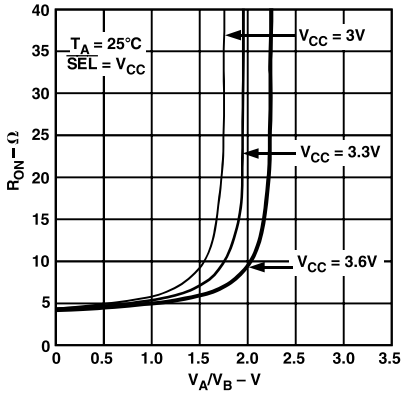
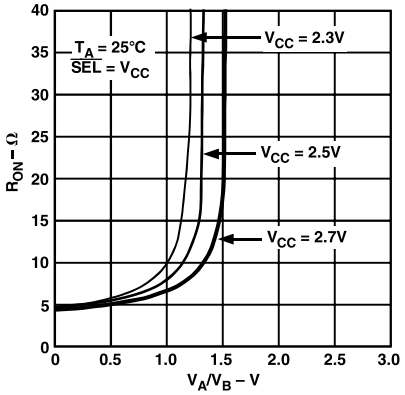
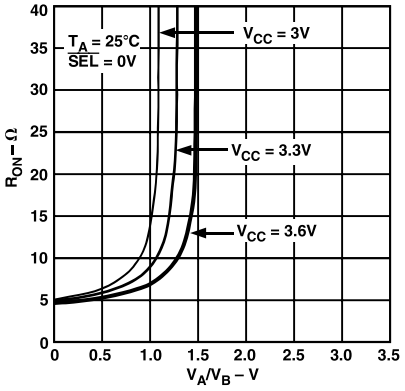


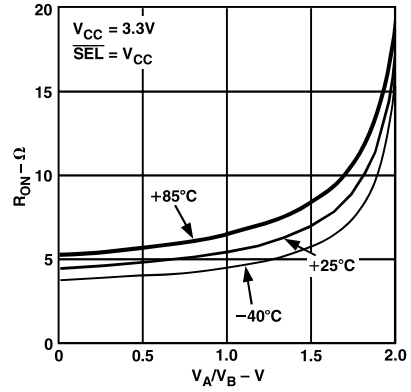
TPC 1. On Resistance vs. Input Voltage



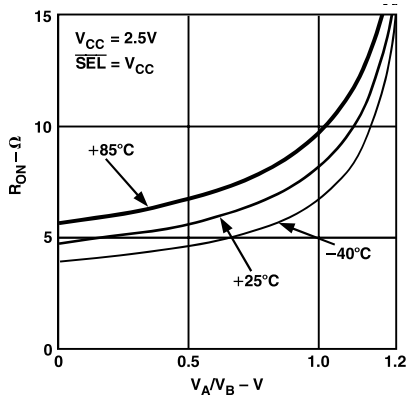
TPC 2. On Resistance vs. Input Voltage



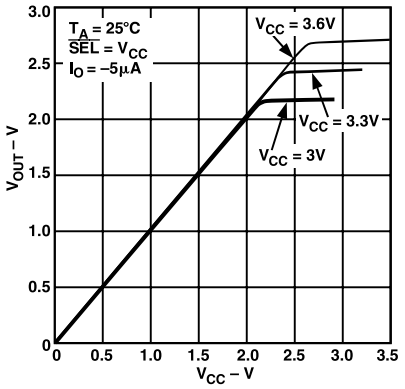
TPC 3. On Resistance vs. Input Voltage



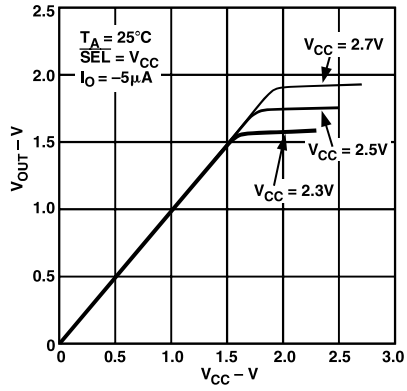
TPC 4. On Resistance vs. Input Voltage for Different Temperatures



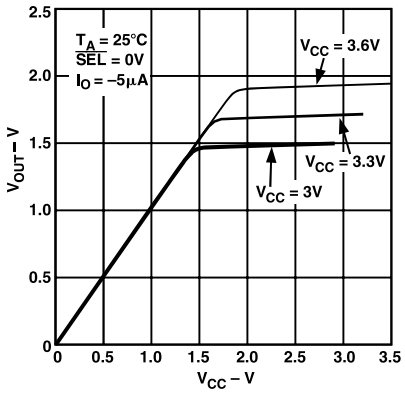
TPC 5. On Resistance vs. Input Voltage for Different Temperatures



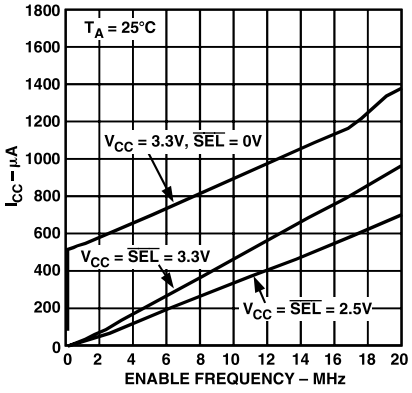
TPC 6. Pass Voltage vs. V_{CC}



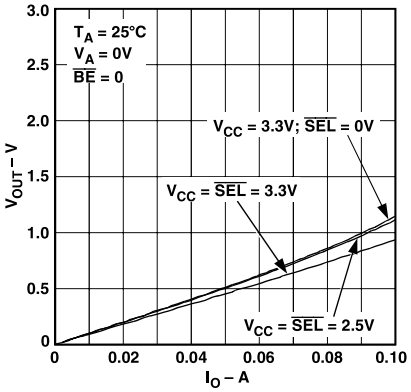
TPC 7. Pass Voltage vs. V_{CC}



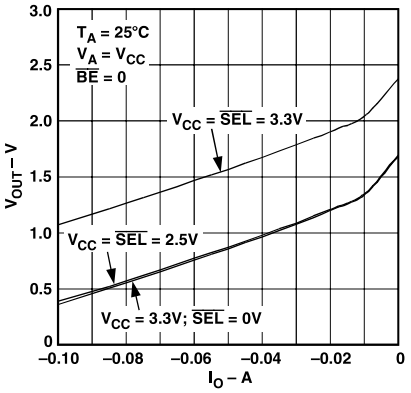
TPC 8. Pass Voltage vs. V_{CC}



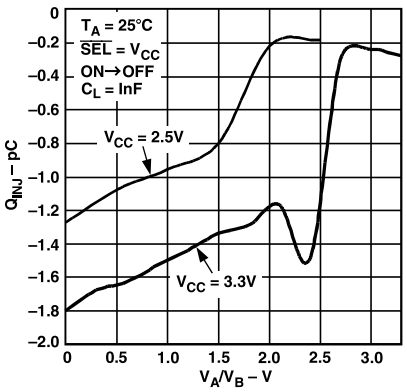
TPC 9. I_{CC} vs. Enable Frequency



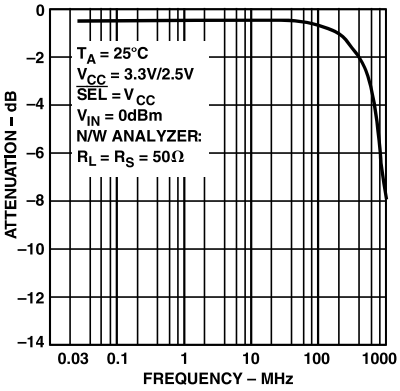
TPC 10. Output Low Characteristic



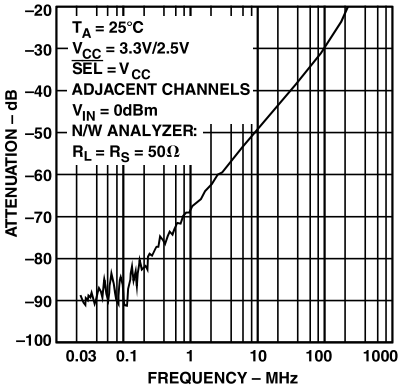
TPC 11. Output High Characteristic



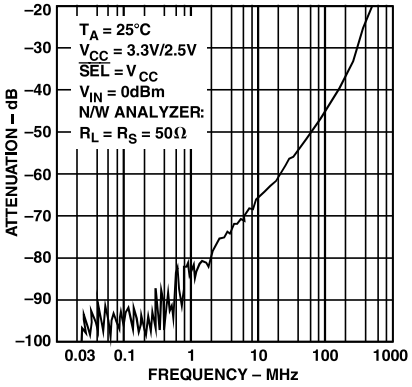
TPC 12. Charge Injection vs. Source Voltage



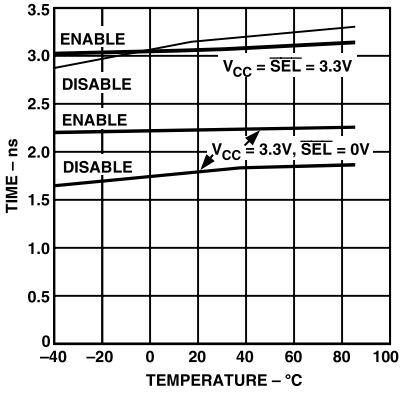
TPC 13. Bandwidth vs. Frequency



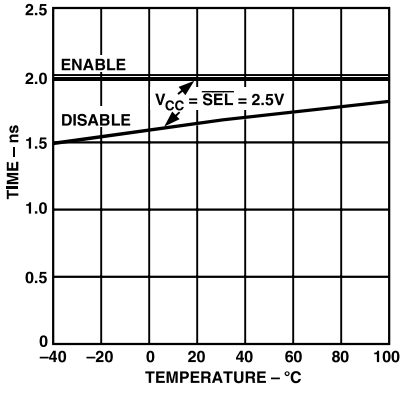
TPC 14. Crosstalk vs. Frequency



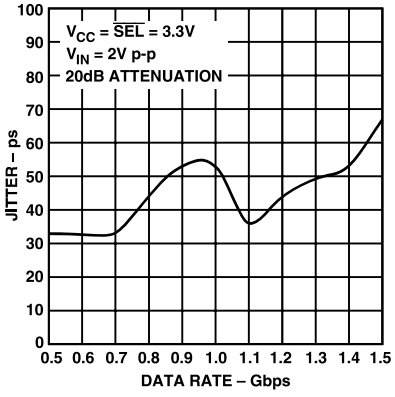
TPC 15. Off Isolation vs. Frequency



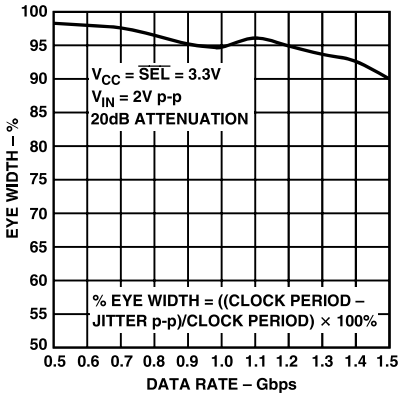
TPC 16. Enable/Disable Time vs. Temperature



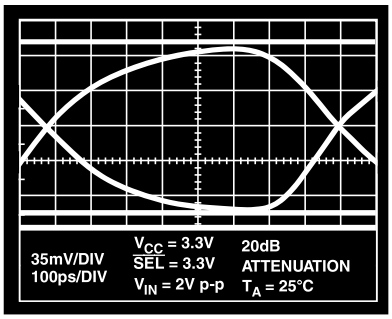
TPC 17. Enable/Disable Time vs. Temperature



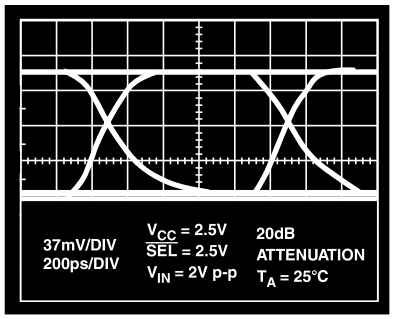
TPC 18. Jitter vs. Data Rate; PRBS 31



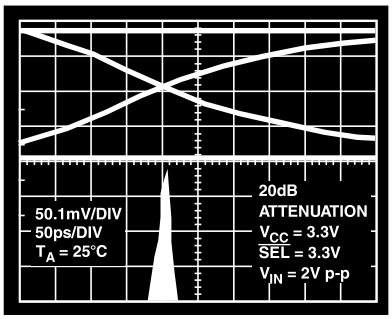
TPC 19. Eye Width vs. Data Rate; PRBS 31



TPC 20. Eye Pattern; 1.244 Gbps, V_{CC} = 3.3 V, PRBS 31



TPC 21. Eye Pattern; 1 Gbps, V_{CC} = 2.5 V, PRBS 31

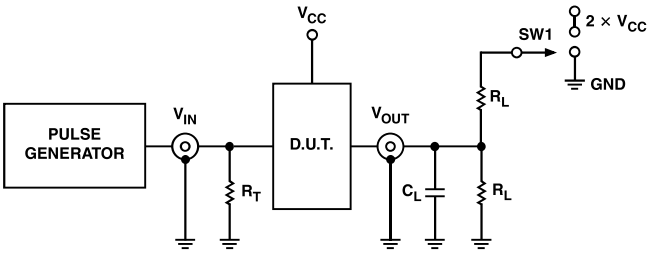


TPC 22. Jitter @ 1.244 Gbps, PRBS 31

TIMING MEASUREMENT INFORMATION

For the following load circuit and waveforms, the notation that is used is V_{IN} and V_{OUT} where

$$V_{IN} = V_A \text{ and } V_{OUT} = V_B \text{ or } V_{IN} = V_B \text{ and } V_{OUT} = V_A$$



NOTES
PULSE GENERATOR FOR ALL PULSES: $t_R \leq 2.5$ns, $t_F \leq 2.5$ns, FREQUENCY $\leq$ 10MHz.
C_L INCLUDES BOARD, STRAY, AND LOAD CAPACITANCES
R_T IS THE TERMINATION RESISTOR, SHOULD BE EQUAL TO Z_{OUT} OF THE PULSE GENERATOR.

Figure 1. Load Circuit

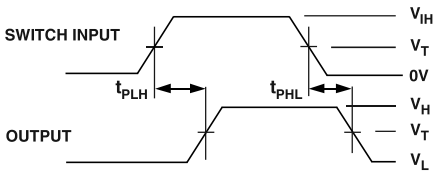


Figure 2. Propagation Delay

Test Conditions

Symbol	V_{CC} = 3.3 V ± 0.3 V ($\overline{SEL}$ = V_{CC})	V_{CC} = 2.5 V ± 0.2 V ($\overline{SEL}$ = V_{CC})	V_{CC} = 3.3 V ± 0.3 V ($\overline{SEL}$ = 0 V)	Unit
R_L	500	500	500	Ω
V_Δ	300	150	150	mV
C_L	50	30	30	pF
V_T	1.5	0.9	0.9	V

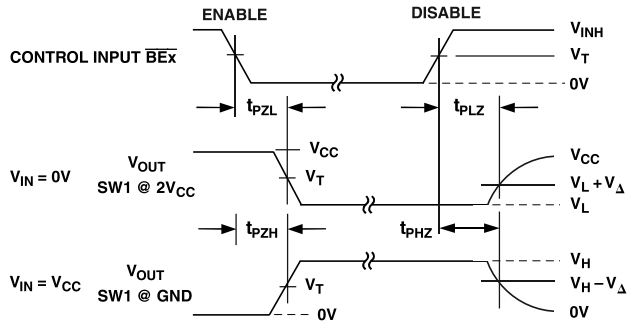


Figure 3. Enable and Disable Times

Table III. Switch Position

TEST	S1
t_{PLZ}, t_{PZL}	2 × V_{CC}
t_{PHZ}, t_{PZH}	GND

BUS SWITCH APPLICATIONS

Mixed Voltage Operation, Level Translation

Bus switches can be used to provide an ideal solution for interfacing between mixed voltage systems. The ADG3247 is suitable for applications where voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 3.3 V to 1.8 V, from 2.5 V to 1.8 V, or from 3.3 V directly to 2.5 V.

Figure 4 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs; therefore placing the ADG3247 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

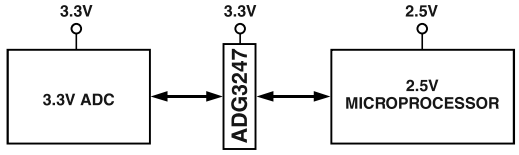


Figure 4. Level Translation between a 3.3 V ADC and a 2.5 V Microprocessor

3.3 V to 2.5 V Translation

When V_{CC} is 3.3 V ($\overline{SEL}$ = V_{CC}) and the input signal range is 0 V to V_{CC}, the maximum output signal will be clamped to within a voltage threshold below the V_{CC} supply.

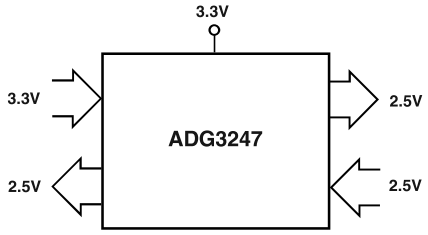


Figure 5. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

In this case, the output will be limited to 2.5 V, as shown in Figure 6.

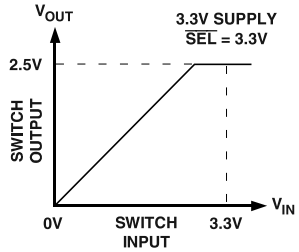


Figure 6. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

2.5 V to 1.8 V Translation

When V_{CC} is 2.5 V ($\overline{SEL}$ = V_{CC}) and the input signal range is 0 V to V_{CC}, the maximum output signal will, as before, be clamped to within a voltage threshold below the V_{CC} supply.

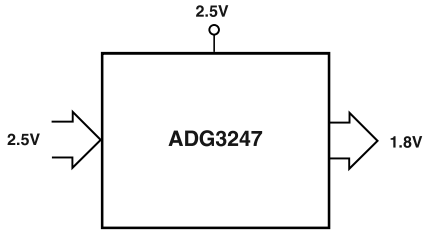


Figure 7. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = V_{CC}

In this case, the output will be limited to approximately 1.8 V, as shown in Figure 7.

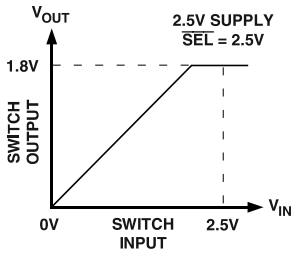


Figure 8. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = V_{CC}

3.3 V to 1.8 V Translation

The ADG3247 offers the option of interfacing between a 3.3 V device and a 1.8 V device. This is possible through use of the $\overline{SEL}$ pin.

$\overline{SEL}$ pin: An active low control pin. $\overline{SEL}$ activates internal circuitry in the ADG3247 that allows voltage translation between 3.3 V devices and 1.8 V devices.

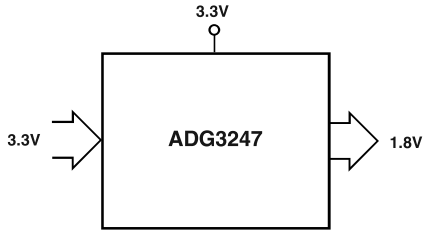


Figure 9. 3.3 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 0 V

When V_{CC} is 3.3 V and the input signal range is 0 V to V_{CC}, the maximum output signal will be clamped to 1.8 V, as shown in Figure 9. To do this, the $\overline{SEL}$ pin must be tied to Logic 0. If $\overline{SEL}$ is unused, it should be tied directly to V_{CC}.

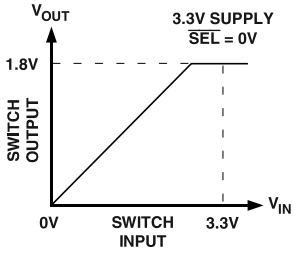


Figure 10. 3.3 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 0 V

Bus Isolation

A common requirement of bus architectures is low capacitance loading of the bus. Such systems require bus bridge devices that extend the number of loads on the bus without exceeding the specifications. Because the ADG3247 is designed specifically for applications that do not need drive yet require simple logic functions, it solves this requirement. The device isolates access to the bus, thus minimizing capacitance loading.

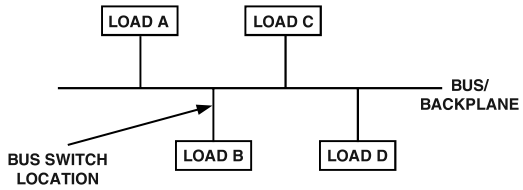


Figure 11. Location of Bus Switched in a Bus Isolation Application

Hot Plug and Hot Swap Isolation

The ADG3247 is suitable for hot swap and hot plug applications. The output signal of the ADG3247 is limited to a voltage that is below the V_{CC} supply, as shown in Figures 6, 8, and 10. Therefore the switch acts like a buffer to take the impact from hot insertion, protecting vital and expensive chipsets from damage.

In hot-plug applications, the system cannot be shutdown when new hardware is being added. To overcome this, a bus switch can be positioned on the backplane between the bus devices and the hot plug connectors. The bus switch is turned off during hot plug. Figure 12 shows a typical example of this type of application.

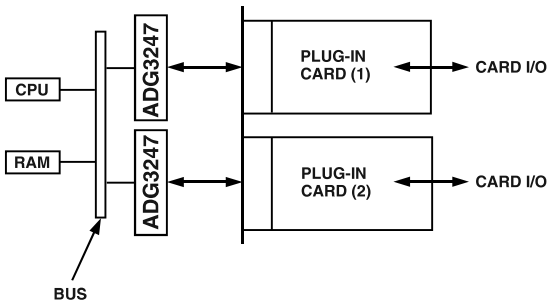


Figure 12. ADG3247 in a Hot Plug Application

There are many systems that require the ability to handle hot swapping, such as docking stations, PCI boards for servers, and line cards for telecommunications switches. If the bus can be isolated prior to insertion or removal, then there is more control over the hot swap event. This isolation can be achieved using a bus switch. The bus switches are positioned on the hot swap card between the connector and the devices. During hot swap, the ground pin of the hot swap card must connect to the ground pin of the back plane before any other signal or power pins.

Analog Switching

Bus switches can be used in many analog switching applications; for example, video graphics. Bus switches can have lower on resistance, smaller ON and OFF channel capacitance and thus improved frequency performance than their analog counterparts. The bus switch channel itself consisting solely of an NMOS switch limits the operating voltage (see TPC 1 for a typical plot), but in many cases, this does not present an issue.

High Impedance during Power-Up/Power-Down

To ensure the high impedance state during power-up or power-down, BEx should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PACKAGE AND PINOUT

The ADG3247 is packaged in a small 38-lead TSSOP. The area of the TSSOP option is 62.7 mm^2.

The ADG3247 in the TSSOP package offers a flowthrough pinout. The term flowthrough signifies that all the inputs are on opposite sides from the outputs. A flowthrough pinout simplifies the PCB layout.

OUTLINE DIMENSIONS

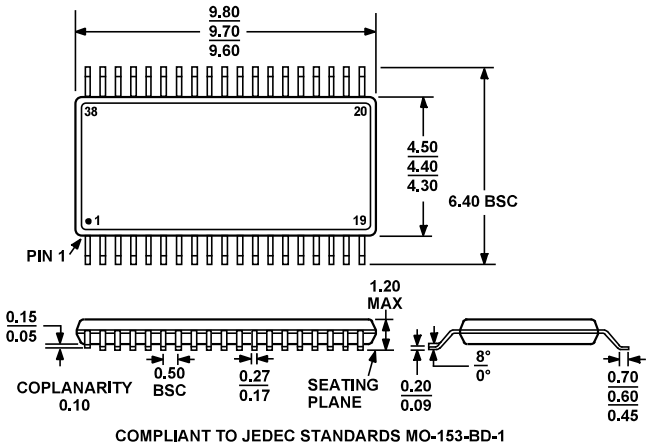


Figure 13. 38-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-38)
Dimensions shown in millimeters

REVISION HISTORY

6/2019—Rev. A to Rev. B

Deleted 40-Lead LFCSP ..... Universal
Changes to Ordering Guide 3
Updated Outline Dimensions 11

5/2017—Rev. 0 to Rev. A

Change to Mixed Voltage Operation, Level Translation Section 9
Updated Outline Dimensions 11

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