The Future of Analog IC Technology

MP157

Smallest Energy Efficient Off-line Regulator with Extended Power Range

DESCRIPTION

MP157 is a primary side regulator providing accurate constant voltage (CV) regulation without the Opto-coupler. It supports Buck, Buck-Boost, Boost and Flyback topologies. A 500V MOSFET is integrated in the regulator, so very simple structure and low cost can be achieved. These features make MP157 an ideal solution for off-line low power applications. Typical applications include home appliance, standby power and industrial control.

MP157 is a green mode operation regulator. When the load decreases, the peak current and the switching frequency decrease with the load. As a result, it still offers excellent efficiency performance at light load, thus better average efficiency is achieved.

MP157 features various protections like Thermal Shutdown (TSD), VCC under Voltage Lockout (UVLO), Over Load Protection (OLP), Short Circuit Protection (SCP), Open Loop Protection.

MP157 is available in the TSOT23-5 and SOIC8 packages.

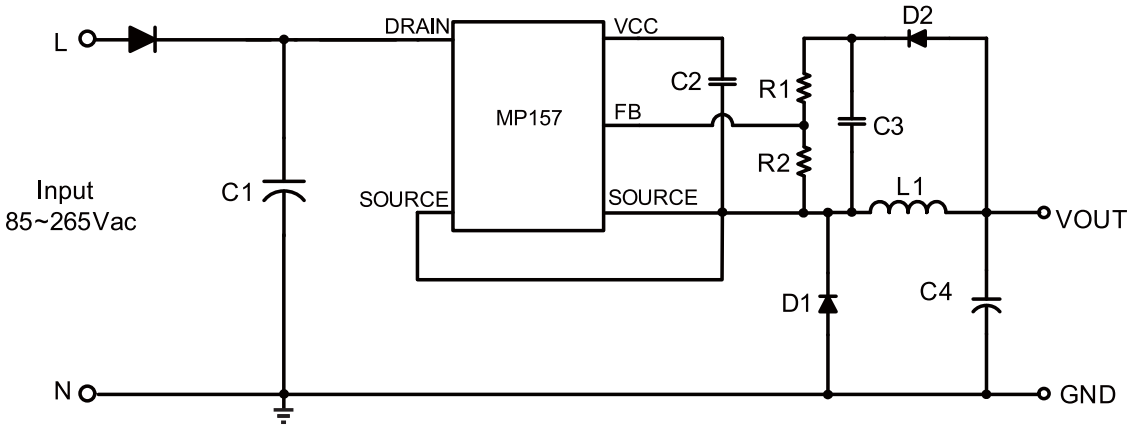
FEATURES

- Primary side constant voltage (CV) control, supporting Buck, Buck-Boost, Boost and Flyback topologies
- Integrated 500V/10Ω MOSFET
- < 100mW No-load power consumption
- Up to 6W output power
- Maximum discontinuous conduction mode (DCM) output current less than 225mA, maximum continuous conduction mode (CCM) output current less than 360mA
- Low Vcc Operating Current
- Frequency Foldback
- Limited maximum frequency
- Peak Current Compression
- Internal High Voltage Current Source
- Internal 400ns Leading Edge Blanking
- Thermal Shutdown (auto restart)
- VCC Under Voltage Lockout with Hysteresis (UVLO)
- Timer based Over Load Protection
- Short Circuit Protection
- Open Loop Protection

APPLICATIONS

- Home Appliances, White Goods and Consumer Electronics
- Industrial Controls
- Standby Power

TYPICAL APPLICATION

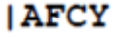


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP157GJ	TSOT23-5	*See Below*
MP157GS	SOIC-8	*See Below*

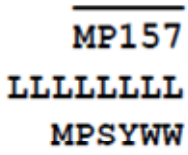
* For Tape & Reel, add suffix –Z (e.g. MP157GJ–Z);
* For Tape & Reel, add suffix –Z (e.g. MP157GS–Z);

TOP MARKING (MP157GJ)



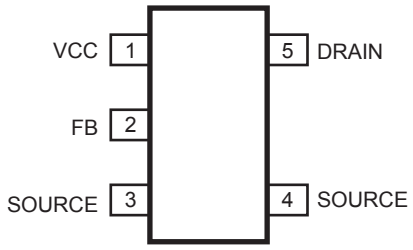
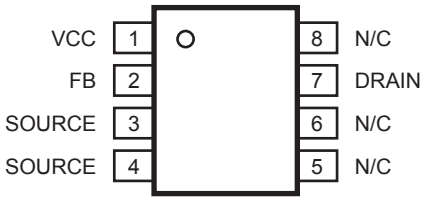
AFC: product code of MP157GJ;
Y: year code;

TOP MARKING (MP157GS)



MP157: product code of MP157GS;
MPS: MPS prefix:
Y: year code;
WW: week code:
LLLLLLLL: lot number;

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
TSOT23-5	**SOIC-8**

ABSOLUTE MAXIMUM RATINGS (1)

Drain to SOURCE ..... -0.3V to 500V
All the other Pin ..... -0.3V to 6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
TSOT23-5 ..... 1W
SOIC8 ..... 1W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -60°C to +150°C
ESD Capability Human Body Mode 2.0kV
ESD Capability Machine Mode 200V

Recommended Operating Conditions (3)

Operating Junction Temp. (T_J). -40°C to +125°C
Operating VCC range ..... 4.45V to 4.6V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-5	100	55	°C/W
SOIC-8	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

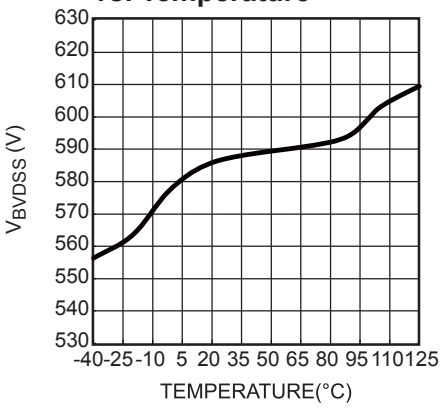
Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-up Current Source (Drain Pin)						
Internal regulator supply current	$I_{regulator}$	V_{CC}=4V;V_{Drain}=100V	2.5	3.5	4.5	mA
Leakage Current from Pin Drain	I_{Leak}	V_{CC}=5V;V_{darin}=400V	--	10	25	μA
Break Down Voltage	$V_{(BR)DSS}$		500	--	--	V
Supply Voltage Management (VCC Pin)						
VCC Increasing Level at which the internal regulator stops	VCC_{OFF}		4.5	4.6	4.9	V
VCC Decreasing Level at which the internal regulator Turns-On	VCC_{ON}		4.3	4.45	4.7	V
VCC Regulator on and off Hysteresis			--	230	--	mV
VCC Decreasing level at which the IC stops working	VCC_{stop}		3.2	3.35	3.5	V
VCC Decreasing Level at which the protection Phase Ends	VCC_{pro}		2.05	2.35	2.65	V
Internal IC Consumption	I_{CC}	V_{CC}=4.6V, Fs=45kHz Duty= 40%	--	--	500	μA
Internal IC Consumption (No Switch)	I_{CC}	V_{CC}=4.6V	--	--	165	uA
Internal IC Consumption, Latch off Phase	$I_{CCLATCH}$	V_{CC}=5V	--	16	--	μA
Internal MOSFET (Drain Pin)						
Break Down Voltage	V_{BRDSS}		500	--	--	V
On-State resistance	R_{on}		--	10	--	Ω
Internal Current Sense						
Peak Current Limit	I_{Limit}		500	640	780	mA
Leading edge blanking	T_{LEB1}		--	400	--	ns
SCP point	I_{SCP}		--	900	1200	mA
Leading edge blanking for SCP (5)	T_{LEB2}		--	180	--	ns
Feedback input (FB Pin)						
Minimum off time	T_{minoff}		10.6	13.1	15.6	us
Feedback Threshold to turn on the primary MOSFET	V_{FB}		2.45	2.55	2.65	V
Feedback Threshold to trigger the OLP	V_{FB_OLP}		1.6	1.7	1.8	V
Over Load Protection Delay time	T_{OLP}	Fs=37kHz	--	150	--	ms
Open loop detection	V_{OLD}		--	60	--	mV
Thermal Shutdown						
Thermal shutdown threshold (5)			--	150	--	ºC

Notes:

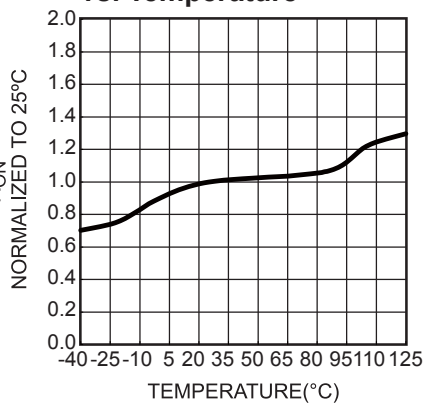
5) Guarantee by Characterization

TYPICAL CHARACTERISTICS

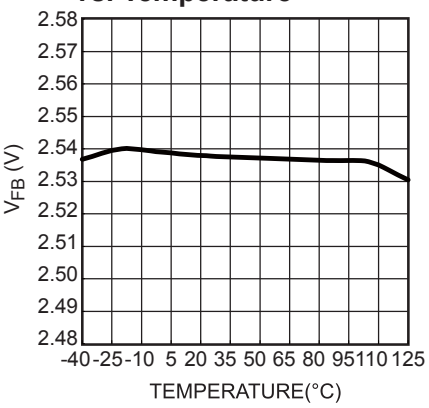
Break Down Voltage vs. Temperature



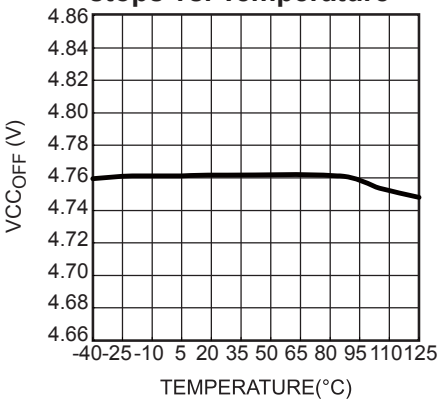
On-State Resistance vs. Temperature



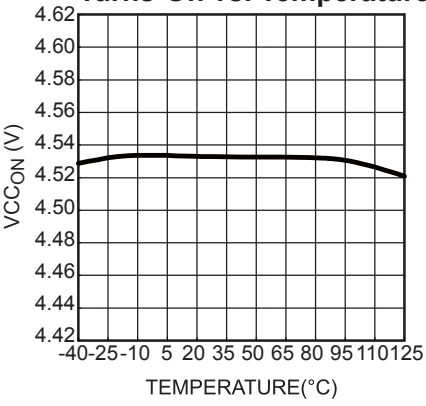
Feedback Threshold vs. Temperature



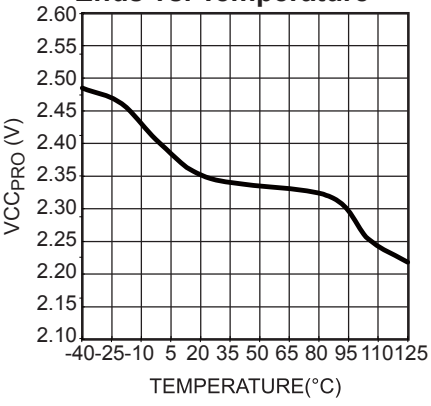
VCC Increasing Level at which the internal regulator stops vs. Temperature



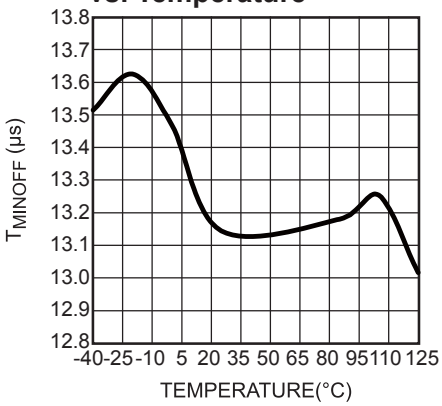
VCC Decreasing Level at which the internal regulator Turns-On vs. Temperature



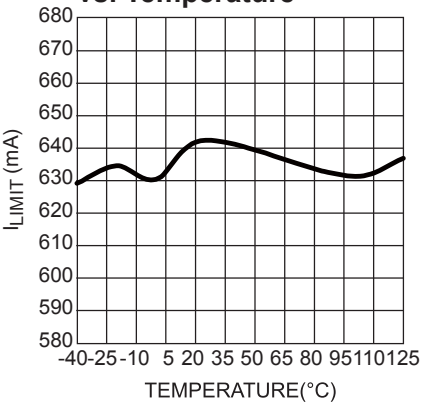
VCC Decreasing Level at which the protection Phase Ends vs. Temperature



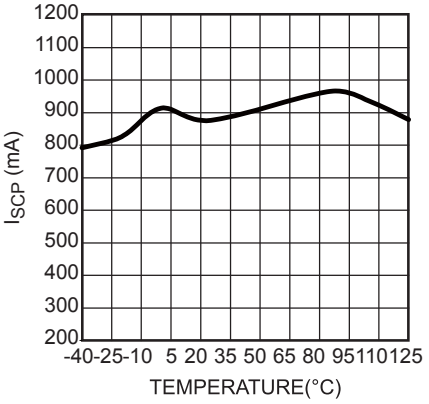
Minimum Off Time vs. Temperature



Peak Current Limit vs. Temperature



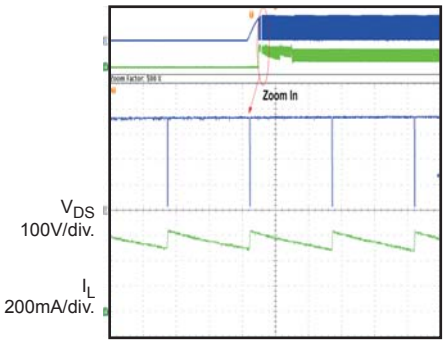
SCP Point vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

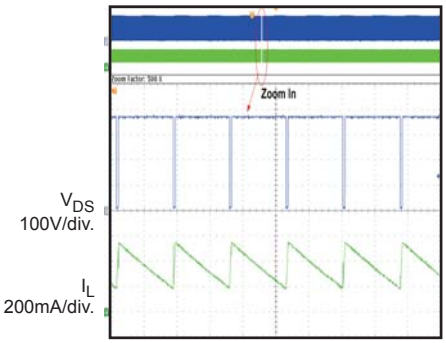
V_{IN} = 265VAC, V_{OUT} = 12V, I_{OUT} = 350mA, L = 1.2mH, C_{OUT} = 100µF, T_A = +25°C, unless otherwise noted.

Start Up



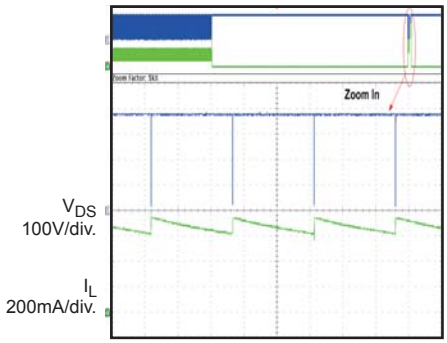
20µs/div.

Normal Operation



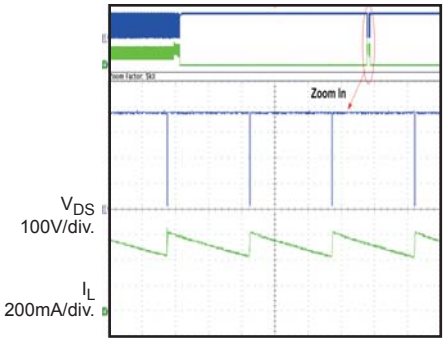
20µs/div.

SCP



20µs/div.

Open Loop

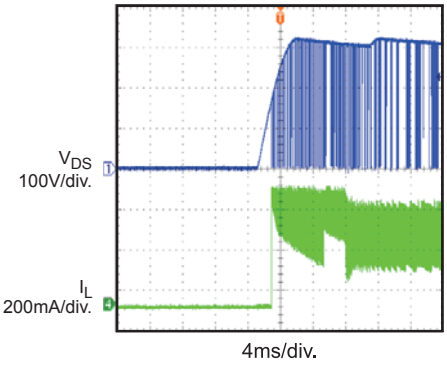


20µs/div.

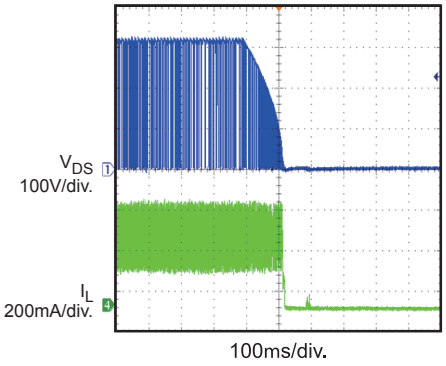
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 230VAC, V_{OUT} = 12V, I_{OUT} = 350mA, L = 1.2mH, C_{OUT} = 100µF, T_A = +25°C, unless otherwise noted.

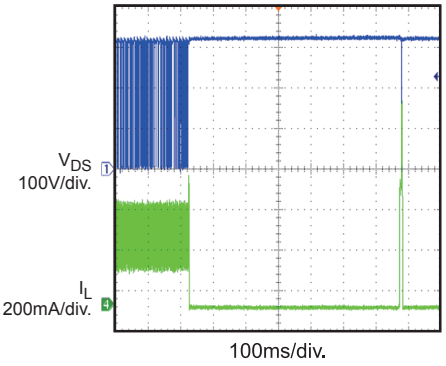
Input Power Start Up



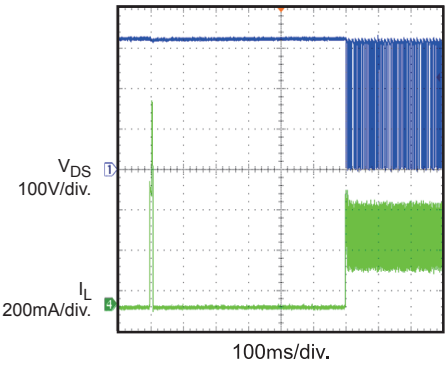
Input Power Shut Down



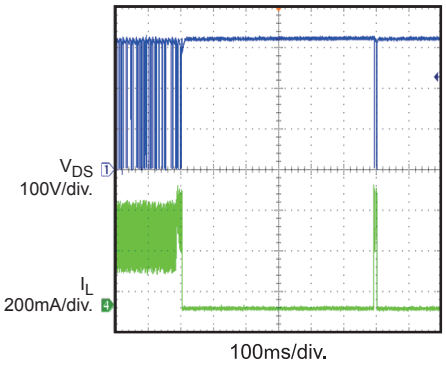
SCP Entry



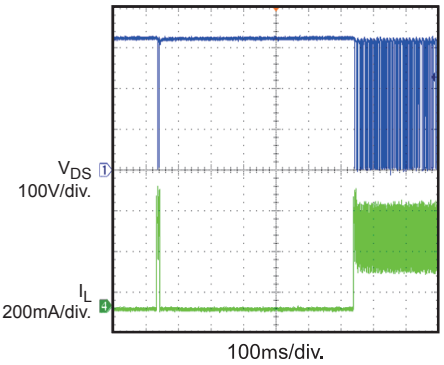
SCP Recovery



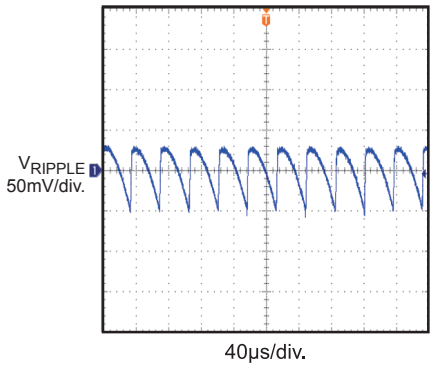
Open Loop Entry



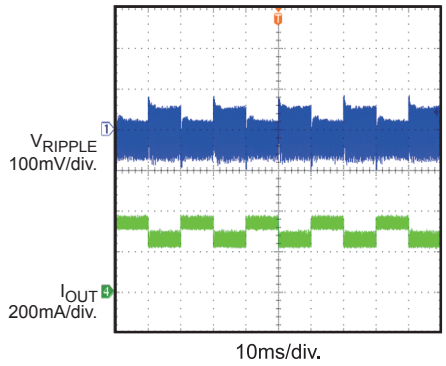
Open Loop Recovery



Output Voltage Ripple



Load Transient



PIN FUNCTIONS

Pin # TSOT23-5	Pin# SOIC8	Name	Description
1	1	VCC	Power supply of all the control circuit.
2	2	FB	Feedback of the regulator.
3,4	3,4	SOURCE	Source of internal power MOSFET. Ground reference for VCC and FB pins.
5	7	DRAIN	Drain of internal power MOSFET. Input of high voltage current source.
	5,6,8	N/C	Not connected.

FUNCTIONAL BLOCK DIAGRAM

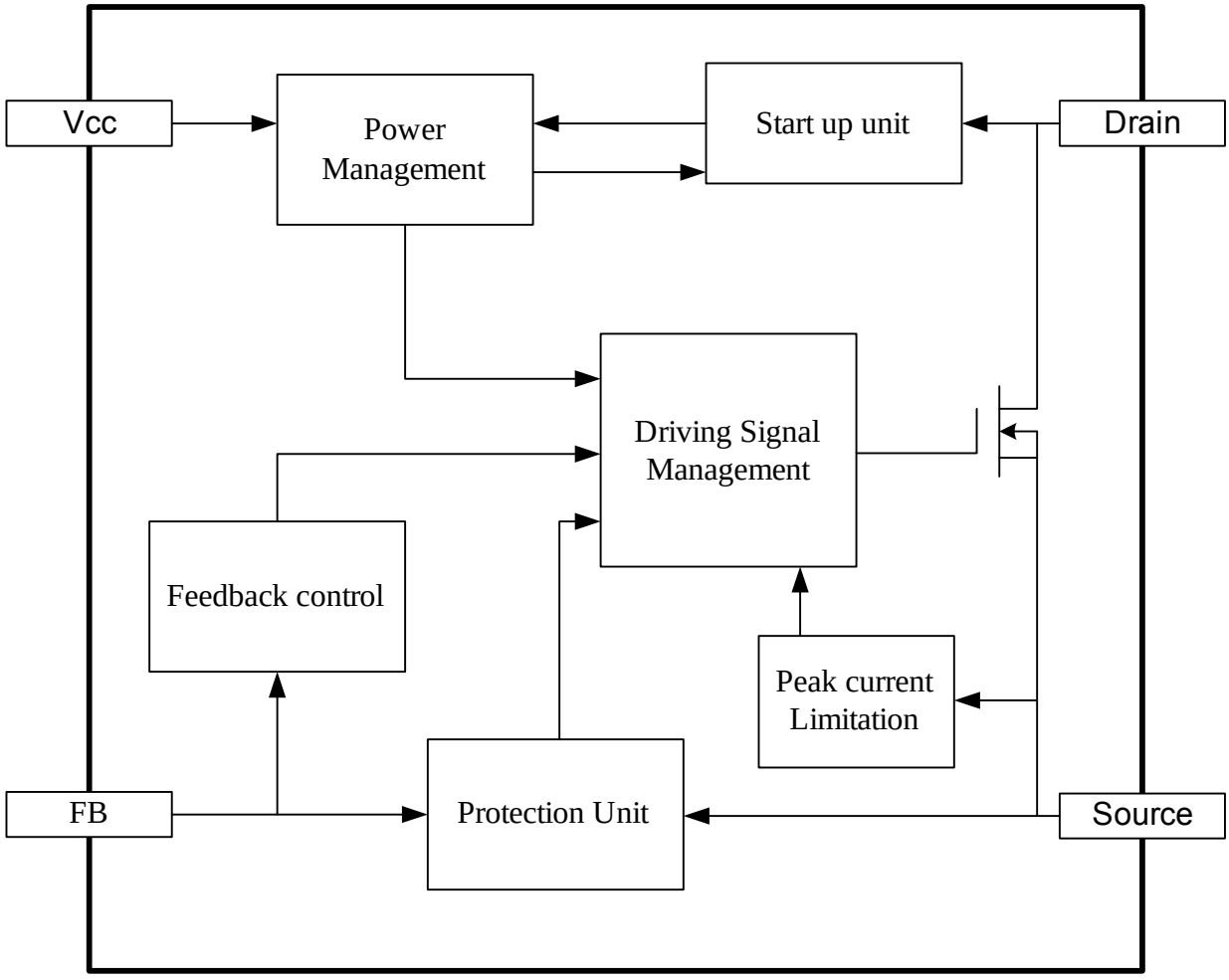


Figure 1: Functional Block Diagram

OPERATION

MP157 is a green mode operation regulator. With the load decreasing, the peak current and the switching frequency will both decreasing with the load. As a result, it still offers excellent efficiency performance at light load, thus better average efficiency is achieved. As shown in the typical application diagram, the regulator is designed to operate with a minimum number of external components. It incorporates the following features as described in the following sections.

Start-up and Under Voltage Lock-out

The internal high voltage regulator self-supplies the IC from the Drain pin. The IC starts switching and the internal high voltage regulator turns off as soon as the voltage on pin VCC reaches VCC_{OFF} (4.6V, typical). the internal high voltage regulator turns on to charge the external Vcc capacitor When the Vcc voltage decreases below VCC_{ON} (4.45V, typical). So a small capacitor such as several uF capacitor is enough to hold on the voltage of Vcc and this can lower the cost by decreasing the value of the capacitor.

When the voltage on Pin Vcc drops blow VCC_{stop} (3.3V, typical), the IC stops working, then the internal high voltage regulator charges the Vcc capacitor again.

When fault conditions happen, such as OLP, SCP, and OTP, the IC stops working and an internal current source, around 16uA, will discharge the Vcc capacitor, before the Vcc drops below VCC_{pro} (2.4V, typical), the internal high voltage regulator will not start to charge the Vcc capacitor again. So when the fault conditions happen, the restart time can be calculated by the following equation,

$$t_{restart} = C_{VCC} \times \frac{V_{CC} - 2.4V}{16uA} + C_{VCC} \times \frac{4.6V - 2.4V}{3.5mA}$$

Figure 2 shows the typical waveform with VCC under voltage lock out.

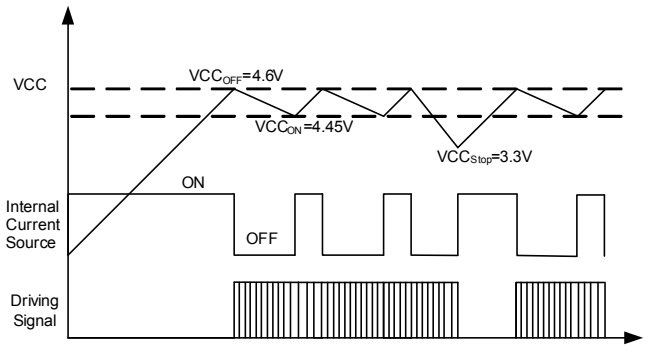


Figure 2: VCC Under-Voltage Lock Out

Constant Voltage Operation

MP157 is a fully integrated regulator when used in the Buck solution, as shown in the typical application on page2.

At the beginning of each cycle, the integrated MOSFET is turned ON when the feedback voltage is below the reference voltage — 2.5V, which indicates insufficient output voltage. The ON period is determined by the peak current limit. After the ON period elapses, the integrated MOSFET is turned OFF. The Freewheeling diode (D1) will not be turned ON until inductor (L1) charges the voltage of the sampling capacitor (C3) to equal the output voltage. The sampling capacitor voltage changes along with the output voltage. The sampling capacitor can sample and hold the output voltage to keep the output voltage regulated. The voltage of the sampling capacitor will decrease when the current of inductor is smaller than the output current. When the feedback voltage falls below the internal reference voltage — 2.5V, another switching cycle begins. The detail operation in CCM is shown as Figure 3.

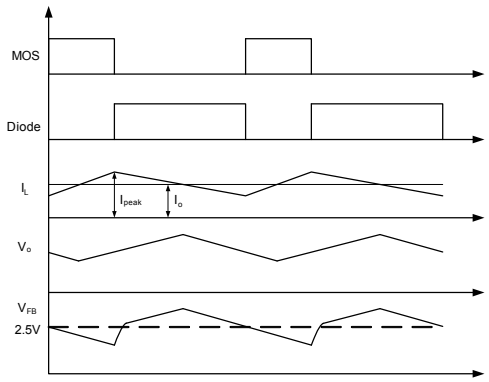


Figure 3: VFB Vs Vout

Thus by monitoring the sampling capacitor, the output voltage can be regulated, and the output voltage is determined by the following equation:

$$Vout = 2.5V \times \frac{R1+R2}{R2}$$

Frequency Foldback

At the light load or no load conditions, the output drops very slowly. This makes the MOSFET OFF time increase. The frequency decreases as the load decreases. So MP157 can maintain a high efficiency under light load condition by reducing the switching frequency automatically.

The switching frequency can be obtained as:

$$f_s = \frac{(V_{in} - V_o)}{2L(I_{peak} - I_o)} \cdot \frac{V_o}{V_{in}}, \text{ For CCM}$$

$$f_s = \frac{2(V_{in} - V_O)}{LI^2_{peak}} \cdot \frac{I_o V_o}{V_{in}}, \text{ for DCM}$$

At the same time, the peak current limit starts to decrease from 640mA as the off-time increases. At standby mode, the frequency and the peak current are both minimum, so smaller dummy load could be added. As a result, peak current compression function helps to save no load consumption. The peak current limit can be calculated by the following equation (T_{off} is the off time of the power module):

$$I_{peak} = 640mA - (3mA/\mu s) \times (T_{off} - 13.1\mu s)$$

Minimum off time limitation

A minimum off time limitation is implemented. During the normal operation, the minimum off time limit is 13.1μs, and during the start up period, the minimum off time limit is shorten gradually from 52.4μs, 26.2μs to 13.1μs (Shown as Figure 4). Each minimum off time retains 128 switching cycle. This soft start function provides safe start-up.

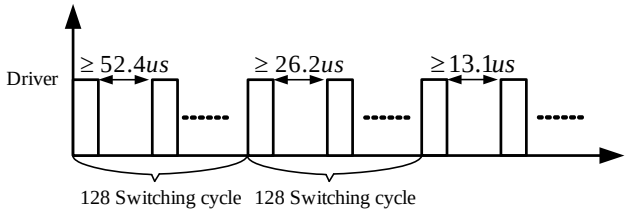


Figure 4: t_{minoff} at start-up

EA Compensation

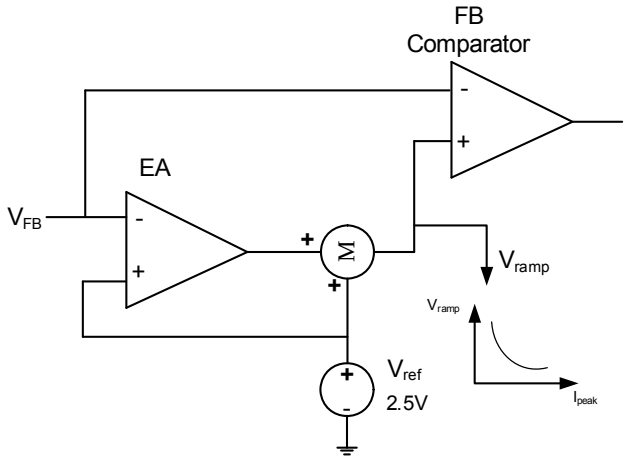


Figure 5: EA and Ramp Compensation

To obtain a better load regulation, MP157 features EA (Error Amplifier) Compensation function (Shown as Figure 5). After 6μs delay of MOSFET turning off, MP157 samples the feedback voltage. So with the EA Compensation, the reference voltage— 2.5V can be regulated with the load. This can make better regulation of power module.

Ramp Compensation

To maintain the precise output voltage, an internal ramp compensation circuit is added --- an exponential voltage sinking source will be added to pull down the reference voltage of the

feedback comparator which is also shown in Figure 5. The ramp compensation is related with the load conditions. At the full load conditions, the compensation is about the 3mV/μs. With the load decreases, the compensation increases exponentially.

Over Load Protection (OLP)

As the load increases, the peak current and the switching frequency both increase. When switching frequency and peak current reaches the maximum, output voltage decreases if the load continues to increase. So FB voltage drops below OLP point.

By continuously monitoring the FB voltage, when FB voltage drops below 1.7V which is considered as an error flag, the timer starts counting. If the error flag removes, the timer resets. If the timer reaches its completion when it has counted to 150ms (Fs=37kHz), OLP takes place. This timer duration avoids triggering OLP function when the power supply is at start up or load transition phase. So power supply should start up in less than 150ms (Fs=37kHz). Different switching frequency (fs) leads to different over load protection delay time, as shown following equation:

$$T_{Dealy} \approx 150ms \times \frac{37kHz}{fs}$$

Short Circuit Protection (SCP)

The MP157 monitors the peak current, and shuts down when the peak current rises above 900mA, featuring a short circuit protection. As soon as the fault disappears, the power supply resumes operation.

Thermal shutdown (TSD)

To prevent from any lethal thermal damage, MP157 shuts down switching cycle when the inner temperature exceeds 150°C. During the thermal shutdown (TSD), the VCC will be discharged to 2.4V, and then be re-charged by the internal high voltage regulator.

Open Loop Detection

If the FB voltage is lower than 60mV, IC will stop working and a re-start cycle will begin. During the start up, the open loop detection is blanked for 128 switching cycles.

Leading Edge Blanking

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading edge blanking (LEB) unit is employed between the current sense resistor inside the IC and the current comparator input. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure 6 shows the leading edge blanking.

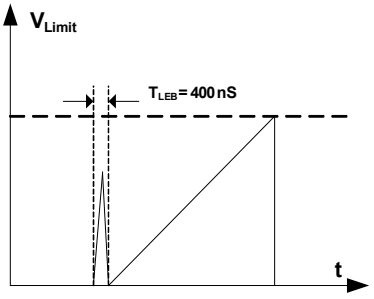
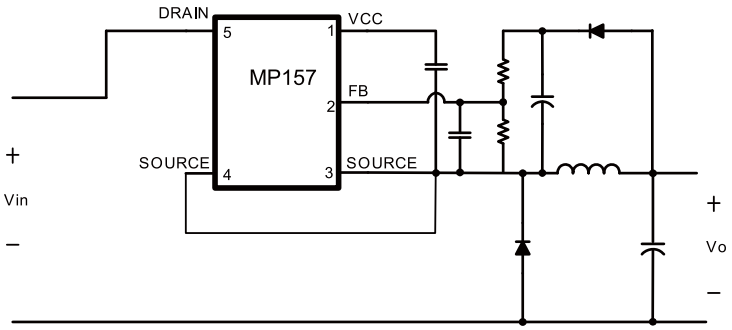
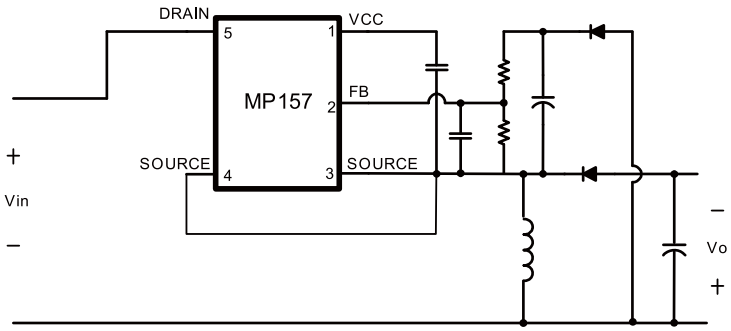
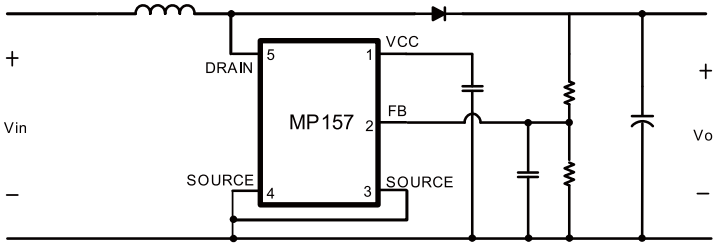
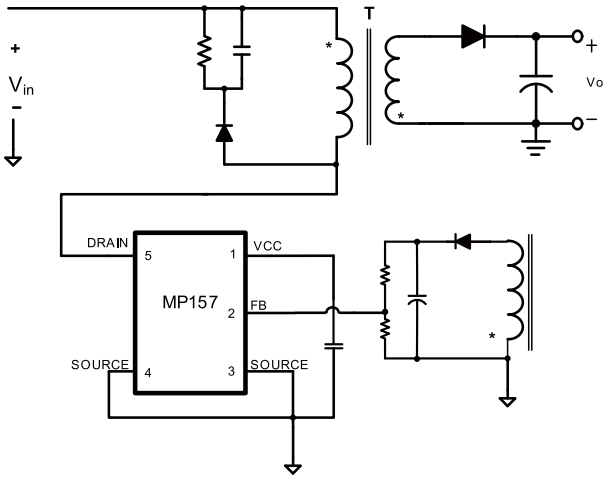


Figure 6: Leading Edge Blanking

APPLICATION INFORMATION

Table 1. Common Topologies Using MP157

Topology	Circuit Schematic	Features
High-Side Buck		1. No-isolation, 2. Positive output 3. Low cost 4. Direct feedback
High-Side Buck-Boost		1. No-isolation, 2. Negative output 3. Low cost 4. Direct feedback
Boost		1. No-isolation, 2. Positive output 3. Low cost 4. Direct feedback
Flyback		1. Isolation, 2. Positive output 3. Low cost 4. Indirect feedback

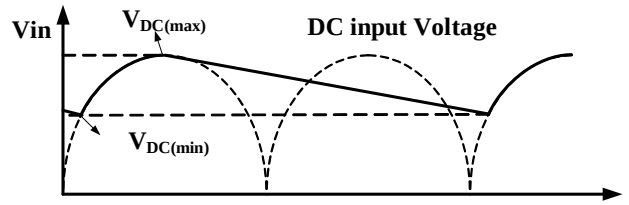
Topology Options

MP157 can be used in common topologies, such as Buck, Buck-Boost, Boost and Flyback. Please find the Table.1 for more information.

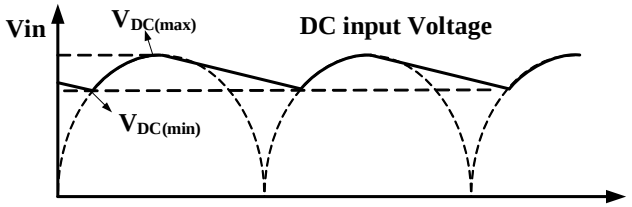
COMPONENT SELECTION

Input Capacitor

The input capacitor is used to supply the DC input voltage for the converter. Figure 7 shows the typical DC bus voltage waveform with half-wave rectifier and full-wave rectifier.



a) DC input with half-wave rectifier



b) DC input with full-wave rectifier

Figure 7: Input voltage waveform

When the half-wave rectifier is used, the input capacitor is usually set as 3uF/W for the universal input condition. And when the full-wave rectifier is used, we could choose a smaller capacitor usually set as 1.5-2uF/W. Avoid the minimum DC voltage below 70V. Low DC input voltage will bring the problem of thermal shutdown. Half-wave rectifier is recommended for <2W output application and full-wave rectifier is recommended for >2W output application.

Inductor

MP157 has a minimum off time limit, and this decides the maximum power it can output. The maximum power increases as the inductor increases. Using a smaller inductor may fail output the full load. The maximum power can be obtained as:

$$P_{omax} = V_o(I_{peak} - \frac{V_o t_{minoff}}{2L}), \text{ For CCM}$$

$$P_{omax} = \frac{1}{2} L I_{peak}^2 \cdot \frac{1}{\tau_{minoff}}, \text{ for DCM}$$

To consider the parameter error of the converter such as peak current limit, minimum off time and so on, we can obtain the minimum value Pmin of the maximum power. The principle of choosing the inductor is that Pmin should be higher than the rated power.

Take the output voltage 12V as examples, the curve of Pmin for 12V is shown as Figure 8, (Ipeak=0.64A, tminoff=13.1μs)

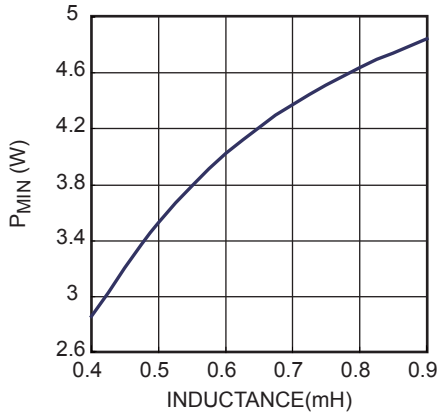


Figure 8: Pmin vs. L at 12V output

For CCM operation, the selection of L should make the frequency of converter lower than 40kHz to reduce the turn-on switching loss cause by reverse recovery of free-wheeling diode at high line input.

Freewheeling Diode

The diode should have a maximum reverse voltage rating which is greater than the maximum input voltage, and the current rating of the diode is determined by the output current.

The reverse recovery of freewheeling diode can affect the efficiency and the circuit operation. For CCM operation. ultra fast diode with Trr<35ns is used such as STTH2R06, STTH1R06, and UGC10JH. For DCM operation, diode with Trr<75ns is used.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated by:

$$V_{CCM\_ripple} = \frac{\Delta i}{8 f_s C_o} + \Delta i \cdot R_{ESR}, \text{ for CCM}$$

$$V_{DCM\_ripple} = \frac{I_o}{f_s C_o} \cdot \left(\frac{I_{pk} - I_o}{I_{pk}} \right)^2 + I_{pk} \cdot R_{ESR}, \text{ for DCM}$$

Ceramic, tantalum or low ESR electrolytic capacitors are used to reduce the output voltage ripple.

Feedback Resistors

The resistor divider determines the output voltage. Choose appropriate values for R1 and R2 to maintain V_{FB} at 2.5V. Avoid large R2 value (typically 4kΩ to 10kΩ).

Feedback Capacitor

The feedback capacitor provides a sample and hold function. Small capacitors result in poor regulation at light loads, and large capacitors affect the circuit operation. Roughly estimate an optimal capacitor value using the following equation:

$$\frac{1}{2} \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \le C_{FB} \le \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o}$$

Choose the nearest appropriate value.

Dummy Load

A dummy load is required to maintain the load regulation. This ensures sufficient inductor energy to charge the sample and hold capacitor to detect the output voltage. Normally a 3mA dummy load is needed and can be adjusted to the regulated voltage. Increasing the dummy load reduces the efficiency and no-load consumption. Use a zener diode if no-load regulation is not a concern.

Auxiliary V_{CC} Supply

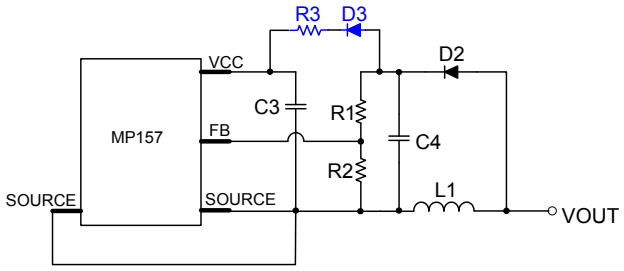


Figure 9: Auxiliary V_{CC} Supply Circuit

If output voltage is higher than the voltage of Vcc, an auxiliary Vcc supply by connecting a diode (D3) and a resistor (R3) between C3 and C4 can be implemented to reduce overall power consumption. Then the voltage of Vcc can be clamped to 5V, and the internal regulator will be turned off all the times. For values above V_O=7V, determine R3 as per the formula below.

$$R \approx \frac{V_o - 5V}{165\mu A}$$

Surge Performance

Select an appropriate input capacitor value to obtain a good surge performance. With the input capacitors C4 (10μF) and C5 (10μF), the board can pass 1000V surge test. Table 2 shows the capacitance required under normal condition for different surge voltage.

Table 2: Recommended Capacitance

Surge voltage	500V	1000V	2000V
C4	3.3μF	10μF	Shown in Figure 9
C5	3.3μF	10μF	

The board can pass 2kV surge test by using the circuit below.

1) Change the fuse resistor F1 (10ohm/1W) to SS-5-2A
2) Add a MOV RV1 (TVR14431)
3) Add a resistor R8 (39Ω)

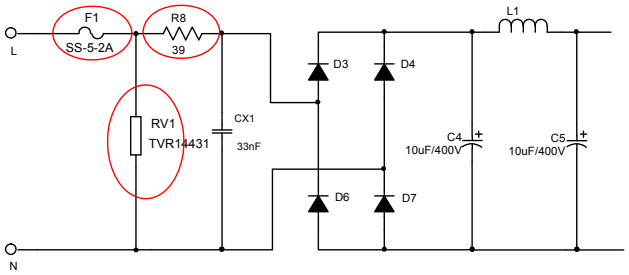
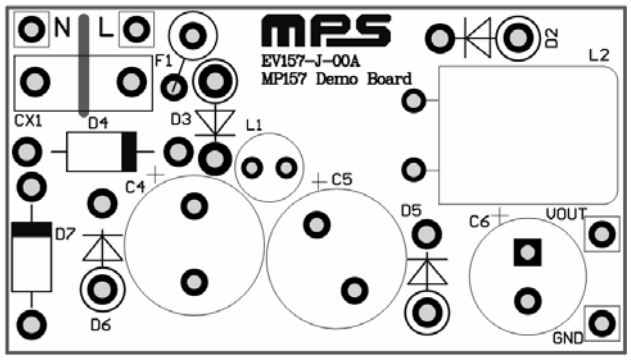


Figure 10: Solution to Pass 2kV Surge Test

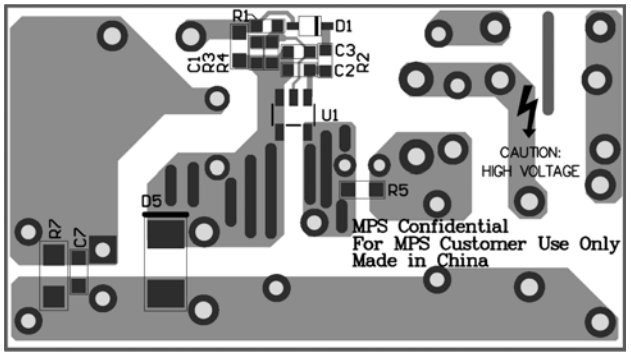
Layout Guide

PCB layout is very important for reliable operation, good EMI and thermal performance. Please follow these guidelines to optimize performance.

1) Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.
2) Place the power inductor far away from the input filter.
3) Place a capacitor valued at several nF between the FB pin and SOURCE as close to the IC as possible.
4) Connect the exposed pad with the DRAIN pin to a larger copper area to improve thermal performance.



a) Top layer



b) Bottom layer

Figure 11: PCB layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 3: Design Example

V_{IN}	85VAC to 265VAC
V_{OUT}	12V
I_{OUT}	350mA

The detailed application schematic is shown in Figure 12. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets -- EV157-J-00A_r1.0 or EV157-S-00A_r1.0.

TYPICAL APPLICATION CIRCUITS

Figure 12 shows a typical application example of a 12V, 350mA non-isolated power supply using MP157.

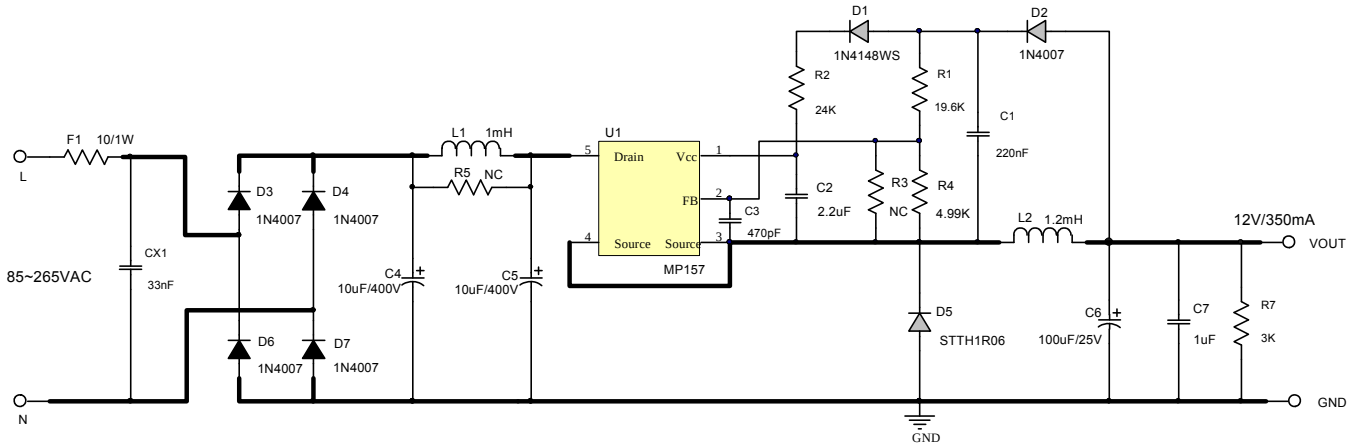
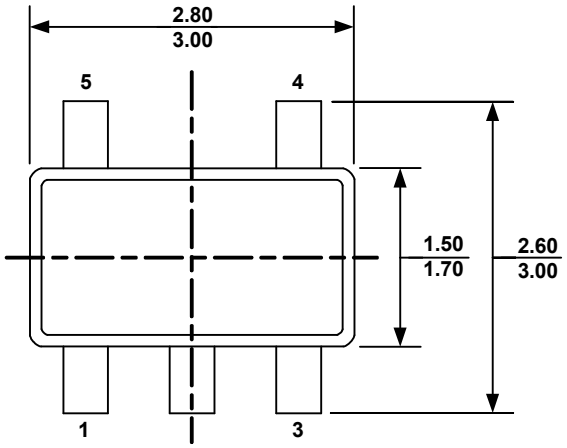


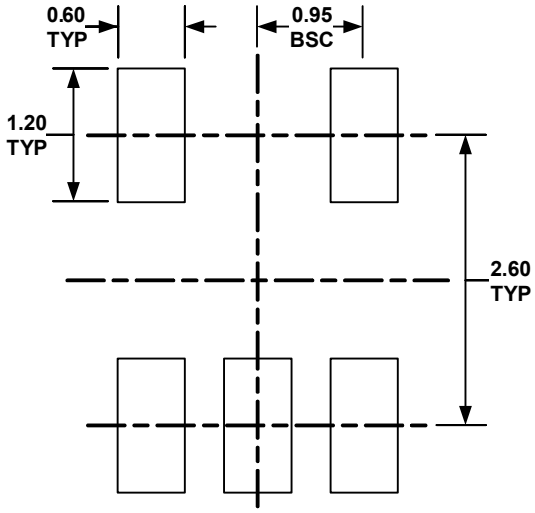
Figure 12: Typical Application at 12V, 350mA

PACKAGE INFORMATION

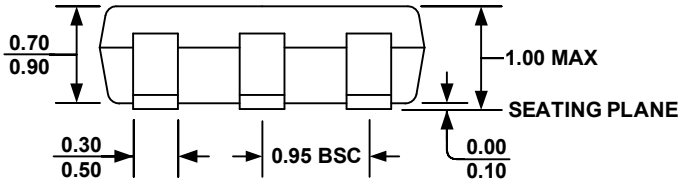
TSOT23-5



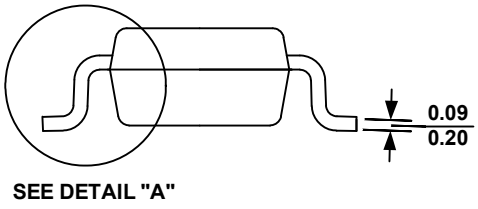
TOP VIEW



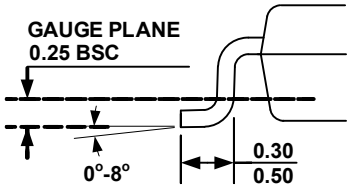
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



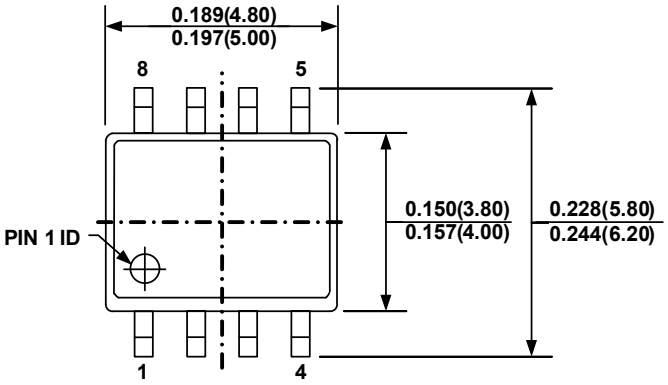
DETAIL "A"

NOTE:

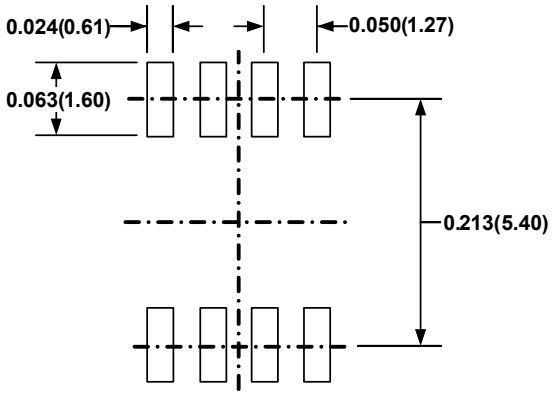
1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA
6) DRAWING IS NOT TO SCALE

PACKAGE INFORMATION

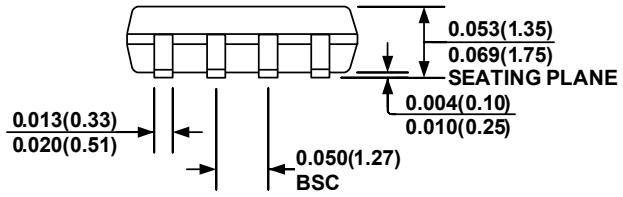
SOIC-8



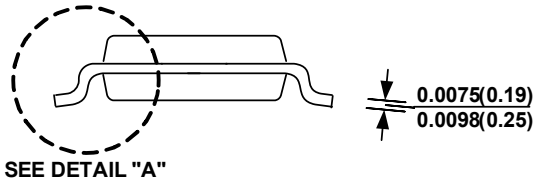
TOP VIEW



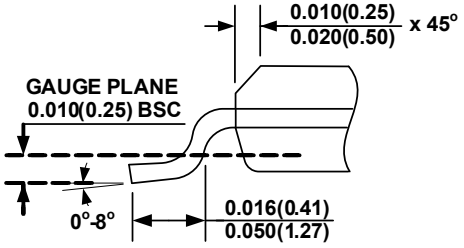
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE