

MOSFET - Power, Single, N-Channel

80 V, 21.1 mΩ, 33 A

NVTFS6H860N

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVTFS6H860NWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	80	V
Gate-to-Source Voltage	V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Notes 1, 2, 3, 4)	I _D	T _C = 25°C	30
		T _C = 100°C	21
Power Dissipation R _{θJC} (Notes 1, 2, 3)	P _D	T _C = 25°C	46
		T _C = 100°C	23
Continuous Drain Current R _{θJA} (Notes 1, 3, 4)	I _D	T _A = 25°C	8.0
		T _A = 100°C	5.5
Power Dissipation R _{θJA} (Notes 1, 3)	P _D	T _A = 25°C	3.1
		T _A = 100°C	1.6
Pulsed Drain Current	I _{DM}	119	A
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)	I _S	38	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 1.5 A)	E _{AS}	138	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C

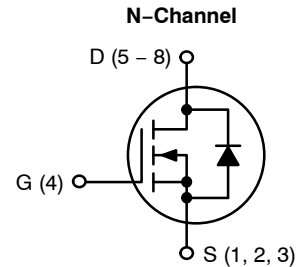
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 3)	R _{θJC}	3.3	°C/W
Junction-to-Ambient – Steady State (Note 3)	R _{θJA}	48.2	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
80 V	21.1 mΩ @ 10 V	33 A

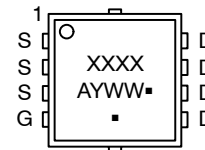


WDFN8 3.3x3.3, 0.65P
CASE 511AB



WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF)
CASE 515AN

MARKING DIAGRAM



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVTFS6H860N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V		T _J = 25°C		10
				T _J = 125°C		250
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 30 μA	2.0		4.0	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		17.3	21.1	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 10 A		41		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 40 V		510		pF
Output Capacitance	C _{oss}			78		
Reverse Transfer Capacitance	C _{rss}			4.2		
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 40 V, I _D = 10 A		1.8		nC
Gate-to-Source Charge	Q _{GS}			2.8		
Gate-to-Drain Charge	Q _{GD}			1.6		
Total Gate Charge	Q _{G(TOT)}			8.7		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 6.0 V, V _{DS} = 64 V, I _D = 10 A		8.0		ns
Rise Time	t _r			14		
Turn-Off Delay Time	t _{d(off)}			18		
Fall Time	t _f			5.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 5 A		T _J = 25°C	0.8	1.2	V
				T _J = 125°C	0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 10 A		29		ns	
Charge Time	t _a			20			
Discharge Time	t _b			9.0			
Reverse Recovery Charge	Q _{RR}			24			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

NVTF56H860N

TYPICAL CHARACTERISTICS

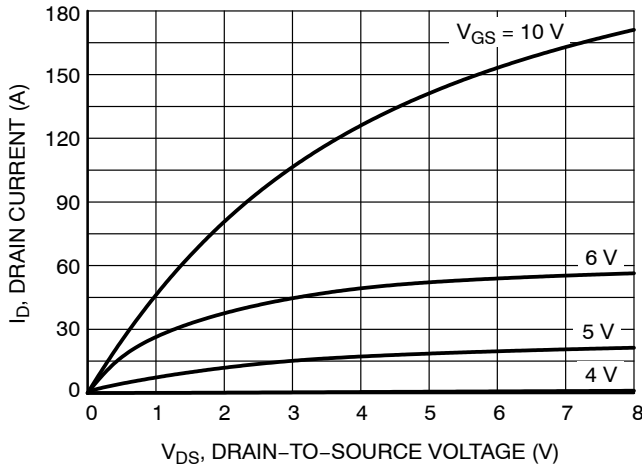


Figure 1. On-Region Characteristics

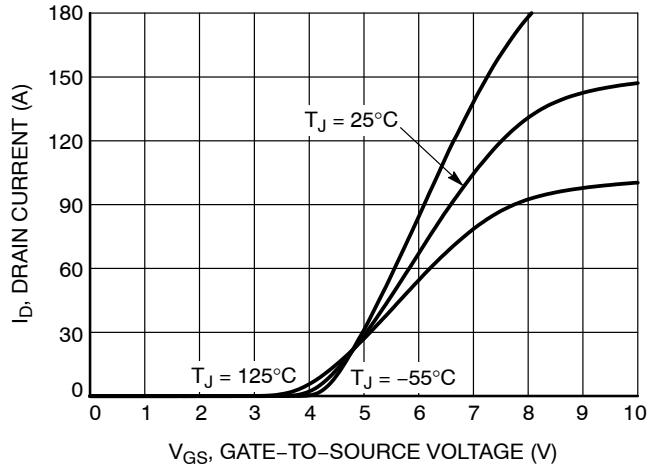


Figure 2. Transfer Characteristics

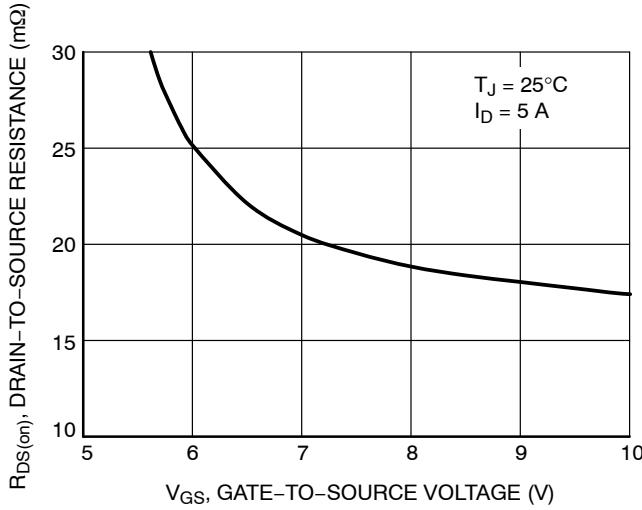


Figure 3. On-Resistance vs. Gate-to-Source Voltage

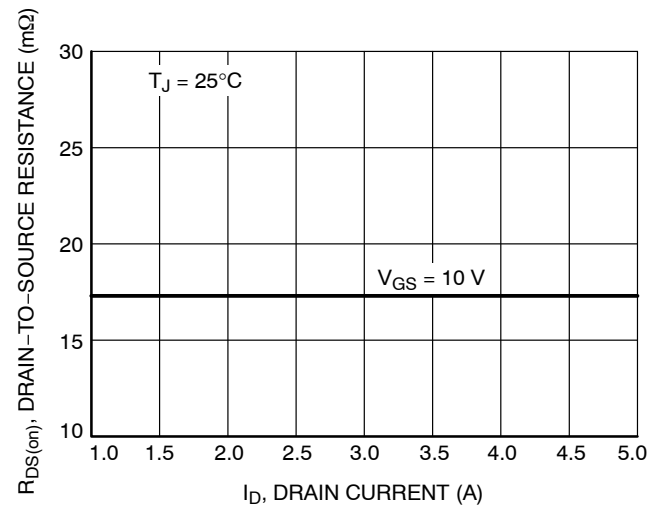


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

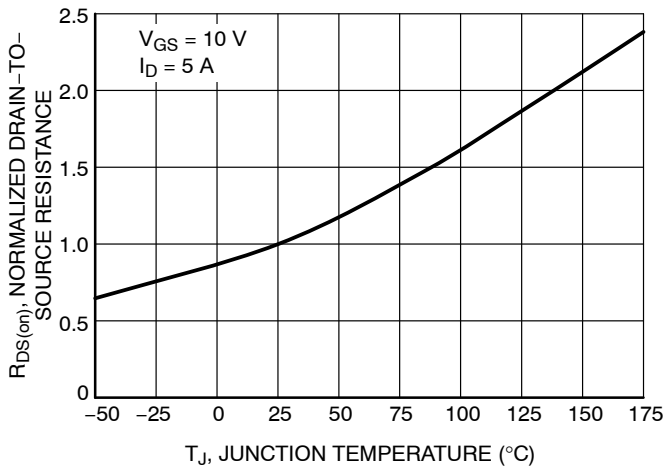


Figure 5. On-Resistance Variation with Temperature

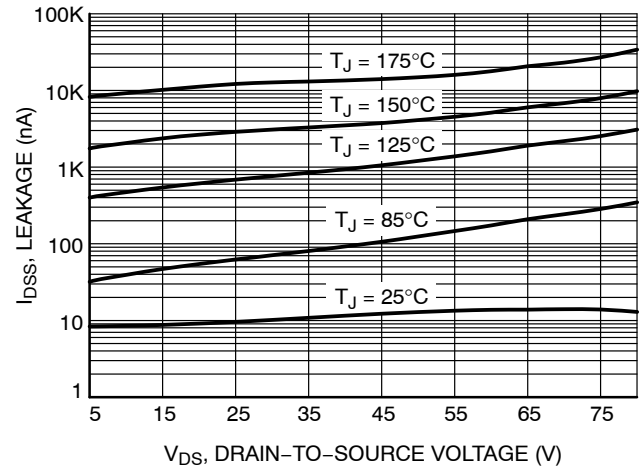


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVTFS6H860N

TYPICAL CHARACTERISTICS

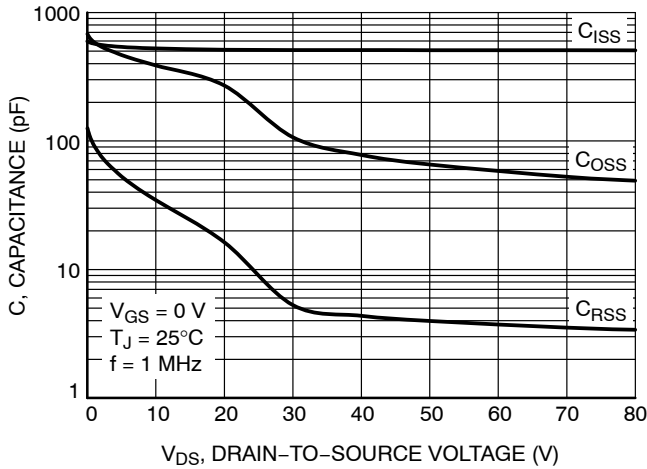


Figure 7. Capacitance Variation

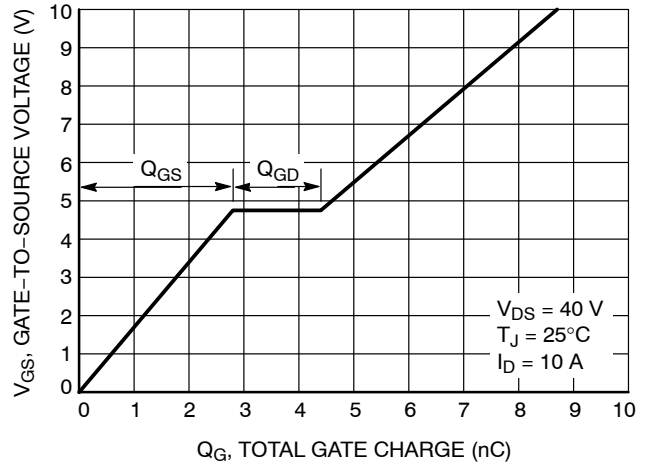


Figure 8. Gate-to-Source Voltage vs. Total Charge

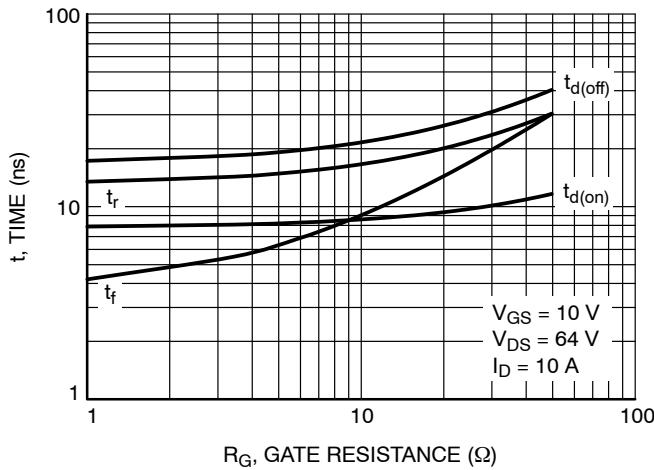


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

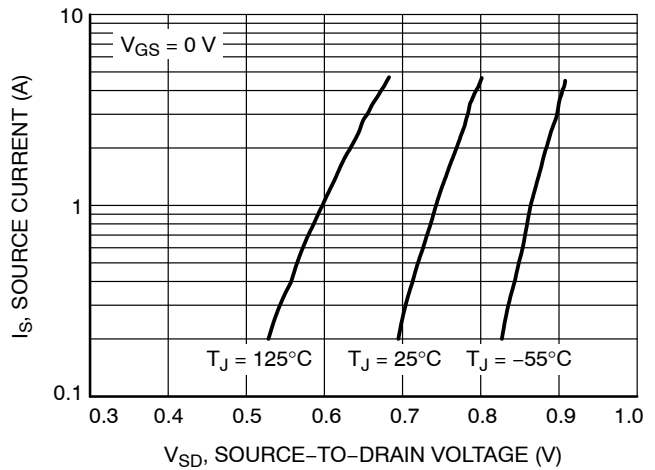


Figure 10. Diode Forward Voltage vs. Current

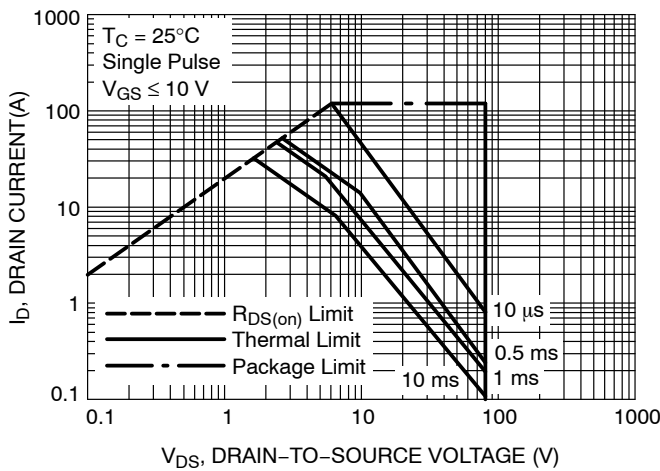


Figure 11. Maximum Rated Forward Biased Safe Operating Area

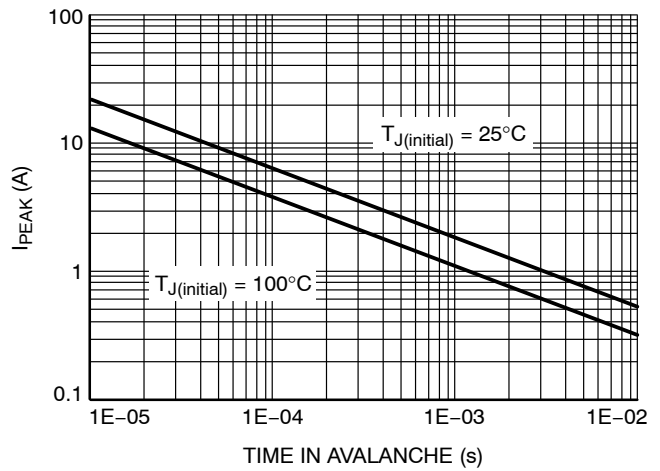


Figure 12. IPEAK vs. Time in Avalanche

NVTFS6H860N

TYPICAL CHARACTERISTICS

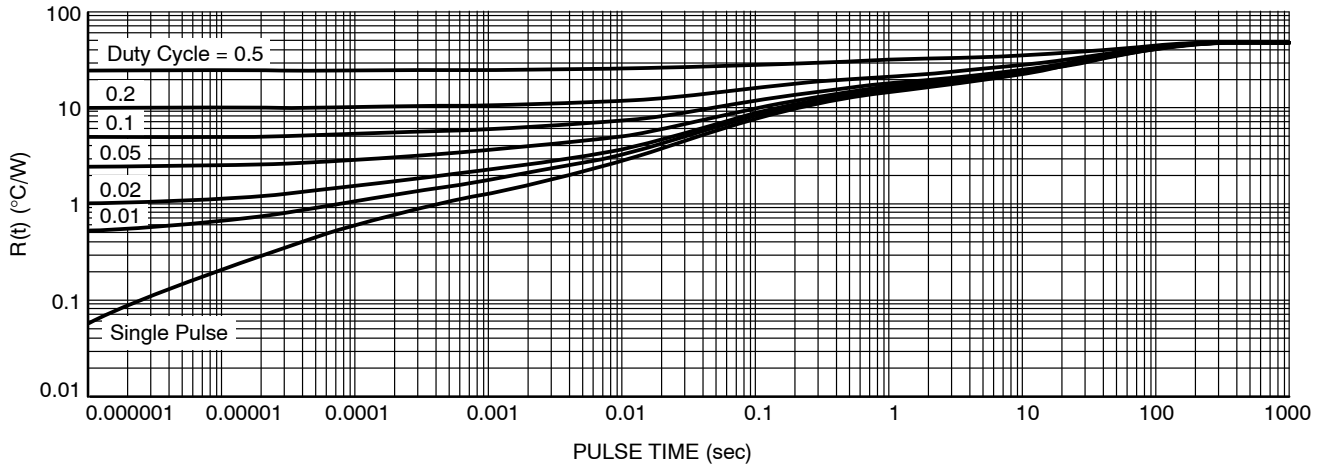


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVTFS6H860NTAG	860N	WDFN8 3.3x3.3, 0.65P (Pb-Free)	1500 / Tape & Reel
NVTFS6H860NWFTAG	60NW	WDFNW8 3.3x3.3, 0.65P (Full-Cut μ 8FL WF) (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°



GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

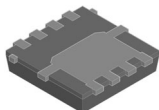
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MECHANICAL CASE OUTLINE

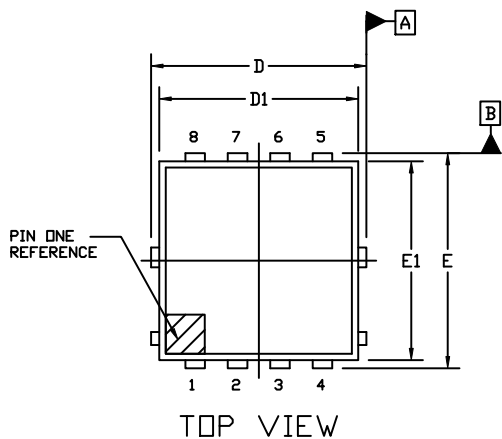
PACKAGE DIMENSIONS

ON Semiconductor®



WDFNW8 3.3x3.3, 0.65P (Full-Cut μ 8FL WF) CASE 515AN ISSUE O

DATE 25 AUG 2020



TOP VIEW

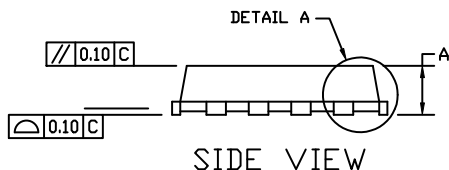


DETAIL A

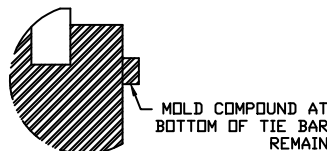
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



SIDE VIEW



DETAIL B



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

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