24 GHz to 44 GHz, Wideband, Microwave Downconverter

Data Sheet

ADMV1014

FEATURES

Wideband RF input frequency range: 24 GHz to 44 GHz
2 downconversion modes
   Direct conversion from RF to baseband I/Q
   Image rejecting downconversion to complex IF
LO input frequency range: 5.4 GHz to 10.25 GHz
LO quadrupler for up to 41 GHz
Matched 50 Ω, single-ended RF input, and complex IF outputs
Option between matched 100 Ω balanced or 50 Ω single-
   ended LO inputs
100 Ω balanced baseband I/Q output impedance with
   adjustable output common-mode voltage level
Image rejection optimization
Square law power detector for setting mixer input power
Variable attenuator for receiver power control
Programmable via a 4-wire SPI interface
32-terminal, 5 mm × 5 mm LGA package

APPLICATIONS

Point to point microwave radios
Radar, electronic warfare systems
Instrumentation, automatic test equipment (ATE)
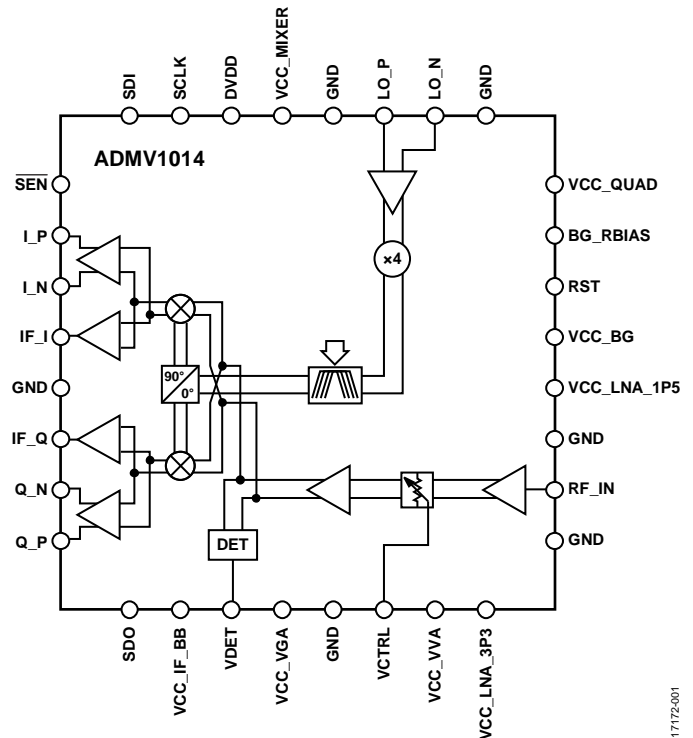
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The ADMV1014 is a silicon germanium (SiGe), wideband, microwave downconverter optimized for point to point microwave radio designs operating in the 24 GHz to 44 GHz frequency range.

The downconverter offers two modes of frequency translation. The device is capable of direct quadrature demodulation to baseband inphase (I)/quadrature (Q) output signals, as well as image rejection downconversion to a complex intermediate frequency (IF) output carrier frequency. The baseband outputs can be dc-coupled, or, more typically, the I/Q outputs are ac-coupled with a sufficiently low high-pass corner frequency to ensure adequate demodulation accuracy. The serial port interface (SPI) allows fine adjustment of the quadrature phase to allow the user to optimize I/Q demodulation performance. Alternatively, the baseband I/Q outputs can be disabled, and the I/Q signals can be passed through an on-chip active balun to

provide two single-ended complex IF outputs anywhere between 800 MHz and 6000 MHz. When used as an image rejecting downconverter, the unwanted image term is typically suppressed to better than 30 dBc below the wanted sideband. The ADMV1014 offers a flexible local oscillator (LO) system, including a frequency quadruple option allowing up to a 41 GHz range of LO input frequencies to cover a radio frequency (RF) input range as wide as 24 GHz to 44 GHz. A square law power detector is provided to allow monitoring of the power levels at the mixer inputs. The detector output provides closed-loop control of the RF input variable attenuator through an external op amp error integrator circuit option.

The ADMV1014 downconverter comes in a compact, thermally enhanced, 5 mm × 5 mm LGA package. The ADMV1014 operates over the −40°C to +85°C case temperature range.

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REVISION HISTORY

SPECIFICATIONS

RF amplitude = −30 dBm, measurements performed with a 0 mV dc bias. VCC_MIXER = VCC_QUAD = VCC_BG = VCC_LNA = VCC_VGA = VCC_IF_BB = 3.3 V, DVDD = VCC_VVA = 1.8 V, Register 0x0B set to 0x727C, Register 0x03, Bits[12:13] set to 11, and ambient temperature (T_A) = 25°C, unless otherwise noted.

Measurements are in IF mode, performed with a 90° hybrid, Register 0x03, Bit 11 = 0, and Register 0x03, Bit 8 = 1, unless otherwise noted.

Measurements in I/Q mode are measured as a composite of the I and Q channel performance, common-mode voltage (V_{CM}) = 1.15 V, Register 0x03, Bit 11 = 1, and Register 0x03, Bit 8 = 0, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGES					
RF Input		24		44	GHz
LO Input		5.4		10.25	GHz
LO Quadrupler		21.6		41	GHz
IF Output		0.8		6.0	GHz
Baseband (BB) I/Q Output		DC		6.0	GHz
LO AMPLITUDE RANGE		−6	0	+6	dBm
I/Q DEMODULATOR PERFORMANCE					
Conversion Gain	At maximum gain				
24 GHz to 42 GHz		12.5	17		dB
42 GHz to 44 GHz		12.5	17		dB
Voltage Variable Attenuator (VVA) Control Range			19		dB
Single Sideband (SSB) Noise Figure	At maximum gain				
24 GHz to 42 GHz			5.5	8	dB
42 GHz to 44 GHz			6	8.5	dB
Input Third-Order Intercept (IP3)	At maximum gain				
24 GHz to 42 GHz			0		dBm
42 GHz to 44 GHz			−1		dBm
Input Second-Order Intercept (IP2)	24 GHz to 44 GHz, at maximum gain		45		dBm
Input 1 dB Compression Point (P1dB)	At maximum gain				
24 GHz to 42 GHz		−14	−10		dBm
42 GHz to 44 GHz		−15	−11		dBm
Amplitude Balance			±0.5		dB
Phase Balance	DC < baseband frequency (f_{BB}) < 2 GHz		1		Degrees
	2 GHz < f_{BB} < 4 GHz		2		Degrees
	4 GHz < f_{BB} < 6 GHz		4		Degrees
Image Rejection	24 GHz to 44 GHz, at maximum gain				
Uncalibrated			45		dBc
Calibrated			52		dBc
IF DOWNCONVERTER PERFORMANCE					
Conversion Gain	At maximum gain				
24 GHz to 42 GHz		12.5	17		dB
42 GHz to 44 GHz		11.5	16		dB
VVA Control Range			19		dB
SSB Noise Figure	At maximum gain				
24 GHz to 42 GHz			5.5	8	dB
42 GHz to 44 GHz			6	8.5	dB
Input IP3	At maximum gain				
24 GHz to 42 GHz			0		dBm
42 GHz to 44 GHz			0.5		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input P1dB	At maximum gain				
24 GHz to 42 GHz		−14	−9		dBm
42 GHz to 44 GHz		−15	−10		dBm
Amplitude Balance			−0.5		dB
Phase Balance	800 MHz < IF frequency (f_{IF}) < 2 GHz		0.5		Degrees
	2 GHz < f_{IF} < 4 GHz		1		Degrees
	4 GHz < f_{IF} < 6 GHz		2.5		Degrees
Image Rejection					
Uncalibrated			30		dBc
Calibrated			35		dBc
RECEIVER (Rx) POWER DETECTOR PERFORMANCE					
Input Level	±1 dB dynamic range				
Minimum			−35		dBm
Maximum			−14		dBm
±1 dB Dynamic Range			20		dB
Output Voltage					
Maximum DC Output			3.3		V
RETURN LOSS					
RF Input	50 Ω single-ended		−13		dB
LO Input	100 Ω differential		−10		dB
IF Output	50 Ω single-ended		−12		dB
BB Output	100 Ω differential		−15		dB
BB I/Q Output Impedance			100		Ω
LEAKAGE	At maximum gain				
Fundamental LO to RF			−70		dBm
4 × LO to RF			−70		dBm
Fundamental LO to IF			−60		dBm
Fundamental LO to I/Q			−60		dBm
LOGIC INPUTS					
Input Voltage Range					
High, V_{INH}		DVDD − 0.4		1.8	V
Low, V_{INL}		0		0.4	V
Input Current, I_{INH}/I_{INL}			100		µA
Input Capacitance, C_{IN}			3		pF
LOGIC OUTPUTS					
Output Voltage Range					
High, V_{OH}		DVDD − 0.4		1.8	V
Low, V_{OL}		0		0.4	V
Output High Current, I_{OH}				500	µA
POWER INTERFACE					
VCC_IF_BB, VCC_VGA, VCC_LNA_3P3, VCC_MIXER, VCC_BG, VCC_QUAD		3.15	3.3	3.45	V
3.3 V Supply Current			437		mA
DVDD, VCC_VVA		1.7	1.8	1.9	V
1.8 V Supply Current			4.2		mA
VCC_LNA_1P5		1.43	1.5	1.57	V
1.5 V Supply Current			33		mA
Total Power Consumption			1.5		W
Power-Down			96	125	mW

SERIAL PORT REGISTER TIMING

Table 2.

| Parameter	Description	Min	Typ	Max	Unit
$t_{SDI, SETUP}$	Data to clock setup time	10			ns
$t_{SDI, HOLD}$	Data to clock hold time	10			ns
$t_{SCLK, HIGH}$	Clock high duration	40 to 60			%
$t_{SCLK, LOW}$	Clock low duration	40 to 60			%
$t_{SCLK, \overline{SEN}\_SETUP}$	Clock to $\overline{SEN}$ setup time	30			ns
$t_{SCLK, DOT}$	Clock to data out transition time			10	ns
$t_{SCLK, DOV}$	Clock to data out valid time			10	ns
$t_{SCLK, \overline{SEN}\_INACTIVE}$	Clock to $\overline{SEN}$ inactive	20			ns
$t_{\overline{SEN}\_INACTIVE}$	Inactive $\overline{SEN}$ (between two operations)	80			ns

Timing Diagram
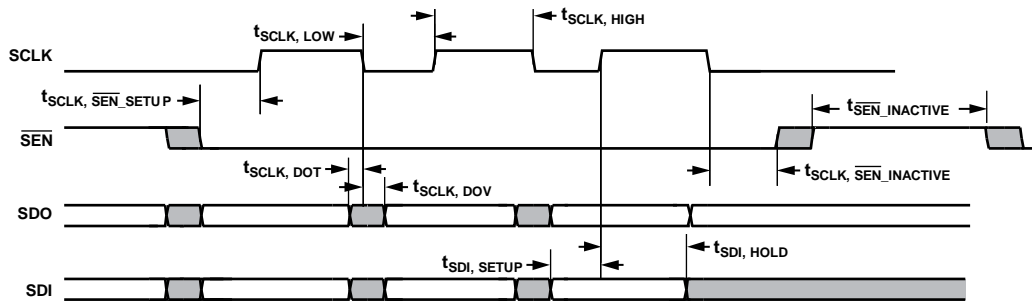
Figure 2. Serial Port Register Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	
VCC_IF_BB, VCC_VGA, VCC_LNA_3P3, VCC_MIXER, VCC_BG, VCC_QUAD, DVDD	4.3 V
VCC_VVA, VCC_LNA_1P5	2.3 V
RF Input Power	0 dBm
LO Input Power	9 dBm
Maximum Junction Temperature	125°C
Maximum Power Dissipation[1]	2.17 W
Lifetime at Maximum Junction Temperature (T_J)	1×10^6 hours
Operating Case Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering 60 sec)	260°C
Moisture Sensitivity Level (MSL) Rating[2]	MSL3
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	3000 V
Field Induced Charged Device Model (FICDM)	750 V

[1] The maximum power dissipation is a theoretical number calculated by $(T_J - 85°C)/\theta_{JC\_TOP}$.
[2] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Only use θ_{JA} and θ_{JC} to compare the thermal performance of different packages when all test conditions listed are similar to JEDEC specifications. Otherwise, use Ψ_{JT} and Ψ_{JB} to calculate the device junction temperature using the following equations:

$$T_J = (P \times \Psi_{JT}) + T_{TOP} \tag{1}$$

where:
T_{TOP} is package top temperature (°C). T_{TOP} is measured at the top center of the package.
Ψ_{JT} is the junction to top thermal characterization number.
P is the total power dissipation in the chip (W).

$$T_J = (P \times \Psi_{JB}) + T_{BOARD} \tag{2}$$

where:
T_{BOARD} is the board temperature measured on the midpoint of the longest side of the package no more than 1 mm from the edge of the package body (°C).
Ψ_{JB} is the junction to board thermal characterization number.
P is the total power dissipation in the chip (W).

As stated in JEDEC51-12, only use Equation 1 and Equation 2 when no heat sink or heat spreader is present. When a heat sink or heat spreader is added, use θ_{JC_TOP} to estimate or calculate the junction temperature.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC_TOP}[3]	θ_{JB}[4]	Ψ_{JT}[5]	Ψ_{JB}[6]	Unit
CC-32-6	33.6	18.4	13.3	4.9	12.6	°C/W

[1] The thermal resistance values specified in Table 4 are simulated based on JEDEC specifications, unless specified otherwise, and must be used in compliance with JESD51-12.
[2] θ_{JA} is the junction to ambient thermal resistance in a natural convection, JEDEC environment.
[3] θ_{JC_TOP} is the junction to case (top) JEDEC thermal resistance.
[4] θ_{JB} is the junction to board JEDEC thermal resistance.
[5] Ψ_{JT} is the junction to top JEDEC thermal characterization parameter.
[6] Ψ_{JB} is the junction to board JEDEC thermal characterization parameter

ESD CAUTION

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
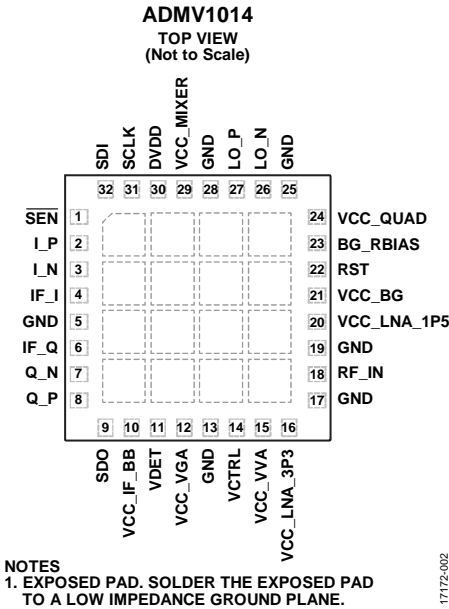
Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SEN	SPI Serial Enable. SEN is a high impedance pin with a logic of 1.8 V.
2, 3	I_P, I_N	Negative (I_N) and Positive (I_P) Differential BB I Outputs. These pins are dc-coupled.
4, 6	IF_I, IF_Q	IF I and IF Q Single-Ended Complex Quadrature Outputs. These pins are dc-coupled to GND, and each pin is matched to 50 Ω.
5, 13, 17, 19, 25, 28	GND	Ground.
7, 8	Q_N, Q_P	Positive (Q_P) and Negative (Q_N) Differential Baseband Q Outputs. These pins are dc-coupled.
9	SDO	SPI Serial Data Output.
10	VCC_IF_BB	3.3 V Power Supply for BB and IF Section. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
11	VDET	Square Law Detector Output Voltage.
12	VCC_VGA	3.3 V Power Supply for RF Amplifier. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
14	VCTRL	RF VVA Control Voltage. The voltage on this pin ranges from 1.8 V (minimum gain) to 0 V (maximum gain). Refer to the ADMV1014-EVALZ user guide for the external component requirements.
15	VCC_VVA	1.8 V Power Supply for VVA Control Circuit. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
16	VCC_LNA_3P3	3.3 V Power Supply for LNA. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
18	RF_IN	RF Input. This pin is dc-coupled internally with a choke to GND, and matched to 50 Ω, single-ended. A dc input above 0 V requires external ac coupling.
20	VCC_LNA_1P5	1.5 V Power Supply for Low Noise Amplifier (LNA). Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
21	VCC_BG	3.3 V Power Supply for Band Gap Circuit. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
22	RST	SPI Reset. Connect this pin to logic high for normal operation.
23	BG_RBIAS	Bang Gap Circuit External High Precision Resistor. Place a 1.1 kΩ, high precision resistor shunt to ground close to this pin.
24	VCC_QUAD	3.3 V Power Supply for Quadruple. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.

Pin No.	Mnemonic	Description
26, 27	LO_N, LO_P	Negative (LO_N) and Positive (LO_P) Differential Local Oscillator Input. These pins are dc-coupled internally with a choke to GND and matched to 100 Ω differential or 50 Ω single-ended. A dc input above 0 V requires external ac coupling. When using the LO input as single-ended, terminate the unused LO port with a 50 Ω impedance to ground.
29	VCC_MIXER	3.3 V Power Supply for the Mixer. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
30	DVDD	1.8 V SPI Digital Supply. Place a 100 pF, 0.01 µF, and a 10 µF capacitor close to this pin.
31	SCLK	SPI Clock Digital Input. SCLK is a high impedance pin.
32	SDI	SPI Serial Data Input. SDI is a high impedance pin.
	EPAD	Exposed Pad. Solder the exposed pad to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

I/Q MODE

RF amplitude = −30 dBm, measurements performed with a 0 mV dc bias. VCC_MIXER = VCC_QUAD = VCC_BG = VCC_LNA = VCC_VGA = VCC_IF_BB = 3.3 V, DVDD = VCC_VVA = 1.8 V, and T_A = 25°C, unless otherwise noted. Register 0x0B is set to 0x727C, Register 0x03, Bits[13:12] are set to 11, V_{CM} = 1.15 V, Register 0x03, Bit 11 = 1, Register 0x03, Bit 8 = 0, and measurements are a composite of the I and Q channels. V_{ATT} is the attenuation voltage at the VCTRL pin. V_{ATT} = 0 V, unless otherwise specified.
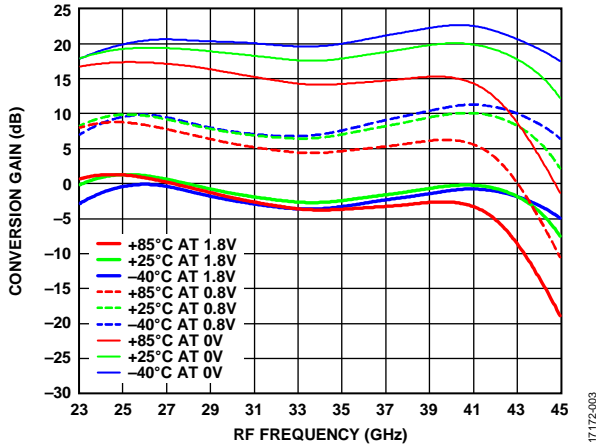
Figure 4. Conversion Gain vs. RF Frequency at Three Different Gain Settings for Various Temperatures, f_{BB} = 100 MHz (Upper Sideband)

Figure 5. Conversion Gain vs. RF Frequency for Various Supply Voltages, f_{BB} = 100 MHz

Figure 6. Conversion Gain vs. RF Frequency for Various LO Inputs, f_{BB} = 100 MHz
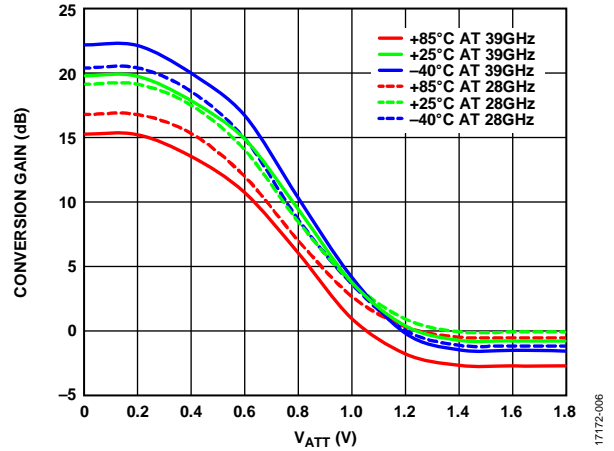
Figure 7. Conversion Gain vs. V_{ATT} for Various RF Frequencies (f_{RF}), f_{BB} = 100 MHz at f_{RF} = 28 GHz and 39 GHz
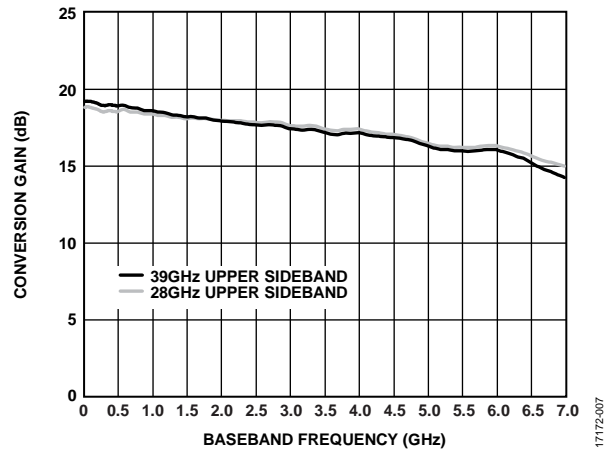
Figure 8. Conversion Gain vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Upper Sideband)
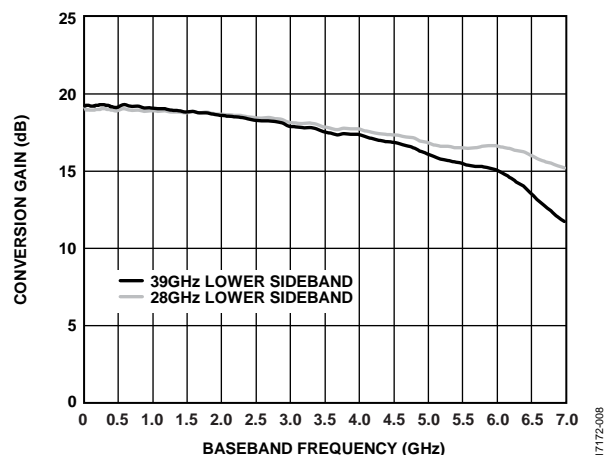
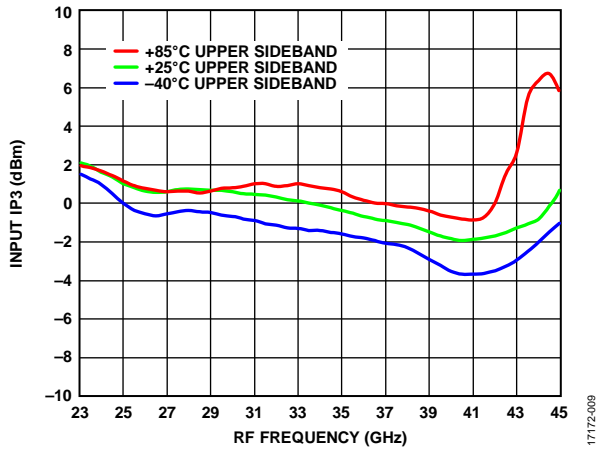Figure 9. Conversion Gain vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Lower Sideband)

Figure 10. Input IP3 vs. RF Frequency at Maximum Gain for Various Temperatures, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)
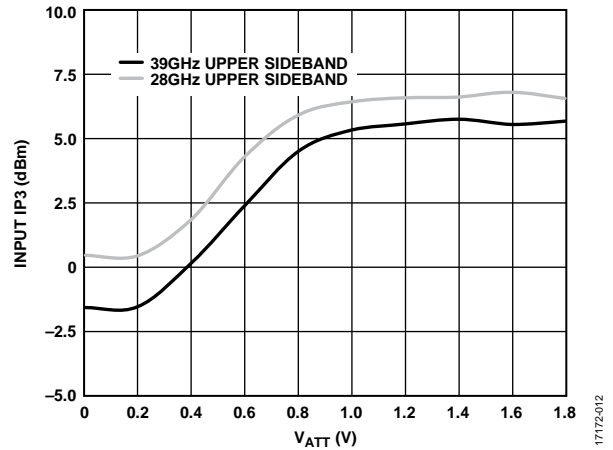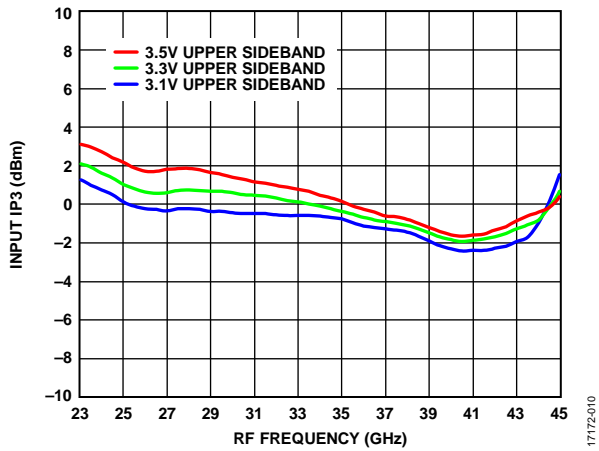

Figure 11. Input IP3 vs. RF Frequency at Maximum Gain for Various Supply Voltages, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)
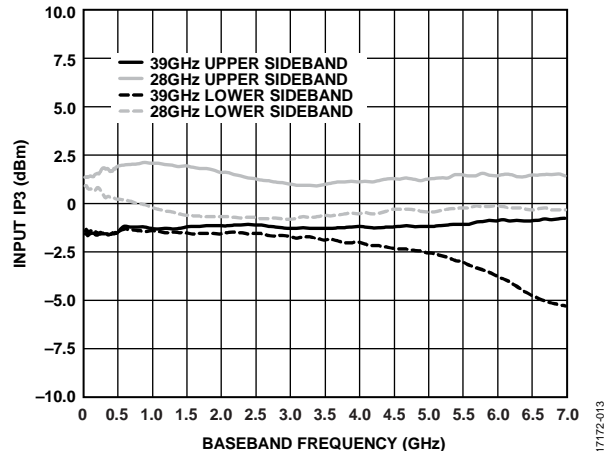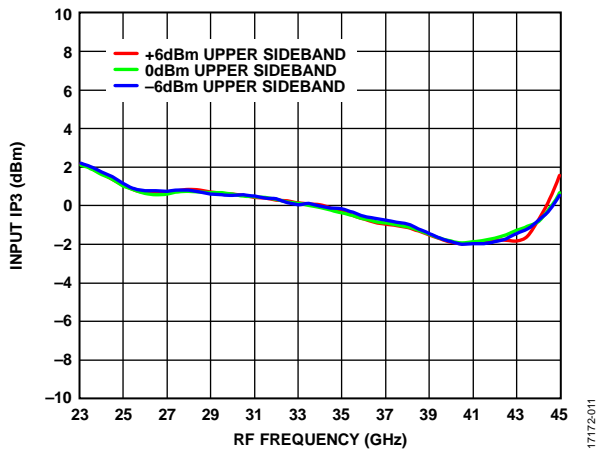

Figure 12. Input IP3 vs. RF Frequency at Maximum Gain for Various LO Inputs, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)
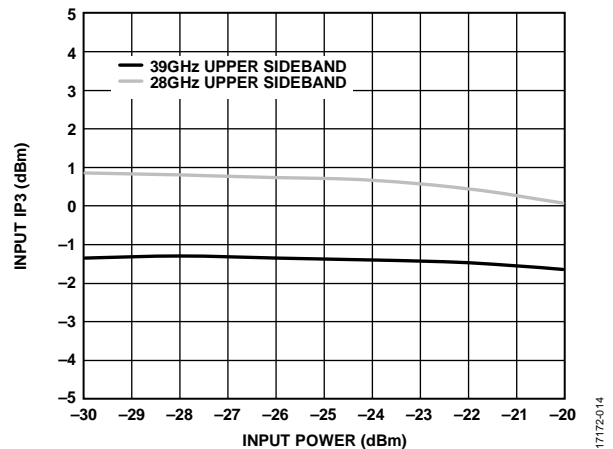

Figure 13. Input IP3 vs. V_{ATT} for Various RF Frequencies (f_{RF}), RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband) at f_{RF} = 28 GHz and 39 GHz

Figure 14. Input IP3 vs. Baseband Frequency at Maximum Gain, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing at f_{RF} = 28 GHz and 39 GHz, Upper Sideband and Lower Sideband

Figure 15. Input IP3 vs. Input Power for Various RF Frequencies (f_{RF}) at 20 MHz Spacing, f_{BB} = 100 MHz, f_{RF} = 28 GHz and 39 GHz
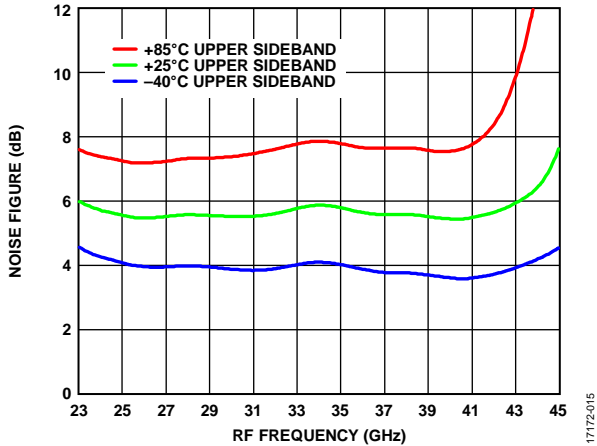
Figure 16. Noise Figure vs. RF Frequency at Maximum Gain for Various Temperatures, $f_{BB} = 100\ MHz$
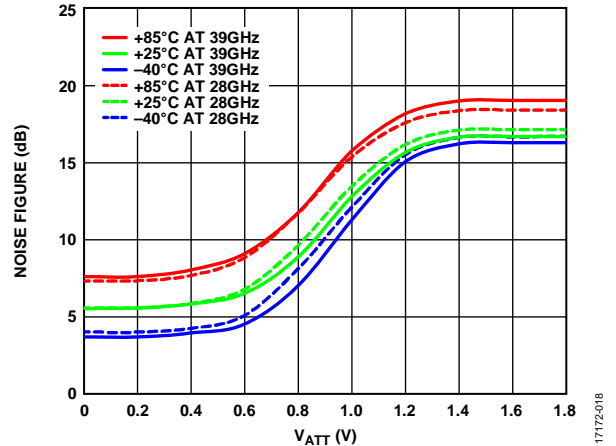

Figure 17. Noise Figure vs. RF Frequency for Various Supply Voltages, $f_{BB} = 100\ MHz$

Figure 18. Noise Figure vs. RF Frequency for Various LO Inputs, $f_{BB} = 100\ MHz$

Figure 19. Noise Figure vs. V_{ATT} for Various RF Frequencies and Temperatures, $f_{BB} = 100\ MHz$ at $f_{RF} = 28\ GHz$ and $39\ GHz$
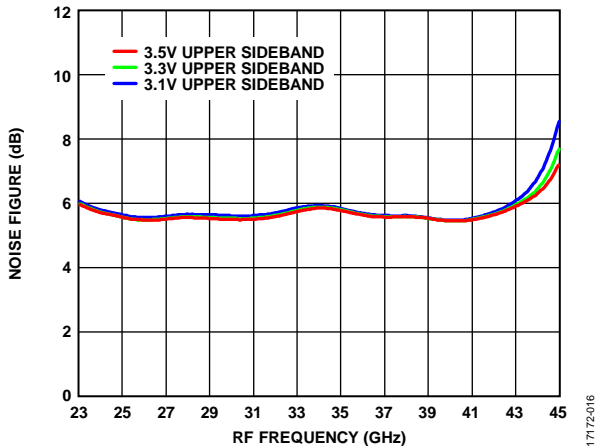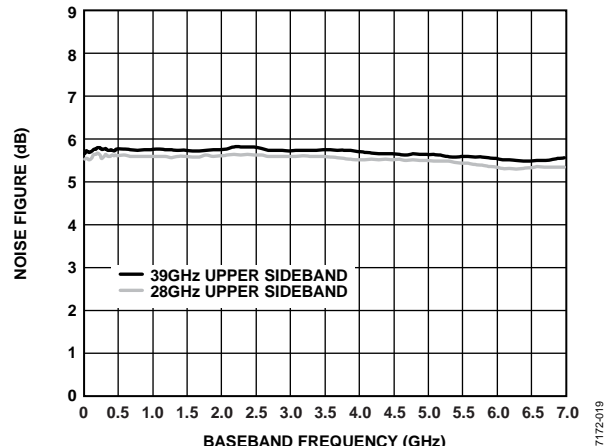

Figure 20. Noise Figure vs. Baseband Frequency at $f_{RF} = 28\ GHz$ and $39\ GHz$ (Upper Sideband)
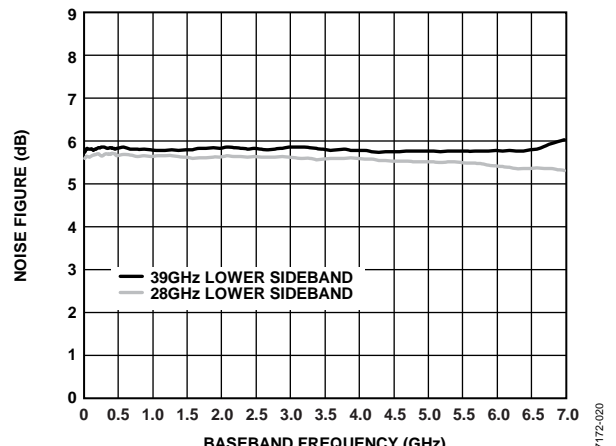

Figure 21. Noise Figure vs. Baseband Frequency at $f_{RF} = 28\ GHz$ and $39\ GHz$ (Lower Sideband)
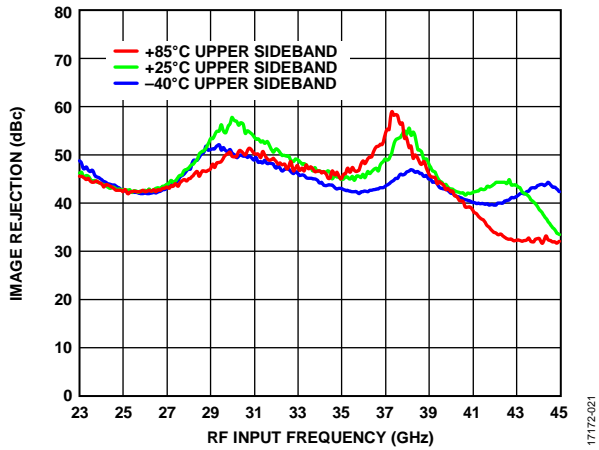
Figure 22. Image Rejection vs. RF Input Frequency at Maximum Gain for Various Temperatures, f_{BB} = 100 MHz, Uncalibrated
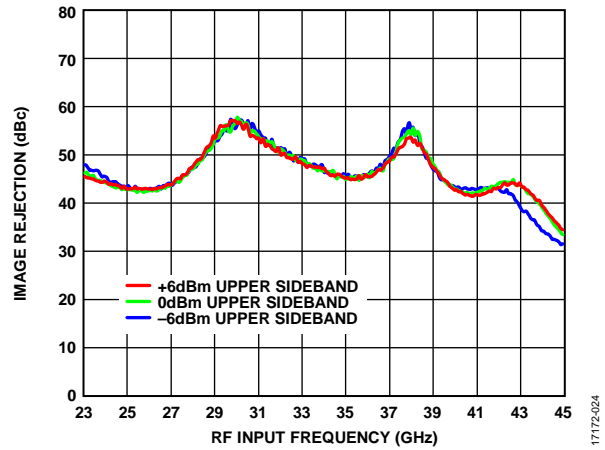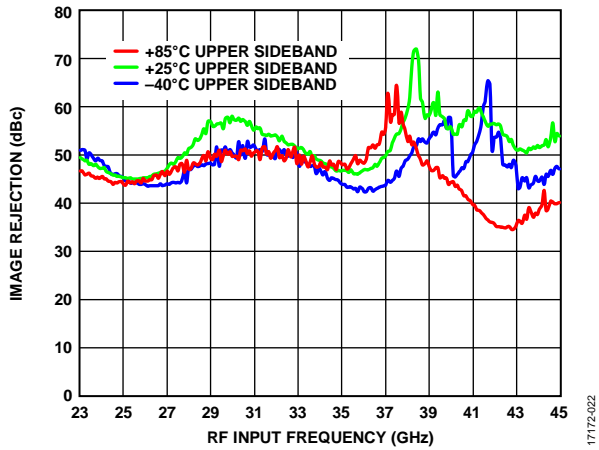

Figure 23. Image Rejection vs. RF Input Frequency at Maximum Gain for Various Temperatures, f_{BB} = 100 MHz, Calibrated

Figure 24. Image Rejection vs. RF Input Frequency for Various Supply Voltages, f_{BB} = 100 MHz

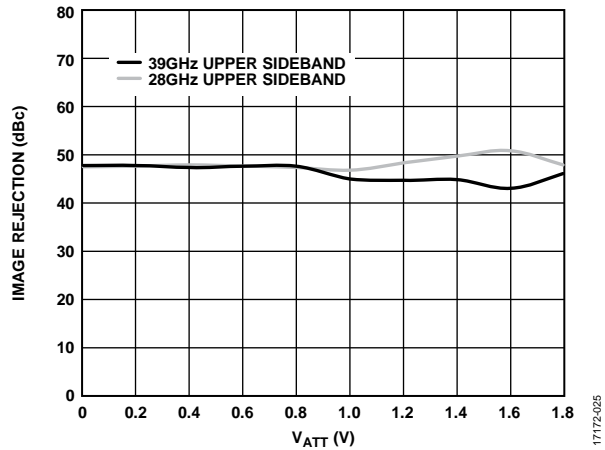Figure 25. Image Rejection vs. RF Input Frequency for Various LO Inputs, f_{BB} = 100 MHz

Figure 26. Image Rejection vs. V_{ATT} for Various RF Frequencies (f_{RF}), f_{BB} = 100 MHz at f_{RF} = 28 GHz and 39 GHz
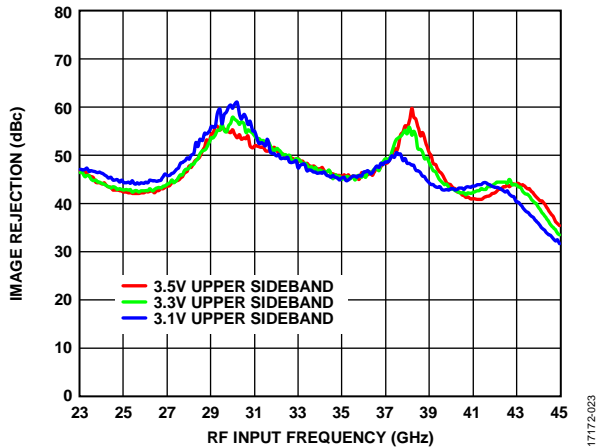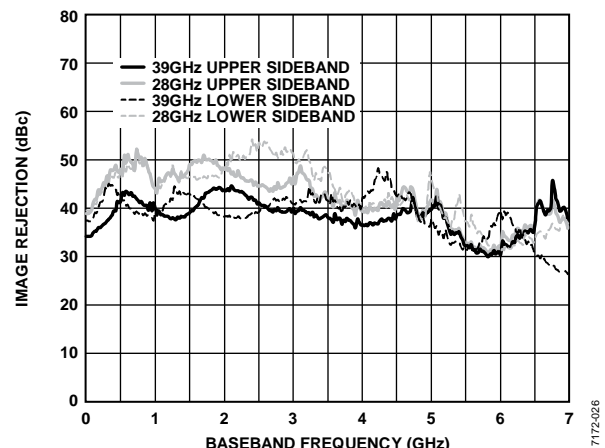

Figure 27. Image Rejection vs. Baseband Frequency at f_{RF} = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
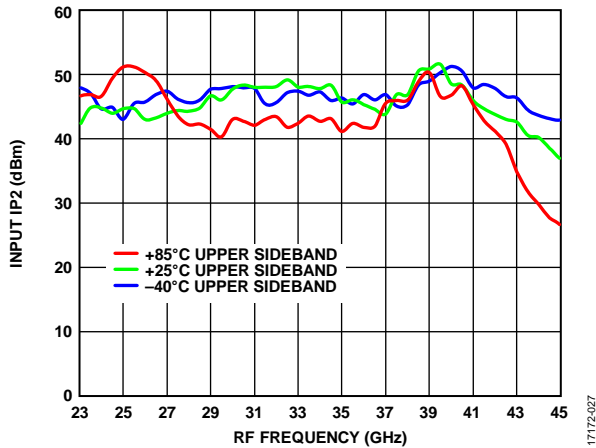
Figure 28. Input IP2 vs. RF Frequency at Maximum Gain for Various Temperatures, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)

Figure 31. Input IP2 vs. V_{ATT} for Various RF Frequencies (f_{RF}), RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband) at f_{RF} = 28 GHz and 39 GHz

Figure 29. Input IP2 vs. RF Frequency (f_{RF}) at Maximum Gain for Various Supply Voltages, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)
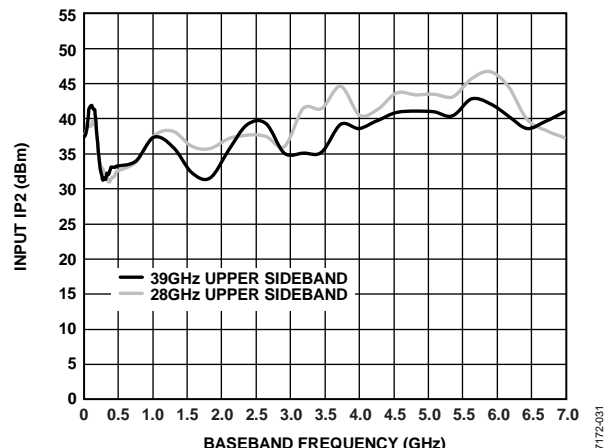
Figure 32. Input IP2 vs. Baseband Frequency at Maximum Gain, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing at f_{RF} = 28 GHz and 39 GHz, Upper Sideband
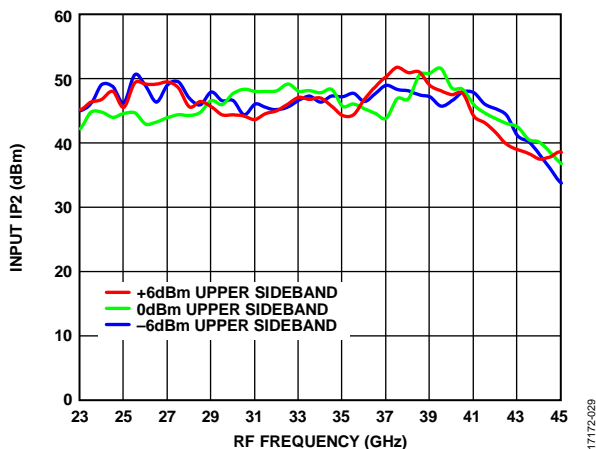
Figure 30. Input IP2 vs. RF Frequency at Maximum Gain for Various LO Inputs, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{BB} = 100 MHz (Upper Sideband)
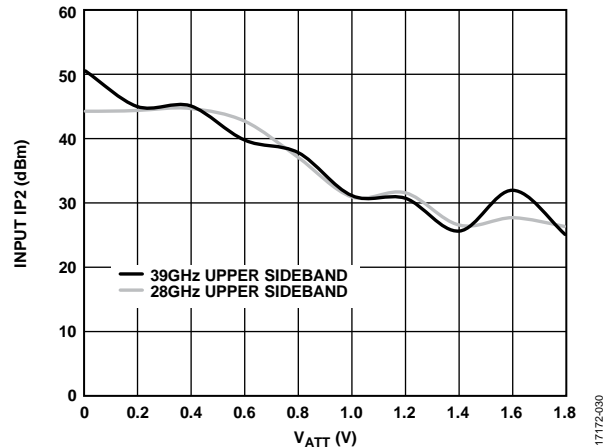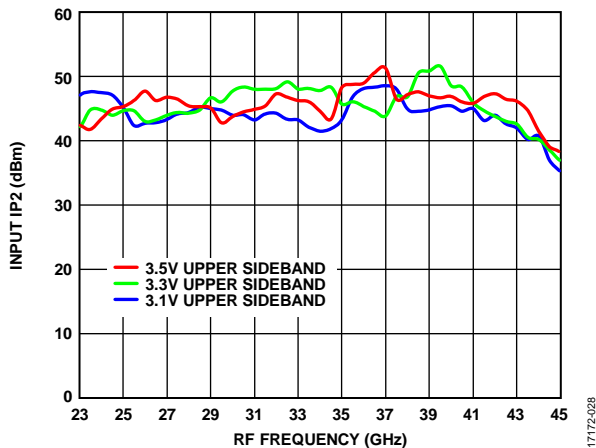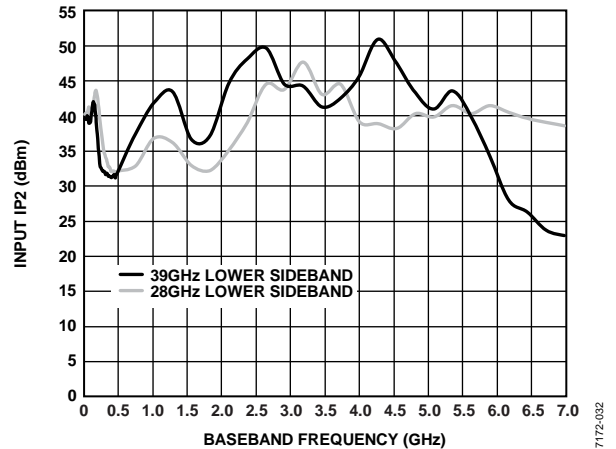

Figure 33. Input IP2 vs. Baseband Frequency for Various RF Frequencies (f_{RF}) at 20 MHz Spacing, f_{BB} = 100 MHz, f_{RF} = 28 GHz and 39 GHz
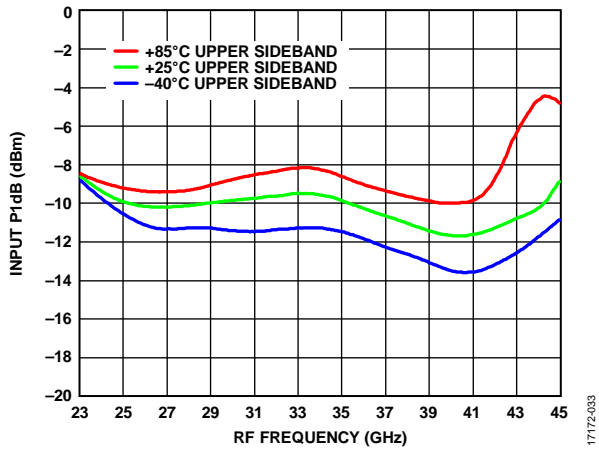
Figure 34. Input P1dB vs. RF Frequency at Maximum Gain for Various Temperatures, $f_{BB} = 100$ MHz
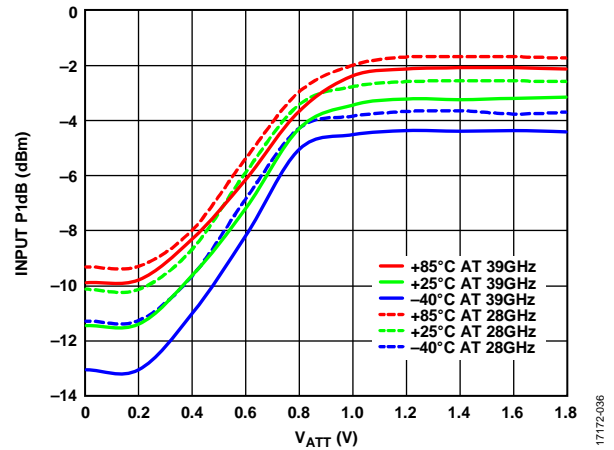
Figure 37. Input P1dB vs. V_{ATT} for Various RF Frequencies (f_{RF}), $f_{BB} = 100$ MHz at $f_{RF} = 28$ GHz and 39 GHz
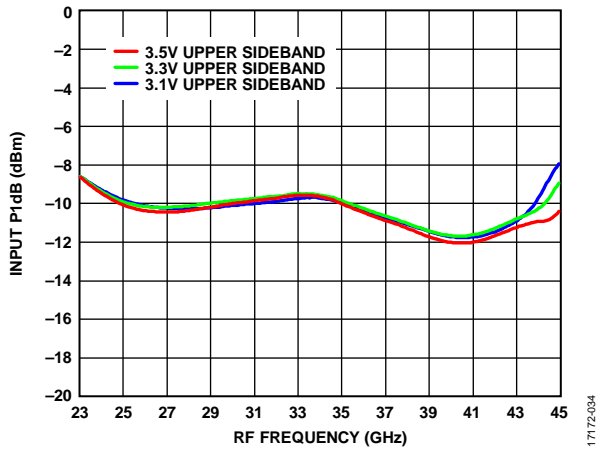
Figure 35. Input P1dB vs. RF Frequency for Various Supply Voltages, $f_{BB} = 100$ MHz
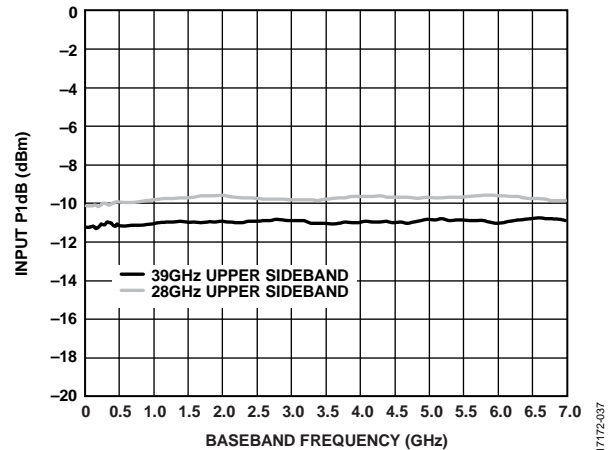
Figure 38. Input P1dB vs. Baseband Output Frequency at $f_{RF} = 28$ GHz and 39 GHz (Upper Sideband)
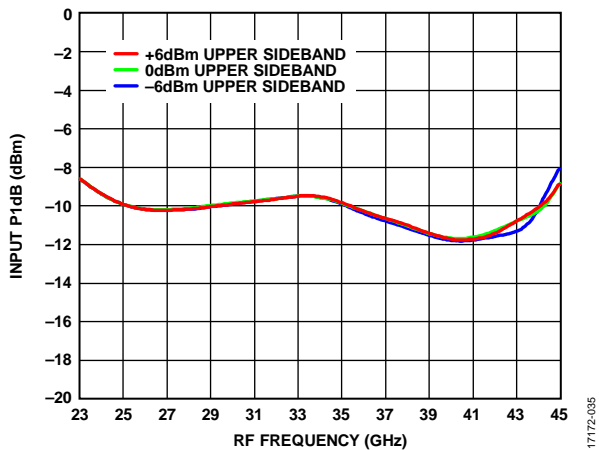
Figure 36. Input P1dB vs. RF Frequency for Various LO Inputs, $f_{BB} = 100$ MHz
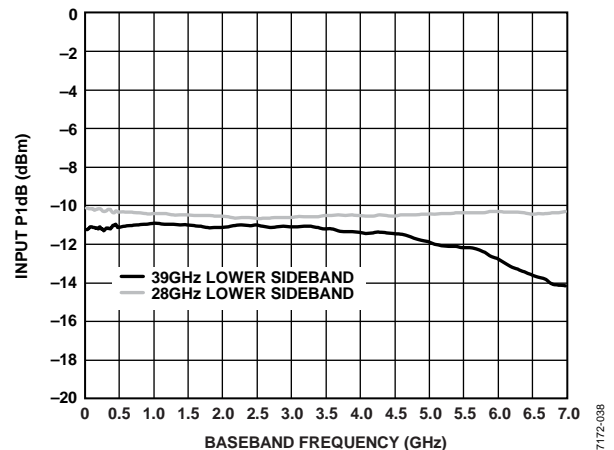
Figure 39. Input P1dB vs. Baseband Output Frequency at $f_{RF} = 28$ GHz and 39 GHz (Lower Sideband)
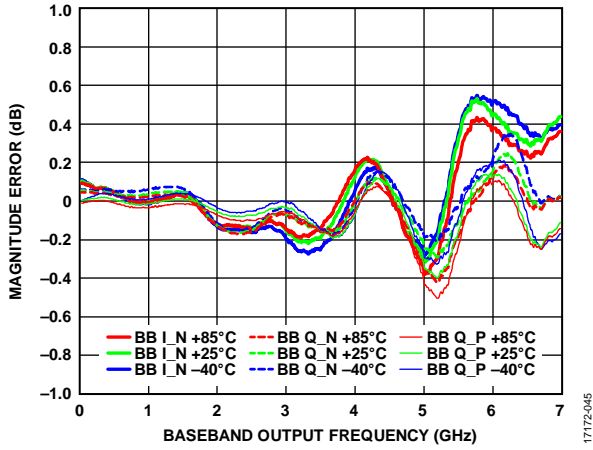
Figure 40. Magnitude Error vs. Baseband Output Frequency, Referenced to I_P Output, f_{RF} = 28 GHz, for Various Temperatures, at Maximum Gain
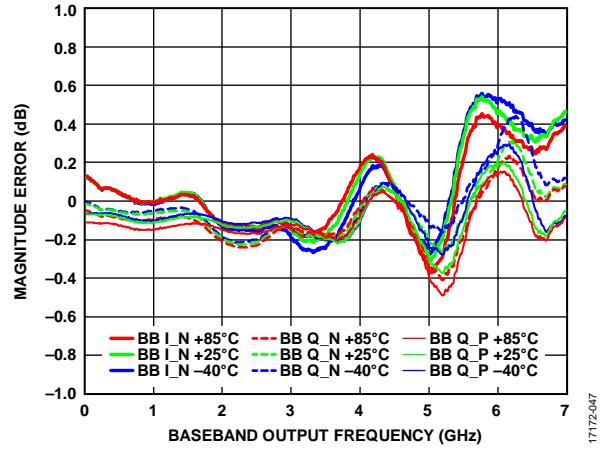
Figure 42. Magnitude Error vs. Baseband Output Frequency, Referenced to I_P Output, f_{RF} = 39 GHz, for Various Temperatures, at Maximum Gain
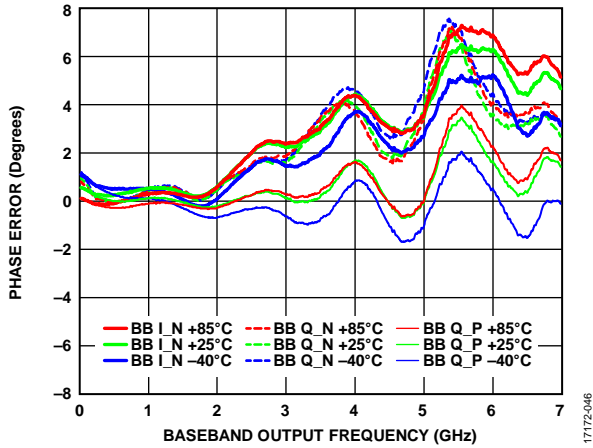
Figure 41. Phase Error vs. Baseband Output Frequency, Referenced to I_P Output, f_{RF} = 28 GHz, for Various Temperatures, at Maximum Gain
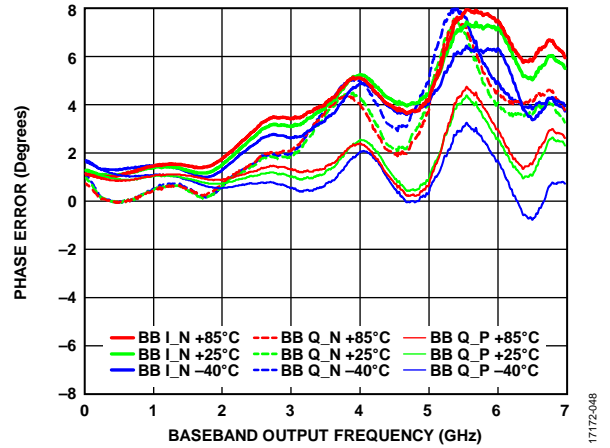
Figure 43. Phase Error vs. Baseband Output Frequency, Referenced to I_P Output, f_{RF} = 39 GHz, for Various Temperatures, at Maximum Gain
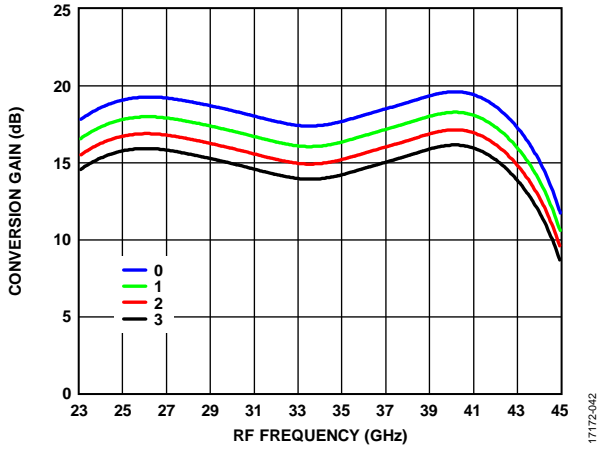
Figure 44. Conversion Gain vs. RF Frequency at Four Different BB_AMP_GAIN_CTRL (Register 0x0A, Bits[2:1]) Settings, f_{BB} = 100 MHz (Upper Sideband)
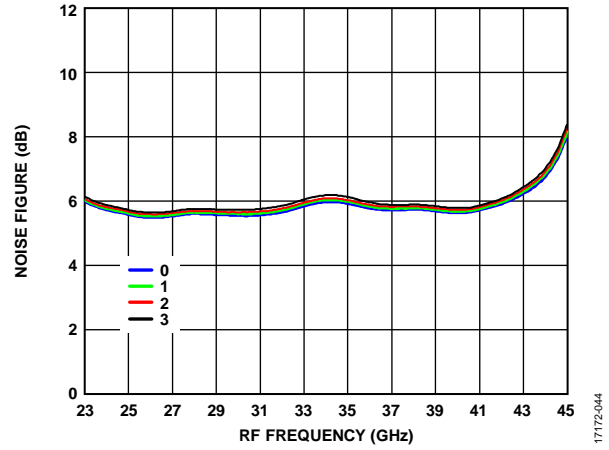
Figure 46. Noise Figure vs. RF Frequency Four Different BB_AMP_GAIN_CTRL (Register 0x0A, Bits[2:1]) Settings, f_{BB} = 100 MHz (Upper Sideband)
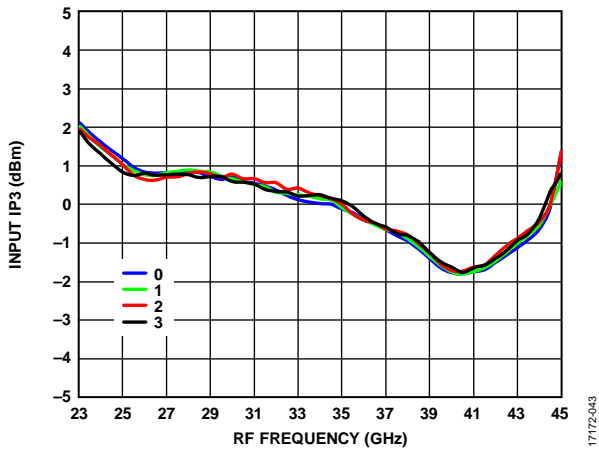
Figure 45. Input IP3 vs. RF Frequency at Four Different BB_AMP_GAIN_CTRL (Register A, Bits[2:1]) Settings, f_{BB} = 100 MHz (Upper Sideband)

IF MODE

RF amplitude = −30 dBm, measurements performed with a 0 mV dc bias. VCC_MIXER = VCC_QUAD = VCC_BG = VCC_LNA = VCC_VGA = VCC_IF_BB = 3.3 V, DVDD = VCC_VVA = 1.8 V, T_A = 25°C unless otherwise specified. Register 0x0B set to 0x727C, Register 0x03, Bits[12:13] set to 11, measurements performed with a 90° hybrid, Register 0x03, Bit 11 = 0, and Register 0x03, Bit 8 = 1.

Figure 47. Conversion Gain vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

Figure 50. Conversion Gain vs. IF Frequency (f_{IF}) at Maximum Gain, f_{RF} = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)

Figure 48. Conversion Gain vs. RF Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

Figure 51. Conversion Gain vs. V_{ATT} at Various Temperatures, f_{IF} = 3.5 GHz, f_{RF} = 28 GHz and 39 GHz (Upper Sideband)
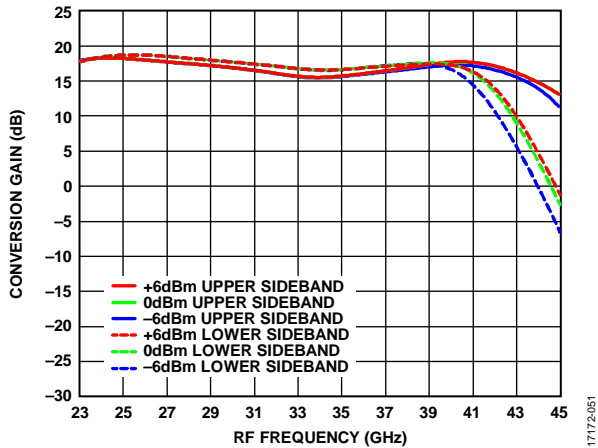
Figure 49. Conversion Gain vs. RF Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

Figure 52. Conversion Gain vs. V_{ATT} at Various Temperatures, f_{IF} = 3.5 GHz , f_{RF} = 28 GHz and 39 GHz (Lower Sideband)

Figure 53. Input IP3 vs. RF Frequency at Maximum Gain for Various Temperatures, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f$_{IF}$ = 3.5 GHz (Upper Sideband and Lower Sideband)

Figure 54. Input IP3 vs. RF Frequency at Maximum Gain for Various Supply Voltages, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f$_{IF}$ = 3.5 GHz (Upper Sideband and Lower Sideband)

Figure 55. Input IP3 vs. RF Frequency at Maximum gain for Various LO Inputs, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f$_{IF}$ = 3.5 GHz (Upper Sideband and Lower Sideband)
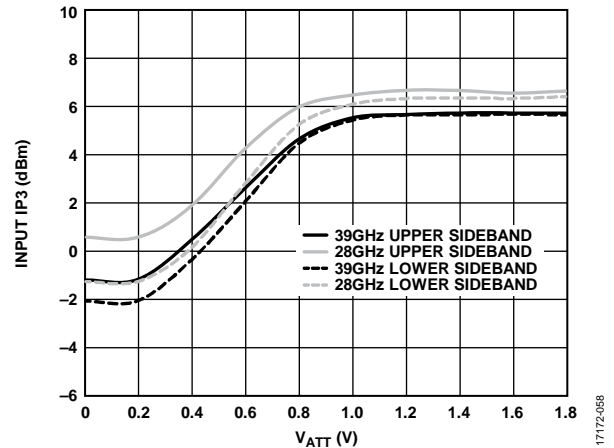
Figure 56. Input IP3 vs. V$_{ATT}$ for Various RF Frequencies (f$_{RF}$), RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f$_{IF}$ = 3.5 GHz at f$_{RF}$ = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
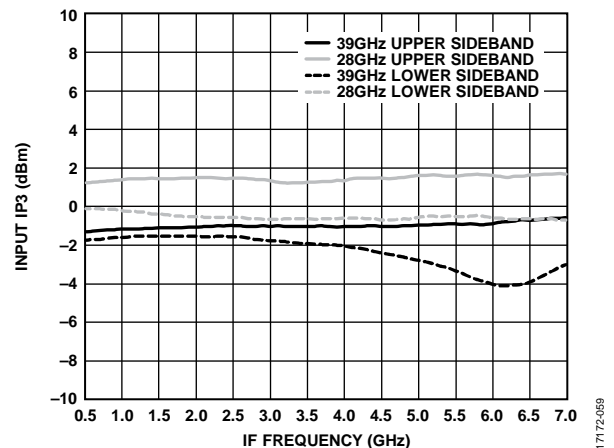
Figure 57. Input IP3 vs. IF Frequency at Maximum Gain, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing at f$_{RF}$ = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
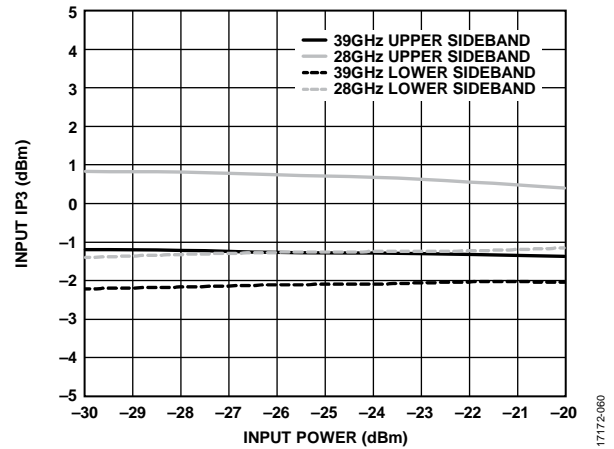
Figure 58. Input IP3 vs. Input Power for Various RF Frequencies (f$_{RF}$), at 20 MHz Spacing, f$_{IF}$ = 3.5 GHz, f$_{RF}$ = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
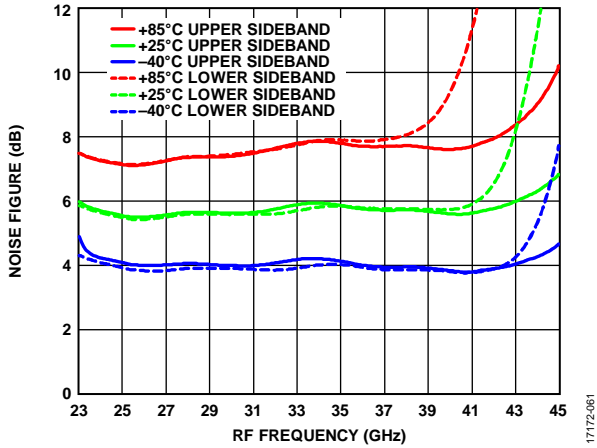
Figure 59. Noise Figure vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

Figure 60. Noise Figure vs. RF Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)

Figure 61. Noise Figure vs. RF Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)
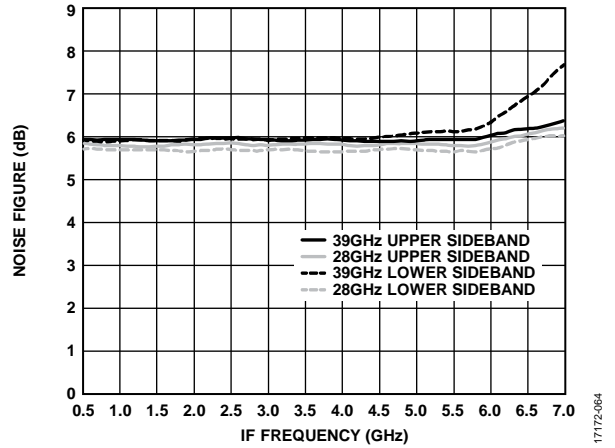
Figure 62. Noise Figure vs. IF Frequency at Maximum Gain, f_{RF} = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
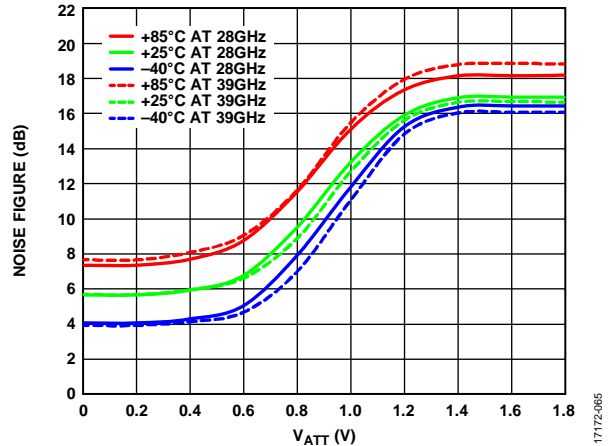
Figure 63. Noise Figure vs. V_{ATT} at Various Temperatures, f_{IF} = 3.5 GHz, f_{RF} = 28 GHz and 39 GHz (Upper Sideband)
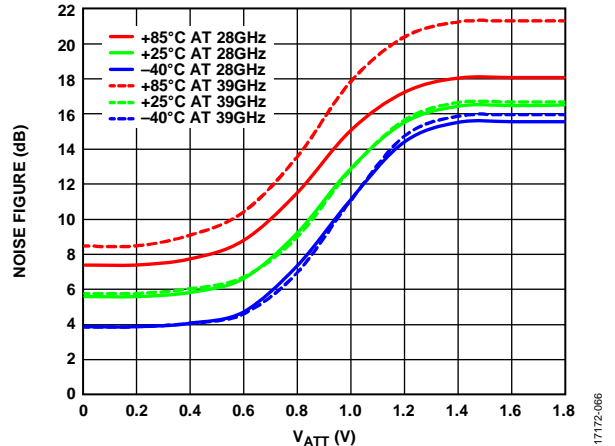
Figure 64. Noise Figure vs. V_{ATT} at Various Temperatures, f_{IF} = 3.5 GHz, f_{RF} = 28 GHz and 39 GHz (Lower Sideband)
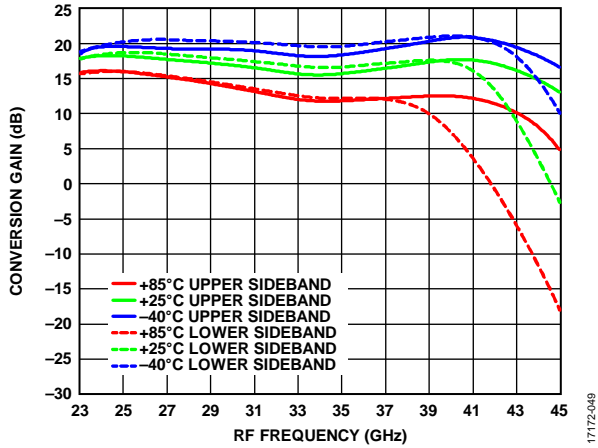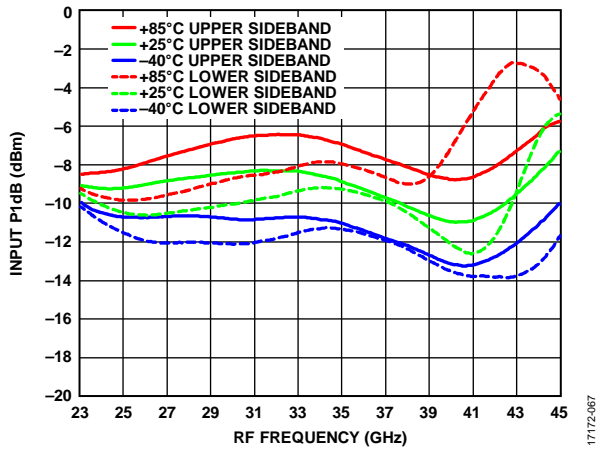
Figure 65. Input P1dB vs. RF Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)
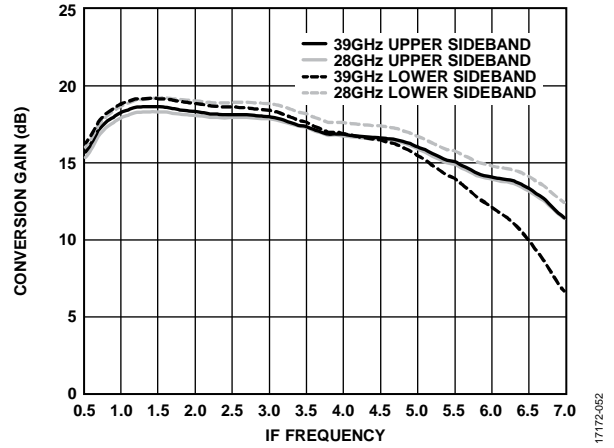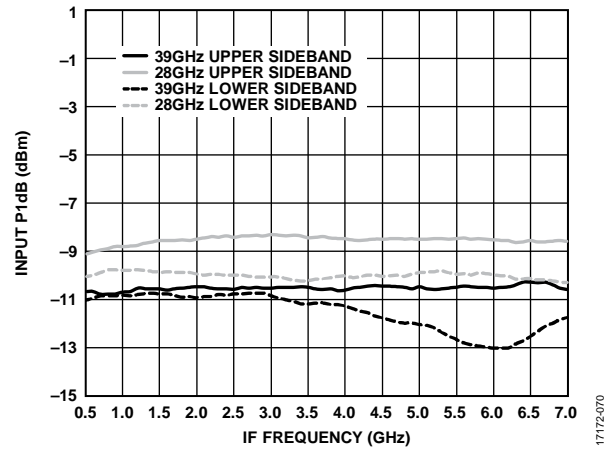

Figure 68. Input P1dB vs. IF Frequency at Maximum Gain, f_{RF} = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
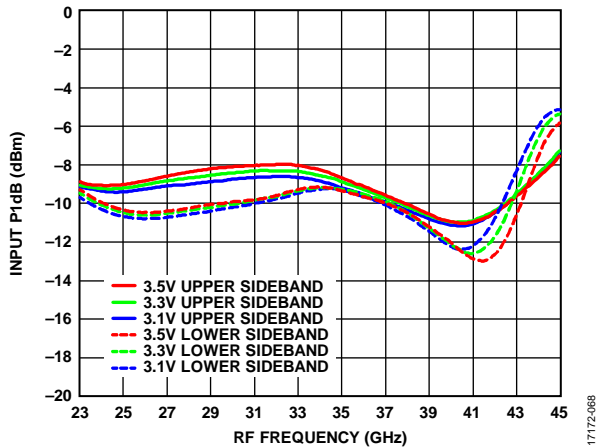
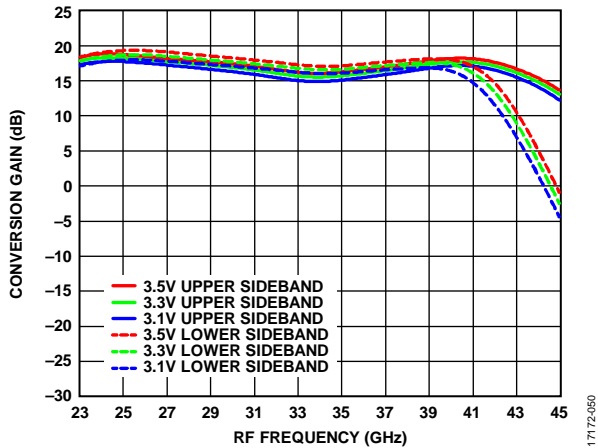

Figure 66. Input P1dB vs. RF Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)
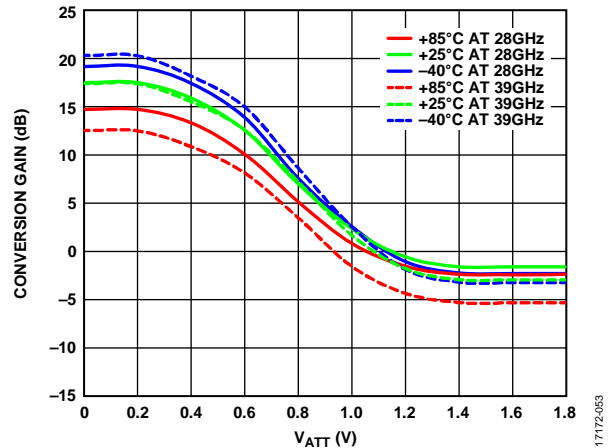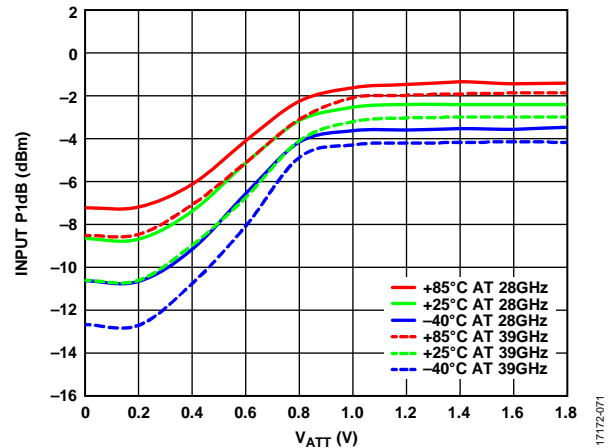

Figure 69. Input P1dB vs. V_{ATT} at Various Temperatures, f_{IF} = 3.5 GHz, f_{RF} = 28 GHz and 39 GHz (Upper Sideband)
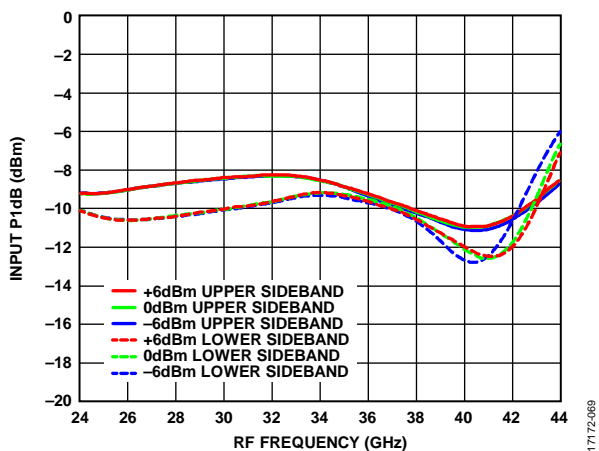
Figure 67. Input P1dB vs. RF Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)
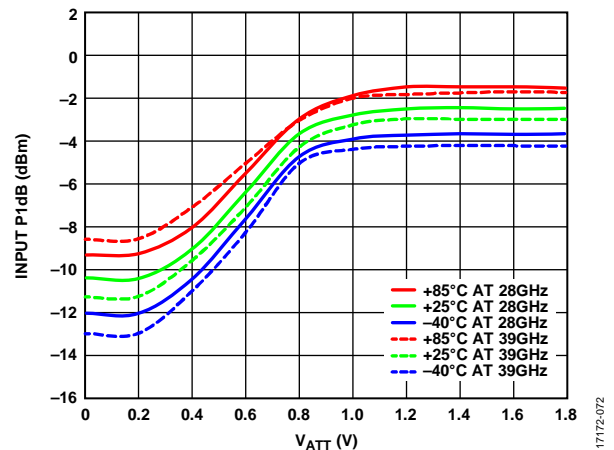
Figure 70. Input P1dB vs. V_{ATT} at Various Temperatures, f_{IF} = 3.5 GHz, f_{RF} = 28 GHz and 39 GHz (Lower Sideband)
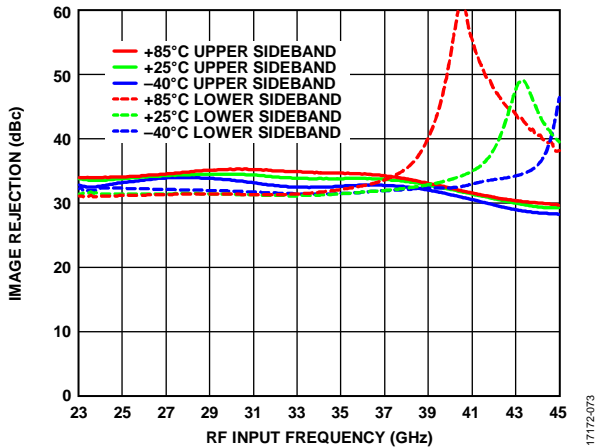
Figure 71. Image Rejection vs. RF Input Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband), Uncalibrated

Figure 72. Image Rejection vs. RF Input Frequency at Maximum Gain for Various Temperatures, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband), Calibrated

Figure 73. Image Rejection vs. RF Input Frequency at Maximum Gain for Various Supply Voltages, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)
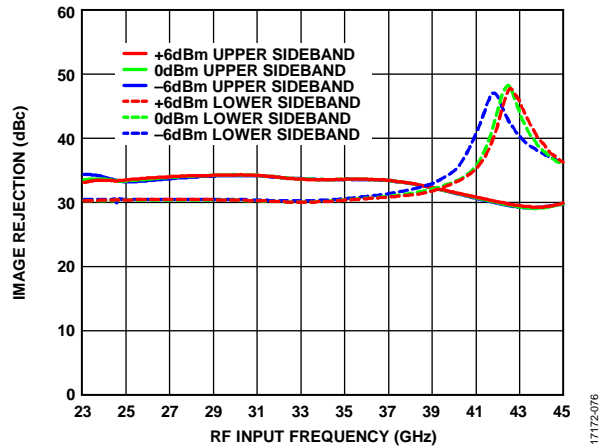
Figure 74. Image Rejection vs. RF Input Frequency at Maximum Gain for Various LO Inputs, f_{IF} = 3.5 GHz (Upper Sideband and Lower Sideband)
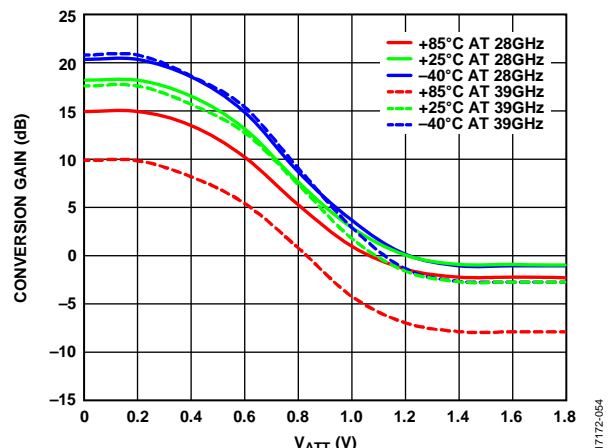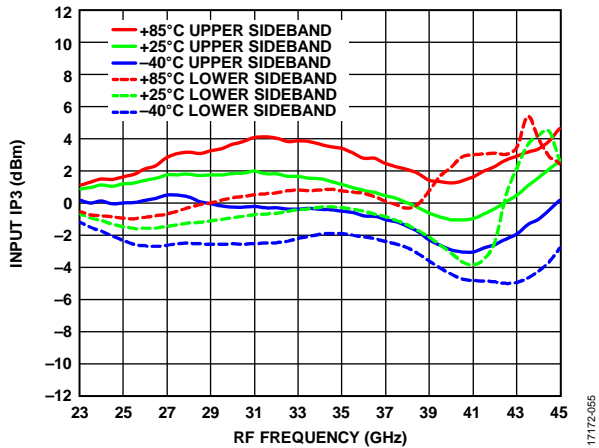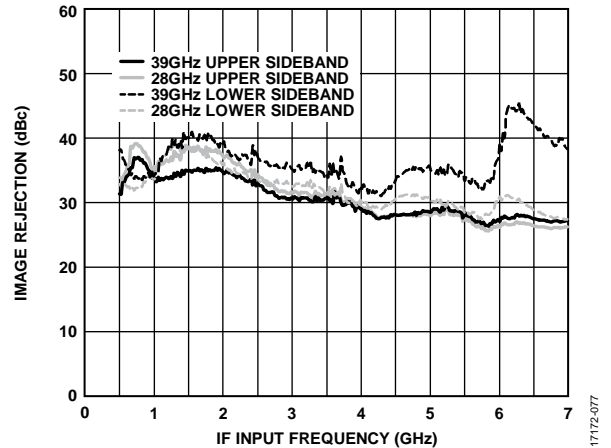

Figure 75. Image Rejection vs. IF Input Frequency at Maximum Gain, f_{RF} = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
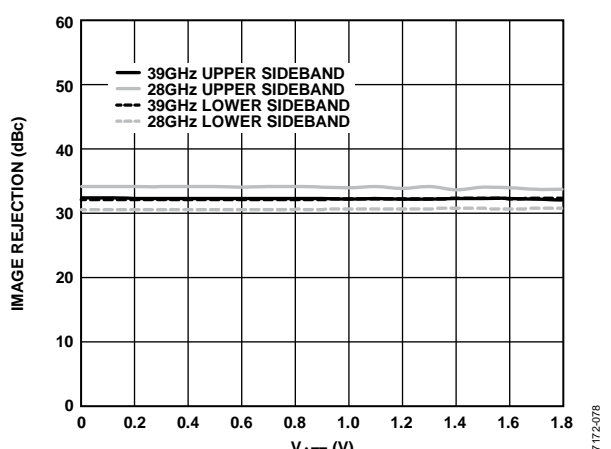
Figure 76. Image Rejection vs. V_{ATT} at Various RF Frequencies (f_{RF}), f_{IF} = 3.5 GHz, f_{RF} = 28 GHz and 39 GHz (Upper Sideband and Lower Sideband)
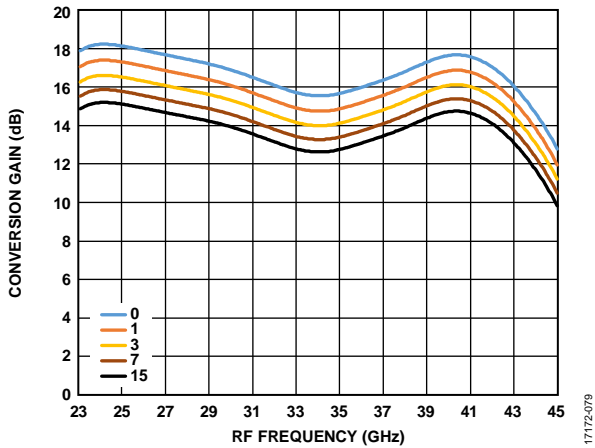
Figure 77. Conversion Gain vs. RF Frequency at Different IF_AMP_COARSE_GAIN_x Settings, f_{IF} = 3.5 GHz (Upper Sideband); Settings for Register 0x08, Bits[11:8] and Register 0x09, Bits[15:12] Are the Same
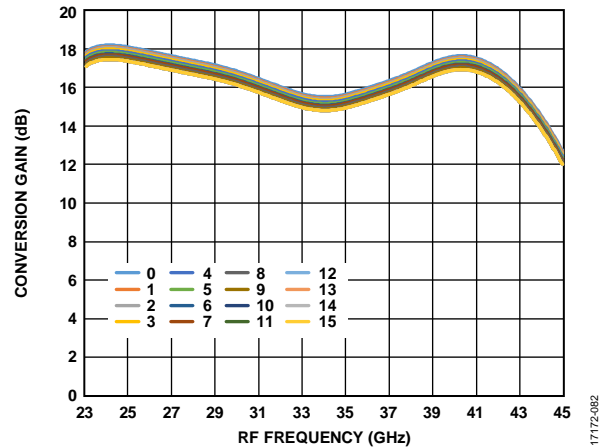
Figure 80. Conversion Gain vs. RF Frequency at Different IF_AMP_ FINE_GAIN_x Settings, f_{IF} = 3.5 GHz (Upper Sideband); Register 0x08, Bits[7:4] and Bits[3:0] Are the Same
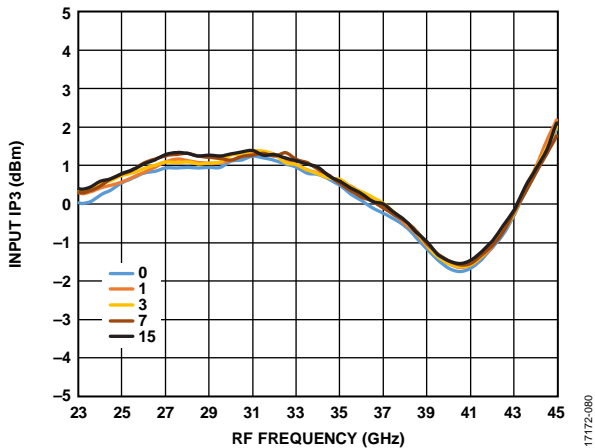
Figure 78. Input IP3 vs. RF Frequency at Different IF_AMP_COARSE_GAIN_x Settings, f_{IF} = 3.5 GHz (Upper Sideband); Settings for Register 0x08, Bits[11:8] and Register 0x09, Bits[15:12] Are the Same
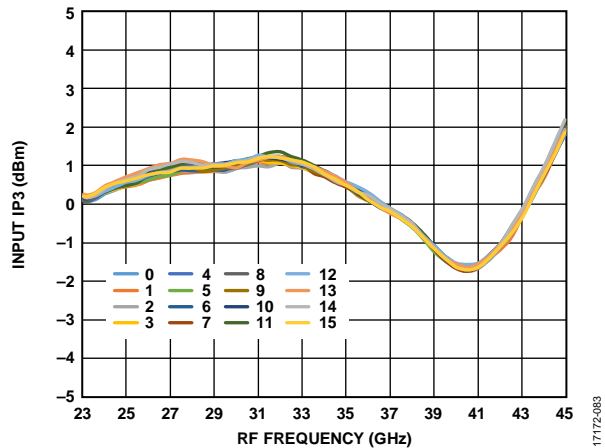
Figure 81. Input IP3 vs. RF Frequency at Different IF_AMP_FINE_GAIN_x Settings, f_{IF} = 3.5 GHz (Upper Sideband); Settings for Register 0x08, Bits[7:4] and Bits[3:0] Are the Same
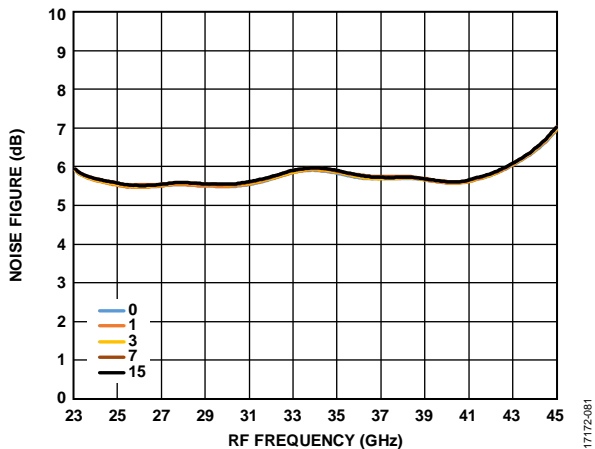
Figure 79. Noise Figure vs. RF Frequency at Different IF_AMP_COARSE_GAIN_x Settings, f_{IF} = 3.5 GHz (Upper Sideband); Settings for Register 0x08, Bits[11:8] and Register 0x09, Bits[15:12] Are the Same
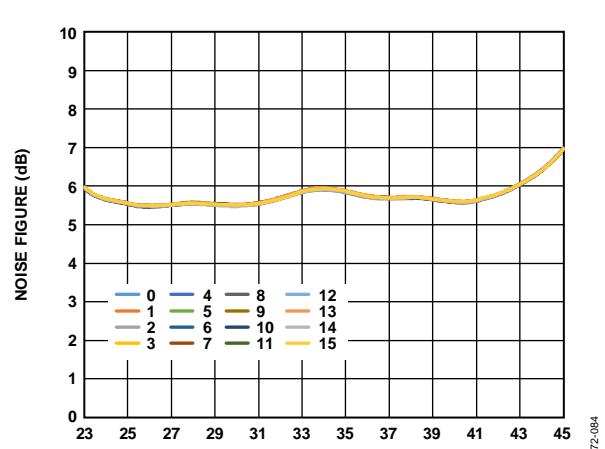
Figure 82. Noise Figure vs. RF Frequency at Different IF_AMP_FINE_GAIN_x Settings, f_{IF} = 3.5 GHz (Upper Sideband); Settings for Register 0x08, Bits[7:4] and Bits[3:0] Are the Same
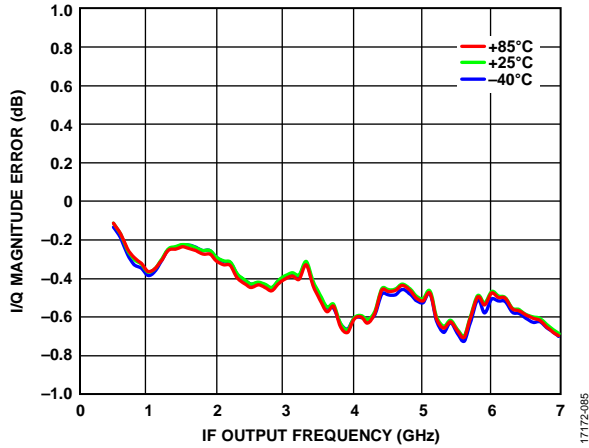
Figure 83. I/Q Magnitude Error vs. IF Output Frequency, Referenced to IF_I Output, f_{RF} = 28 GHz, for Various Temperatures, at Maximum Gain
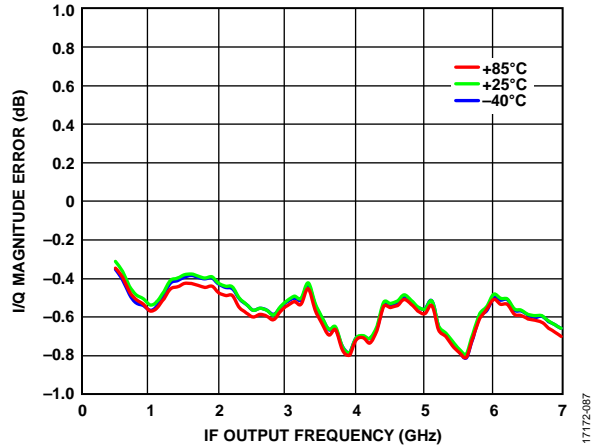
Figure 85. I/Q Magnitude Error vs. IF Output Frequency, Referenced to IF_I Output, f_{RF} = 39 GHz, for Various Temperatures, at Maximum Gain
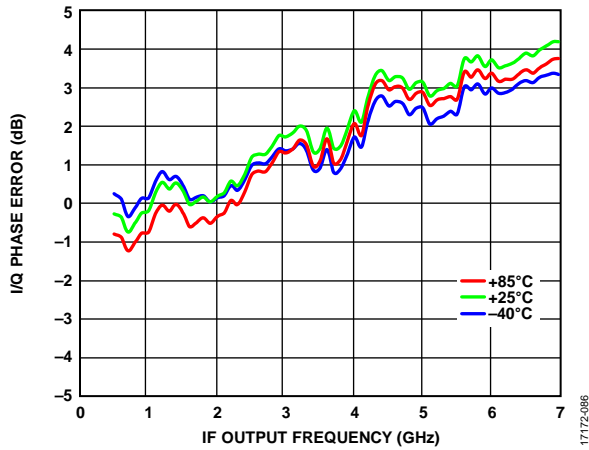
Figure 84. I/Q Phase Error vs. IF Output Frequency, Referenced to IF_I Output, f_{RF} = 28 GHz, for Various Temperatures, at Maximum Gain
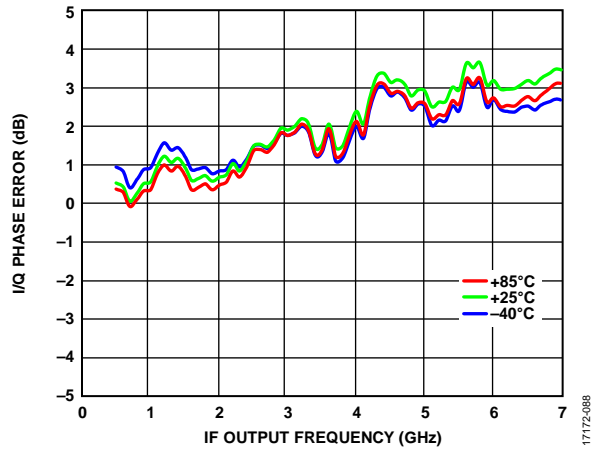
Figure 86. I/Q Phase Error vs. IF Output Frequency, Referenced to IF_I Output, f_{RF} = 39 GHz, for Various Temperatures, at Maximum Gain

OUTPUT DETECTOR PERFORMANCE

RF amplitude = −30 dBm, measurements performed with a 0 mV dc bias. VCC_MIXER = VCC_QUAD = VCC_BG = VCC_LNA = VCC_VGA = VCC_IF_BB = 3.3 V, DVDD = VCC_VVA = 1.8 V, Register 0x0B is set to 0x727C, Register 0x03, Bit 6 = 0, Register 0x03, Bits[13:12] set to 11, and T_A = 25°C, unless otherwise noted.
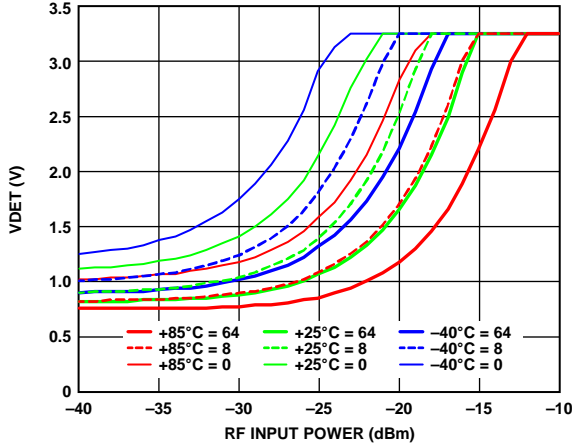
Figure 87. VDET vs. RF Input Power, f_{RF} = 28 GHz for Various Temperatures and DET_PROG Settings
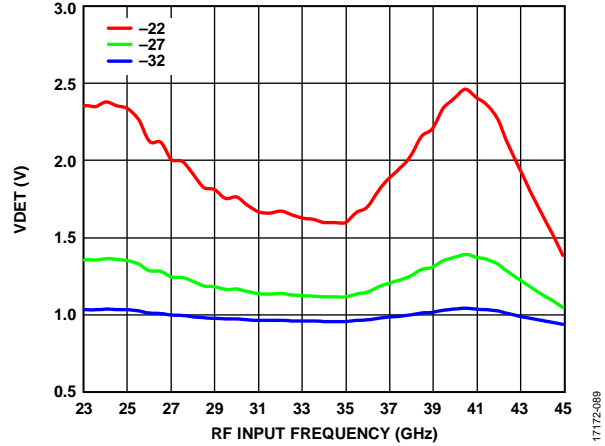
Figure 89. VDET vs. RF Input Frequency at Various Input Power Levels, DET_PROG = 8
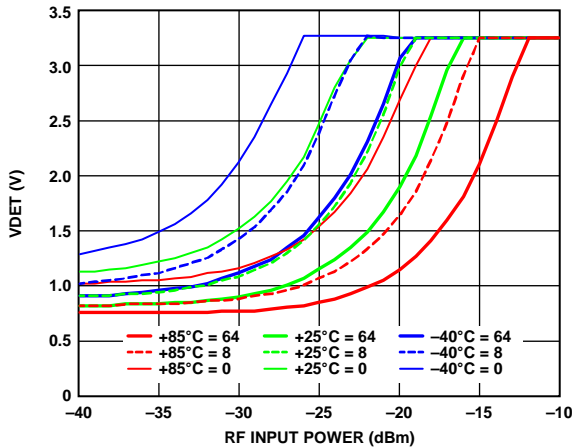
Figure 88. VDET vs. RF Input Power, f_{RF} = 39 GHz for Various Temperatures and DET_PROG Settings
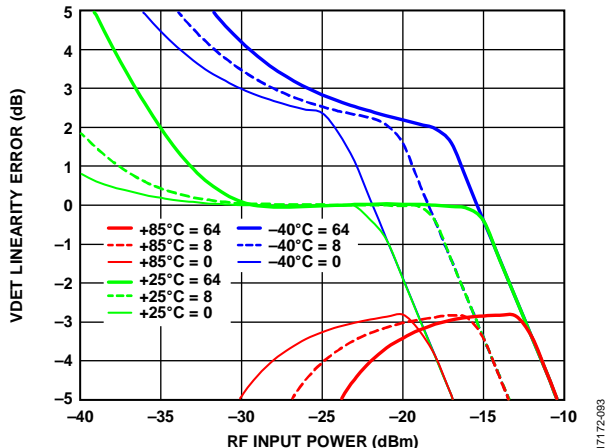
Figure 90. VDET Linearity Error vs. RF Input Power, f_{RF} = 28 GHz for Various Temperatures and DET_PROG Settings
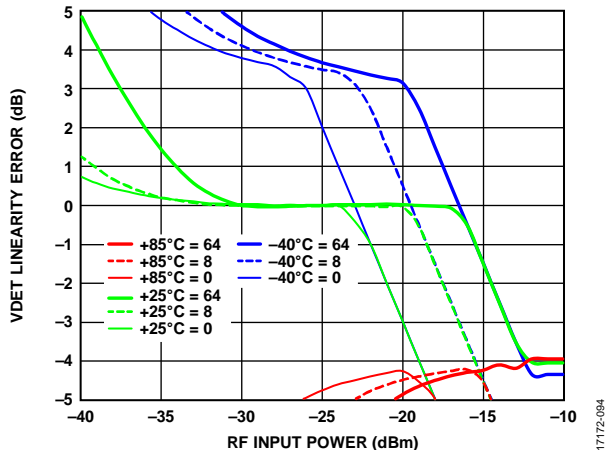
Figure 91. VDET Linearity Error vs. RF Input Power, f_{RF} = 39 GHz for Various Temperatures and DET_PROG Settings

RETURN LOSS AND ISOLATIONS

RF amplitude = −30 dBm, measurements performed with a 0 mV dc bias. VCC_MIXER = VCC_QUAD = VCC_BG = VCC_LNA = VCC_VGA = VCC_IF_BB = 3.3 V, DVDD = VCC_VVA = 1.8 V, Register 0x0B is set to 0x727C, Register 0x03, Bits[13:12] are set to 11, and T_A = 25°C, unless otherwise noted.

Measurements in IF mode performed with a 90° hybrid, Register 0x03, Bit 11 = 0, Register 0x03, Bit 8 = 1, unless otherwise noted. Measurements in I/Q mode are measured as a composite of the I and Q channel performed, V_{CM} = 1.15 V, Register 0x03, Bit 11 = 1, and Register 0x03, Bit 8 = 0, unless otherwise noted.
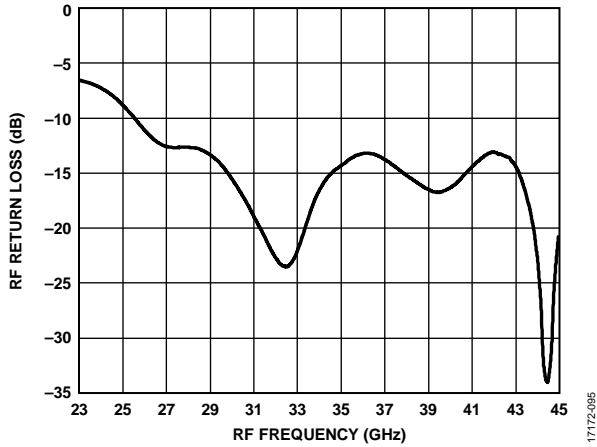
Figure 92. RF Input Return Loss vs. RF Frequency
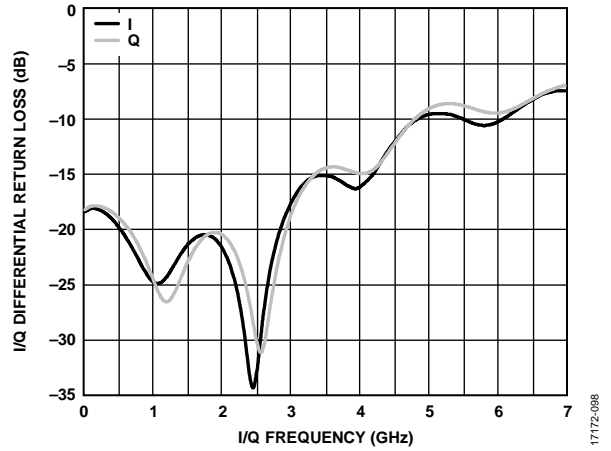
Figure 95. I/Q Differential Return Loss vs. I/Q Frequency (Taken Without Hybrids or Baluns)
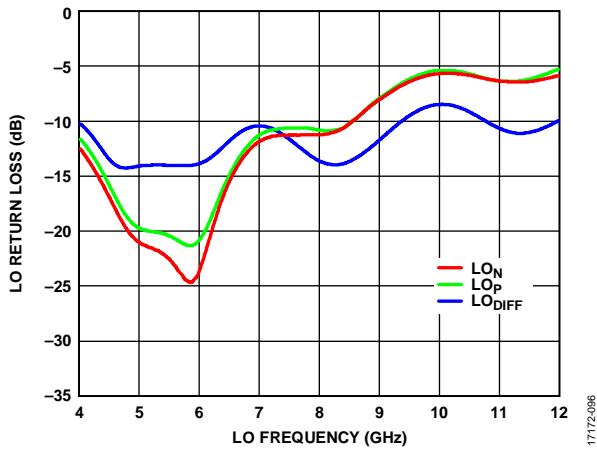
Figure 93. LO Return Loss vs. LO Frequency
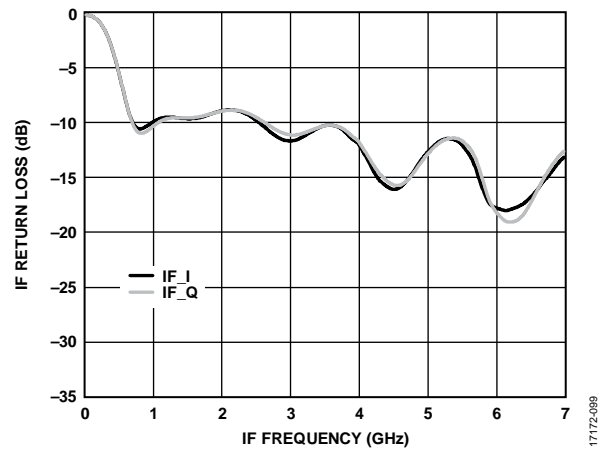
Figure 96. IF Return Loss vs. IF Frequency (Taken Without Hybrid)
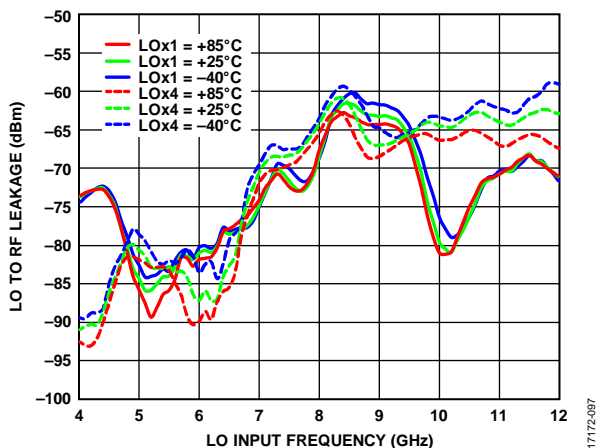
Figure 94. LO to RF Leakage vs. LO Input Frequency for Various Temperatures at Different Gain Settings
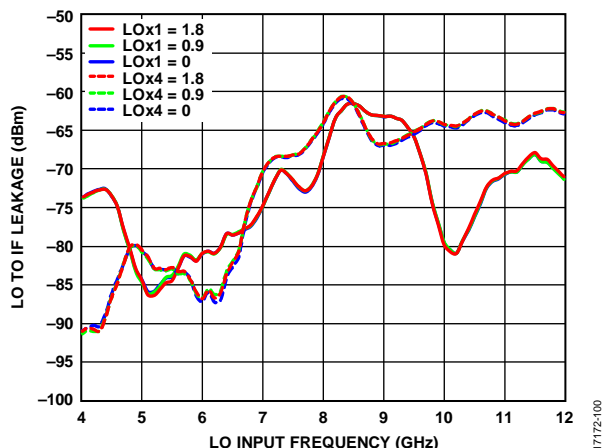
Figure 97. LO to IF Leakage vs. LO Input Frequency at Different VCTRL Settings
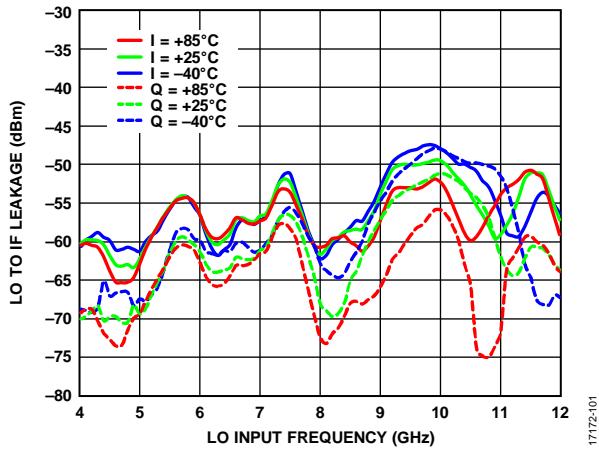
Figure 98. LO to IF Leakage vs. LO Input Frequency at Various Temperatures

Figure 99. LO to I/Q Leakage vs. LO Input Frequency at Various Temperatures (Taken Without Hybrid)
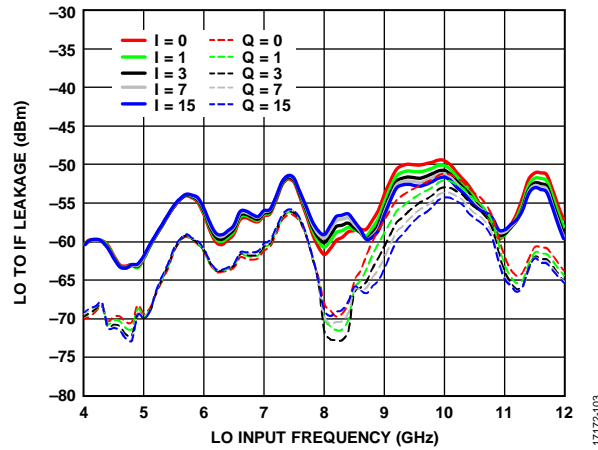
Figure 100. LO to IF Leakage, vs. LO Input Frequency at Different IF Amplifier Gain Settings (Taken Without Hybrid)
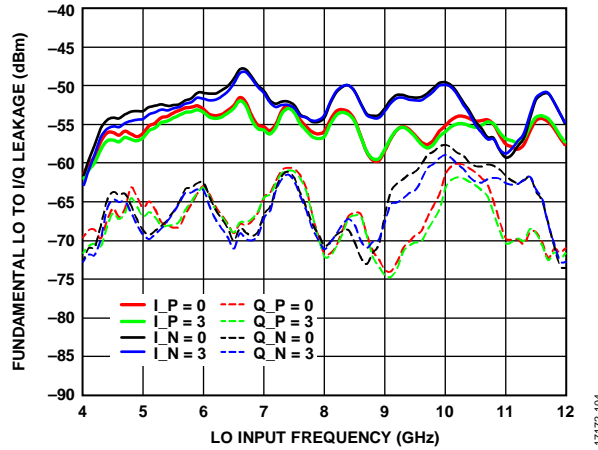
Figure 101. Fundamental LO to I/Q Leakage vs. LO Input Frequency at Different Baseband Amplifier Gain Settings

M × N SPURIOUS PERFORMANCE

Mixer spurious products are measured in dBc from the IF output power level. Spurious values are measured using the following equation:

$$|(M \times RF)+ (N \times LO)|$$

N/A means not applicable. Blank cells in the spurious performance tables indicate that the frequency is above 50 GHz and is not measured.

The LO frequencies are referred from the frequencies applied to the LO_x pin of the ADMV1014. RF amplitude = −30 dBm, measurements performed with a 0 mV dc bias. VCC_MIXER = VCC_QUAD = VCC_BG = VCC_LNA = VCC_VGA = VCC_IF_BB = 3.3 V, DVDD = VCC_VVA = 1.8 V, Register 0x0B is set to 0x727C, Register 0x03, Bits[13:12] are set to 11, and T_A = 25°C, unless otherwise noted.

Measurements in IF mode performed with Register 0x03, Bit 11 = 0 and Register 0x03, Bit 8 = 1, unless otherwise noted.

The measurements in I/Q mode are as follows: V_{CM} = 1.15 V, Register 0x03, Bit 11 = 1, and Register 0x03, Bit 8 = 0, unless otherwise noted.

I/Q Mode

Measurements are made on the I_P port. Data is taken without any hybrids or baluns.

BB frequency (f_{BB}) =100 MHz, LO= 6.975 GHz at 0 dBm, and f_{RF} = 28 GHz at −30 dBm.

		N × LO								
		0	1	2	3	4	5	6	7	8
M × RF	−2		85	87	87	82	86	103	96	59
	−1	61	90	54	46	0	45	52	106	82
	0	N/A	43	55	65		48	76	78	81
	+1	61	91	80	82					

f_{BB} = 100 MHz, LO= 9.725 GHz at 0 dBm, and f_{RF} = 39 GHz at −30 dBm.

		N × LO								
		0	1	2	3	4	5	6	7	8
M × RF	−2				85	88	87	92	87	60
	−1	63	92	56	47	0	51	61	85	84
	0	N/A	42	48	67	51	85			
	+1	42	48							

IF Mode

Measurements are made on the IF_I port. Data is taken without any 90° hybrid.

IF frequency (f_{IF}) = 3.5 GHz, LO= 6.125 GHz at 0 dBm, and f_{RF} = 28 GHz at −30 dBm.

		N × LO								
		0	1	2	3	4	5	6	7	8
M × RF	−2		81	93	85	93	93	99	96	白 醍
	−1	66	94	89	63	0	44	46	92	78
	0	N/A	45	43	65	54	71	64	80	58
	+1	66	84	84	81					

f_{IF} = 3.5 GHz, LO= 8.875 GHz at 0 dBm, and f_{RF} = 39 GHz at −30 dBm.

		N × LO								
		0	1	2	3	4	5	6	7	8
M × RF	−2					84	92	91	93	59
	−1	62	93	81	71	0	39	91	92	89
	0	N/A	47	68	75	50	75			
	+1	62	89							

f_{IF} = 3.5 GHz, LO= 7.875 GHz at 0 dBm, and f_{RF} = 28 GHz at −30 dBm.

		N × LO								
		0	1	2	3	4	5	6	7	8
M × RF	−2		90	86	83	95	94	83	89	58
	−1	70	93	70	41	0	65	90	89	83
	0	N/A	47	62	66	49	74	86		
	+1	70	90	88						

f_{IF} = 3.5 GHz, LO= 10.5 GHz at 0 dBm, and f_{RF} =39 GHz at −30 dBm

		N × LO								
		0	1	2	3	4	5	6	7	8
M × RF	−2				85	87	94	94	90	58
	−1	61	91	81	35	0	87	84	84	82
	0	N/A	39	51	62	53				
	+1	61	89							

THEORY OF OPERATION

The ADMV1014 is a wideband microwave downconverter optimized for microwave radio designs operating in the 24 GHz to 44 GHz frequency range. See Figure 1 for a functional block diagram of the device. The ADMV1014 digital settings are controlled via the SPI. The ADMV1014 has two modes of operation:

- Baseband quadrature demodulation (I/Q mode)
- Image reject I/Q downconversion (IF mode)

START-UP SEQUENCE

The ADMV1014 SPI settings require its default settings to be changed during startup for optimum performance. To use the SPI, toggle the RST pin to logic low and then logic high to perform a hard reset before starting up the device.

Set Register 0x0B to 0x727C after every power-up or reset. Set Register 0x03, Bits[13:12] to 11 after every power-up or reset.

BASEBAND QUADRATURE DEMODULATION (I/Q MODE)

In I/Q mode, the output impedance of the baseband I/Q ports is 100 Ω differential. These outputs are designed to be loaded to a dc-coupled, differential, 100 Ω load. I_P and I_N are the differential baseband I outputs. Q_P and Q_N are the differential baseband Q outputs.

To set the ADMV1014 in I/Q mode, set BB_AMP_PD (Register 0x03, Bit 8) to 0 and set IF_AMP_PD (Register 0x03, Bit 11) to 1.

The baseband I/Q ports are designed to operate from dc to 6.0 GHz at each I and Q channel.

The BB output V_{CM} can be changed from 1.05 V to 1.85 V. To change the V_{CM}, set BB_SWITCH_HIGH_LOW_COMMMON (Register 0x0A, Bit 0) to be the opposite of Register 0x0A, Bit 6. Also, set the MIXER_VGATE bit field (Register 0x07, Bits[15:9]) and the BB_AMP_REF_GEN bit field (Register 0x0A, Bits[6:3]) based on Table 6.

Table 6 provides the correct setting for these bit fields vs. the required common-mode voltage.

The V_{CM} can be further adjusted on each I or Q channel by ±15 mV by setting the BB_AMP_OFFSET_I bit field (Register 0x09, Bits[4:0]) and the BB_AMP_OFFSET_Q bit field (Register 0x09, Bits[9:5]) for each V_{CM} setting shown in Table 6.

The most significant bit (MSB) for each bit field is the sign bit. When the MSB is 1, the values of the four lower bits are positive. When the MSB is 0, the values of the four lower bits are negative. These bits also offer input IP2 and common-mode rejection optimization.

The BB I/Q section of the ADMV1014 also features a baseband amplifier with a digital attenuator that is controlled by setting the BB_AMP_GAIN_CTRL bit field (Register 0x0A, Bits[2:1]). Figure 44, Figure 45, and Figure 46 show the performance of the baseband digital attenuator.

The Baseband Quadrature Demodulation to Very Low Frequencies section shows the baseband performance to very low demodulation frequencies.

Table 6. Common-Mode Voltage Settings

V_{CM} (V)	MIXER_VGATE (Register 0x07, Bits[15:9])	BB_AMP_REF_GEN (Register 0x0A, Bits[6:3])	BB_SWITCH_HIGH_LOW_COMMON_MODE (Register 0x0A, Bit 0)
1.05	1101010	0000	1
1.10	1101011	0001	1
1.15	1101100	0010	1
1.20	1101110	0011	1
1.25	1101111	0100	1
1.30	1110000	0101	1
1.35	1110001	0110	1
1.40	1110010	0111	1
1.50	1110101	1000	0
1.55	1110110	1001	0
1.60	1110111	1010	0
1.65	1111000	1011	0
1.70	1111010	1100	0
1.75	1111011	1101	0
1.80	0101100	1110	0
1.85	0101101	1111	0

IMAGE REJECTION DOWNCONVERSION

The ADMV1014 features the ability to downconvert to a real IF output anywhere from 800 MHz to 6000 MHz, while suppressing the unwanted image sideband by typically better than 30 dBc. The IF outputs are quadrature to each other, 50 Ω single-ended, and are internally ac coupled. IF_I and IF_Q are the quadrature IF outputs. An external 90° hybrid is required to select the appropriate sideband.

To configure the ADMV1014 in IF mode, set BB_AMP_PD (Register 0x03, Bit 8) to 1 and set IF_AMP_PD (Register 0x03, Bit 11) to 0

Each IF output features an amplifier with a digital attenuator. The digital attenuator can be adjusted using fine or coarse steps. The coarse steps for the IF_I can be adjusted using the IF_AMP_COARSE_GAIN_I bit field (Register 0x08, Bits[11:8]). The coarse steps for the IF_Q can be adjusted using the IF_AMP_COARSE_GAIN_Q bit field (Register 0x09, Bits[15:12]). Each course gain bit field has five settings. The fine steps for IF_I can be adjusted using the IF_AMP_FINE_GAIN_I bit field (Register 0x08, Bits[3:0]). The fine steps for the IF_Q can be adjusted using the IF_AMP_FINE_GAIN_Q bit field (Register 0x08, Bits[7:4]). Figure 77 to Figure 82 show the performance of these four bit fields.

DETECTOR

The ADMV1014 features a square law detector that produces a voltage linearly, according to the square of the RF voltage output from the low noise amplifier. The detector can be enabled by setting the DET_EN bit (Register 0x03, Bit 6) to 0. The detector can be turned off by setting this bit to 1. The detector linear range can be adjusted by setting the DET_PROG bit field (Register 0x07, Bits[6:0]). These ranges are specified based on the input power into the detector coming from the output of the low noise amplifier. Each DET_PROG setting offers an approximate 20 dB of ±1 dB dynamic range based on a two-point linear regression from an ideal line for one temperature at each DET_PROG setting. See Figure 89 to Figure 91 for more performance information of the detector.

LO INPUT PATH

The LO input path operates from 5.4 GHz to 10.25 GHz with an LO amplitude range of −6 dBm to +6 dBm. The LO has an internal quadrupler (×4) and a programmable band-pass filter. The LO band-pass filter is programmable using QUAD_FILTERS (Register 0x04 Bits[3:0]). See the Performance at Different Quad Filter Settings section for more information on the QUAD_FILTERS settings.

The LO path can operate either differentially or single-ended (SE). LOIP and LOIN are the inputs to the LO path. The LO

path can switch from differential to single-ended operation by setting the QUAD_SE_MODE bits (Register 0x04, Bits[9:6]). See the Performance Between Differential vs. Single-Ended LO Input section for more information.

Figure 102 shows a block diagram of the LO path.
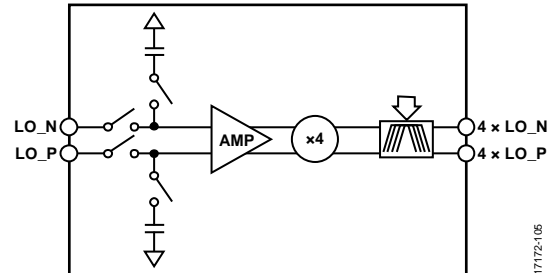
Figure 102. LO Path Block Diagram

Enable the quadrupler by setting the QUAD_IBIAS_PD bit (Register 0x03, Bit 7) to 0 and the QUAD_BG_PD bit (Register 0x03, Bit 9) to 0. To power down the quadrupler, set both of these bits to 1.

An unwanted image can be downconverted from the quadrature error in generating the quadrature LO signals. Deviation from ideal quadrature (that is, total image rejection and no image tone is downconverted) on these signals limits the amount of achievable image rejection.

The ADMV1014 offers about 25° of quadrature phase adjustment in the LO path quadrature signals. Make these adjustments through the LOAMP_PH_ADJ_I_FINE bits (Register 0x05, Bits[15:9]) and the LOAMP_PH_ADJ_Q_FINE (Register 0x05, Bits[8:2]) bits. These bits reject the unwanted sideband signal. In IF mode amplitude adjustments can be made to the complex outputs via IF_AMP_FINE_GAIN_Q (Register 0x08, Bits[7:4]) and IF_AMP_FINE_GAIN_I (Register 0x08, Bits[3:0]) to further reduce the unwanted sideband.

POWER-DOWN

The SPI of the ADMV1014 allows the user to power down device circuits and reduce power consumption. There are two power-down modes: band gap power-down mode (BG_PD) and individual power-down circuits mode. The BG_PD bit (Register 0x03, Bit 5) and the QUAD_BG_PD bit (Register 0x03, Bit 9) power down the band gap circuit. The QUAD_IBIAS_PD bit (Register 0x03, Bit 7) and the IBIAS_PD bit (Register 0x03, Bit 14) power down the specific circuits.

Table 7 shows the circuits that are controlled by their related power-down bit, the typical power savings, and the latency requirement to power the circuits back up.

Table 7. Power-Down Power and Latency Requirements

Bit Name	Circuit	Typical Power Savings (mW)	Power-Up Latency (µs)	Power-Down Latency (µs)
IBIAS_PD	Receiver bias current (I$_{BIAS}$)	1172	5	<1
QUAD_IBIAS_PD	LO path	238	4	<1
BG_PD and QUAD_BG_PD	Band gap	1423	4.5	<1
IBIAS_PD, IF_AMP_PD, QUAD_BG_PD, BB_AMP_PD, QUAD_IBIAS_PD, BG_PD	Entire chip	1435	5	<1
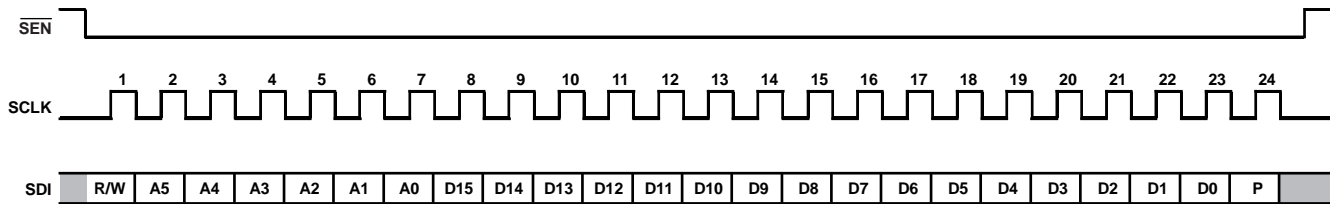
Figure 103. Write Serial Port Timing Diagram
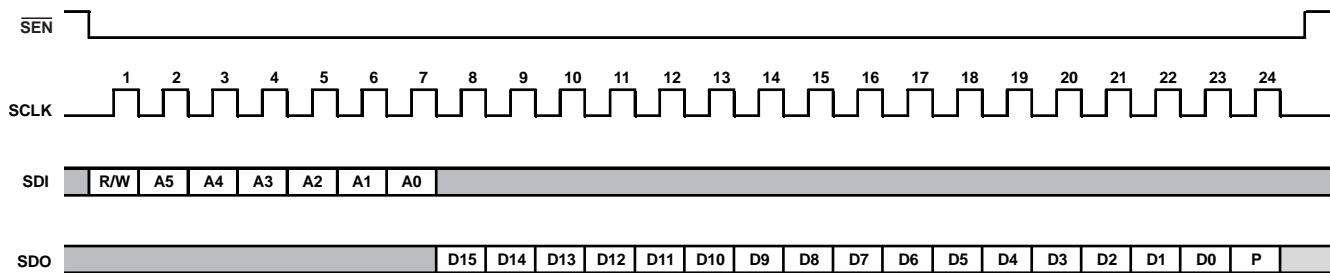
Figure 104. Read Serial Port Timing Diagram

SERIAL PORT INTERFACE (SPI)

The SPI of the ADMV1014 allows the user to configure the device for specific functions or operations via a 4-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of four control lines: SCLK, SDIN, SDO, and SEN.

The ADMV1014 protocol consists of a write/read bit followed by six register address bits, 16 data bits, and a parity bit. Both the address and data fields are organized most significant bit (MSB) first and end with the least significant bit. For a write, set the first bit to 0. For a read, set the first bit to 1.

The write cycle sampling must be performed on the rising edge. The 16 bits of the serial write data are shifted in, MSB to Lower

Sideband. The ADMV1014 input logic level for the write cycle supports an 1.8 V interface.

For a read cycle, up to 16 bits of serial read data are shifted out, MSB first. After the 16 bits of data shift out, the parity bit shifts out. The output logic level for a read cycle is 1.8 V.

The parity bit always follows the direction of the data. If parity is not used, the transmitting end transmits zero instead of parity. The parity is odd, which means that the total number of ones transmitted during a command, including the read/write bit, the address bit, the data bit, and the parity bit, must be odd.

Figure 103 and Figure 104 show the SPI write and read protocol, respectively.

APPLICATIONS INFORMATION

ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

Figure 105 shows the EVM vs. input power performance of the ADMV1014 in IF mode at maximum gain, upper sideband, 25°C and 0 dBm LO input power. The EVM measurement was performed using four 100 MHz, 5G-NR, 256QAM waveforms. The EVM shown is the average of the four channels. The EVM of the test equipment was not de-embedded.

Figure 106 shows the constellation diagram and EVM statistics of each of the four channels at −30 dBm input power.
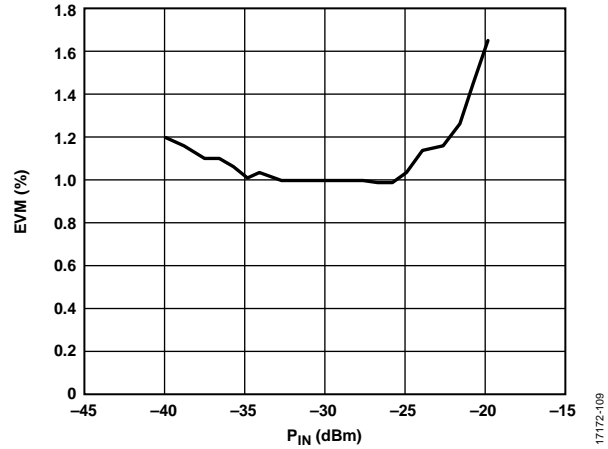
Figure 105. EVM vs. Input Power at 28 GHz, VCTRL = 0 V, T_A = 25°C, LO = 0 dBm, Upper Sideband (Low-Side LO), IF = 3.5 GHz
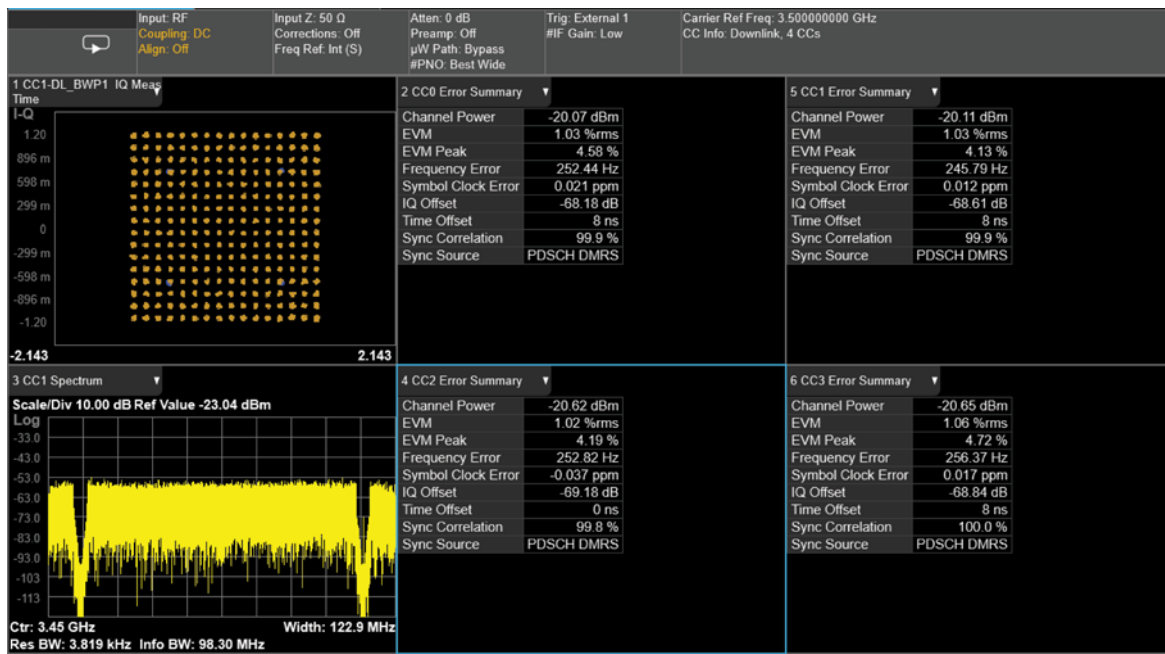
Figure 106. Constellation Diagram and EVM Statistics per Channel

BASEBAND QUADRATURE DEMODULATION TO VERY LOW FREQUENCIES

Figure 107 to Figure 111 show the I/Q mode performance at low baseband frequencies. The measurements were performed at 28 GHz, −25 dBm input power, V_{CM} = 1.15 V, Register 0x03, Bit 11 = 1, Register 0x03, Bit 8 = 0, 6 dBm LO input power, and T_A = 25°C.
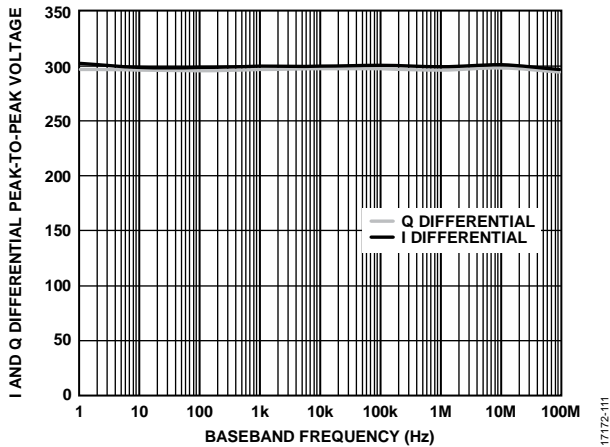
Figure 107. I and Q Differential Peak-to-Peak Voltage vs. Baseband Frequency
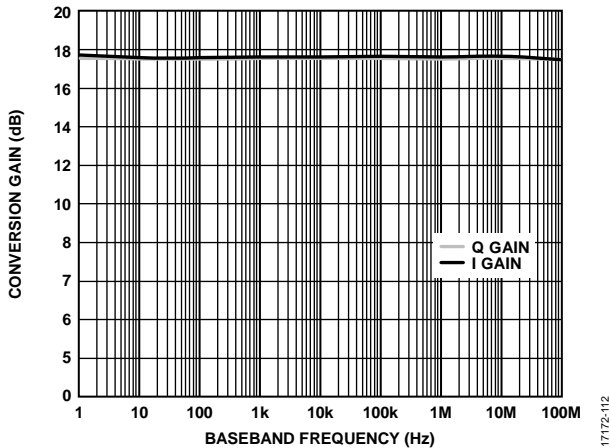
Figure 108. Conversion Gain vs. Baseband Frequency
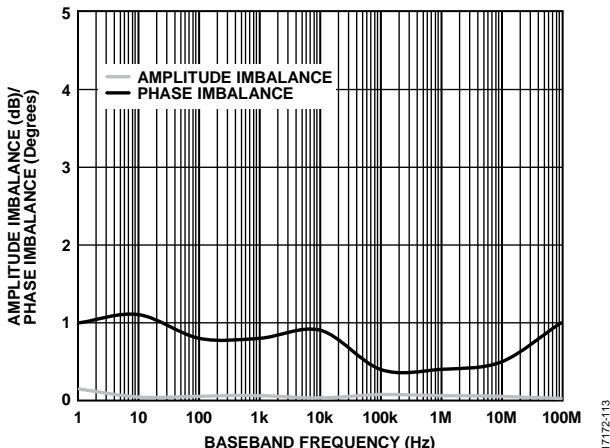
Figure 109. Amplitude Imbalance and Phase Imbalance vs. Baseband Frequency
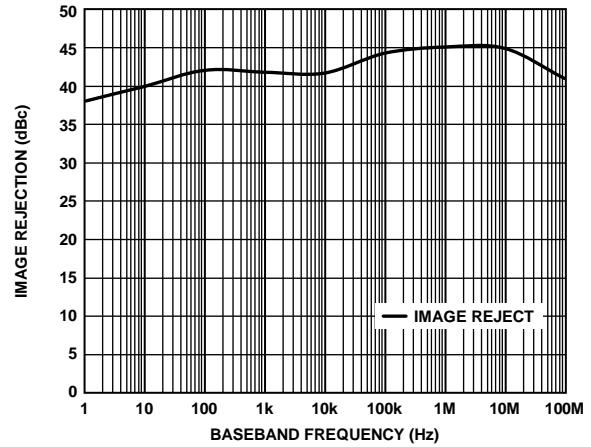
Figure 110. Image Rejection vs. Baseband Frequency
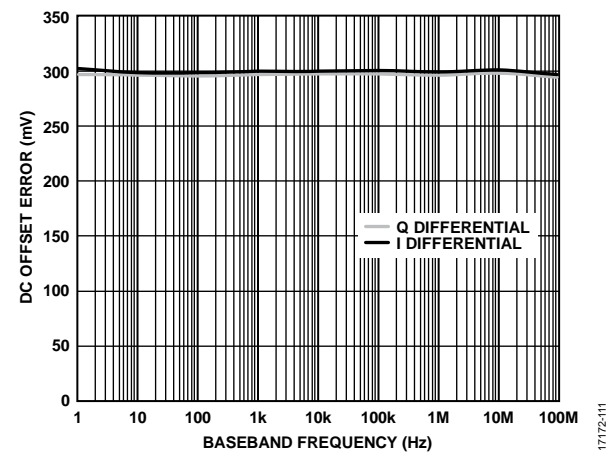
Figure 111. DC Offset Error vs. Baseband Frequency

PERFORMANCE AT DIFFERENT QUAD FILTER SETTINGS

Figure 112 shows the conversion gain vs. RF frequency in IF mode at 25°C and LO input power = 6 dBm, for different QUAD_FILTERS settings. Figure 113 shows the LO to IF_I and LO to IF_Q leakage vs. LO frequency at different quad filter settings.
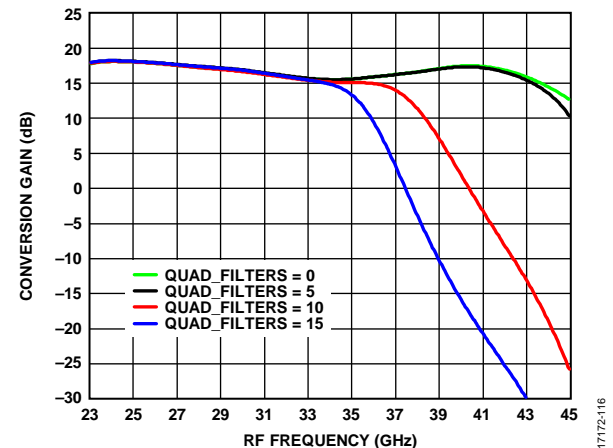
Figure 112. Conversion Gain vs. RF Frequency for Four Different QUAD_FILTERS Settings, f_{IF} = 3.5 GHz (Upper Sideband)
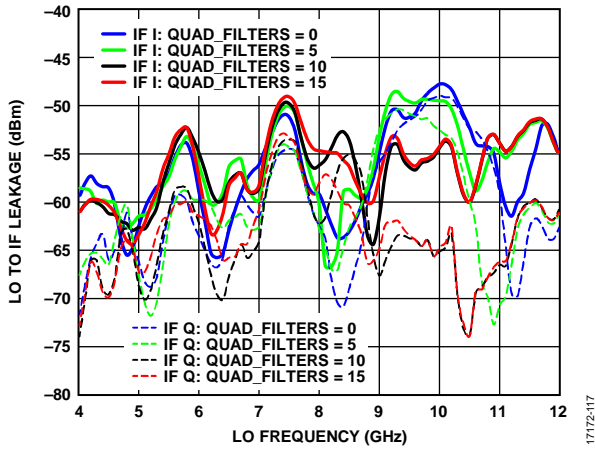
Figure 113. LO To IF Leakage vs. RF Frequency for Four Different QUAD_FILTERS Settings, f_IF = 3.5 GHz (Upper Sideband)

VVA TEMPERATURE COMPENSATION

Figure 114 shows the conversion gain vs. RF frequency at two different Register 0x0B settings and three different temperatures for IF mode. The recommended value suggested in the Start-Up Sequence section provides the highest conversion gain. If the priority is to decrease the conversion gain variation across temperature, Register 0x0B can be set to 0x726C. However, at this value, the conversion gain is lower at each temperature.
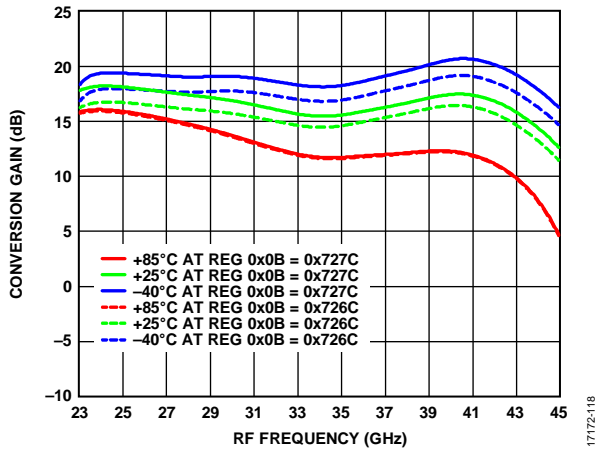
Figure 114. Conversion Gain vs. RF Frequency at Maximum Gain for Various Register 0x0B Settings and Various Temperatures

PERFORMANCE BETWEEN DIFFERENTIAL vs. SINGLE-ENDED LO INPUT

Figure 115 to Figure 117 show the conversion gain, input IP3 and image rejection performance for operating the ADMV1014 LO input as differential vs. SE. The measurements were performed with 0 dBm LO input power, IF mode, with an IF frequency of 3.5 GHz, upper sideband, and $T_A = 25°C$.
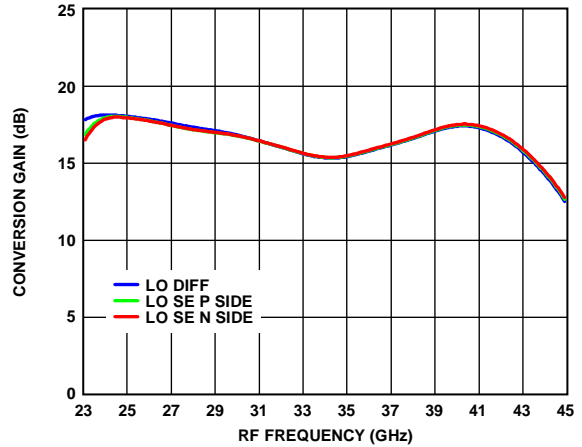
Figure 115. Conversion Gain vs. RF Frequency for Three Different LO Mode Settings, f_IF = 3.5 GHz (Upper Sideband)
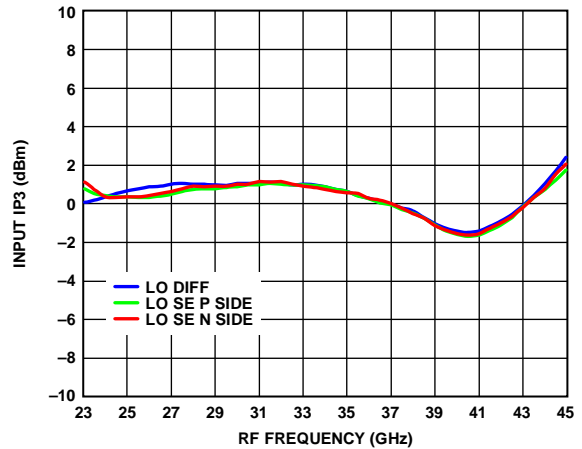
Figure 116. Input IP3 vs. RF Frequency for Three Different LO Mode Settings, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_IF = 3.5 GHz (Upper Sideband)
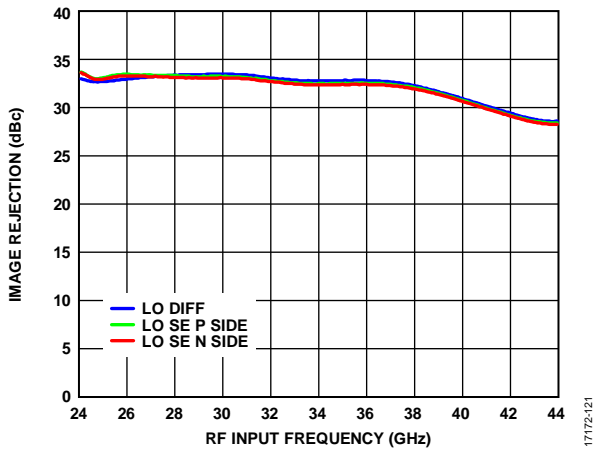
Figure 117. Image Rejection vs. RF Input Frequency for Three Different LO Mode Settings, RF Amplitude = −30 dBm per Tone at 20 MHz Spacing, f_{IF} = 3.5 GHz (Upper Sideband)

PERFORMANCE ACROSS RF FREQUENCY AT FIXED IF AND BASEBAND FREQUENCIES

The ADMV1014 quadrupler operates from 21.6 GHz to 41 GHz. When using high-side LO injection, the conversion gain starts rolling off gradually after the quadrupler frequency reaches 41 GHz. When using low-side LO, the conversion gain starts rolling off when the quadrupler frequency is 21.6 GHz.

Figure 118 and Figure 119 show the conversion gain vs. RF frequency in IF mode for fixed IF frequencies (T_A = 25°C, LO = 6 dBm) for upper sideband and lower sideband, respectively. Figure 120 and Figure 121 show the conversion gain vs. RF frequency in IQ mode for fixed BB frequencies (T_A = 25°C, LO = 6 dBm) for upper sideband and lower sideband, respectively.
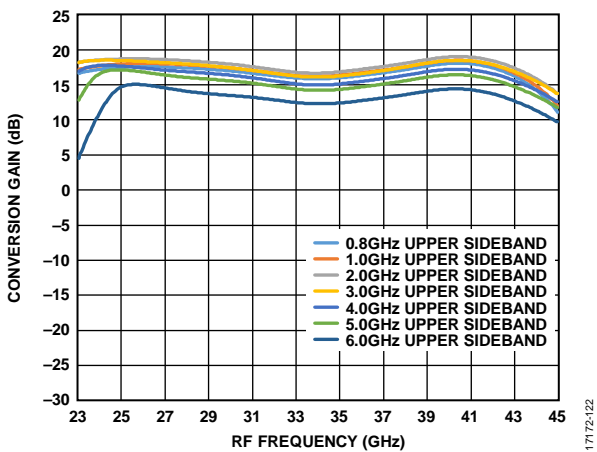
Figure 118. Conversion Gain vs. RF Frequency for Multiple IF Frequency Settings (Upper Sideband)
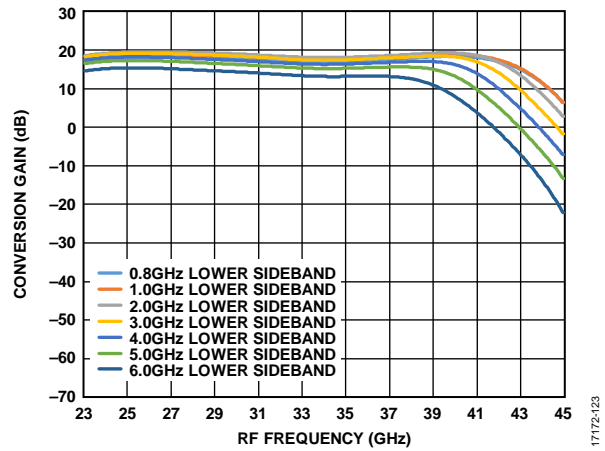
Figure 119. Conversion Gain vs. RF Frequency at Multiple IF Frequency Settings (Lower Sideband)
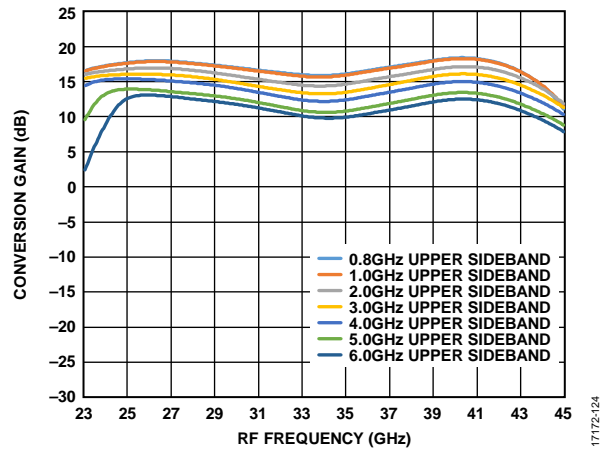
Figure 120. Conversion Gain vs. RF Frequency at Multiple I/Q Frequency Settings (Upper Sideband)
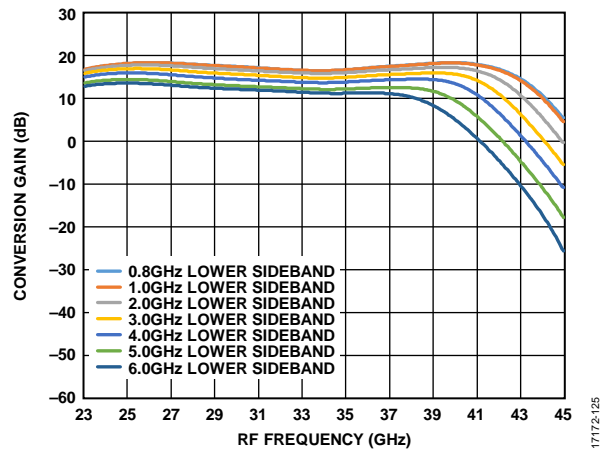
Figure 121. Conversion Gain vs. RF Frequency at Multiple IQ Frequency Settings (Lower Sideband)

RECOMMENDED LAND PATTERN

Solder the exposed pad on the underside of the ADMV1014 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package.
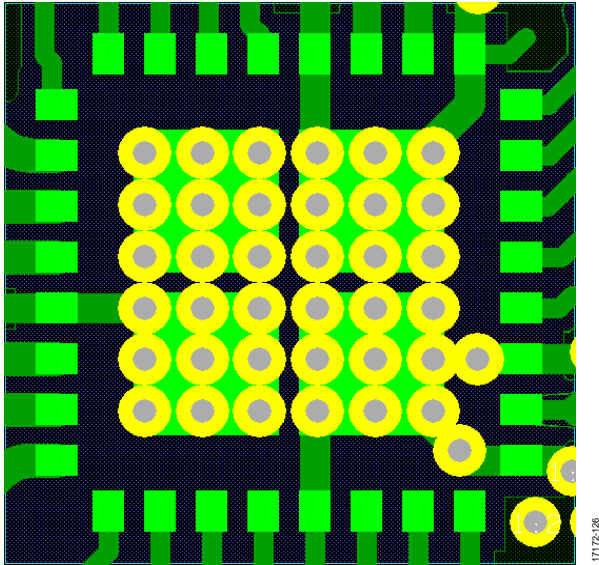
Figure 122. Evaluation Board Layout for the LGA package

EVALUATION BOARD INFORMATION

For more information about the ADMV1014 evaluation board, refer to the ADMV1014-EVALZ user guide.

REGISTER SUMMARY

Table 8. Register Summary

Reg.	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W
0x00	SPI_CONTROL	[15:8]	PARITY_EN	SPI_SOFT_RESET	RESERVED		CHIP_ID[7:4]				0x0093	R/W
		[7:0]	CHIP_ID[3:0]				REVISION					
0x01	ALARM	[15:8]	PARITY_ERROR	TOO_FEW_ERRORS	TOO_MANY_ERRORS	ADDRESS_RANGE_ERROR	RESERVED				0x0000	R
		[7:0]	RESERVED									
0x02	ALARM_MASKS	[15:8]	PARITY_ERROR_MASK	TOO_FEW_ERRORS_MASK	TOO_MANY_ERRORS_MASK	ADDRESS_RANGE_ERROR_MASK	RESERVED				0xFFFF	R/W
		[7:0]	RESERVED									
0x03	ENABLE	[15:8]	RESERVED	IBIAS_PD	P1DB_COMPENSATION		IF_AMP_PD	RESERVED	QUAD_BG_PD	BB_AMP_PD	0x0157	R/W
		[7:0]	QUAD_IBIAS_PD	DET_EN	BG_PD	RESERVED						
0x04	QUAD	[15:8]	RESERVED						QUAD_SE_MODE[3:2]		0x5700	R/W
		[7:0]	QUAD_SE_MODE[1:0]		RESERVED		QUAD_FILTERS					
0x05	LO_AMP_PHASE_ADJUST1	[15:8]	LOAMP_PH_ADJ_I_FINE							LOAMP_PH_ADJ_Q_FINE[6]	0x4101	R/W
		[7:0]	LOAMP_PH_ADJ_Q_FINE[5:0]						RESERVED			
0x07	MIXER	[15:8]	MIXER_VGATE							RESERVED	0xD808	R/W
		[7:0]	RESERVED		DET_PROG							
0x08	IF_AMP	[15:8]	RESERVED				IF_AMP_COARSE_GAIN_I				0x0000	R/W
		[7:0]	IF_AMP_FINE_GAIN_Q				IF_AMP_FINE_GAIN_I					
0x09	IF_AMP_BB_AMP	[15:8]	IF_AMP_COARSE_GAIN_Q				RESERVED		BB_AMP_OFFSET_Q[4:3]		0x0000	R/W
		[7:0]	BB_AMP_OFFSET_Q[2:0]			BB_AMP_OFFSET_I						
0x0A	BB_AMP__AGC	[15:8]	RESERVED								0x2390	R/W
		[7:0]	RESERVED	BB_AMP_REF_GEN			BB_AMP_GAIN_CTRL			BB_SWITCH_HIGH_LOW_COMMON_MODE		
0x0B	VVA_TEMP_COMP	[15:8]	VVA_TEMPERATURE_COMPENSATION[15:8]								0x4A5C	R/W
		[7:0]	VVA_TEMPERATURE_COMPENSATION[7:0]									

REGISTER DETAILS

Address: 0x00, Reset: 0x0093, Name: SPI_CONTROL
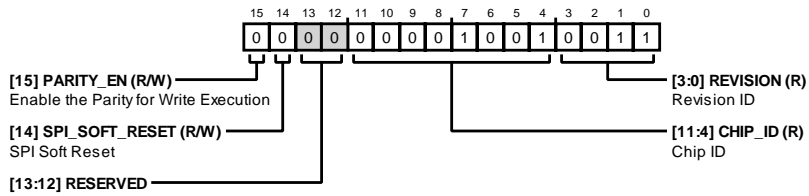
Table 9. Bit Descriptions for SPI_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
15	PARITY_EN		Enable the Parity for Write Execution	0x0	R/W
14	SPI_SOFT_RESET		SPI Soft Reset	0x0	R/W
[13:12]	RESERVED		Reserved	0x0	R
[11:4]	CHIP_ID		Chip ID	0x9	R
[3:0]	REVISION		Revision ID	0x3	R

Address: 0x01, Reset: 0x0000, Name: ALARM
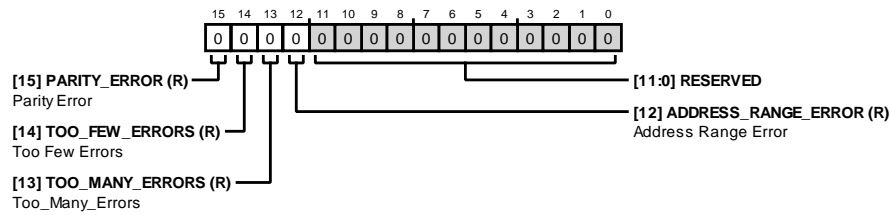
Table 10. Bit Descriptions for ALARM

Bits	Bit Name	Settings	Description	Reset	Access
15	PARITY_ERROR		Parity Error	0x0	R
14	TOO_FEW_ERRORS		Too Few Errors	0x0	R
13	TOO_MANY_ERRORS		Too Many Errors	0x0	R
12	ADDRESS_RANGE_ERROR		Address Range Error	0x0	R
[11:0]	RESERVED		Reserved	0x0	R

Address: 0x02, Reset: 0xFFFF, Name: ALARM_MASKS
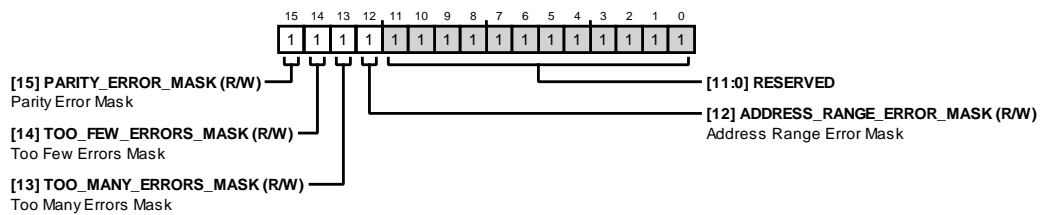
Table 11. Bit Descriptions for ALARM_MASKS

Bits	Bit Name	Settings	Description	Reset	Access
15	PARITY_ERROR_MASK		Parity Error Mask	0x1	R/W
14	TOO_FEW_ERRORS_MASK		Too Few Errors Mask	0x1	R/W
13	TOO_MANY_ERRORS_MASK		Too Many Errors Mask	0x1	R/W
12	ADDRESS_RANGE_ERROR_MASK		Address Range Error Mask	0x1	R/W
[11:0]	RESERVED		Reserved	0xFFF	R

Address: 0x03, Reset: 0x0157, Name: ENABLE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	1

[15] RESERVED

[14] IBIAS_PD (R/W)
Power Down the RX Ibias

[13:12] P1DB_COMPENSATION (R/W)
Turn on bits to optimize P1dB

[11] IF_AMP_PD (R/W)
Power Down the IF Amp

[10] RESERVED

[9] QUAD_BG_PD (R/W)
Power Down the Quadrupler BandGap

[4:0] RESERVED

[5] BG_PD (R/W)
Power Down the RX BG

[6] DET_EN (R/W)
Digital RX Detector Enable

[7] QUAD_IBIAS_PD (R/W)
Power Down the Quadrupler Bias Current.

[8] BB_AMP_PD (R/W)
Power Down the Base-Band Amp

Table 12. Bit Descriptions for ENABLE

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Reserved	0x0	R
14	IBIAS_PD		Power Down the Rx I_{BIAS}	0x0	R/W
[13:12]	P1DB_COMPENSATION		Turn on bits to optimize P1dB	0x0	R/W
11	IF_AMP_PD		Power Down the IF Amp	0x0	R/W
10	RESERVED		Reserved	0x0	R
9	QUAD_BG_PD		Power Down the Quadrupler Band Gap	0x0	R/W
8	BB_AMP_PD		Power Down the Baseband Amp	0x1	R/W
7	QUAD_IBIAS_PD		Power Down the Quadrupler Bias Current	0x0	R/W
6	DET_EN		Digital Rx Detector Enable	0x1	R/W
5	BG_PD		Power Down the Rx BG	0x0	R/W
[4:0]	RESERVED		Reserved	0x1	R

Address: 0x04, Reset: 0x5700, Name: QUAD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0

[15:10] RESERVED

[9:6] QUAD_SE_MODE (R/W)
Switch Differential/SE Modes
0110: SE_Mode_N_Side.
1001: SE_Mode_P_Side.
1100: Differential Mode.

[3:0] QUAD_FILTERS (R/W)
LO Filters BW Selection
0000: LO Frequency BW: 8.625 to 10.25GHz.
0101: LO Frequency BW: 6.6 to 9.2GHz.
1010: LO Frequency BW: 5.4 to 8GHz.
1111: LO Frequency BW: 5.4 to 7GHz.
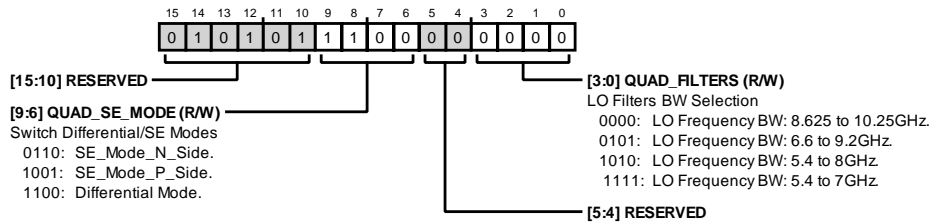
[5:4] RESERVED

Table 13. Bit Descriptions for QUAD

Bits	Bit Name	Settings	Description	Reset	Access
[15:10]	RESERVED		Reserved	0x15	R
[9:6]	QUAD_SE_MODE		Switch Differential/SE Modes	0xC	R/W
		0110	SE Mode N Side		
		1001	SE Mode P Side		
		1100	Differential Mode		
[5:4]	RESERVED		Reserved.	0x0	R
[3:0]	QUAD_FILTERS		LO Filters BW Selection	0x0	R/W
		0000	LO Frequency BW: 8.625 GHz to 10.25 GHz		
		0101	LO Frequency BW: 6.6 GHz to 9.2 GHz		
		1010	LO Frequency BW: 5.4 GHz to 8 GHz		
		1111	LO Frequency BW: 5.4 GHz to 7 GHz		

Address: 0x05, Reset: 0x4101, Name: LO_AMP_PHASE_ADJUST1

[15:9] LOAMP_PH_ADJ_I_FINE (R/W)
Mixer Image Rejection Calibration
0x00:Maximum Phase, 0x7F: Minimum
Phase

[8:2] LOAMP_PH_ADJ_Q_FINE (R/W)
Mixer Image Rejection Calibration
0x00:Maximum Phase, 0x7F: Minimum
Phase

[1:0] RESERVED
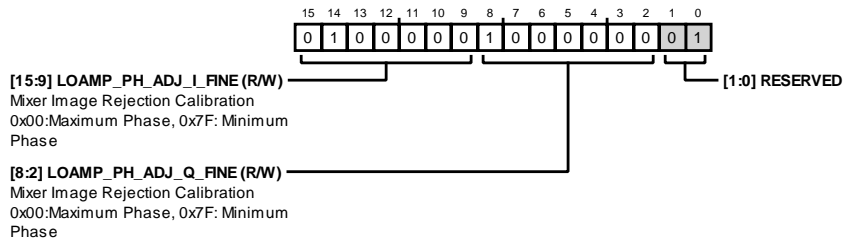
Table 14. Bit Descriptions for LO_AMP_PHASE_ADJUST1

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	LOAMP_PH_ADJ_I_FINE		Mixer Image Rejection Calibration 0x00: Maximum Phase, 0x7F: Minimum Phase	0x20	R/W
[8:2]	LOAMP_PH_ADJ_Q_FINE		Mixer Image Rejection Calibration 0x0: Maximum Phase, 0x7F: Minimum Phase	0x40	R/W
[1:0]	RESERVED		Reserved.	0x1	R

Address: 0x07, Reset: 0xD808, Name: MIXER

[15:9] MIXER_VGATE (R/W)
Control BB Common Mode Voltage
(Please see the application section
for more Information)

[8:7] RESERVED

[6:0] DET_PROG (R/W)
Digital RX Detector Program
0: From -12 to +4dBm.
1: From -13 to +3dBm.
10: From -14 to +2dBm.
100: From -15 to +1dBm.
1000: From -15.5 to +0.5dBm.
10000: From -16.25 to -0.25dBm.
100000: From -17 to -1dBm.
1000000: From -18 to -2dBm.
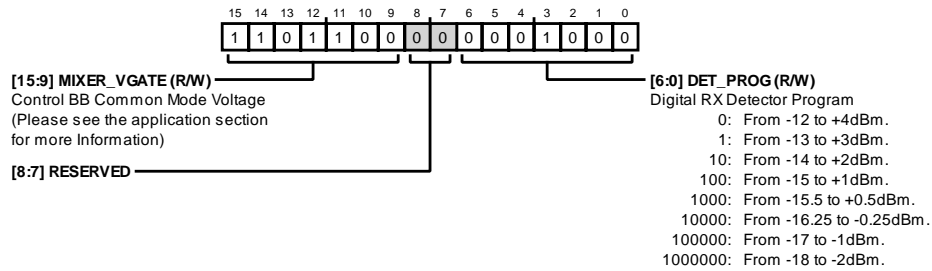
Table 15. Bit Descriptions for MIXER

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	MIXER_VGATE		Control BB Common Mode Voltage. See the Applications Information section for more information)	0x6C	R/W
[8:7]	RESERVED		Reserved.	0x0	R
[6:0]	DET_PROG		Digital Rx Detector Program.	0x8	R/W
		0	From −12 dBm to +4 dBm.		
		1	From −13 dBm to +3 dBm.		
		10	From −14 dBm to +2 dBm.		
		100	From −15 dBm to +1 dBm.		
		1000	From −15.5 dBm to +0.5 dBm.		
		10000	From −16.25 dBm to −0.25 dBm.		
		100000	From −17 dBm to −1 dBm.		
		1000000	From −18 dBm to −2 dBm.		

Address: 0x08, Reset: 0x0000, Name: IF_AMP

[15:12] RESERVED

[11:8] IF_AMP_COARSE_GAIN_I (R/W)
Digital IF Amp 1dB Step Gain_I
0: Refer to Figure 77 to Figure 79.
1: Refer to Figure 77 to Figure 79.
11: Refer to Figure 77 to Figure 79.
111: Refer to Figure 77 to Figure 79.
1111: Refer to Figure 77 to Figure 79.

[3:0] IF_AMP_FINE_GAIN_I (R/W)
IF Amp I, 10 Fine Steps from 0x0 to
0xA (Total attenuation ~1dB). Refer
to Figure 80 to Figure 82.

[7:4] IF_AMP_FINE_GAIN_Q (R/W)
IF Amp Q, 10 Fine Steps from 0x0
to 0xA (Total attenuation ~1dB). Refer
to Figure 80 to Figure 82.

Table 16. Bit Descriptions for IF_AMP

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Reserved.	0x0	R
[11:8]	IF_AMP_COARSE_GAIN_I		Digital IF Amp Step Gain I.	0x0	R/W
		0	Refer to Figure 77 to Figure 79.		
		1	Refer to Figure 77 to Figure 79.		
		11	Refer to Figure 77 to Figure 79.		
		111	Refer to Figure 77 to Figure 79.		
		1111	Refer to Figure 77 to Figure 79.		
[7:4]	IF_AMP_FINE_GAIN_Q		IF Amp Q, 10 Fine Steps from 0x0 to 0xA. Refer to Figure 80 to Figure 82.	0x0	R/W
[3:0]	IF_AMP_FINE_GAIN_I		IF Amp I, 10 Fine Steps from 0x0 to 0xA. Refer to Figure 80 to Figure 82.	0x0	R/W

Address: 0x9, Reset: 0x0000, Name: IF_AMP__BB_AMP

[15:12] IF_AMP_COARSE_GAIN_Q (R/W)
Digital IF Amp 1dB Step Gain_Q
0: Refer to Figure 77 to Figure 79.
1: Refer to Figure 77 to Figure 79.
11: Refer to Figure 77 to Figure 79.
111: Refer to Figure 77 to Figure 79.
1111: Refer to Figure 77 to Figure 79.

[11:10] RESERVED

[4:0] BB_AMP_OFFSET_I (R/W)
BB Amp I. Bit 4: Use as Sign Bit, b'1
is for positive values and b'0 is for
negative values; Bits [3:0] Minimum
Offset, 0xF: Maximum Offset.

[9:5] BB_AMP_OFFSET_Q (R/W)
BB Amp Q. Bit 9: Use as Sign Bit,
b'1is for positive values and b'0 is
for negative values; Bit [8:5] Minimum
Offset, 0xF: Maximum Offset.

Table 17. Bit Descriptions for IF_AMP__BB_AMP

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	IF_AMP_COARSE_GAIN_Q		Digital IF Amp 1 dB Step Gain Q	0x0	R/W
		0	Refer to Figure 77 to Figure 79		
		1	Refer to Figure 77 to Figure 79		
		11	Refer to Figure 77 to Figure 79		
		111	Refer to Figure 77 to Figure 79		
		1111	Refer to Figure 77 to Figure 79		
[11:10]	RESERVED		Reserved.	0x0	R
[9:5]	BB_AMP_OFFSET_Q		BB Amp Q (Bit 9: Use as Sign Bit, 1 is for positive values and 0 is for negative values; Bits[8:5]: Minimum Offset, 0xF: Maximum Offset)	0x0	R/W
[4:0]	BB_AMP_OFFSET_I		BB Amp I (Bit 4: Use as Sign Bit, 1 is for positive values and 0 is for negative values; Bits[3:0]: Minimum Offset, 0xF: Maximum Offset)	0x0	R/W

Address: 0x0A, Reset: 0x2390, Name: BB_AMP_AGC

```
15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0
 0   0   1   0   0   0   1   1   1   0   0   1   0   0   0   0
```

[15:7] RESERVED

[6:3] BB_AMP_REF_GEN (R/W)
Control BB Common Mode Voltage
See the Baseband Quadrature Demodulation
(I/Q Mode) section for more information.

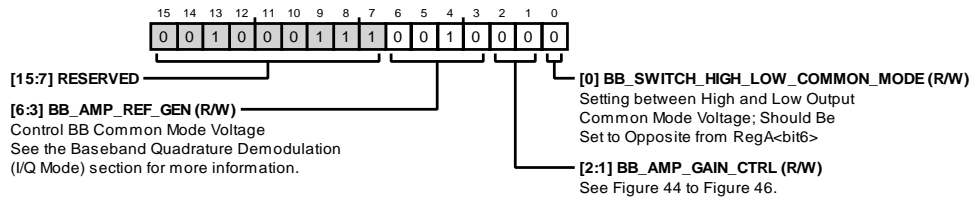[0] BB_SWITCH_HIGH_LOW_COMMON_MODE (R/W)
Setting between High and Low Output
Common Mode Voltage; Should Be
Set to Opposite from RegA<bit6>

[2:1] BB_AMP_GAIN_CTRL (R/W)
See Figure 44 to Figure 46.

Table 18. Bit Descriptions for BB_AMP_AGC

Bits	Bit Name	Settings	Description	Reset	Access
[15:7]	RESERVED		Reserved.	0x4	R
[6:3]	BB_AMP_REF_GEN		Control BB Common-Mode Voltage. See the Baseband Quadrature Demodulation (I/Q Mode) section for more information.	0x2	R/W
[2:1]	BB_AMP_GAIN_CTRL		See Figure 44 to Figure 46.	0x0	R/W
0	BB_SWITCH_HIGH_LOW_COMMON_MODE		Setting between High and Low Output Common-Mode Voltage. This bit must be set to opposite from Register 0x0A, Bit 6. See the Baseband Quadrature Demodulation (I/Q Mode) section for more information.	0x0	R/W

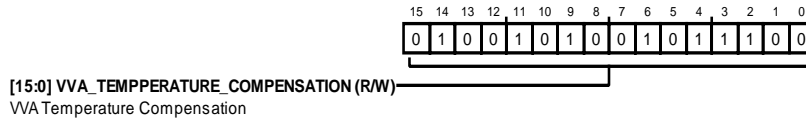**Address: 0x0B, Reset: 0x4A5C, Name: VVA_TEMP_COMP**

```
15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0
 0   1   0   0   1   0   1   0   0   1   0   1   1   1   0   0
```

[15:0] VVA_TEMPPERATURE_COMPENSATION (R/W)
VVA Temperature Compensation

Table 19. Bit Descriptions for VVA_TEMP_COMP

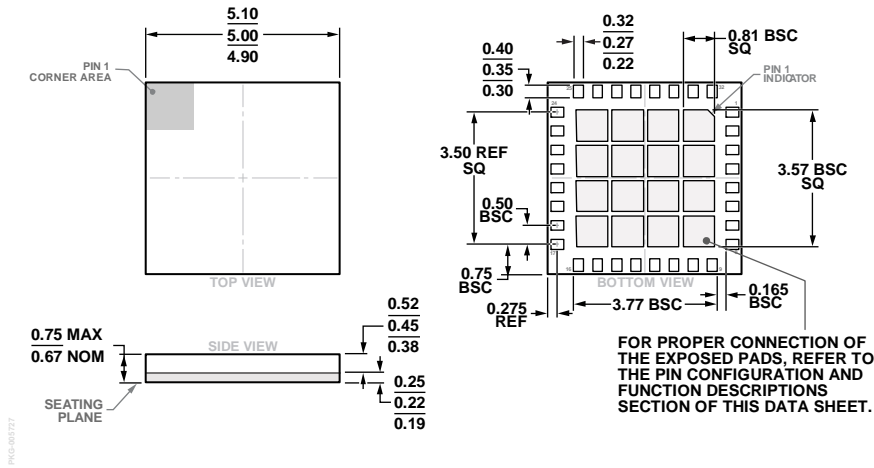| Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	VVA_TEMPERATURE_COMPENSATION		VVA Temperature Compensation. Set to 0x727C. See the Start-Up Sequence section and the VVA Temperature Compensation section for more information. Disable PARITY_EN when updating the VVA temperature compensation.	0x4A5C	R/W

OUTLINE DIMENSIONS

Figure 123. 32-Terminal Land Grid Array [LGA]
(CC-32-6)
Dimensions shown in millimeters

FOR PROPER CONNECTION OF THE EXPOSED PADS, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADMV1014ACCZ	−40°C to +85°C	32-Terminal Land Grid Array Package [LGA]	CC-32-6
ADMV1014ACCZ-R7	−40°C to +85°C	32-Terminal Land Grid Array Package [LGA]	CC-32-6
ADMV1014-EVALZ		Evaluation Board	

[1] Z = RoHS-Compliant Part.

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