AD9543 Register Map Reference Manual

UG-1167

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Register Map Reference Manual for the AD9543

INTRODUCTION

This reference manual contains the complete register map and details for the AD9543, used in conjunction with the AD9543 data sheet.

The AD9543 has five differential outputs, and the user can reconfigure each differential output as two single-ended outputs.

The pin names for each differential output follows the naming convention OUTxyP/N where x is 0 for DPLL Channel 0 and 1 for DPLL Channel 1. In this naming convention, y refers to the output number and can be 0, 1, or 2 for DPLL Channel 0, and either 0 or 1 for DPLL Channel 1.

Each output has a distribution divider that follows the naming convention Qxy for positive outputs and Qxyy for negative (or complementary) outputs. Distribution Divider Qxy connects to Output Driver OUTxyP, and Distribution Divider Qxyy connects to OUTxyN. For example, Distribution Divider Q0AA connects to the output driver connected to the OUT0AN pin, and Distribution Divider Q1B connects to the output driver connected to the OUT1BP pin.

Note that throughout this reference manual, multifunction pins, such as SDO/M5, are referred to either by the entire pin name or by a single function of the pin, for example, M5, when only that function is relevant.

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REVISION HISTORY

10/2017—Revision 0: Initial Version

REGISTERS

SERIAL PORT REGISTERS—REGISTER 0x0000 TO REGISTER 0x0023

Table 1. Serial Port Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0000	Configuration	Soft reset	LSB first (SPI only)	Address ascension (SPI only)	SDO active (SPI only)		Address ascension (SPI only)	LSB first (SPI only)	Soft reset	0x00	0x00
0x0001		Reserved		Read buffer register	Reserved		Reset sans registers	Reserved		0x00	R/W
0x0004	Part ID	Part ID [7:0]								0x21	R
0x0005		Part ID [15:8]								0x01	R
0x000B	SPI version	SPI version								0x00	R
0x000C	Vendor ID	Vendor ID [7:0]								0x56	R
0x000D		Vendor ID [15:8]								0x04	R
0x000F	IO_UPDATE	Reserved						Address loop IO_UPDATE	IO_UPDATE	0x00	R/W
0x0010	Loop length	Address loop length								0x00	R/W
0x0020	Scratch pad	User scratchpad [7:0]								0x00	R/W
0x0021		User scratchpad [15:8]								0x00	R/W
0x0022		User scratchpad [23:16]								0x00	R/W
0x0023		User scratchpad [31:24]								0x00	R/W

Table 2. Serial Port Registers Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0000	Configuration	7	Soft reset		Soft reset. This bit must be set identically to the other soft reset bit in this register.	0x0	R/W
		6	LSB first (SPI only)		Serial peripheral interface (SPI) least significant bit (LSB) first. This bit must be set identically to the other LSB first (SPI only) bit in this register.	0x0	R/W
				0	Most significant bit (MSB) first.		
				1	LSB first.		
		5	Address ascension (SPI only)		SPI address ascension. This bit must be set identically to the other address ascension bit in this register.	0x0	R/W
				0	Address descension mode.		
				1	Address ascension mode.		
		4	SDO active (SPI only)		Enable SPI 4-wire mode. This bit must be set identically to the other serial data output (SDO) active bit in this register.	0x0	R/W
				0	3-wire SPI mode.		
				1	4-wire SPI mode (SDO pin active)		
		3	SDO active (SPI only)		Enable SPI 4-wire mode. This bit enables SPI port SDO pin. This bit has no effect in I^2C mode.	0x0	R/W
				0	3-wire SPI mode.		
				1	4-wire SPI mode (SDO pin active).		
		2	Address ascension (SPI only)		SPI address ascension. This bit controls whether the register address is automatically incremented during a multibyte transfer. This bit has no effect in I^2C mode.	0x0	R/W
				0	Address descension mode. The address pointer is automatically decremented. For multibyte bit fields, the most significant byte is read first.		
				1	Address ascension mode. The address pointer is automatically incremented. For multibyte bit fields, the least significant byte is read first.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	LSB first (SPI only)		SPI LSB first. This bit sets the bit order for SPI port. Setting this bit to 1 selects SPI LSB first mode, and setting it to 0 selects MSB first mode. This bit has no effect in I²C mode.	0x0	R/W
				0	MSB first.		
				1	LSB first.		
		0	Soft reset		Soft reset. Invokes an EEPROM download or pin program ROM download if EEPROM is enabled.	0x0	R/W
0x0001		[7:6]	Reserved		Reserved.	0x0	R
		5	Read buffer register		Read buffer register. For buffered registers, this bit controls whether the value read from the serial port is from the actual active registers or the buffered copy.	0x0	R/W
				0	Reads the register values that are currently active (default).		
				1	Reads buffered values that take effect on the next IO_UPDATE command.		
		[4:3]	Reserved		Reserved.	0x0	R
		2	Reset sans register map		Reset sans register map. This autoclearing bit resets the device while maintaining the current settings.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R
0x0004	Part ID	[7:0]	Part ID [7:0]		Part ID. This read only bit field identifies this device as a member of the AD9542, AD9543, AD9544, and AD9545 family	0x21	R
0x0005		[7:0]	Part ID [15:8]			0x01	R
0x000B	SPI version	[7:0]	SPI version		Version of Analog Devices, Inc., unified SPI protocol.	0x0	R
0x000C	Vendor ID	[7:0]	Vendor ID [7:0]		Analog Devices unified SPI vendor ID.	0x56	R
				0x0456	Analog Devices.		
				0x0000	Other vendor.		
0x000D		[7:0]	Vendor ID [15:8]		Analog Devices unified SPI vendor ID.	0x4	R
				0x0456	Analog Devices.		
				0x0000	Other vendor.		
0x000F	IO_UPDATE	[7:2]	Reserved		Reserved.	0x0	R
		1	Address loop IO_UPDATE		When this bit is 1, an IO_UPDATE command is automatically issued each time the address field loops. This is useful when polling a range of registers, and an IO_UPDATE command must be issued after each cycle.	0x0	R/W
		0	IO_UPDATE		Input/output update. Setting this autoclearing bit to Logic 1 transfers values from the buffered to the active register space, and this action is called an IO_UPDATE command in this reference manual. Unless a register is identified as a live register, the user must perform this command for the value written to a buffered register to take effect and for a read only buffered register to read back its most current value.	0x0	WC
0x0010	Loop length	[7:0]	Address loop length		Address loop length. The number of consecutive addresses that are written or read in each cycle in an address loop.	0x0	R/W
0x0020	Scratch pad	[7:0]	User scratchpad [7:0]		User scratchpad. This register has no effect on device operation. It is available for device debugging or register setting revision control.	0x0	R/W
0x0021		[7:0]	User scratchpad [15:8]			0x0	R/W
0x0022		[7:0]	User scratchpad [23:16]			0x0	R/W
0x0023		[7:0]	User scratchpad [31:24]			0x0	R/W

Mx PIN STATUS CONTROL REGISTERS—REGISTER 0x0100 TO REGISTER 0x010B

Table 3. Mx Pin Status Control Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0100	Mx pin mode	M3 driver/receiver		M2 driver/receiver		M1 driver/receiver		M0 driver/receiver		0x00	R/W
0x0101		Reserved		M6 driver/receiver		M5 driver/receiver		M4 driver/receiver		0x00	R/W
0x0102	M0	M0 output enable	M0 control/status function							0x00	R/W
0x0103	M1	M1 output enable	M1 control/status function							0x00	R/W
0x0104	M2	M2 output enable	M2 control/status function							0x00	R/W
0x0105	M3	M3 output enable	M3 control/status function							0x00	R/W
0x0106	M4	M4 output enable	M4 control/status function							0x00	R/W
0x0107	M5	M5 output enable	M5 control/status function							0x00	R/W
0x0108	M6	M6 output enable	M6 control/status function							0x00	R/W
0x0109	Pin drive strength	SPI configuration	M6 configuration	M5 configuration	M4 configuration	M3 configuration	M2 configuration	M1 configuration	M0 configuration	0x00	R/W
0x010A	Watchdog timer	Watchdog timer (ms) [7:0]								0x00	R/W
0x010B		Watchdog timer (ms) [15:8]								0x00	R/W

Table 4. Mx Pin Status Control Register Description

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0100	Mx pin mode	[7:6]	M3 driver		M3 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high complementary metal-oxide semiconductor (CMOS).	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain positive metal-oxide semiconductor (PMOS) (requires an external pull-down resistor).		
				11	Open-drain negative metal-oxide semiconductor (NMOS) (requires an external pull-up resistor).		
		[7:6]	M3 receiver		M3 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined so at least one must be high for the assigned control input to be considered true.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				11	OR inverted mode. This mode allows two or more Mx pins to be combined so at least one must be low for the assigned control input to be considered true.		
		[5:4]	M2 driver		M2 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[5:4]	M2 receiver		M2 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined so at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined so at least one must be low for the assigned control input to be considered true.		
		[3:2]	M1 driver		M1 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[3:2]	M1 receiver		M1 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined so at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined so at least one must be low for the assigned control input to be considered true.		
		[1:0]	M0 driver		M0 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[1:0]	M0 receiver		M0 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined so at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined so t at least one must be low for the assigned control input to be considered true.		
0x0101	Mx pin mode	[7:6]	Reserved		Reserved.	0x0	R
		[5:4]	M6 driver		M6 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[5:4]	M6 receiver		M6 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined so at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined so at least one must be low for the assigned control input to be considered true.		
		[3:2]	M5 driver		M5 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[3:2]	M5 receiver		M5 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined so at least one must be high for the assigned control input to be considered true.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				11	OR inverted mode. This mode allows two or more Mx pins to be combined so at least one must be low for the assigned control input to be considered true.		
		[1:0]	M4 driver		M4 driver mode. These settings allow the user to control the polarity of a status signal, as well as allow logical AND and OR functions by combining multiple Mx pins. The default mode is active high CMOS.	0x0	R/W
				00	CMOS true (active high).		
				01	CMOS inverted (active low).		
				10	Open-drain PMOS (requires an external pull-down resistor).		
				11	Open-drain NMOS (requires an external pull-up resistor).		
		[1:0]	M4 receiver		M4 receiver mode. These settings allow the user to have an input function be the logical combination of the Mx pin inputs. The default mode is AND true.	0x0	R/W
				00	AND true mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be high for the assigned input function to be considered true.		
				01	AND inverted mode. This mode allows two or more Mx pins to be combined so all pins assigned a given function must be low for the assigned input function to be considered true.		
				10	OR true mode. This mode allows two or more Mx pins to be combined so at least one must be high for the assigned control input to be considered true.		
				11	OR inverted mode. This mode allows two or more Mx pins to be combined so at least one must be low for the assigned control input to be considered true.		
0x0102	M0	7	M0 output enable		M0 output/$\overline{\text{input}}$ enable. The M0 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M0 control function		M0 pin function input. These bits determine the control function of the M0 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0103	M1	7	M1 output enable		M1 output/$\overline{\text{input}}$ enable. The M1 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M1 control function		M1 pin function input. These bits determine the control function of the M1 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0104	M2	7	M2 output enable		M2 output/$\overline{\text{input}}$ enable. The M2 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M2 control function		M2 pin function input. These bits determine the control function of the M2 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0105	M3	7	M3 output enable		M3 output/$\overline{\text{input}}$ enable. The M3 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M3 control function		M3 pin function input. These bits determine the control function of the M3 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0106	M4	7	M4 output enable		M4 output/input enable. The M4 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M4 control function		M4 pin function input. These bits determine the control function of the M4 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0107	M5	7	M5 output enable		M5 output/input enable. The M5 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M5 control function		M5 pin function input. These bits determine the control function of the M5 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0108	M6	7	M6 output enable		M6 output/input enable. The M6 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	M6 control function		M6 pin function input. These bits determine the control function of the M6 pin. See Table 6 for details about the available control inputs. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
0x0109	Pin drive strength	7	SPI configuration		SPI drive strength.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		6	M6 configuration		M6 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		5	M5 configuration		M5 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		4	M4 configuration		M4 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		3	M3 configuration		M3 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		2	M2 configuration		M2 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		1	M1 configuration		M1 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
		0	M0 configuration		M0 drive.	0x0	R/W
				0	High drive strength; 6 mA (nominal) drive strength.		
				1	Low drive strength; 3 mA (nominal) drive strength.		
0x010A	Watchdog timer	[7:0]	Watchdog timer (ms) [7:0]		Watchdog timer. The watchdog timer stops when this register is written and restarts on the next IO_UPDATE command. Writing all zeros to this register disables the function. The units are in milliseconds.	0x0	R/W
0x010B		[7:0]	Watchdog timer (ms) [15:8]			0x0	R/W

Mx PIN STATUS AND CONTROL FUNCTION REGISTERS—REGISTER 0x0102 TO REGISTER 0x0108

Table 5. Mx Pin Conrol Function Register Summary

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0102 to 0x0108	Mx	[7:0]	Mx output enable	Mx status/control function							0x00	R/W

Table 6. Mx Pin Control Function Register Details

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0102 to 0x0108	Mx	7	Mx output enable		Mx output/input. The M0 pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	Mx control function		Mx pin function input. These bits determine the control function of the Mx pin. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
				0x0	No function. No destination proxy.		
				0x1	IO_UPDATE command. Destination proxy is Register 0x000F, Bit 0.		
				0x2	Full power-down. Destination proxy is Register 0x2000, Bit 0.		
				0x3	Clear watchdog timer. Destination proxy is Register 0x2005, Bit 7.		
				0x4	Sync all distribution dividers. Destination proxy is Register 0x2000, Bit 3.		
				0x10	Clear all interrupt requests (IRQs). Destination proxy is Register 0x2005, Bit 0.		
				0x11	Clear common IRQs. Destination proxy is Register 0x2005, Bit 1.		
				0x12	Clear PLL0 IRQs. Destination proxy is Register 0x2005, Bit 2.		
				0x13	Clear PLL1 IRQs. Destination proxy is Register 0x2005, Bit 3.		
				0x20	Force REFA invalid. Destination proxy is Register 0x2003, Bit 0.		
				0x21	Force REFAA invalid. Destination proxy is Register 0x2003, Bit 1.		
				0x22	Force REFB invalid. Destination proxy is Register 0x2003, Bit 2.		
				0x23	Force REFBB invalid. Destination proxy is Register 0x2003, Bit 3.		
				0x28	Force REFA validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 0.		
				0x29	Force REFAA validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 1.		
				0x2A	Force REFB validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 2.		
				0x2B	Force REFBB validation timeout (bypass validation timer). Destination proxy is Register 0x2002, Bit 3.		
				0x30	The Mx pin signal is routed to Auxiliary TDC 0. No destination proxy.		
				0x31	The Mx pin signal is routed to Auxiliary TDC 1. No destination proxy.		
				0x32	Each rising edge of the Mx pin signal is alternately routed to Auxiliary TDC 0 and Auxiliary TDC 1. No destination proxy.		
				0x40	Power-down Channel 0. Destination proxy is Register 0x2100, Bit 0.		
				0x41	DPLL0 force freerun mode. Destination proxy is Register 0x2105, Bit 0.		
				0x42	DPLL0 force holdover mode. Destination proxy is Register 0x2105, Bit 1.		
				0x43	DPLL0 clear tuning word history. Destination proxy is Register 0x2107, Bit 1.		
				0x44	DPLL0 synchronize dividers. Destination proxy is Register 0x2101, Bit 3.		
				0x45	DPLL0 translation profile select, Bit 0. Destination proxy is Register 0x2105, Bit 4.		
				0x46	DPLL0 translation profile select, Bit 1. Destination proxy is Register 0x2105, Bit 5.		
				0x47	DPLL0 translation profile select, Bit 2. Destination proxy is Register 0x2105, Bit 6.		
				0x50	Mute OUT0A. Destination proxy is Register 0x2102, Bit 2.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0x51	Mute OUT0AA. Destination proxy is Register 0x2102, Bit 3.		
				0x52	Reset OUT0A/OUT0AA. Destination proxy is Register 0x2102, Bit 5.		
				0x53	Mute OUT0B. Destination proxy is Register 0x2103, Bit 2.		
				0x54	Mute OUT0BB. Destination proxy is Register 0x2103, Bit 3.		
				0x55	Reset OUT0B/OUT0BB. Destination proxy is Register 0x2103, Bit 5.		
				0x56	Mute OUT0C. Destination proxy is Register 0x2104, Bit 2.		
				0x57	Mute OUT0CC. Destination proxy is Register 0x2104, Bit 3.		
				0x58	Reset OUT0C/OUT0CC. Destination proxy is Register 0x2104, Bit 5.		
				0x59	Mute all Channel 0 drivers. Destination proxy is Register 0x2101, Bit 1.		
				0x5A	Reset all Channel 0 drivers. Destination proxy is Register 0x2101, Bit 2.		
				0x5B	Channel 0 JESD204B N-shot request. Destination proxy is Register 0x2101, Bit 0.		
				0x60	Power-down Channel 1. Destination proxy is Register 0x2200, Bit 0.		
				0x61	DPLL1 force freerun mode. Destination proxy is Register 0x2205, Bit 0.		
				0x62	DPLL1 force holdover mode. Destination proxy is Register 0x2205, Bit 1.		
				0x63	DPLL1 clear tuning word history. Destination proxy is Register 0x2207, Bit 1.		
				0x64	DPLL1 synchronize dividers. Destination proxy is Register 0x2201, Bit 3.		
				0x65	DPLL1 translation profile select, Bit 0. Destination proxy is Register 0x2205, Bit 4.		
				0x66	DPLL1 translation profile select, Bit 1. Destination proxy is Register 0x2205, Bit 5.		
				0x67	DPLL1 translation profile select, Bit 2. Destination proxy is Register 0x2205, Bit 6.		
				0x70	Mute OUT1A. Destination proxy is Register 0x2202, Bit 2.		
				0x71	Mute OUT1AA. Destination proxy is Register 0x2202, Bit 3.		
				0x72	Reset OUT1A/OUT1AA. Destination proxy is Register 0x2202, Bit 5.		
				0x73	Mute OUT1B. Destination proxy is Register 0x2203, Bit 2.		
				0x74	Mute OUT1BB. Destination proxy is Register 0x2203, Bit 3.		
				0x75	Reset OUT1B/OUT1BB. Destination proxy is Register 0x2203, Bit 5.		
				0x76	Mute all Channel 1 drivers. Destination proxy is Register 0x2201, Bit 1.		
				0x77	Reset all Channel 1 drivers. Destination proxy is Register 0x2201, Bit 2.		
				0x78	Channel 1 JESD204B N-shot request. Destination proxy is Register 0x2201, Bit 0.		

Table 7. Mx Pin Status Register Details

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x102 to 0x108	Mx	7	Mx output enable		Mx output. The Mx pin is a status signal (output) if this bit is set to Logic 1, and is a control (input) if set to Logic 0.	0x0	R/W
		[6:0]	Mx status function		Mx pin status output. These bits determine the status function of the Mx pins. Default is 0x00 = high impedance control pin, no function assigned.	0x0	R/W
				0x0	Static Logic 0. No source proxy.		
				0x1	Static Logic 1. No source proxy.		
				0x2	System clock divided by 96. No source proxy.		
				0x3	Watchdog timer output. The duration of this strobe equals (96/(one system clock period)) when timer expires. No source proxy.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0x4	System clock phase-locked loop (PLL) calibration in progress. Source proxy is Register 0x3001, Bit 2.		
				0x5	System clock PLL lock detect. Source proxy is Register 0x3001, Bit 0.		
				0x6	System clock PLL stable. Source proxy is Register 0x3001, Bit 1.		
				0x7	All PLLs locked. Source proxy is the logical AND of the following bits in Register 0x3001: Bit 5, Bit 4, and Bit 1.		
				0x8	Channel 0 PLLs locked. Source proxy is Register 0x3001, Bit 4.		
				0x9	Channel 1 PLLs locked. Source proxy is Register 0x3001, Bit 5.		
				0xA	EEPROM upload (write to EEPROM) in progress. Source proxy is Register 0x3000, Bit 0.		
				0xB	EEPROM download (read from EEPROM) in progress. Source proxy is Register 0x3000, Bit 1.		
				0xC	EEPROM general fault detected. Source proxy is Register 0x3000, Bit 2.		
				0xD	Temperature sensor limit alarm. Source proxy is Register 0x3002, Bit 0.		
				0x10	All IRQs. (IRQ common) OR (IRQ PLL0) OR (IRQ PLL1). No source proxy.		
				0x11	Common IRQ. This activates general IRQs not related to one channel or the other (for example, EEPROM fault or temperature sensor alarm). No source proxy.		
				0x12	Channel 0 IRQ. No source proxy.		
				0x13	Channel 1 IRQ. No source proxy.		
				0x14	REFA embedded clock to selected Mx pin. No source proxy.		
				0x16	REFAA embedded clock to selected Mx pin. No source proxy.		
				0x18	REFB embedded clock to selected Mx pin. No source proxy.		
				0x1A	REFBB embedded clock to selected Mx pin. No source proxy.		
				0x1C	REFA R divider resynchronized. No source proxy.		
				0x1D	REFAA R divider resynchronized. No source proxy.		
				0x1E	REFB R divider resynchronized. No source proxy.		
				0x1F	REFBB R divider resynchronized. No source proxy.		
				0x20	REFA faulted. Source proxy is Register 0x3005, Bit 3.		
				0x21	REFAA faulted. Source proxy is Register 0x3006, Bit 3.		
				0x22	REFB faulted. Source proxy is Register 0x3007, Bit 3.		
				0x23	REFBB faulted. Source proxy is Register 0x3008, Bit 3.		
				0x24	REFA valid. Source proxy is Register 0x3005, Bit 4.		
				0x25	REFAA valid. Source proxy is Register 0x3006, Bit 4.		
				0x26	REFB valid. Source proxy is Register 0x3007, Bit 4.		
				0x27	REFBB valid. Source proxy is Register 0x3008, Bit 4.		
				0x28	REFA active. No source proxy.		
				0x29	REFAA active. No source proxy.		
				0x2A	REFB active. No source proxy.		
				0x2B	REFBB active. No source proxy.		
				0x2C	Auxiliary NCO 0 active. No source proxy.		
				0x2D	Auxiliary NCO 1 active. No source proxy.		
				0x2E	Channel 0 feedback TDC active. No source proxy.		
				0x2F	Channel 1 feedback TDC active. No source proxy.		
				0x30	DPLL0 phase locked. Source proxy is Register 0x3100, Bit 1.		
				0x31	DPLL0 frequency locked. Source proxy is Register 0x3100, Bit 2.		
				0x32	APLL0 locked. Source proxy is Register 0x3100, Bit 3.		
				0x33	APLL0 calibration in progress. Source proxy is Register 0x3100, Bit 4.		
				0x34	DPLL0 actively tracking a reference input. No source proxy.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0x35	DPLL0 in freerun mode. Source proxy is Register 0x3101, Bit 0.		
				0x36	DPLL0 in holdover mode. Source proxy is Register 0x3101, Bit 1.		
				0x37	DPLL0 switching reference inputs. Source proxy is Register 0x3101, Bit 2.		
				0x38	DPLL0 holdover history available. Source proxy is Register 0x3102, Bit 0.		
				0x39	DPLL0 holdover history updated. Source proxy is Register 0x3011, Bit 2.		
				0x3A	DPLL0 frequency clamp is active. Source proxy is Register 0x3102, Bit 1.		
				0x3B	DPLL0 phase slew limiter is active. Source proxy is Register 0x3102, Bit 2.		
				0x3C	Channel 0 output distribution sync event. No source proxy.		
				0x3E	DPLL0 phase step detected. No source proxy.		
				0x3F	DPLL0 fast acquisition active. Source proxy is Register 0x3102, Bit 4.		
				0x40	DPLL0 fast acquisition complete. Source proxy is Register 0x3102, Bit 5.		
				0x41	DPLL0 N-divider resynchronized. No source proxy.		
				0x42	Channel 0 distribution phase slew in progress. Source proxy is Register 0x310D logical OR of Bit 0 to Bit 5.		
				0x43	Channel 0 distribution phase control error. Source proxy is Register 0x310E logical OR of Bit 0 to Bit 5.		
				0x50	DPLL1 phase locked. Source proxy is Register 0x3200, Bit 1.		
				0x51	DPLL1 frequency locked. Source proxy is Register 0x3200, Bit 2.		
				0x52	APLL1 locked. Source proxy is Register 0x3200, Bit 3.		
				0x53	APLL1 calibration in progress. Source proxy is Register 0x3200, Bit 4.		
				0x54	DPLL1 actively tracking a reference input. No source proxy.		
				0x55	DPLL1 in freerun mode. Source proxy is Register 0x3201, Bit 0.		
				0x56	DPLL1 in holdover mode. Source proxy is Register 0x3201, Bit 1.		
				0x57	DPLL1 switching reference inputs. Source proxy is Register 0x3201, Bit 2.		
				0x58	DPLL1 holdover history available. Source proxy is Register 0x3202, Bit 0.		
				0x59	DPLL1 holdover history updated. No source proxy.		
				0x5A	DPLL1 frequency clamp is active. Source proxy is Register 0x3202, Bit 1.		
				0x5B	DPLL1 phase slew limiter is active. Source proxy is Register 0x3202, Bit 2.		
				0x5C	Channel 1 output distribution sync event. Source proxy is Register 0x3019, Bit 4.		
				0x5E	DPLL1 phase step detected. No source proxy.		
				0x5F	DPLL1 fast acquisition active. Source proxy is Register 0x3202, Bit 4.		
				0x60	DPLL1 fast acquisition complete. Source proxy is Register 0x3202, Bit 5.		
				0x61	DPLL1 N-divider resynchronized. No source proxy.		
				0x62	Channel 1 distribution phase slew in progress. Source proxy is the logical OR of Register 0x320D, Bit 3 through Bit 0.		
				0x63	Channel 1 distribution phase control error. Source proxy is the logical OR of Register 0x320E, Bit 3 through Bit 0.		
				0x70	Auxiliary NCO 0 output to Mx pin (fundamental mode). No source proxy.		

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
				0x74	Auxiliary digital phase-locked loop (DPLL) locked. Source proxy is Register 0x3002, Bit 1.		
				0x75	Auxiliary DPLL reference fault. Source proxy is Register 0x3002, Bit 2.		
				0x71	Auxiliary NCO 0 output to Mx pin (tagged mode). No source proxy.		
				0x72	Auxiliary NCO 1 output to Mx pin (fundamental mode). No source proxy.		
				0x73	Auxiliary NCO 1 output to Mx pin (tagged mode). No source proxy.		
				0x78	Timestamp 0 time code available. Source proxy is Register 0x300F, Bit 2.		
				0x79	Timestamp 1 time code available. Source proxy is Register 0x300F, Bit 3.		
				0x7A	A predefined skew measurement is updated. Source proxy is Register 0x3000F, Bit 4.		

IRQ MAP COMMON MASK REGISTERS—REGISTER 0x010C TO REGISTER 0x0110

Table 8. IRQ Map Common Mask Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x010C	System clock (SYSCLK)	SYSCLK unlocked	SYSCLK stabilized	SYSCLK locked	SYSCLK calibration completed	SYSCLK calibration started	Watchdog timeout	EEPROM faulted	EEPROM completed	0x00	R/W
0x010D	Auxiliary DPLL	Reserved		Skew limit exceeded	Temperature warning	Auxiliary DPLL unfaulted	Auxiliary DPLL faulted	Auxiliary DPLL unlocked	Auxiliary DPLL locked	0x00	R/W
0x010E	REFA	REFAA R divider resynced	REFAA validated	REFAA unfaulted	REFAA faulted	REFA R divider resynced	REFA validated	REFA unfaulted	REFA faulted	0x00	R/W
0x010F	REFB	REFBB R divider resynced	REFBB validated	REFBB unfaulted	REFBB faulted	REFB R divider resynced	REFB validated	REFB unfaulted	REFB faulted	0x00	R/W
0x0110	Timestamp	Reserved			Skew updated	Timestamp 1 event	Timestamp 0 event	Auxiliary NCO 1 event	Auxiliary NCO 0 event	0x00	R/W

Table 9. IRQ Map Common Mask Registers Details

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x010C	SYSCLK	7	SYSCLK unlocked		System clock unlocked. Set this bit to Logic 1 to enable the SYSCLK unlocked IRQ. This IRQ alerts the user when a system clock PLL unlocked event occurs.	0x0	R/W
		6	SYSCLK stabilized		System clock stabilized. Set this bit to Logic 1 to enable the SYSCLK stabilized IRQ. This IRQ alerts the user that the system clock PLL has stabilized.	0x0	R/W
		5	SYSCLK locked		System clock locked. Set this bit to Logic 1 to enable the SYSCLK locked IRQ. This IRQ alerts the user when a system clock PLL unlocked event occurs.	0x0	R/W
		4	SYSCLK calibration completed		System clock calibration completed. Set this bit to Logic 1 to enable the SYSCLK calibration completed IRQ. This IRQ alerts the user when the system clock calibration is either not running or is completed.	0x0	R/W
		3	SYSCLK calibration started		System clock calibration started. Set this bit to Logic 1 to enable the SYSCLK calibration started IRQ. This IRQ alerts the user that the system clock calibration is in progress.	0x0	R/W
		2	Watchdog timeout		Watchdog timeout. Set this bit to Logic 1 to enable the watchdog timer timeout IRQ.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	EEPROM faulted		EEPROM faulted. Set this bit to Logic 1 to enable the EEPROM faulted IRQ.	0x0	R/W
		0	EEPROM completed		EEPROM operation completed. Set this bit to Logic 1 to enable the EEPROM operation completed IRQ.	0x0	R/W
0x010D	Auxiliary DPLL	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew limit exceeded		Skew limit exceeded. Set this bit to Logic 1 to enable the reference input skew measurement limit exceeded IRQ.	0x0	R/W
		4	Temperature warning		Temperature range warning. Set to Logic 1 to enable the temperature warning IRQ. This IRQ alerts the user when the temperature sensor is out of range. This IRQ activates if enabled and the temperature limits are configured before the system clock locks.	0x0	R/W
		3	Auxiliary DPLL unfaulted		Closed-loop SYSCLK compensation DPLL unfaulted. Set this bit to Logic 1 to enable the auxiliary DPLL unfaulted IRQ.	0x0	R/W
		2	Auxiliary DPLL faulted		Closed-loop SYSCLK compensation DPLL faulted. Set this bit to Logic 1 to enable the auxiliary DPLL faulted IRQ.	0x0	R/W
		1	Auxiliary DPLL unlocked		Closed-loop SYSCLK compensation DPLL unlocked. Set this bit to Logic 1 to enable the auxiliary DPLL unlocked IRQ.	0x0	R/W
		0	Auxiliary DPLL locked		Closed-loop SYSCLK compensation DPLL locked. Set this bit to Logic 1 to enable the auxiliary DPLL locked IRQ.	0x0	R/W
0x010E	REFA	7	REFAA R divider resynced		REFAA R divider resynced. Set this bit to Logic 1 to enable the REFAA R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		6	REFAA validated		REFAA validated. Set this bit to Logic 1 to enable the REFAA validated IRQ.	0x0	R/W
		5	REFAA unfaulted		REFAA unfaulted. Set this bit to Logic 1 to enable the REFAA unfaulted IRQ.	0x0	R/W
		4	REFAA faulted		REFAA faulted. Set this bit to Logic 1 to enable the REFAA faulted IRQ.	0x0	R/W
		3	REFA R divider resynced		REFA R divider resynced. Set this bit to Logic 1 to enable the REFA R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		2	REFA validated		REFA validated. Set this bit to Logic 1 to enable the REFA validated IRQ.	0x0	R/W
		1	REFA unfaulted		REFA unfaulted. Set this bit to Logic 1 to enable the REFA unfaulted IRQ.	0x0	R/W
		0	REFA faulted		REFA faulted. Set to Logic 1 to enable the REFA faulted IRQ	0x0	R/W
0x010F	REFB	7	REFBB R divider resynced		REFBB R divider resynced. Set this bit to Logic 1 to enable the REFBB R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		6	REFBB validated		REFBB validated. Set this bit to Logic 1 to enable the REFBB validated IRQ.	0x0	R/W
		5	REFBB unfaulted		REFBB unfaulted. Set this bit to Logic 1 to enable the REFBB unfaulted IRQ.	0x0	R/W
		4	REFBB faulted		REFBB faulted. Set this bit to Logic 1 to enable the REFBB faulted IRQ.	0x0	R/W
		3	REFB R divider resynced		REFB R divider resynced. Set this bit to Logic 1 to enable the REFB R divider resynced IRQ. This IRQ alerts the user of a resynchronization between a reference input demodulated edge and a DPLL feedback edge.	0x0	R/W
		2	REFB validated		REFB validated. Set this bit to Logic 1 to enable the REFB validated IRQ.	0x0	R/W
		1	REFB unfaulted		REFB unfaulted. Set this bit to Logic 1 to enable the REFB unfaulted IRQ.	0x0	R/W

Address	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	REFB faulted		REFB faulted. Set this bit to Logic 1 to enable the REFB faulted IRQ.	0x0	R/W
0x0110	Timestamp	[7:5]	Reserved		Reserved.	0x0	R
		4	Skew updated		Skew measurement updated. Set this bit to Logic 1 to enable the reference input skew measurement updated IRQ.	0x0	R/W
		3	Timestamp 1 event		Timestamp 1 time code available. Set this bit to Logic 1 to enable the Timestamp 1 event IRQ. This IRQ can be configured to activate only when tagged NCO 1 events are generated.	0x0	R/W
		2	Timestamp 0 event		Timestamp 0 time code available. Set this bit to Logic 1 to enable the Timestamp 0 event IRQ. This IRQ can be configured to activate only when tagged NCO 0 events are generated.	0x0	R/W
		1	Auxiliary NCO 1 event		Auxiliary NCO 1 event. Set this bit to Logic 1 to enable the auxiliary NCO 1 event IRQ. This IRQ activates at the interval set by the auxiliary NCO 1 frequency, regardless of the tag ratio.	0x0	R/W
		0	Auxiliary NCO 0 event		Auxiliary NCO 0 event. Set this bit to Logic 1 to enable the auxiliary NCO 0 event IRQ. This IRQ activates at the interval set by the auxiliary NCO 0 frequency regardless, of the tag ratio.	0x0	R/W

IRQ MAP DPLL0 MASK REGISTERS—REGISTER 0x0111 TO REGISTER 0x0115

Table 10. IRQ Map DPLL0 Mask Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0111	Lock	DPLL0 frequency clamp deactivated	DPLL0 frequency clamp activated	DPLL0 phase slew limiter deactivated	DPLL0 phase slew limiter activated	DPLL0 frequency unlocked	DPLL0 frequency locked	DPLL0 phase unlocked	DPLL0 phase locked	0x00	R/W
0x0112	State	DPLL0 reference switching	DPLL0 freerun entered	DPLL0 holdover entered	DPLL0 hitless entered	DPLL0 hitless exited	DPLL0 history updated	Reserved	DPLL0 phase step detected	0x00	R/W
0x0113	Fast acquisition	Reserved			DPLL0 N-divider resynced	DPLL0 fast acquisition completed	DPLL0 fast acquisition started	Reserved		0x00	R/W
0x0114	Activated profile	Reserved		DPLL0 Profile 5 activated	DPLL0 Profile 4 activated	DPLL0 Profile 3 activated	DPLL0 Profile 2 activated	DPLL0 Profile 1 activated	DPLL0 Profile 0 activated	0x00	R/W
0x0115	APLL	Reserved			DPLL0 distribution synced	APLL0 unlocked	APLL0 locked	APLL0 calibration completed	APLL0 calibration started	0x00	R/W

Table 11. IRQ Map DPLL0 Mask Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0111	Lock	7	DPLL0 frequency clamp deactivated		Frequency clamp deactivated. Set this bit to Logic 1 to enable IRQ for DPLL0 frequency clamp deactivated.	0x0	R/W
		6	DPLL0 frequency clamp activated		Frequency clamp activated. Set this bit to Logic 1 to enable IRQ for DPLL0 frequency clamp activated.	0x0	R/W
		5	DPLL0 phase slew limiter deactivated		Phase slew limiter deactivated. Set this bit to Logic 1 to enable IRQ for DPLL0 phase slew limiter deactivated.	0x0	R/W
		4	DPLL0 phase slew limiter activated		Phase slew limiter activated. Set this bit to Logic 1 to enable IRQ for DPLL0 phase slew limiter activated.	0x0	R/W
		3	DPLL0 frequency unlocked		Frequency unlocked. Set this bit to Logic 1 to enable IRQ for DPLL0 frequency unlock detected (lock to unlock transition).	0x0	R/W
		2	DPLL0 frequency locked		Frequency locked. Set this bit to Logic 1 to enable IRQ for DPLL0 frequency lock detected (unlock to lock transition).	0x0	R/W
		1	DPLL0 phase unlocked		Phase unlocked. Set this bit to Logic 1 to enable IRQ for DPLL0 phase unlock detected (lock to unlock transition).	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	DPLL0 phase locked		Phase locked. Set this bit to Logic 1 to enable IRQ for DPLL0 phase lock detected (unlock to lock transition).	0x0	R/W
0x0112	State	7	DPLL0 reference switching		Reference switching. Set this bit to Logic 1 to enable IRQ for DPLL0 reference input switching.	0x0	R/W
		6	DPLL0 freerun entered		Freerun mode entered. Set this bit to Logic 1 to enable IRQ for DPLL0 freerun mode entered.	0x0	R/W
		5	DPLL0 holdover entered		Holdover mode entered. Set this bit to Logic 1 to enable IRQ for DPLL0 holdover mode entered.	0x0	R/W
		4	DPLL0 hitless entered		Hitless mode entered. Set this bit to Logic 1 to enable IRQ for DPLL0 hitless mode entered.	0x0	R/W
		3	DPLL0 hitless exited		Hitless mode exited. Set this bit to Logic 1 to enable IRQ for DPLL0 hitless mode exited.	0x0	R/W
		2	DPLL0 history updated		Holdover history updated. Set this bit to Logic 1 to enable IRQ for DPLL0 tuning word holdover history updated.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DPLL0 phase step detected		Phase step detected. Set this bit to Logic 1 to enable IRQ for DPLL0 reference input phase step detected.	0x0	R/W
0x0113	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 N-divider resynced		N-divider resynchronized. Set this bit to Logic 1 to enable IRQ for DPLL0 N-divider resynced.	0x0	R/W
		3	DPLL0 fast acquisition completed		Fast acquisition completed. Set this bit to Logic 1 to enable IRQ for DPLL0 fast acquisition completed.	0x0	R/W
		2	DPLL0 fast acquisition started		Fast acquisition started. Set this bit to Logic 1 to enable IRQ for DPLL0 fast acquisition started.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R/W
0x0114	Activated profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 Profile 5 activated		Profile 5 activated. Set this bit to Logic 1 to enable IRQ for DPLL0 Profile 5 activated.	0x0	R/W
		4	DPLL0 Profile 4 activated		Profile 4 activated. Set this bit to Logic 1 to enable IRQ for DPLL0 Profile 4 activated.	0x0	R/W
		3	DPLL0 Profile 3 activated		Profile 3 activated. Set this bit to Logic 1 to enable IRQ for DPLL0 Profile 3 activated.	0x0	R/W
		2	DPLL0 Profile 2 activated		Profile 2 activated. Set this bit to Logic 1 to enable IRQ for DPLL0 Profile 2 activated.	0x0	R/W
		1	DPLL0 Profile 1 activated		Profile 1 activated. Set this bit to Logic 1 to enable IRQ for DPLL0 Profile 1 activated.	0x0	R/W
		0	DPLL0 Profile 0 activated		Profile 0 activated. Set this bit to Logic 1 to enable IRQ for DPLL0 Profile 0 activated.	0x0	R/W
0x0115	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 distribution synced		Clock distribution synced. Set this bit to Logic 1 to enable IRQ for DPLL0 clock distribution synced.	0x0	R/W
		3	APLL0 unlocked		Unlock detected. Set this bit to Logic 1 to enable IRQ for APLL0 unlocked detect (lock to unlock transition).	0x0	R/W
		2	APLL0 locked		Lock detected. Set this bit to Logic 1 to enable IRQ for APLL0 lock detected (unlock to lock transition).	0x0	R/W
		1	APLL0 calibration completed		Calibration completed. Set this bit to Logic 1 to enable IRQ for APLL0 calibration completed.	0x0	R/W
		0	APLL0 calibration started		Calibration started. Set this bit to Logic 1 to enable IRQ for APLL0 calibration started.	0x0	R/W

IRQ MAP DPLL1 MASK REGISTERS—REGISTER 0x0116 TO REGISTER 0x011A

Table 12. IRQ Map DPLL1 Mask Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0116	Lock	DPLL1 frequency clamp deactivated	DPLL1 frequency clamp activated	DPLL1 phase slew limiter deactivated	DPLL1 phase slew limiter activated	DPLL1 frequency unlocked	DPLL1 frequency locked	DPLL1 phase unlocked	DPLL1 phase locked	0x00	R/W
0x0117	State	DPLL1 reference switching	DPLL1 freerun entered	DPLL1 holdover entered	DPLL1 hitless entered	DPLL1 hitless exited	DPLL1 history updated	Reserved	DPLL1 phase step detect	0x00	R/W
0x0118	Fast acqui-sition	Reserved			DPLL1 N-divider resynced	DPLL1 fast acquisition completed	DPLL1 fast acquisition started	Reserved		0x00	R/W
0x0119	Activated profile	Reserved		DPLL1 Profile 5 activated	DPLL1 Profile 4 activated	DPLL1 Profile 3 activated	DPLL1 Profile 2 activated	DPLL1 Profile 1 activated	DPLL1 Profile 0 activated	0x00	R/W
0x011A	APLL	Reserved			DPLL1 distribution synced	APLL1 unlocked	APLL1 locked	APLL1 calibration completed	APLL1 calibration started	0x00	R/W

Table 13. IRQ_MAP_DPLL_1_MASK Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0116	Lock	7	DPLL1 frequency clamp deactivated		Frequency clamp deactivated. Set this bit to Logic 1 to enable IRQ for DPLL1 frequency clamp deactivated.	0x0	R/W
		6	DPLL1 frequency clamp activated		Frequency clamp activated. Set this bit to Logic 1 to enable IRQ for DPLL1 frequency clamp activated.	0x0	R/W
		5	DPLL1 phase slew limiter deactivated		Phase slew limiter deactivated. Set this bit to Logic 1 to enable IRQ for DPLL1 phase slew limiter deactivated.	0x0	R/W
		4	DPLL1 phase slew limiter activated		Phase slew limiter activated. Set this bit to Logic 1 to enable IRQ for DPLL1 phase slew limiter activated.	0x0	R/W
		3	DPLL1 frequency unlocked		Frequency unlocked. Set this bit to Logic 1 to enable IRQ for DPLL1 frequency unlocked detect (lock to unlock transition).	0x0	R/W
		2	DPLL1 frequency locked		Frequency locked. Set this bit to Logic 1 to enable IRQ for DPLL1 frequency lock detected (unlock to lock transition).	0x0	R/W
		1	DPLL1 phase unlocked		Phase unlocked. Set this bit to Logic 1 to enable IRQ for DPLL1 phase unlock detected (lock to unlock transition).	0x0	R/W
		0	DPLL1 phase locked		Phase locked. Set this bit to Logic 1 to enable IRQ for DPLL1 phase lock detected (unlock to lock transition).	0x0	R/W
0x0117	State	7	DPLL1 reference switching		Reference switching. Set this bit to Logic 1 to enable IRQ for DPLL1 reference input switching.	0x0	R/W
		6	DPLL1 freerun entered		Freerun mode entered. Set this bit to Logic 1 to enable IRQ for DPLL1 freerun mode entered.	0x0	R/W
		5	DPLL1 holdover entered		Holdover mode entered. Set this bit to Logic 1 to enable IRQ for DPLL1 holdover mode entered.	0x0	R/W
		4	DPLL1 hitless entered		Hitless mode entered. Set this bit to Logic 1 to enable IRQ for DPLL1 hitless mode entered.	0x0	R/W
		3	DPLL1 hitless exited		Hitless mode exited. Set this bit to Logic 1 to enable IRQ for DPLL1 hitless mode exited.	0x0	R/W
		2	DPLL1 history updated		Holdover history updated. Set this bit to Logic 1 to enable IRQ for DPLL1 tuning word holdover history updated.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DPLL1 phase step detect		Phase step detected. Set this bit to Logic 1 to enable IRQ for DPLL1 reference input phase step detected.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0118	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 N-divider resynced		N-divider resynchronized. Set this bit to Logic 1 to enable IRQ for DPLL1 N-divider resync.	0x0	R/W
		3	DPLL1 fast acquisition completed		Fast acquisition completed. Set to Logic 1 to enable IRQ for DPLL1 fast acquisition completed.	0x0	R/W
		2	DPLL1 fast acquisition started		Fast Acquisition Started. Set to Logic 1 to enable IRQ for DPLL1 fast acquisition started.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R/W
0x0119	Activated profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 Profile 5 activated		Profile 5 activated. Set this bit to Logic 1 to enable IRQ for DPLL1 Profile 5 activated.	0x0	R/W
		4	DPLL1 Profile 4 activated		Profile 4 activated. Set this bit to Logic 1 to enable IRQ for DPLL1 Profile 4 activated.	0x0	R/W
		3	DPLL1 Profile 3 activated		Profile 3 activated. Set this bit to Logic 1 to enable IRQ for DPLL1 Profile 3 activated.	0x0	R/W
		2	DPLL1 Profile 2 activated		Profile 2 activated. Set this bit to Logic 1 to enable IRQ for DPLL1 Profile 2 activated.	0x0	R/W
		1	DPLL1 Profile 1 activated		Profile 1 activated. Set this bit to Logic 1 to enable IRQ for DPLL1 Profile 1 activated.	0x0	R/W
		0	DPLL1 Profile 0 activated		Profile 0 activated. Set this bit to Logic 1 to enable IRQ for DPLL1 Profile 0 activated.	0x0	R/W
0x011A	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 distribution synced		Clock distribution synced. Set to Logic 1 to enable IRQ for DPLL1 clock distribution synced.	0x0	R/W
		3	APLL1 unlocked		Unlock detected. Set to Logic 1 to enable IRQ for APLL1 unlocked detect (lock to unlock transition).	0x0	R/W
		2	APLL1 locked		Lock detected. Set to Logic 1 to enable IRQ for APLL1 lock detected (unlock to lock transition).	0x0	R/W
		1	APLL1 calibration completed		Calibration completed. Set to Logic 1 to enable IRQ for APLL1 calibration completed.	0x0	R/W
		0	APLL1 calibration started		Calibration started. Set to Logic 1 to enable IRQ for APLL1 calibration started.	0x0	R/W

SYSTEM CLOCK (SYSCLK) REGISTERS—REGISTER 0x0200 TO REGISTER 0x0209

Table 14. System Clock Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0200	Feedback divider ratio	Feedback divider ratio								0x00	R/W
0x0201	Input	Reserved				Enable maintaining amplifier	SYSCLK input divider ratio		Enable SYSCLK doubler	0x00	R/W
0x0202	Reference frequency	SYSCLK reference frequency [7:0]								0x00	R/W
0x0203		SYSCLK reference frequency [15:8]								0x00	R/W
0x0204		SYSCLK reference frequency [23:16]								0x00	R/W
0x0205		SYSCLK reference frequency [31:24]								0x00	R/W
0x0206		SYSCLK reference frequency [39:32]								0x00	R/W
0x0207	Stability timer	System clock stability period [7:0]								0x00	R/W
0x0208		System clock stability period [15:8]								0x00	R/W
0x0209		Reserved				System clock stability period [19:16]				0x00	R/W

Table 15. System Clock Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0200	Feedback divider ratio	[7:0]	Feedback divider ratio		SYSCLK PLL feedback divide ratio. This bit field is the SYSCLK PLL multiplication ratio.	0x0	R/W
0x0201	Input	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable maintaining amplifier		Enable SYSCLK maintaining amplifier.	0x0	R/W
				0	Crystal maintaining amplifier disabled. Use this setting when not using a crystal as the system clock input.		
				1	Crystal maintaining amplifier enabled. Use this setting when using a crystal as the system clock input.		
		[2:1]	SYSCLK input divider ratio		SYSCLK prescaler ratio. This bit field controls the system clock input divider.	0x0	R/W
				0	Prescalar bypassed.		
				1	Divide by 2. System clock input frequency is divided by 2.		
				2	Divide by 4. System clock input frequency is divided by 4.		
				3	Divide by 8. System clock input frequency is divided by 8.		
		0	Enable SYSCLK doubler		Enable SYSCLK doubler. The system clock doubler decreases the noise contribution of the system clock PLL. However, refer to the AD9543 data sheet for the input duty cycle requirements to use the doubler.	0x0	R/W
				0	System clock doubler disabled.		
				1	System clock doubler enabled.		
0x0202	Reference frequency	[7:0]	SYSCLK reference frequency [7:0]		SYSCLK reference frequency. This 40-bit unsigned integer bit field contains the system clock reference frequency in units of millihertz. For example, the bit field setting for a 49.152 MHz crystal is 49,152,000,000 decimal (0x0B71B00000).	0x0	R/W
0x0203		[7:0]	SYSCLK reference frequency [15:8]			0x0	R/W
0x0204		[7:0]	SYSCLK reference frequency [23:16]			0x0	R/W
0x0205		[7:0]	SYSCLK reference frequency [31:24]			0x0	R/W
0x0206		[7:0]	SYSCLK reference frequency [39:32]			0x0	R/W
0x0207	Stability timer	[7:0]	System clock stability period [7:0]		SYSCLK stability period. This 20-bit unsigned integer bit field is the amount of time that the system clock PLL must be locked before the system clock stable bit is Logic 1. This time is in units of milliseconds. For example, for a system clock stability period of 50 ms, the value in this bit field is 50 decimal (0x32).	0x0	R/W
0x0208		[7:0]	System clock stability period [15:8]			0x0	R/W
0x0209		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	System clock stability period [19:16]		SYSCLK stability period. This 20-bit unsigned integer bit field is the amount of time that the system clock PLL must be locked before the system clock stable bit is Logic 1. This time is in units of milliseconds. For example, for a system clock stability period of 50 ms, the value in this bit field is 50 decimal (0x32).	0x0	R/W

SYSCLK COMPENSATION REGISTERS—REGISTER 0x0280 TO REGISTER 0x029C

Table 16. SYSCLK Compensation Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0280	Auxiliary DPLL and reference time to digital converter (TDC) compensation source	Reserved		Compen-sate auxiliary DPLL via DPLLx	Compen-sate auxiliary DPLL via coefficients	Reserved	Compen-sate TDCs via auxiliary DPLL	Compen-sate TDCs via DPLLx	Compen-sate TDCs via coefficients	0x00	R/W
0x0281	Auxiliary NCO compensation source	Reserved	Compensate Auxiliary NCO 1 via auxiliary DPLL	Compen-sate Auxiliary NCO 1 via DPLLx	Compen-sate Auxiliary NCO 1 via coefficients	Reserved	Compen-sate Auxiliary NCO 0 via auxiliary DPLL	Compen-sate Auxiliary NCO 0 via DPLLx	Compen-sate Auxiliary NCO 0 via coefficients	0x00	R/W
0x0282	DPLL compensation source	Reserved	Compensate DPLL1 via auxiliary DPLL	Compen-sate DPLL1 via DPLLx	Compen-sate DPLL1 via coefficients	Reserved	Compen-sate DPLL0 via auxiliary DPLL	Compen-sate DPLL0 via DPLLx	Compen-sate DPLL0 via coefficients	0x00	R/W
0x0283	Rate change limit	Reserved					Slew rate limit			0x00	R/W
0x0284	Closed-loop source	Reserved			Auxiliary DPLL source					0x00	R/W
0x0285	Auxiliary DPLL Bandwidth 0	Auxiliary DPLL bandwidth [7:0]								0x00	R/W
0x0286	Compensation Bandwidth 1	Auxiliary DPLL bandwidth [15:8]								0x00	R/W
0x0287	Error source	Reserved							DPLL channel error source	0x00	R/W
0x0288	Open-loop cutoff	Reserved					Coefficient output filter cutoff			0x00	R/W
0x0289	SYSCLK compensation polynomial	Constant compensation value [7:0]								0x00	R/W
0x028A		Constant compensation value [15:8]								0x00	R/W
0x028B		Constant compensation value [23:16]								0x00	R/W
0x028C		Constant compensation value [31:24]								0x00	R/W
0x028D		Constant compensation value [39:32]								0x00	R/W
0x028E		T^1 significand [7:0]								0x00	R/W
0x028F		T^1 significand [15:8]								0x00	R/W
0x0290		T^1 exponent								0x00	R/W
0x0291		T^2 significand [7:0]								0x00	R/W
0x0292		T^2 significand [15:8]								0x00	R/W
0x0293		T^2 exponent								0x00	R/W
0x0294		T^3 significand [7:0]								0x00	R/W
0x0295		T^3 significand [15:8]								0x00	R/W
0x0296		T^3 exponent								0x00	R/W
0x0297		T^4 significand [7:0]								0x00	R/W
0x0298		T^4 significand [15:8]								0x00	R/W
0x0299		T^4 exponent								0x00	R/W
0x029A		T^5 significand [7:0]								0x00	R/W
0x029B		T^5 significand [15:8]								0x00	R/W
0x029C		T^5 exponent								0x00	R/W

Table 17. SYSCLK Compensation Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0280	Auxiliary DPLL and reference TDC compensation source	[7:6]	Reserved		Reserved.	0x0	R
		5	Compensate auxiliary DPLL via DPLLx		Use DPLLx as the source to compensate the auxiliary DPLL. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to the auxiliary DPLL. DPLL0 is chosen if the channel error source bit is Logic 0, and DPLL1 is chosen if this bit is Logic 1. This mode is useful if one of the DPLLs is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		4	Compensate auxiliary DPLL via coefficients		Use temperature compensation polynomial for the auxiliary DPLL. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for the auxiliary DPLL. This mode is useful if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/ W
		3	Reserved		Reserved.	0x0	R
		2	Compensate TDCs via auxiliary DPLL		Use the auxiliary DPLL as the source to compensate TDCs. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to the time to digital converters, including both the auxiliary TDCs, as well as the reference TDCs. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source. This bit must be set for the auxiliary DPLL frequency corrections to go to the DPLL reference input frequency monitoring logic.	0x0	R/W
		1	Compensate TDCs via DPLLx		Use DPLLx as the source to compensate TDCs. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to the time to digital converters, including both the auxiliary TDCs, as well as the reference TDCs. DPLL0 is chosen if the channel error source bit is Logic 0, and DPLL1 is chosen if this bit is Logic 1. This mode is useful if one of the DPLLs is locked to a reference input with a frequency considered more accurate than the system clock source, and this bit must be set for the frequency corrections to go to the DPLL reference input frequency monitoring logic.	0x0	R/W
		0	Compensate TDCs via coefficients		Use temperature compensation polynomial for TDCs. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for TDCs, including the auxiliary TDCs, as well as the reference TDCs. This mode is useful if applying a known frequency vs. temperature characteristic to the TDCs that can be fit to a fifth-order polynomial, and this bit must be set for the frequency corrections to go to the DPLL reference input frequency monitoring logic.	0x0	R/W
0x0281	Auxiliary NCO compensation source	7	Reserved		Reserved.	0x0	R
		6	Compensate Auxiliary NCO 1 via auxiliary DPLL		Use auxiliary DPLL as the source to compensate Auxiliary NCO 1. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to Auxiliary NCO 1. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		5	Compensate Auxiliary NCO 1 via DPLLx		Use DPLLx as the source to compensate Auxiliary NCO 1. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to Auxiliary NCO 1. DPLL0 is chosen if the channel error source bit is Logic 0, and DPLL1 is chosen if this bit is Logic 1. This mode is useful if one of the DPLLs is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		4	Comp Auxiliary NCO 1 via coefficients		Use temperature compensation polynomial for Auxiliary NCO 1. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for Auxiliary NCO 0. This mode is useful if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	Reserved		Reserved.	0x0	R
		2	Compensate Auxiliary NCO 0 via auxiliary DPLL		Use auxiliary DPLL as the source to compensate Auxiliary NCO 0. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to Auxiliary NCO 0. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		1	Compensate Auxiliary NCO 0 via DPLLx		Use DPLLx as the source to compensate Auxiliary NCO 0. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to Auxiliary NCO 0. DPLL0 is chosen if the channel error source bit is Logic 0, and DPLL1 is chosen if this bit is Logic 1. This mode is useful if one of the DPLLs is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		0	Compensate Auxiliary NCO 0 via coefficients		Use temperature compensation polynomial for Auxiliary NCO 0. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for Auxiliary NCO 0. This mode is useful if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/W
0x0282	DPLL compensation source	7	Reserved		Reserved.	0x0	R
		6	Compensate DPLL1 via auxiliary DPLL		Use auxiliary DPLL as the source to compensate DPLL1. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to DPLL1. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		5	Compensate DPLL1 via DPLLx		Use DPLLx as the source to compensate DPLL1. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to DPLL1. The channel error source bit must be set to Logic 0 so that DPLL0 is chosen to compensate DPLL1. This mode is useful if DPLL0 is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		4	Compensate DPLL1 via coefficients		Use temperature compensation polynomial for DPLL1. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for DPLL0. This mode is useful if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	Compensate DPLL0 via auxiliary DPLL		Use auxiliary DPLL as the source to compensate DPLL0. Setting this bit to Logic 1 enables the auxiliary DPLL to apply frequency corrections to DPLL0. This mode is useful if the auxiliary DPLL is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		1	Compensate DPLL0 via DPLLx		Use DPLLx as the source to compensate DPLL0. Setting this bit to Logic 1 enables DPLLx (where x is either 0 or 1) to apply frequency corrections to DPLL0. The channel error source bit must be set to Logic 1 so that DPLL1 is chosen to compensate DPLL0. This mode is useful if DPLL1 is locked to a reference input with a frequency considered more accurate than the system clock source.	0x0	R/W
		0	Compensate DPLL0 via coefficients		Use temperature compensation polynomial for DPLL0. Setting this bit to Logic 1 enables the open-loop polynomial temperature compensation for DPLL0. This mode is useful if if applying a known frequency vs. temperature characteristic that can be fit to a fifth-order polynomial.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0283	Rate change limit	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Slew rate limit		Error compensation rate change limiting. This 3-bit bit field controls the system clock compensation rate change limiting. It prevents the system clock compensation block from introducing system clock frequency changes that can cause system instabilities.	0x0	R/W
				000	None.		
				001	0.715 ppm/sec.		
				010	1.43 ppm/sec.		
				011	2.86 ppm/sec.		
				100	5.72 ppm/sec.		
				101	11.44 ppm/sec.		
				110	22.88 ppm/sec.		
				111	45.76 ppm/sec.		
0x0284	Closed-loop source	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Auxiliary DPLL source		Auxiliary DPLL closed-loop source. This 5-bit bit field selects the source of the auxiliary DPLL when using auxiliary DPLL compensation. For example, if the clock input connected to REFA is considered to be more accurate frequency source in the system, select REFA in this bit field.	0x0	R/W
				0	Reference A.		
				1	Reference AA.		
				2	Reference B.		
				3	Reference BB.		
				6	Auxiliary TDC 0.		
				7	Auxiliary TDC 1.		
0x0285	Auxiliary DPLL Bandwidth 0	[7:0]	Auxiliary DPLL bandwidth [7:0]		Auxiliary DPLL bandwidth. This 16-bit bit field is the loop bandwidth of the auxiliary DPLL tracks the system clock frequency error and provides a correction to the AD9543 digital logic. It is in units of 0.1 Hz (decihertz). For example, to set a loop bandwidth of 247.6 Hz, enter 2476 decimal (0x09AC) into this bit field.	0x0	R/W
0x0286	Compensation Bandwidth 1	[7:0]	Auxiliary DPLL bandwidth [15:8]		Auxiliary DPLL bandwidth. This 16-bit bit field is the loop bandwidth of the auxiliary DPLL tracks the system clock frequency error and provides a correction to the AD9543 digital logic. It is in units of 0.1 Hz (decihertz). For example, to set a loop bandwidth of 247.6 Hz, enter 2476 decimal (0x09AC) into this bit field.	0x0	R/W
0x0287	Error source	[7:1]	Reserved		Reserved.	0x0	R
		0	DPLL channel error source		Compensation error source for DPLL Channel x. This bit allows the user to select which DPLL to use as the reference for correcting the system clock frequency error while using DPLL channel compensation.	0x0	R/W
				0	DPLL0. Selects DPLL0 as the source of system clock compensation error signal.		
				1	DPLL1. Selects DPLL1 as the source of system clock compensation error signal.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0288	Open-loop cutoff	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Coefficient output filter cutoff		Open-loop compensation filter cutoff frequency. This 3-bit bit field controls the open-loop compensation low-pass filter cutoff frequency.	0x0	R/W
				000	400 Hz (maximum).		
				001	200 Hz.		
				010	100 Hz.		
				011	50 Hz.		
				100	25 Hz.		
				101	12 Hz.		
				110	6 Hz.		
				111	3 Hz (minimum).		
0x0289	SYSCLK compensation polynomial	[7:0]	Constant compensation value [7:0]		Constant compensation value. This 40-bit bit field is the T^0 temperature compensation coefficient used in the open-loop direct compensation method. This bit field applies a fixed correction to the oscillator frequency and is useful for compensating for oscillator aging. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x028A		[7:0]	Constant compensation value [15:8]			0x0	R/W
0x028B		[7:0]	Constant compensation value [23:16]			0x0	R/W
0x028C		[7:0]	Constant compensation value [31:24]			0x0	R/W
0x028D		[7:0]	Constant compensation value [39:32]			0x0	R/W
0x028E		[7:0]	T^1 significand [7:0]		T^1 coefficient significand. This bit field is the significand portion of the T^1 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.T^1 coefficient significand. This bit field is the significand portion of the T^1 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the data sheet for details about calculating these coefficients.	0x0	R/W
0x028F		[7:0]	T^1 significand [15:8]			0x0	R/W
0x0290		[7:0]	T^1 exponent		T^1 coefficient exponent. This bit field is the exponent portion of the T^1 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x0291		[7:0]	T^2 significand [7:0]		T^2 coefficient significand. This bit field is the significand portion of the T^2 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x0292		[7:0]	T^2 significand [15:8]			0x0	R/W
0x0293		[7:0]	T^2 exponent		T^2 coefficient exponent. This bit field is the exponent portion of the T^2 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x0294		[7:0]	T^3 significand [7:0]		T^3 coefficient significand. This bit field is the significand portion of the T^3 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x0295		[7:0]	T^3 significand [15:8]			0x0	R/W
0x0296		[7:0]	T^3 exponent		T^3 coefficient exponent. This bit field is the exponent portion of the T^3 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x0297		[7:0]	T^4 significand [7:0]		T^4 coefficient significand. This bit field is the significand portion of the T^4 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x0298		[7:0]	T^4 significand [15:8]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0299		[7:0]	T^4 exponent		T^4 coefficient exponent. This bit field is the exponent portion of the T^4 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x029A		[7:0]	T^5 significand [7:0]		T^5 coefficient significand. This bit field is the significand portion of the T^5 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients.	0x0	R/W
0x029B		[7:0]	T^5 significand [15:8]			0x0	R/W
0x029C		[7:0]	T^5 exponent		T^5 coefficient exponent. This bit field is the exponent portion of the T^5 temperature compensation coefficient used in the open-loop direct compensation method. Refer to the AD9543 data sheet for details about calculating these coefficients	0x0	R/W

REFERENCE GENERAL A REGISTERS—REGISTER 0x0300 TO REGISTER 0x0303

Table 18. Reference General A Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0300	Receiver settings	REFAA single-ended mode		REFA single-ended mode		REFA differential mode		Reserved	REFA input mode	0x00	R/W
0x0301	Demodulator band	Reserved							REFA/REFAA demodulator band select	0x01	R/W
0x0302	Demodulator settings	Enable REFA demodulator polarity	Enable REFA demodulator persist	REFA demodulator sync edge		Enable REFA demodulator	REFA demodulator event polarity	REFA demodulator sensitivity		0x40	R/W
0x0303		Enable REFAA demodulator polarity	Enable REFAA demodulator persist	REFAA demodulator sync edge		Enable REFAA demodulator	REFAA demodulator event polarity	REFAA demodulator sensitivity		0x40	R/W

Table 19. Reference General A Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0300	Receiver settings	[7:6]	REFAA single-ended mode		REFAA single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V, CMOS, single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		
		[5:4]	REFA single-ended mode		REFA single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V CMOS single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:2]	REFA differential mode		REFA differential mode.	0x0	R/W
				0	Self biased ac-coupled. Use this mode for ac-coupled differential clocks. The self generated dc bias voltage is approximately 0.6 V, and the minimum input frequency depends on the size of the decoupling capacitors.		
				1	DC-coupled differential mode. Use this mode for dc-coupled differential clocks with common-mode voltages of approximately 0.6 V. There is no internally generated dc bias voltage in this mode. See the AD9543 data sheet for the actual limits.		
				10	DC-coupled low voltage differential signaling (LVDS) mode. Use this mode for dc-coupled LVDS clocks <450 MHz. The expected dc bias level is approximately 1.2 V. See the AD9543 data sheet for the actual limits, and in cases of a discrepancy, use the specification in the data sheet.		
		1	Reserved		Reserved.	0x0	R
		0	REFA input mode		REFA input mode.	0x0	R/W
				0	The REFA and REFAA input pins are single-ended inputs.		
				1	The REFA and REFAA input pins form a differential pair.		
0x0301	Demodulator band	[7:1]	Reserved		Reserved.	0x0	R
		0	REFA/REFAA demodulator band select		REFA/REFAA demodulator band select. This bit selects the low or high range of the REFA input carrier frequency.	0x1	R/W
				0	Low band. Use this mode for carrier frequencies <30 MHz.		
				1	High band. Use this mode for carrier frequencies ≥30 MHz.		
0x0302	Demodulator settings	7	Enable REFA demodulator polarity		Enable REFA demodulator polarity. This bit enables automatic demodulator polarity detection for REFA. If this bit is Logic 0, automatic demodulator polarity is disabled, and the demodulator polarity is set using the REFA demodulator event polarity bit.	0x0	R/W
				0	Disable automatic polarity detection.		
				1	Enable automatic polarity detection.		
		6	Enable REFA demodulator persist		Enable REFA demodulator persist.	0x0	R/W
				0	The demodulator does not produce continuous events on the demodulator output signal.		
				1	The demodulator produces continuous events on the demodulator output signal if five or more consecutive modulation events appear on the input reference signal.		
		[5:4]	REFA demodulator sync edge		REFA demodulator sync edge. These bits control the latency and allow the user to delay the REFA modulator output. The value in this 2-bit field is the number of sync edges (after the base edge) to delay the demodulator output.	0x0	R/W
		3	Enable REFA demodulator		Enable REFA demodulator.	0x0	R/W
				0	REFA demodulator disabled.		
				1	REFA demodulator enabled.		
		2	REFA demodulator event polarity		REFA demodulator event polarity. This bit controls whether the narrow or wide pulse occurs first in a demodulation event.	0x0	R/W
				0	The first pulse width modulation (PWM) pulse is narrow (<50% duty cycle), and is followed by a wide pulse (>50% duty cycle).		
				1	The first PWM pulse is wide (>50% duty cycle), and is followed by a narrow pulse (<50% duty cycle).		
		[1:0]	REFA demodulator sensitivity		REFA demodulator sensitivity. These bits control the sensitivity of the REFA demodulator. The default value of x'b00 is the most sensitive and x'b11 is the least sensitive. Demodulation events that have only a small variation in pulse width require a higher level of sensitivity.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0303	Demodulator settings	7	Enable REFAA demodulator polarity		Enable REFAA demodulator polarity. This bit enables automatic demodulator polarity detection for REFAA. If this bit is Logic 0, automatic demodulator polarity is disabled, and the demodulator polarity is set using the REFAA demodulator event polarity bit.	0x0	R/W
				0	Disable automatic polarity detection.		
				1	Enable automatic polarity detection.		
		6	Enable REFAA demodulator persist		Enable REFAA demodulator persist.	0x0	R/W
				0	The demodulator does not produce continuous events on the demodulator output signal.		
				1	The demodulator produces continuous events on the demodulator output signal if five or more consecutive modulation events appear on the input reference signal.		
		[5:4]	REFAA demodulator sync edge		REFAA demodulator sync edge. These bits control the latency and allow the user delay the REFAA modulator output. The value in this 2-bit register is the number of sync edges (after the base edge) to delay the demodulator output.	0x0	R/W
		3	Enable REFAA demodulator		Enable REFAA demodulator.	0x0	R/W
				0	REFAA demodulator disabled.		
				1	REFAA demodulator enabled.		
		2	REFAA demodulator event polarity		REFAA demodulator event polarity. This bit controls whether the narrow or wide pulse occurs first in a demodulation event.	0x0	R/W
				0	The first PWM pulse is narrow (<50% duty cycle) and is followed by a wide pulse (>50% duty cycle).		
				1	The first PWM pulse is wide (>50% duty cycle) and is followed by a narrow pulse (<50% duty cycle).		
		[1:0]	REFAA demodulator sensitivity		REFAA demodulator sensitivity. This register controls the sensitivity of the REFAA demodulator. The default value of 00b is the most sensitive, and 11b is the least sensitive. Demodulation events that have only a small variation in pulse width require a higher level of sensitivity.	0x0	R/W

REFERENCE GENERAL B REGISTERS—REGISTER 0x0304 TO REGISTER 0x0307

Table 20. Reference General B Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0304	Receiver settings	REFBB single-ended mode		REFB single-ended mode		REFB differential mode		Reserved	REFB input mode	0x00	R/W
0x0305	Demodulator band	Reserved							REFB/REFBB demodulator band select	0x01	R/W
0x0306	Demodulator settings	Enable REFB demodulator polarity	Enable REFB demodulator persist	REFB demodulator sync edge		Enable REFB demodulator	REFB demodulator event polarity	REFB demodulator sensitivity		0x40	R/W
0x0307		Enable REFBB demodulator polarity	Enable REFBB demodulator persist	REFBB demodulator sync edge		Enable REFBB demodulator	REFBB demodulator event polarity	REFBB demodulator sensitivity		0x40	R/W

Table 21. Reference General B Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0304	Receiver settings	[7:6]	REFBB single-ended mode		REFBB single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc-coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V, CMOS, single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		
		[5:4]	REFB single-ended mode		REFB single-ended mode.	0x0	R/W
				0	AC-coupled 1.2 V. Use this mode for ac coupling a single-ended reference input. The input impedance is approximately 23.5 kΩ with a dc bias voltage of approximately 0.6 V.		
				1	DC-coupled 1.2 V CMOS. Use this mode for single-ended, dc coupled, 1.2 V CMOS.		
				10	DC-coupled 1.8 V CMOS. Use this mode for single-ended, dc-coupled, 1.8 V CMOS.		
				11	Disable pull-down resistor. This 1.2 V CMOS single-ended mode has an input resistance of approximately 46 kΩ to 1.2 V. The internal bias prevents chatter if this input is left unconnected.		
		[3:2]	REFB differential mode		REFB differential mode.	0x0	R/W
				0	Self biased ac-coupled. Use this mode for ac-coupled differential clocks. The self generated dc bias voltage is approximately 0.6 V, and the minimum input frequency depends on the size of the decoupling capacitors.		
				1	DC-coupled differential mode. Use this mode for dc-coupled differential clocks with common-mode voltages of approximately 0.6 V. There is no internally generated dc bias voltage in this mode. See the AD9543 data sheet for the actual limits.		
				10	DC-coupled LVDS mode. Use this mode for dc-coupled LVDS clocks <450 MHz. The expected dc bias level is approximately 1.2 V. See the AD9543 data sheet for the actual limits, and in cases of a discrepancy, use the specification in the data sheet.		
		1	Reserved		Reserved.	0x0	R
		0	REFB input mode		REFB input mode.	0x0	R/W
				0	The REFB and REFBB input pins are single-ended inputs.		
				1	The REFB and REFBB input pins form a differential pair.		
0x0305	Demodulator band	[7:1]	Reserved		Reserved.	0x0	R
		0	REFB/REFBB demodulator band select		REFB/REFBB demodulator band select. This bit selects the low or high range of the REFB input carrier frequency.	0x1	R/W
				0	Low band. Use this mode for carrier frequencies <30 MHz.		
				1	High band. Use this mode for carrier frequencies ≥30 MHz.		
0x0306	Demodulator settings	7	Enable REFB demodulator polarity		Enable REFB demodulator polarity. This bit enables automatic demodulator polarity detection for REFB. If this bit is Logic 0, automatic demodulator polarity is disabled, and the demodulator polarity is set using the REFB demodulator event polarity bit.	0x0	R/W
				0	Disable automatic polarity detection.		
				1	Enable automatic polarity detection.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		6	Enable REFB demodulator persist		Enable REFB demodulator persist.	0x0	R/W
				1	The demodulator does not produce continuous events on the demodulator output signal.		
				0	The demodulator produces continuous events on the DEMOD OUT signal if five or more consecutive modulation events appear on the input reference signal.		
		[5:4]	REFB demodulator sync edge		REFB demodulator sync edge. These bits control the latency and allow the user delay the REFB modulator output. The value in this 2-bit field is the number of sync edges (after the base edge) to delay the demodulator output.	0x0	R/W
		3	Enable REFB demodulator		Enable REFB demodulator.	0x0	R/W
				0	REFB demodulator disabled.		
				1	REFB demodulator enabled.		
		2	REFB demodulator event polarity		REFB demodulator event polarity. This bit controls whether the narrow or wide pulse occurs first in a demodulation event.	0x0	R/W
				0	The first PWM pulse is narrow (<50% duty cycle) and is followed by a wide pulse (>50% duty cycle).		
				1	The first PWM pulse is wide (>50% duty cycle) and is followed by a narrow pulse (<50% duty cycle).		
		[1:0]	REFB demodulator sensitivity		REFB demodulator sensitivity. This bit field controls the sensitivity of the REFB demodulator. The default value of x'b00 is the most sensitive, and x'b11 is the least sensitive. Demodulation events that have only a small variation in pulse width require a higher level of sensitivity.	0x0	R/W
0x0307	Demodulator settings	7	Enable REFBB demodulator polarity		Enable REFBB demodulator polarity. This bit enables automatic demodulator polarity detection for REFBB. If this bit is Logic 0, automatic demodulator polarity is disabled, and the demodulator polarity is set using the REFBB demodulator event polarity bit.	0x0	R/W
				0	Disable automatic polarity detection.		
				1	Enable automatic polarity detection.		
		6	Enable REFBB demodulator persist		Enable REFBB demodulator persist.	0x0	R/W
				0	The demodulator does not produce continuous events on the demodulator output signal.		
				1	The demodulator produces continuous events on the demodulator output signal if five or more consecutive modulation events appear on the input reference signal.		
		[5:4]	REFBB demodulator sync edge		REFBB demodulator sync edge. These bits control the latency and allow the user delay the REFBB modulator output. The value in this 2-bit field is the number of sync edges (after the base edge) to delay the demodulator output.	0x0	R/W
		3	Enable REFBB demodulator		Enable REFBB demodulator.	0x0	R/W
				0	REFBB demodulator disabled.		
				1	REFBB demodulator enabled.		
		2	REFBB demodulator event polarity		REFBB demodulator event polarity. This bit controls whether the narrow or wide pulse occurs first in a demodulation event.	0x0	R/W
				0	The first PWM pulse is narrow (<50% duty cycle) and is followed by a wide pulse (>50% duty cycle).		
				1	The first PWM pulse is wide (>50% duty cycle) and is followed by a narrow pulse (<50% duty cycle).		
		[1:0]	REFBB demodulator sensitivity		REFBB demodulator sensitivity. This bit field controls the sensitivity of the REFBB demodulator. The default value of x'b00 is the most sensitive, and x'b11 is the least sensitive. Demodulation events that have only a small variation in pulse width require a higher level of sensitivity.	0x0	R/W

REFERENCE INPUT A (REFA) REGISTERS—REGISTER 0x0400 TO REGISTER 0x0414

Table 22. Reference Input A Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0400	R divider	REFA R divide ratio [7:0]								0x00	R/W
0x0401		REFA R divide ratio [15:8]								0x00	R/W
0x0402		REFA R divide ratio [23:16]								0x00	R/W
0x0403		Reserved		REFA R divide ratio [29:24]						0x00	R/W
0x0404	Input period	REFA nominal period [7:0]								0x00	R/W
0x0405		REFA nominal period [15:8]								0x00	R/W
0x0406		REFA nominal period [23:16]								0x00	R/W
0x0407		REFA nominal period [31:24]								0x00	R/W
0x0408		REFA nominal period [39:32]								0x00	R/W
0x0409		REFA nominal period [47:40]								0x00	R/W
0x040A		Reserved							REFA nominal period [48]	0x00	R/W
0x040B	Reserved	Reserved								0x00	R
0x040C	Offset limit	REFA offset limit [7:0]								0xA0	R/W
0x040D		REFA offset limit [15:8]								0x86	R/W
0x040E		REFA offset limit [23:16]								0x01	R/W
0x040F	Monitor hysteresis	Reserved					REFA monitor hysteresis			0x03	R/W
0x0410	Validation timer	REFA validation timer [7:0]								0x0A	R/W
0x0411		REFA validation timer [15:8]								0x00	R/W
0x0412		Reserved				REFA validation timer [19:16]				0x00	R/W
0x0413	Jitter tolerance	REFA jitter tolerance [7:0]								0x00	R/W
0x0414		REFA jitter tolerance [15:8]								0x00	R/W

Table 23. Reference Input A Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0400	R divider	[7:0]	REFA R divide ratio [7:0]		REFA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0401		[7:0]	REFA R divide ratio [15:8]			0x0	R/W
0x0402		[7:0]	REFA R divide ratio [23:16]			0x0	R/W
0x0403		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFA R divide ratio [29:24]		REFA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0404	Input period	[7:0]	REFA nominal period [7:0]		REFA nominal period. This bit field is called T_{REF} in the AD9543 evaluation software and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0405		[7:0]	REFA nominal period [15:8]			0x0	R/W
0x0406		[7:0]	REFA nominal period [23:16]			0x0	R/W
0x0407		[7:0]	REFA nominal period [31:24]			0x0	R/W
0x0408		[7:0]	REFA nominal period [39:32]			0x0	R/W
0x0409		[7:0]	REFA nominal period [47:40]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x040A		[7:1]	Reserved		Reserved.	0x0	R
		0	REFA nominal period [48]		REFA nominal period. This bit field is called T_{REF} in the evaluation software and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x040B	Reserved	[7:0]	Reserved		Reserved.	0x0	R
0x040C	Offset limit	[7:0]	REFA offset limit [7:0]		REFA offset limit. This bit field is called ΔT_{REF} in the data sheet. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x040D		[7:0]	REFA offset limit [15:8]			0x86	R/W
0x040E		[7:0]	REFA offset limit [23:16]			0x1	R/W
0x040F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFA monitor hysteresis		REFA monitor hysteresis. This bit field is called T_{HYS} in the data sheet and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of ΔT_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of ΔT_{REF}.		
				2	6.25% of ΔT_{REF}.		
				3	12.5% of ΔT_{REF}.		
				4	25% of ΔT_{REF}.		
				5	50% of ΔT_{REF}.		
				6	75% of ΔT_{REF}.		
				7	87.5% of ΔT_{REF}.		
0x0410	Validation timer	[7:0]	REFA validation timer [7:0]		REFA validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x0411		[7:0]	REFA validation timer [15:8]			0x0	R/W
0x0412		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFA validation timer [19:16]		REFA validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values 0x00000 and 0xFFFFF are not allowed.	0x0	R/W
0x0413	Jitter tolerance	[7:0]	REFA jitter tolerance [7:0]		REFA jitter tolerance. This bit field is called T_{TOL} in the data sheet, and determines the maximum amount of rms jitter before the excess jitter status bit is activated. This 16-bit value is in units of nanoseconds, and setting this bit to zero disables this feature.	0x0	R/W
0x0414		[7:0]	REFA jitter tolerance [15:8]			0x0	R/W

REFERENCE INPUT AA (REFAA) REGISTERS—REGISTER 0x0420 TO REGISTER 0x0434

Table 24. Reference Input AA Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0420	R divider	REFAA R divide ratio [7:0]								0x00	R/W
0x0421		REFAA R divide ratio [15:8]								0x00	R/W
0x0422		REFAA R divide ratio [23:16]								0x00	R/W
0x0423		Reserved		REFAA R divide ratio [29:24]						0x00	R/W
0x0424	Input period	REFAA nominal period [7:0]								0x00	R/W
0x0425		REFAA nominal period [15:8]								0x00	R/W
0x0426		REFAA nominal period [23:16]								0x00	R/W
0x0427		REFAA nominal period [31:24]								0x00	R/W
0x0428		REFAA nominal period [39:32]								0x00	R/W
0x0429		REFAA nominal period [47:40]								0x00	R/W
0x042A		Reserved							REFAA nominal period [48]	0x00	R/W
0x042B	Reserved	Reserved								0x00	R
0x042C	Offset limit	REFAA offset limit [7:0]								0xA0	R/W
0x042D		REFAA offset limit [15:8]								0x86	R/W
0x042E		REFAA offset limit [23:16]								0x01	R/W
0x042F	Monitor hysteresis	Reserved					REFAA monitor hysteresis			0x03	R/W
0x0430	Validation timer	REFAA validation timer [7:0]								0x0A	R/W
0x0431		REFAA validation timer [15:8]								0x00	R/W
0x0432		Reserved				REFAA validation timer [19:16]				0x00	R/W
0x0433	Jitter tolerance	REFAA jitter tolerance [7:0]								0x00	R/W
0x0434		REFAA jitter tolerance [15:8]								0x00	R/W

Table 25. Reference Input AA Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0420	R divider	[7:0]	REFAA R divide ratio [7:0]		REFAA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0421		[7:0]	REFAA R divide ratio [15:8]			0x0	R/W
0x0422		[7:0]	REFAA R divide ratio [23:16]			0x0	R/W
0x0423		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFAA R divide ratio [29:24]		REFAA integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0424	Input period	[7:0]	REFAA nominal period [7:0]		REFAA nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0425		[7:0]	REFAA nominal period [15:8]			0x0	R/W
0x0426		[7:0]	REFAA nominal period [23:16]			0x0	R/W
0x0427		[7:0]	REFAA nominal period [31:24]			0x0	R/W
0x0428		[7:0]	REFAA nominal period [39:32]			0x0	R/W
0x0429		[7:0]	REFAA nominal period [47:40]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x042A		[7:1]	Reserved		Reserved.	0x0	R
		[0]	REFAA nominal period [48]		REFAA nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x042B	Reserved	[7:0]	Reserved		Reserved	0x0	R
0x042C	Offset limit	[7:0]	REFAA offset limit [7:0]		REFAA offset limit. This bit field is called ΔT_{REF} in the data sheet. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x042D	Offset limit	[7:0]	REFAA offset limit [15:8]		REFAA offset limit. This bit field is called ΔT_{REF} in the data sheet. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0x86	R/W
0x042E	Offset limit	[7:0]	REFAA offset limit [23:16]		REFAA offset limit. This bit field is called ΔT_{REF} in the data sheet. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0x1	R/W
0x042F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFAA monitor hysteresis		REFAA monitor hysteresis. This bit field is called T_{HYS} in the data sheet and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of ΔT_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of ΔT_{REF}.		
				2	6.25% of ΔT_{REF}.		
				3	12.5% of ΔT_{REF}.		
				4	25% of ΔT_{REF}.		
				5	50% of ΔT_{REF}.		
				6	75% of ΔT_{REF}.		
				7	87.5% of ΔT_{REF}.		
0x0430	Validation timer	[7:0]	REFAA validation timer [7:0]		REFAA validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x0431		[7:0]	REFAA validation timer [15:8]			0x0	R/W
0x0432		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFAA validation timer [19:16]		REFAA validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0x0	R/W
0x0433	Jitter tolerance	[7:0]	REFAA jitter tolerance [7:0]		REFAA jitter tolerance. This bit field is called T_{TOL} in the data sheet and determines the maximum amount of rms jitter before the excess jitter status bit is activated. This 16-bit value is in units of nanoseconds, and setting this bit to zero disables this feature.	0x0	R/W
0x0434		[7:0]	REFAA jitter tolerance [15:8]			0x0	R/W

REFERENCE INPUT B (REFB) REGISTERS—REGISTER 0x0440 TO REGISTER 0x0454

Table 26. Reference Input B Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0440	R divider	REFB R divide ratio [7:0]								0x00	R/W
0x0441		REFB R divide ratio [15:8]								0x00	R/W
0x0442		REFB R divide ratio [23:16]								0x00	R/W
0x0443		Reserved		REFB R divide ratio [29:24]						0x00	R/W
0x0444	Input period	REFB nominal period [7:0]								0x00	R/W
0x0445		REFB nominal period [15:8]								0x00	R/W
0x0446		REFB nominal period [23:16]								0x00	R/W
0x0447		REFB nominal period [31:24]								0x00	R/W
0x0448		REFB nominal period [39:32]								0x00	R/W
0x0449		REFB nominal period [47:40]								0x00	R/W
0x044A		Reserved							REFB nominal period [48]	0x00	R/W
0x044B	Reserved	Reserved								0x00	R
0x044C	Offset limit	REFB offset limit [7:0]								0xA0	R/W
0x044D		REFB offset limit [15:8]								0x86	R/W
0x044E		REFB offset limit [23:16]								0x01	R/W
0x044F	Monitor hysteresis	Reserved					REFB monitor hysteresis			0x03	R/W
0x0450	Validation timer	REFB validation timer [7:0]								0x0A	R/W
0x0451		REFB validation timer [15:8]								0x00	R/W
0x0452		Reserved				REFB validation timer [19:16]				0x00	R/W
0x0453	Jitter tolerance	REFB jitter tolerance [7:0]								0x00	R/W
0x0454		REFB jitter tolerance [15:8]								0x00	R/W

Table 27. Reference Input B Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0440	R divider	[7:0]	REFB R divide ratio [7:0]		REFB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0441		[7:0]	REFB R divide ratio [15:8]			0x0	R/W
0x0442		[7:0]	REFB R divide ratio [23:16]			0x0	R/W
0x0443		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFB R divide ratio [29:24]		REFB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0444	Input period	[7:0]	REFB nominal period [7:0]		REFB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0445		[7:0]	REFB nominal period [15:8]			0x0	R/W
0x0446		[7:0]	REFB nominal period [23:16]			0x0	R/W
0x0447		[7:0]	REFB nominal period [31:24]			0x0	R/W
0x0448		[7:0]	REFB nominal period [39:32]			0x0	R/W
0x0449		[7:0]	REFB nominal period [47:40]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x044A		[7:1]	Reserved		Reserved.	0x0	R
		[0]	REFB nominal period [48]		REFB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x044B	Reserved	[7:0]	Reserved		Reserved	0x0	R
0x044C	Offset limit	[7:0]	REFB offset limit [7:0]		REFB offset limit. This bit field is called Δ T_{REF} in the data sheet. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x044D	Offset limit	[7:0]	REFB offset limit [15:8]			0x86	R/W
0x044E	Offset limit	[7:0]	REFB offset limit [23:16]			0x1	R/W
0x044F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFB monitor hysteresis		REFB monitor hysteresis. This bit field is called T_{HYS} in the data sheet and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of Δ T_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of Δ T_{REF}.		
				2	6.25% of Δ T_{REF}.		
				3	12.5% of Δ T_{REF}.		
				4	25% of Δ T_{REF}.		
				5	50% of Δ T_{REF}.		
				6	75% of Δ T_{REF}.		
				7	87.5% of Δ T_{REF}.		
0x0450	Validation timer	[7:0]	REFB validation timer [7:0]		REFB validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x0451		[7:0]	REFB validation timer [15:8]			0x0	R/W
0x0452		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFB validation timer [19:16]		REFB validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed. REFB jitter tolerance. This bit field is called T_{TOL} in the data sheet, and determines the maximum amount of rms jitter before the excess jitter status bit is activated. This 16-bit value is in units of nanoseconds, and setting this bit to zero disables this feature.	0x0	R/W
0x0453	Jitter tolerance	[7:0]	REFB jitter tolerance [7:0]			0x0	R/W
0x0454		[7:0]	REFB jitter tolerance [15:8]			0x0	R/W

REFERENCE INPUT BB (REFBB) REGISTERS—REGISTER 0x0460 TO REGISTER 0x0474

Table 28. Reference Input BB Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0460	R divider	REFBB R divide ratio [7:0]								0x00	R/W
0x0461		REFBB R divide ratio [15:8]								0x00	R/W
0x0462		REFBB R divide ratio [23:16]								0x00	R/W
0x0463		Reserved		REFBB R divide ratio [29:24]						0x00	R/W
0x0464	Input period	REFBB nominal period [7:0]								0x00	R/W
0x0465		REFBB nominal period [15:8]								0x00	R/W
0x0466		REFBB nominal period [23:16]								0x00	R/W
0x0467		REFBB nominal period [31:24]								0x00	R/W
0x0468		REFBB nominal period [39:32]								0x00	R/W
0x0469		REFBB nominal period [47:40]								0x00	R/W
0x046A		Reserved							REFBB nominal period [48]	0x00	R/W
0x046B	Reserved	Reserved								0x00	R
0x046C	Offset limit	REFBB offset limit [7:0]								0xA0	R/W
0x046D		REFBB offset limit [15:8]								0x86	R/W
0x046E		REFBB offset limit [23:16]								0x01	R/W
0x046F	Monitor hysteresis	Reserved					REFBB monitor hysteresis			0x03	R/W
0x0470	Validation timer	REFBB validation timer [7:0]								0x0A	R/W
0x0471		REFBB validation timer [15:8]								0x00	R/W
0x0472		Reserved				REFBB validation timer [19:16]				0x00	R/W
0x0473	Jitter tolerance	REFBB jitter tolerance [7:0]								0x00	R/W
0x0474		REFBB jitter tolerance [15:8]								0x00	R/W

Table 29. Reference Input BB Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0460	R divider	[7:0]	REFBB R divide ratio [7:0]		REFBB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0461		[7:0]	REFBB R divide ratio [15:8]			0x0	R/W
0x0462		[7:0]	REFBB R divide ratio [23:16]			0x0	R/W
0x0463		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	REFBB R divide ratio [29:24]		REFBB integer reference divider. The value of the R divide ratio is the value stored in this register plus 1. For example, 0x00000 equals an R divider of 1.	0x0	R/W
0x0464	Input period	[7:0]	REFBB nominal period [7:0]		REFBB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x0465		[7:0]	REFBB nominal period [15:8]			0x0	R/W
0x0466		[7:0]	REFBB nominal period [23:16]			0x0	R/W
0x0467		[7:0]	REFBB nominal period [31:24]			0x0	R/W
0x0468		[7:0]	REFBB nominal period [39:32]			0x0	R/W
0x0469		[7:0]	REFBB nominal period [47:40]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x046A		[7:1]	Reserved		Reserved.	0x0	R
		[0]	REFBB nominal period [48]		REFBB nominal period. This bit field is called T_{REF} in the evaluation software, and is the reciprocal of the input frequency. This 49-bit value is in units of attoseconds (10^{-18} sec). Note that the minimum allowable input frequency is 2 kHz, which corresponds to a maximum value of 0x01C6BF52634000 for this bit field.	0x0	R/W
0x046B	Reserved	[7:0]	Reserved		Reserved	0x0	R
0x046C	Offset limit	[7:0]	REFBB offset limit [7:0]		REFBB offset limit. This bit field is called ΔT_{REF} in the data sheet. It controls the maximum allowable frequency error before a reference becomes faulted. This 24-bit value is in units of parts per billion.	0xA0	R/W
0x046D		[7:0]	REFBB offset limit [15:8]			0x86	R/W
0x046E		[7:0]	REFBB offset limit [23:16]			0x1	R/W
0x046F	Monitor hysteresis	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	REFBB monitor hysteresis		REFBB monitor hysteresis. This bit field is called T_{HYS} in the data sheet and controls the amount of hysteresis in the reference input monitor. This 3-bit value is specified as a percentage of ΔT_{REF}. The smaller the value, the more likely the reference monitor chatters if the input clock frequency is near the limit of the allowable frequency error.	0x3	R/W
				0	No hysteresis.		
				1	3.125% of ΔT_{REF}.		
				2	6.25% of ΔT_{REF}.		
				3	12.5% of ΔT_{REF}.		
				4	25% of ΔT_{REF}.		
				5	50% of ΔT_{REF}.		
				6	75% of ΔT_{REF}.		
				7	87.5% of ΔT_{REF}.		
0x0470	Validation timer	[7:0]	REFBB validation timer [7:0]		REFBB validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds. The values of 0x00000 and 0xFFFFF are not allowed.	0xA	R/W
0x0471		[7:0]	REFBB validation timer [15:8]			0x0	R/W
0x0472		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	REFBB validation timer [19:16]		REFBB validation timer. This bit field is called T_{VALID} in the data sheet and is the amount of time a reference input clock is within the programmed frequency tolerance before that reference is declared valid. This 20-bit value is in units of milliseconds.. The values of 0x00000 and 0xFFFFF are not allowed.	0x0	R/W
0x0473	Jitter tolerance	[7:0]	REFBB jitter tolerance [7:0]		REFBB jitter tolerance. This bit field is called T_{TOL} in the data sheet and determines the maximum amount of rms jitter before the excess jitter status bit is activated. This 16-bit value is in units of nanoseconds, and setting this bit to zero disables this feature.	0x0	R/W
0x0474		[7:0]	REFBB jitter tolerance [15:8]			0x0	R/W

SOURCE PROFILE 0 A REGISTERS—REGISTER 0x0800 TO REGISTER 0x0811

Table 30. Source Profile 0 A Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0800	Phase lock threshold	Profile 0 phase lock threshold [7:0]								0xBC	R/W
0x0801		Profile 0 phase lock threshold [15:8]								0x02	R/W
0x0802		Profile 0 phase lock threshold [23:16]								0x00	R/W
0x0803	Phase lock fill rate	Profile 0 phase lock fill rate								0x0A	R/W
0x0804	Phase lock drain rate	Profile 0 phase lock drain rate								0x0A	R/W
0x0805	Frequency lock threshold	Profile 0 frequency lock threshold [7:0]								0xBC	R/W
0x0806		Profile 0 frequency lock threshold [15:8]								0x02	R/W
0x0807		Profile 0 frequency lock threshold [23:16]								0x00	R/W
0x0808	Frequency lock fill rate	Profile 0 frequency lock fill rate								0x0A	R/W
0x0809	Frequency lock drain rate	Profile 0 frequency lock drain rate								0x0A	R/W
0x080A	Phase step threshold	Profile 0 phase step threshold [7:0]								0x00	R/W
0x080B		Profile 0 phase step threshold [15:8]								0x00	R/W
0x080C		Profile 0 phase step threshold [23:16]								0x00	R/W
0x080D		Profile 0 phase step threshold [31:24]								0x00	R/W
0x080E	Phase skew	Profile 0 phase skew [7:0]								0x00	R/W
0x080F		Profile 0 phase skew [15:8]								0x00	R/W
0x0810		Profile 0 phase skew [23:16]								0x00	R/W
0x0811	Phase refinement	Profile 0 phase skew refinement steps								0x00	R/W

Table 31. Source Profile 1 AA Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0820 to 0x0831	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 32. Source Profile 2 B Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0840 to 0x0851	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 33. Source Profile 3 BB Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0860 to 0x0871	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 34. Source Profile 4 NCO 0 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0880 to 0x0891	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 35. Source Profile 5 NCO 1 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x08A0 to 0x08B1	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 36. Source Profile 6 DPLL0 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x08C0 to 0x08D1	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 37. Source Profile 7 DPLL1 Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x08E0 to 0x08F1	These registers mimic the Source Profile 0 A registers (Register 0x0800 through Register 0x0811), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 38. Source Profile 0 A Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0800	Phase lock threshold	[7:0]	Profile 0 phase lock threshold [7:0]		Profile 0 phase lock threshold. Phase lock detector threshold (in picoseconds).	0xBC	R/W
0x0801		[7:0]	Profile 0 phase lock threshold [15:8]			0x2	R/W
0x0802		[7:0]	Profile 0 phase lock threshold [23:16]			0x0	R/W
0x0803	Phase lock fill rate	[7:0]	Profile 0 phase lock fill rate		Profile 0 phase lock fill rate. Phase lock detector fill rate per phase frequency detector (PFD) cycle.	0xA	R/W
0x0804	Phase lock drain rate	[7:0]	Profile 0 phase lock drain rate		Profile 0 phase lock drain rate. Phase lock detector lock drain rate per PFD cycle.	0xA	R/W
0x0805	Frequency lock threshold	[7:0]	Profile 0 frequency lock threshold [7:0]		Profile 0 frequency lock threshold. Frequency lock detector threshold (in picoseconds).	0xBC	R/W
0x0806		[7:0]	Profile 0 frequency lock threshold [15:8]			0x2	R/W
0x0807		[7:0]	Profile 0 frequency lock threshold [23:16]			0x0	R/W
0x0808	Frequency lock fill rate	[7:0]	Profile 0 frequency lock fill rate		Profile 0 frequency lock fill rate. Frequency lock detector fill rate per PFD cycle.	0xA	R/W
0x0809	Frequency lock drain rate	[7:0]	Profile 0 frequency lock drain rate		Profile 0 frequency lock drain rate. Frequency lock detector drain rate per PFD cycle.	0xA	R/W
0x080A	Phase step threshold	[7:0]	Profile 0 phase step threshold [7:0]		Profile 0 phase step detector threshold. This 32-bit bit field is the threshold (in picoseconds) at which the DPLL declares that an input reference phase step occurred. The value of this register must always be set so the detector only activates during a reference switching event and never during normal PLL operation (when the DPLL is not switching). A value of zero indicates that the feature is disabled.	0x0	R/W
0x080B		[7:0]	Profile 0 phase step threshold [15:8]			0x0	R/W
0x080C		[7:0]	Profile 0 phase step threshold [23:16]			0x0	R/W
0x080D		[7:0]	Profile 0 phase step threshold [31:24]			0x0	R/W
0x080E	Phase skew	[7:0]	Profile 0 phase skew [7:0]		Profile 0 phase skew. Closed-loop phase skew adjustment in picoseconds.	0x0	R/W
0x080F		[7:0]	Profile 0 phase skew [15:8]			0x0	R/W
0x0810		[7:0]	Profile 0 phase skew [23:16]			0x0	R/W
0x0811	Phase refinement	[7:0]	Profile 0 Phase skew refinement steps		Profile 0 phase skew refinement steps. This 8-bit bit field contains the number of the PFD cycles averaged during a phase build out acquisition.	0x0	R/W

LOOP FILTER COEFFICIENTS 0 REGISTERS—REGISTER 0x0C00 TO REGISTER 0x0C0B

Table 39. Loop Filter Coefficients 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0C00	Base Loop Filter 0	Alpha Significand 0 [7:0]								0xC2	R/W
0x0C01		Alpha Significand 0 [15:8]								0xF0	R/W
0x0C02		Alpha Exponent 0								0xB3	R/W
0x0C03		Beta Significand 0 [7:0]								0x55	R/W
0x0C04		Beta Significand 0 [15:8]								0xC9	R/W
0x0C05		Beta Exponent 0								0xFB	R/W
0x0C06		Gamma Significand 0 [7:0]								0x5C	R/W
0x0C07		Gamma Significand 0 [15:8]								0xF6	R/W
0x0C08		Gamma Exponent 0								0xCA	R/W
0x0C09		Delta Significand 0 [7:0]								0x11	R/W
0x0C0A		Delta Significand 0 [15:8]								0xDF	R/W
0x0C0B		Delta Exponent 0								0xCC	R/W

Table 40. Loop Filter Coefficients 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0C00	Base Loop Filter 0	[7:0]	Alpha Significand 0 [7:0]		Alpha Significand 0.	0xC2	R/W
0x0C01		[7:0]	Alpha Significand 0 [15:8]		Alpha Significand 0.	0xF0	R/W
0x0C02		[7:0]	Alpha Exponent 0		Alpha Exponent 0.	0xB3	R/W
0x0C03		[7:0]	Beta Significand 0 [7:0]		Beta Significand 0.	0x55	R/W
0x0C04		[7:0]	Beta Significand 0 [15:8]		Beta Significand 0.	0xC9	R/W
0x0C05		[7:0]	Beta Exponent 0		Beta Exponent 0.	0xFB	R/W
0x0C06		[7:0]	Gamma Significand 0 [7:0]		Gamma Significand 0.	0x5C	R/W
0x0C07		[7:0]	Gamma Significand 0 [15:8]		Gamma Significand 0.	0xF6	R/W
0x0C08		[7:0]	Gamma Exponent 0		Gamma Exponent 0.	0xCA	R/W
0x0C09		[7:0]	Delta Significand 0 [7:0]		Delta Significand 0.	0x11	R/W
0x0C0A		[7:0]	Delta Significand 0 [15:8]		Delta Significand 0.	0xDF	R/W
0x0C0B		[7:0]	Delta Exponent 0		Delta Exponent 0.	0xCC	R/W

LOOP FILTER COEFFICIENTS 1 REGISTERS—REGISTER 0x0C0C TO REGISTER 0x0C17

Table 41. Loop Filter Coefficients 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0C0C	Base Loop Filter 1	Alpha Significand 1 [7:0]								0xA9	R/W
0x0C0D		Alpha Significand 1 [15:8]								0xA0	R/W
0x0C0E		Alpha Exponent 1								0xB7	R/W
0x0C0F		Beta Significand 1 [7:0]								0xCD	R/W
0x0C10		Beta Significand 1 [15:8]								0xDB	R/W
0x0C11		Beta Exponent 1								0xF3	R/W
0x0C12		Gamma Significand 1 [7:0]								0x79	R/W
0x0C13		Gamma Significand 1 [15:8]								0xD4	R/W
0x0C14		Gamma Exponent 1								0xCE	R/W
0x0C15		Delta Significand 1 [7:0]								0x4D	R/W
0x0C16		Delta Significand 1 [15:8]								0xA7	R/W
0x0C17		Delta Exponent 1								0xCF	R/W

Table 42. Loop Filter Coefficients 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0C0C	Base Loop Filter 1	[7:0]	Alpha Significand 1 [7:0]		Alpha Significand 1.	0xA9	R/W
0x0C0D		[7:0]	Alpha Significand 1 [15:8]		Alpha Significand 1.	0xA0	R/W
0x0C0E		[7:0]	Alpha Exponent 1		Alpha Exponent 1.	0xB7	R/W
0x0C0F		[7:0]	Beta Significand 1 [7:0]		Beta Significand 1.	0xCD	R/W
0x0C10		[7:0]	Beta Significand 1 [15:8]		Beta Significand 1.	0xDB	R/W
0x0C11		[7:0]	Beta Exponent 1		Beta Exponent 1.	0xF3	R/W
0x0C12		[7:0]	Gamma Significand 1 [7:0]		Gamma Significand 1.	0x79	R/W
0x0C13		[7:0]	Gamma Significand 1 [15:8]		Gamma Significand 1.	0xD4	R/W
0x0C14		[7:0]	Gamma Exponent 1		Gamma Exponent 1.	0xCE	R/W
0x0C15		[7:0]	Delta Significand 1 [7:0]		Delta Significand 1.	0x4D	R/W
0x0C16		[7:0]	Delta Significand 1 [15:8]		Delta Significand 1.	0xA7	R/W
0x0C17		[7:0]	Delta Exponent 1		Delta Exponent 1.	0xCF	R/W

DPLL CHANNEL 0 REGISTERS—REGISTER 0x1000 TO REGISTER 0x102A

Table 43. DPLL Channel 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1000	Freerun tuning word	DPLL0 freerun tuning word [7:0]								0x00	R/W
0x1001		DPLL0 freerun tuning word [15:8]								0x00	R/W
0x1002		DPLL0 freerun tuning word [23:16]								0x00	R/W
0x1003		DPLL0 freerun tuning word [31:24]								0x00	R/W
0x1004		DPLL0 freerun tuning word [39:32]								0x00	R/W
0x1005		Reserved		DPLL0 freerun tuning word [45:40]						0x00	R/W
0x1006	Tuning word clamp	DPLL0 freerun tuning word offset clamp [7:0]								0xFF	R/W
0x1007		DPLL0 freerun tuning word offset clamp [15:8]								0xFF	R/W
0x1008		DPLL0 freerun tuning word offset clamp [23:16]								0xFF	R/W
0x1009	NCO gain	Reserved				DPLL0 NCO gain filter bandwidth				0x00	R/W
0x100A	History accumulation timer	DPLL0 history accumulation timer [7:0]								0x0A	R/W
0x100B		DPLL0 history accumulation timer [15:8]								0x00	R/W
0x100C		DPLL0 history accumulation timer [23:16]								0x00	R/W
0x100D		Reserved				DPLL0 history accumulation timer [27:24]				0x00	R/W
0x100E		Reserved		DPLL0 delay history while not slew limiting	DPLL0 delay history frequency lock	DPLL0 delay history phase lock	DPLL0 quick start history	DPLL0 single sample history	DPLL0 persistent history	0x38	R/W
0x100F		Reserved					DPLL0 pause history while phase slew limiting	DPLL0 pause history frequency unlocked	DPLL0 pause history phase unlocked	0x00	R/W
0x1010	History accumulator hold off	DPLL0 history hold off time								0x00	R/W
0x1011	Phase slew limit	DPLL0 phase slew limit rate [7:0]								0x00	R/W
0x1012		DPLL0 phase slew limit rate [15:8]								0x00	R/W
0x1013		DPLL0 phase slew limit rate [23:16]								0x00	R/W
0x1014		DPLL0 phase slew limit rate [31:24]								0x06	R/W
0x1015	Phase offset	DPLL0 phase offset [7:0]								0x00	R/W
0x1016		DPLL0 phase offset [15:8]								0x00	R/W
0x1017		DPLL0 phase offset [23:16]								0x00	R/W
0x1018		DPLL0 phase offset [31:24]								0x00	R/W
0x1019		DPLL0 phase offset [39:32]								0x00	R/W

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x101A	Phase temperature compensation polynomial	DPLL0 phase temperature compensation C_1 significand [7:0]								0x00	R/W
0x101B		DPLL0 phase temperature compensation C_1 significand [15:8]								0x00	R/W
0x101C		DPLL0 phase temperature compensation C_1 exponent								0x00	R/W
0x101D		DPLL0 phase temperature compensation C_2 significand [7:0]								0x00	R/W
0x101E		DPLL0 phase temperature compensation C_2 significand [15:8]								0x00	R/W
0x101F		DPLL0 phase temperature compensation C_2 exponent								0x00	R/W
0x1020		DPLL0 phase temperature compensation C_3 significand [7:0]								0x00	R/W
0x1021		DPLL0 phase temperature compensation C_3 significand [15:8]								0x00	R/W
0x1022		DPLL0 phase temperature compensation C_3 exponent								0x00	R/W
0x1023		DPLL0 phase temperature compensation C_4 significand [7:0]								0x00	R/W
0x1024		DPLL0 phase temperature compensation C_4 significand [15:8]								0x00	R/W
0x1025		DPLL0 phase temperature compensation C_4 exponent								0x00	R/W
0x1026		DPLL0 phase temperature compensation C_5 significand [7:0]								0x00	R/W
0x1027		DPLL0 phase temperature compensation C_5 significand [15:8]								0x00	R/W
0x1028		DPLL0 phase temperature compensation C_5 exponent								0x00	R/W
0x1029	Phase adjust filter bandwidth	Reserved					DPLL0 phase temperature compensation filter bandwidth			0x00	R/W
0x102A	Inactive profile	Reserved					DPLL0 inactive profile index			0x00	R/W

Table 44. DPLL Channel 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1000	Freerun tuning word	[7:0]	DPLL0 freerun tuning word [7:0]		DPLL0 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL0 while it is in freerun mode.	0x0	R/W
0x1001		[7:0]	DPLL0 freerun tuning word [15:8]			0x0	R/W
0x1002		[7:0]	DPLL0 freerun tuning word [23:16]			0x0	R/W
0x1003		[7:0]	DPLL0 freerun tuning word [31:24]			0x0	R/W
0x1004		[7:0]	DPLL0 freerun tuning word [39:32]			0x0	R/W
0x1005		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 freerun tuning word [45:40]		DPLL0 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL0 while it is in freerun mode.	0x0	R/W
0x1006	Tuning word clamp	[7:0]	DPLL0 freerun tuning word offset clamp [7:0]		DPLL0 freerun tuning word offset clamp. This 24-bit bit field sets the DPLL0 tuning word offset clamp, f_{CLAMP}. The formula is f_{CLAMP} = DPLL0 freerun tuning word offset clamp × (f_S/236), where f_S is the system clock frequency.	0xFF	R/W
0x1007		[7:0]	DPLL0 freerun tuning word offset clamp [15:8]			0xFF	R/W
0x1008		[7:0]	DPLL0 freerun tuning word offset clamp [23:16]			0xFF	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1009	NCO gain	[7:4]	Reserved		Reserved.	0x0	R/W
		[3:0]	DPLL0 NCO gain filter bandwidth		DPLL0 NCO gain freerun tuning word filter bandwidth. This 4-bit bit field controls the low pass filter, −3 dB cutoff frequency of the DPLL0 NCO.	0x0	R/W
				0x0	250 kHz (maximum).		
				0x1	120 kHz.		
				0x2	62 kHz.		
				0x3	31 kHz.		
				0x4	16 kHz.		
				0x5	7.8 kHz.		
				0x6	3.9 kHz.		
				0x7	1.9 kHz.		
				0x8	970 Hz.		
				0x9	490 Hz.		
				0xa	240 Hz.		
				0xb	120 Hz.		
				0xc	61 Hz.		
				0xd	30 Hz.		
				0xe	15 Hz.		
				0xf	7.6 Hz (minimum).		
0x100A	History accumulation timer	[7:0]	DPLL0 history accumulation timer [7:0]		DPLL0 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the data sheet. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and the behavior is undefined for a timer value of 0x0000.	0xA	R/W
0x100B		[7:0]	DPLL0 history accumulation timer [15:8]			0x0	R/W
0x100C		[7:0]	DPLL0 history accumulation timer [23:16]			0x0	R/W
0x100D		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL0 history accumulation timer [27:24]		DPLL0 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the data sheet. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and the behavior is undefined for a timer value of 0x0000.	0x0	R/W
0x100E		[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 delay history until not phase slew limiting		DPLL0 delay history until not phase slew limiting. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL0 phase slew limiter is inactive. At that point, the tuning word averaging is further delayed by the value in the DPLL0 history hold off time. This bit ensures that the holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase slew limiter.	0x1	R/W
		4	DPLL0 delay history frequency locked		DPLL0 delay history until frequency locked. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL0 is frequency locked. At that point, the tuning word averaging is further delayed by the value in the DPLL0 history hold off time. This bit ensures that the holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the frequency lock detector.	0x1	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	DPLL0 delay history phase locked		DPLL0 delay history until phase locked. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL0 is phase locked. At this point, the tuning word averaging is further delayed by the value in the DPLL0 history hold off time. This bit ensures that holdover history averaging begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase lock detector.	0x1	R/W
		2	DPLL0 quick start history		DPLL0 quick start history. Setting this bit to Logic 1 allows the DPLL0 tuning word history to be available in 1/4 of the time specified in the DPLL0 history accumulation timer. This bit ensures that there is sufficient holdover history in cases where the DPLL is locked to a reference for a short period.	0x0	R/W
		1	DPLL0 single sample history		DPLL0 single sample history. Setting this bit to Logic 1 allows DPLL0 to use the most recent tuning word for holdover in the event that the tuning word history is not available. This bit can be used in conjunction with the quick start history bit in this register. This bit ensures that there is a minimal holdover history available in cases where the DPLL is locked to a reference for a short period.	0x0	R/W
		0	DPLL0 persistent history		DPLL0 persistent history. Setting this bit to Logic 1 prevents the DPLL0 tuning word history from being reset if there is an interruption in the tuning word averaging. This bit ensures that there is sufficient holdover history in cases where the DPLL is locked to a reference for a short period. When this bit is Logic 0, the history accumulation resets when the DPLL exits holdover and reacquires.	0x0	R/W
0x100F		[7:3]	Reserved		Reserved.	0x0	R
		2	DPLL0 pause history while slew limiting		DPLL0 pause history while phase slew limiting. Setting this bit to Logic 1 pauses the tuning word history averaging when DPLL0 is phase slewing. The tuning word history is reset when the DPLL regains phase lock if the persistent history bit is Logic 0. This bit ensures that tuning word history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase slewing.	0x0	R/W
		1	DPLL0 pause history frequency unlocked		DPLL0 pause history while frequency unlocked. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when DPLL0 is frequency unlocked. The holdover history is reset when the DPLL regains frequency lock if the persistent history bit is Logic 0. This bit ensures that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of frequency lock status.	0x0	R/W
		0	DPLL0 pause history phase unlocked		DPLL0 pause history while phase unlocked. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when the DPLL0 phase slew limiter is active. The holdover history is reset when the DPLL is no longer phase slew limited if the persistent history bit is Logic 0. This bit ensures that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase lock status.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1010	History accumulation hold off	[7:0]	DPLL0 history hold off time		DPLL0 history hold off time. This 8-bit bit field is the amount of time (in milliseconds) that the DPLL tuning word history accumulation is delayed. Hold off is disabled if this bit field is 0x00.	0x0	R/W
0x1011	Phase slew limit	[7:0]	DPLL0 phase slew limit rate [7:0]		DPLL0 phase slew limit rate. This 28-bit bit field is the DPLL0 phase slew limit rate (in picoseconds/second) and is referred to as t_{OFST} in the data sheet.	0x0	R/W
0x1012		[7:0]	DPLL0 phase slew limit rate [15:8]			0x0	R/W
0x1013		[7:0]	DPLL0 phase slew limit rate [23:16]			0x0	R/W
0x1014		[7:0]	DPLL0 phase slew limit rate [31:24]			0x6	R/W
0x1015	Phase offset	[7:0]	DPLL0 phase offset [7:0]		DPLL0 closed-loop phase offset. This signed 40-bit bit field is the DPLL0 closed-loop phase offset (in picoseconds) and is referred to as t_{OFST} in the data sheet.	0x0	R/W
0x1016		[7:0]	DPLL0 phase offset [15:8]			0x0	R/W
0x1017		[7:0]	DPLL0 phase offset [23:16]			0x0	R/W
0x1018		[7:0]	DPLL0 phase offset [31:24]			0x0	R/W
0x1019		[7:0]	DPLL0 phase offset [39:32]			0x0	R/W
0x101A	Phase temperature compensation polynomial	[7:0]	DPLL0 phase temperature compensation C_1 significand [7:0]		DPLL0 temperature compensation C_1 significand. This 10-bit bit field is the significand for the C_1 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x101B		[7:0]	DPLL0 phase temperature compensation C_1 significand [15:8]			0x0	R/W
0x101C		[7:0]	DPLL0 phase temperature compensation C_1 exponent		DPLL0 temperature compensation C_1 exponent. This 6-bit bit field is the exponent for the C_1 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x101D		[7:0]	DPLL0 phase temperature compensation C_2 significand [7:0]		DPLL0 temperature compensation C_2 significand. This 10-bit bit field is the significand for the C_2 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x101E		[7:0]	DPLL0 phase temperature compensation C_2 significand [15:8]			0x0	R/W
0x101F		[7:0]	DPLL0 phase temperature compensation C_2 exponent		DPLL0 temperature compensation C_2 exponent. This 6-bit bit field is the exponent for the C_2 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1020		[7:0]	DPLL0 phase temperature compensation C_3 significand [7:0]		DPLL0 temperature compensation C_3 significand. This 10-bit bit field is the significand for the C_3 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1021		[7:0]	DPLL0 phase temperature compensation C_3 significand [15:8]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1022		[7:0]	DPLL0 phase temperature compensation C_3 exponent		DPLL0 temperature compensation C_3 exponent. This 6-bit bit field is the exponent for the C_3 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1023		[7:0]	DPLL0 phase temperature compensation C_4 significand [7:0]		DPLL0 temperature compensation C_4 significand. This 10-bit bit field is the significand for the C_4 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1024		[7:0]	DPLL0 phase temperature compensation C_4 significand [15:8]			0x0	R/W
0x1025		[7:0]	DPLL0 phase temperature compensation C_4 exponent		DPLL0 temperature compensation C_4 exponent. This 6-bit bit field is the exponent for the C_4 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1026		[7:0]	DPLL0 phase temperature compensation C_5 significand [7:0]		DPLL0 temperature compensation C_5 significand. This 10-bit bit field is the significand for the C_5 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1027		[7:0]	DPLL0 phase temperature compensation C_5 significand [15:8]			0x0	R/W
0x1028		[7:0]	DPLL0 phase temperature compensation C_5 exponent		DPLL0 temperature compensation C_5 exponent. This 6-bit bit field is the exponent for the C_5 coefficient of the DPLL0 temperature compensation polynomial.	0x0	R/W
0x1029	Phase adjust filter bandwidth	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL0 phase temperature compensation filter bandwidth		DPLL0 temperature compensation low-pass filter bandwidth. This 3-bit bit field controls the low pass filter −3 dB cutoff frequency of the DPLL0 delay compensation block.	0x0	R/W
				0x0	240 Hz (maximum).		
				0x1	120 Hz.		
				0x2	60 Hz.		
				0x3	30 Hz.		
				0x4	15 Hz.		
				0x5	7.6 Hz.		
				0x6	3.8 Hz.		
				0x7	1.9 Hz (minimum).		
0x102A	Inactive profile	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL0 inactive profile index		DPLL0 inactive profile index. The inactive profile index is used while DPLL0 is in holdover to retain the exact DPLL configuration, including the desired input/output phase relationship.	0x0	R/W

APLL CHANNEL 0 REGISTERS—REGISTER 0x1080 TO REGISTER 0x1083

Table 45. APLL Channel 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1080	Charge pump current	Enable APLL0 manual charge pump current	APLL0 manual charge pump current							0x94	R/W
0x1081	M0 divider	APLL0 M0 feedback divider								0x00	R/W
0x1082	Loop filter control	APLL0 loop filter zero resistor (R1)			APLL0 loop filter pole capacitor (C2)			APLL0 loop filter second pole resistor (R3)		0xE0	R/W
0x1083	DC offset current	Reserved				APLL0 dc offset current direction	APLL0 dc offset current value		Enable APLL0 dc offset current	0x03	R/W

Table 46. APLL Channel 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1080	Charge pump current	7	Enable APLL0 manual charge pump current		Enables manual control of the APLL0 charge pump current.	0x0	R/W
				0	Disables manual charge pump current control. Disables manual control of the APLL0 charge pump current.		
				1	Enables manual charge pump current control. Enables manual control of the APLL0 charge pump current.		
		[6:0]	APLL0 manual charge pump current		APLL0 manual charge pump current (LSB = 3.5 μA). The user must set the enable manual charge pump current control bit in this register for this setting to be enabled.	0x0	R/W
				0000001b	1 × LSB.		
				0000010b	2 × LSB.		
				…	…		
				1111111b	127 × LSB.		
0x1081	M0 divider	[7:0]	APLL0 M0 feedback divider		APLL multiplication ratio. APLL0 M0 feedback divider ratio. Allowable values are 14 to 255.	0x0	R/W
0x1082	Loop filter control	[7:5]	APLL0 loop filter zero resistor (R1)		Loop Filter R1. APLL0 Loop Filter R1 (zero resistor) value.	0x0	R/W
				000	0 Ω (short).		
				001	250 Ω.		
				010	500 Ω.		
				011	750 Ω.		
				100	1.00 kΩ.		
				101	1.25 kΩ.		
				110	1.50 kΩ.		
				111	1.75 kΩ.		
		[4:2]	APLL0 loop filter pole capacitor (C2)		Loop Filter C2. APLL0 Loop Filter C2 (pole capacitor) value.	0x0	R/W
				000	8 pF.		
				001	24 pF.		
				010	40 pF.		
				011	56 pF.		
				100	72 pF.		
				101	88 pF.		
				110	104 pF.		
				111	120 pF.		
		[1:0]	APLL0 loop filter second pole resistor (R3)		Loop Filter R3. APLL0 Loop Filter R3 (second pole resistor) value.	0x0	R/W
				00	200 Ω.		
				01	250 Ω.		
				10	333 Ω.		
				11	500 Ω.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1083	DC offset current	[7:4]	Reserved		Reserved.	0x0	R
		3	APLL0 dc offset current direction		DC offset current direction. This bit sets the direction of the APLL0 dc offset current.	0x0	R/W
				0	Up. The dc offset current offset is positive.		
				1	Down. The dc offset current offset is negative.		
		[2:1]	APLL0 dc offset current value		DC offset current. Magnitude of the APLL0 charge pump dc offset current value.	0x0	R/W
				00	50% offset current. Offset current is 50% of the programmed APLL0 charge pump current (default).		
				01	25% offset current. Offset current is 25% of the programmed APLL0 charge pump current.		
				10	12.5% offset current. Offset current is 12.5% of the programmed APLL0 charge pump current.		
				11	6.25% offset current. Offset current is 6.25% of the programmed APLL0 charge pump current.		
		0	Enable APLL0 dc offset current		DC offset current enable. Setting this bit enables the APLL0 dc offset current.	0x0	R/W

DISTRIBUTION GENERAL 0 REGISTERS—REGISTER 0x10C0 TO REGISTER 0x10DC

Table 47. Distribution General 0 Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x10C0	Modulation step	Modulation step [7:0]								0x00	R/W
0x10C1		Modulation step [15:8]								0x00	R/W
0x10C2	Modulation Counter A	Q0A modulation counter [7:0]								0x00	R/W
0x10C3		Q0A modulation counter [15:8]								0x00	R/W
0x10C4		Q0A modulation counter [23:16]								0x00	R/W
0x10C5		Reserved				Q0A modulation counter [27:24]				0x00	R/W
0x10C6	Modulation Counter B	Q0B modulation counter [7:0]								0x00	R/W
0x10C7		Q0B modulation counter [15:8]								0x00	R/W
0x10C8		Q0B modulation counter [23:16]								0x00	R/W
0x10C9		Reserved				Q0B modulation counter [27:24]				0x00	R/W
0x10CA	Modulation Counter C	Q0C modulation counter [7:0]								0x00	R/W
0x10CB		Q0C modulation counter [15:8]								0x00	R/W
0x10CC		Q0C modulation counter [23:16]								0x00	R/W
0x10CD		Reserved				Q0C modulation counter [27:24]				0x00	R/W
0x10CE	FB clock sync edge	Reserved						Feedback divider sync edge		0x00	R/W
0x10CF	Modulator A settings	Reserved				Enable Q0A N-shot modulator	Enable Q0A single-pulse modulator	Q0A modulator polarity	Enable Q0A modulator	0x00	R/W
0x10D0	Modulator B settings	Reserved				Enable Q0B N-shot modulator	Enable Q0B single-pulse modulator	Q0B modulator polarity	Enable Q0B modulator	0x00	R/W
0x10D1	Modulator C settings	Reserved				Enable Q0C N-shot modulator	Enable Q0C single-pulse modulator	Q0C modulator polarity	Enable Q0C modulator	0x00	R/W
0x10D2	N-shot gaps	N-shot gap								0x00	R/W
0x10D3	N-shot request	Reserved	N-shot request mode	N-shot						0x00	R/W
0x10D4	N-shot enable	Enable Q0BB PRBS	Enable Q0BB N-shot	Enable Q0B PRBS	Enable Q0B N-shot	Enable Q0AAPRBS	Enable Q0AA N-shot	Enable Q0A PRBS	Enable Q0A N-shot	0x00	R/W
0x10D5	N-shot settings	Reserved				Enable Q0CC PRBS	Enable Q0CC N-shot	Enable Q0C PRBS	Enable Q0C N-shot	0x00	R/W
0x10D6	N-shot retime	Reserved							Enable N-shot retime	0x00	R/W

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x10D7	Driver A configuration	Reserved		Bypass mute retiming Channel A	OUT0A driver mode		OUT0A driver current		Enable OUT0A HCSL	0x01	R/W
0x10D8	Driver B configuration	Reserved		Bypass mute retiming Channel B	OUT0B driver mode		OUT0B driver current		Enable OUT0B HCSL	0x01	R/W
0x10D9	Driver C configuration	Reserved		Bypass mute retiming Channel C	OUT0C driver mode		OUT0C driver current		Enable OUT0C HCSL	0x01	R/W
0x10DA	Secondary clock path	Reserved				Enable SYSCLK Q0C	Enable SYSCLK Q0B	Enable SYSCLK Q0A	Enable SYSCLK Sync Mask	0x00	R/W
0x10DB	Sync control	Reserved					Enable DPLL0 reference sync	Autosync mode		0x00	R/W
0x10DC	Automute control	Mask OUT0CC autounmute	Mask OUT0C autounmute	Mask OUT0BB autounmute	Mask OUT0B autounmute	Mask OUT0AA autounmute	Mask OUT0A autounmute	DPLL0 autounmute mode		0x00	R/W

Table 48. Distribution General 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10C0	Modulation step	[7:0]	Modulation step [7:0]		Modulation step. This 16-bit bit field controls the duty cycle step, which is the duty cycle deviation of a modulation event. The unit is the number of distribution clock half cycles.	0x0	R/W
0x10C1		[7:0]	Modulation step [15:8]			0x0	R/W
0x10C2	Modulation Counter A	[7:0]	Q0A modulation counter [7:0]		Q0A modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x10C3		[7:0]	Q0A modulation counter [15:8]			0x0	R/W
0x10C4		[7:0]	Q0A modulation counter [23:16]			0x0	R/W
0x10C5		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Q0A modulation counter [27:24]		Q0A modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x10C6	Modulation Counter B	[7:0]	Q0B modulation counter [7:0]		Q0B modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x10C7		[7:0]	Q0B modulation counter [15:8]			0x0	R/W
0x10C8		[7:0]	Q0B modulation counter [23:16]			0x0	R/W
0x10C9		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Q0B modulation counter [27:24]		Q0B modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10CA	Modulation Counter C	[7:0]	Q0C modulation counter [7:0]		Q0C modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x10CB		[7:0]	Q0C modulation counter [15:8]			0x0	R/W
0x10CC		[7:0]	Q0C modulation counter [23:16]			0x0	R/W
0x10CD		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Q0C modulation counter [27:24]		Q0C modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x10CE	Feedback clock sync edge	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Feedback divider sync edge		Feedback divider sync edge. This bit field is only used when embedded output clock modulation is turned on, and allows the user to delay the synchronization edge (relative to the modulation base edge) of the feedback divider. Allowable values (in decimal) are 0, 1, 2, or 3 clock edges.	0x0	R/W
0x10CF	Modulator A settings	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable Q0A N-shot modulator		Enable Q0A modulator N-shot. Setting this bit to Logic 1 enables the embedded clock modulator controller to use the N-shot request signal to trigger five modulation events when the N-shot request mode bit is Logic 0 (edge triggered) or continuously when the N-shot request mode bit is Logic 1 (level sensitive).	0x0	R/W
		2	Enable Q0A single-pulse modulation		Single-pulse modulation.	0x0	R/W
				0	DC balanced duty cycle modulation.		
				1	Single-pulse modulation.		
		1	Q0A modulation polarity		Modulation polarity. This bit sets the type of (duty cycle) modulation event.	0x0	R/W
				0	The first modulated falling edge occurs earlier than nominal. In dc balanced mode, the second modulated falling edge occurs later than nominal.		
				1	The first modulated falling edge occurs later than nominal. In dc balanced mode, the second modulated falling edge occurs earlier than nominal.		
		0	Enable Q0A modulator		Enable embedded clock modulator. Setting this bit to Logic 1 enables the embedded clock (pulse width/duty cycle) modulation.	0x0	R/W
0x10D0	Modulator B settings	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable Q0B N-shot modulator		Enable Q0A Modulator N-shot. Setting this bit to Logic 1 enables the embedded clock modulator controller to use the N-shot request signal to trigger five modulation events when the N-shot request mode bit is Logic 0 (edge triggered) or continuously when the N-shot request mode bit is Logic 1 (level sensitive).	0x0	R/W
		2	Enable Q0B single-pulse modulation		Single-pulse modulation.	0x0	R/W
				0	DC balanced duty cycle modulation.		
				1	Single-pulse modulation.		
		1	Q0B modulation polarity		Modulation polarity. This bit sets the type of (duty cycle) modulation event.	0x0	R/W
				0	The first modulated falling edge occurs earlier than nominal. In dc balanced mode, the second modulated falling edge occurs later than nominal.		
				1	The first modulated falling edge occurs later than nominal. In dc balanced mode, the second modulated falling edge occurs earlier than nominal.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Enable Q0B modulator		Enable embedded clock modulator. Setting this bit to Logic 1 enables the embedded clock (pulse width/duty cycle) modulator.	0x0	R/W
0x10D1	Modulator C settings	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable Q0C N-shot modulator		Enable Q0A modulator N-shot. Setting this bit to Logic 1 enables the embedded clock modulator controller to use the N-shot request signal to trigger five modulation events when the N-shot request mode bit is Logic 0 (edge triggered) or continuously when the N-shot request mode bit is Logic 1 (level sensitive).	0x0	R/W
		2	Enable Q0C single-pulse modulation		Single-pulse modulation.	0x0	R/W
				0	DC balanced duty cycle modulation.		
				1	Single-pulse modulation.		
		1	Q0C modulation polarity		Modulation polarity. This bit sets the type of (duty cycle) modulation event.	0x0	R/W
				0	The first modulated falling edge occurs earlier than nominal. In dc balanced mode, the second modulated falling edge occurs later than nominal.		
				1	The first modulated falling edge occurs later than nominal. In dc balanced mode, the second modulated falling edge occurs earlier than nominal.		
		0	Enable Q0C modulator		Enable embedded clock modulator. Setting this bit to Logic 1 enables the embedded clock (pulse width/duty cycle) modulator.	0x0	R/W
0x10D2	N-shot gaps	[7:0]	N-shot gap		N-shot gap. This unsigned, 8-bit bit field contains the length (measured in Q divider output cycles) of the gap in a JESD204B N-shot pattern generation.	0x0	R/W
0x10D3	N-shot request	7	Reserved		Reserved.	0x0	R
		6	N-shot request mode		Channel 0 N-shot request mode.	0x0	R/W
				0	The N-shot generators operate in burst mode, and the rising edge of the trigger signal initiates the burst.		
				1	The N-shot generators operate in period gapped mode. In this mode, N-shot bursts occur as long as the trigger is in a Logic 1 state; for this reason, it is referred to as a level sensitive trigger mode.		
		[5:0]	N-shot		Number of clock pulses in an N-shot burst. This unsigned, 6-bit bit field contains the number of clock cycles in an N-shot burst.	0x0	R/W
0x10D4	N-shot enable	7	Enable Q0BB PRBS		Q0BB JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at divider output rate.	0x0	R/W
		6	Enable Q0BB N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
		5	Enable Q0B PRBS		Q0B JESD204B PRBS enable. Setting this bit to Logic 1 enables pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		4	Enable Q0B N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
		3	Enable Q0AA PRBS		Q0AA JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		2	Enable Q0AA N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	Enable Q0A PRBS		Q0A JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		0	Enable Q0A N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
0x10D5	N-shot settings	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable Q0CC PRBS		Q0CC JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		2	Enable Q0CC N-shot		N-shot Enable	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
		1	Enable Q0C PRBS		Q0C JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		0	Enable Q0C N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
0x10D6	N-shot retime	[7:1]	Reserved		Reserved.	0x0	R
		0	Enable N-shot retime		Enable N-shot retiming.	0x0	R/W
				0	Mx pins or registers (user-selectable) provide the JESD204B N-shot retiming source.		
				1	the N short retiming block provides the JESD204B N-shot retiming source.		
0x10D7	Driver A configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel A		Removes retiming from Channel A mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function, and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT0A driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q0A determines the divide ratio.		
				1	Dual- or single-ended output driven by Divider Q0A. Divider Q0A determines the divide ratio.		
				10	Dual- or single-ended output driven by separate Q dividers. Both Divider Q0A and Divider Q0AA are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT0A driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT0A HCSL		Selects current source (HCSL) or current sink (CML) mode.	0x0	R/W
				0	CML mode. An external pull-up resistor is required.		
				1	HCSL mode. An external pull-down resistor is required.		
0x10D8	Driver B configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel B		Removes retiming from Channel B mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function and mutes the channel immediately.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:3]	OUT0B driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q0B determines the divide ratio.		
				1	Dual- or single-ended output driven by Divider Q0A. Divider Q0B determines the divide ratio.		
				10	Dual- or single-ended output driven by separate Q dividers. Both Divider Q0B and Divider Q0BB are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT0B driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT0B HCSL		Selects HCSL or CML mode.	0x0	R/W
				0	CML mode. An external pull-up resistor is required.		
				1	HCSL mode. An external pull-down resistor is required.		
0x10D9	Driver C configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel C		Removes retiming from Channel C mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function, and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT0C driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q0C determines the divide ratio.		
				1	Dual- or single-ended output driven by Divider Q0A. Divider Q0C determines the divide ratio.		
				10	Dual- or single-ended output driven by separate Q dividers. Both Divider Q0C and Divider Q0CC are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT0C driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT0C HCSL		Selects HCSL or CML mode.	0x0	R/W
				0	CML mode mode. An external pull-up resistor is required.		
				1	HCSL mode. An external pull-down resistor is required.		
0x10DA	Secondary clock path	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable SYSCLK Q0C		Enable SYSCLK to Divider Q0C. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q0C.	0x0	R/W
		2	Enable SYSCLK Q0B		Enable SYSCLK to Channel 0B. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q0B.	0x0	R/W
		1	Enable SYSCLK Q0A		Enable SYSCLK to Channel 0A. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q0A.	0x0	R/W
		0	Enable SYSCLK sync mask		Enable SYSCLK sync mask. Setting this bit to Logic 1 ensures no sync events occur on outputs that are assigned to outputting the SYSCLK. The purpose of this feature is to ensure no runt pulses or stalled clocks occur when a SYSCLK output clocks a microprocessor. Set this bit to Logic 1 only when the SYSCLK is fully configured and stable, because runt pulses can occur while configuring the SYSCLK.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x10DB	Sync control	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable DPLL0 reference sync		DPLL0 reference sync enable. Setting this bit to Logic 1 enables automatic reference synchronization on DPLL0. Reference sync works only when a hitless translation profile is active. Reference sync does not occur when a phase buildout profile is active.	0x0	R/W
		[1:0]	Autosync mode		Autosync mode. This bit field controls when the clock distribution block receives a synchronization event. The output drivers do not toggle until there is a synchronization event.	0x0	R/W
				0	Manual sync. Automatic output synchronization disabled. In this mode, the user must issue a clock distribution synchronization command manually.		
				1	Immediate. Output synchronization occurs immediately after APLL lock.		
				10	DPLL phase lock. Output synchronization occurs when the DPLL phase locks.		
				11	DPLL frequency lock. Output synchronization occurs when the DPLL frequency locks.		
0x10DC	Automute control	7	Mask OUT0CC autounmute		Mask OUT0CC autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		6	Mask OUT0C autounmute		Mask OUT0C autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		5	Mask OUT0BB autounmute		Mask OUT0BB autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		4	Mask OUT0B autounmute		Mask OUT0B autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		3	Mask OUT0AA autounmute		Mask OUT0AA autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		2	Mask OUT0A autounmute		Mask OUT0A autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		[1:0]	DPLL0 autounmute mode		DPLL0 autounmute mode. This bit field controls at which point the output drivers start to toggle during acquisition while DPLL0 is in hitless mode.	0x0	R/W
				0	Disabled. Automatic unmuting is disabled and the output driver starts toggling immediately.		
				1	Hitless acquisition. Automatic driver unmuting occurs upon activation of a hitless profile.		
				10	Phase lock detect (hitless mode only). Automatic driver unmuting occurs when phase lock is detected and the DPLL is in hitless mode.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				11	Frequency lock detect (hitless mode only). Automatic driver unmuting occurs when frequency lock is detected and the DPLL is in hitless mode.		

DISTRIBUTION DIVIDER Q0A REGISTERS—REGISTER 0x1100 TO REGISTER 0x1108

Table 49. Distribution Divider Q0A Registers Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1100	Divide ratio	Q0A divide ratio [7:0]								0x00	R/W
0x1101		Q0A divide ratio [15:8]								0x00	R/W
0x1102		Q0A divide ratio [23:16]								0x00	R/W
0x1103		Q0A divide ratio [31:24]								0x00	R/W
0x1104	Phase offset	Q0A phase [7:0]								0x00	R/W
0x1105		Q0A phase [15:8]								0x00	R/W
0x1106		Q0A phase [23:16]								0x00	R/W
0x1107		Q0A phase [31:24]								0x00	R/W
0x1108	Phase slew configuration	Reserved	Q0A Phase [32]	Enable Q0A half divide	Enable Q0A pulse width control	Q0A phase slew mode	Maximum phase slew step			0x07	R/W

Table 50. Distribution Divider Q0AA Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1109 to 0x1111		These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 51. Distribution Divider Q0B Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1112 to 0x111A		These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 52. Distribution Divider Q0BB Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x111B to 0x1123		These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 53. Distribution Divider Q0C Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1124 to 0x112C		These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 54. Distribution Divider Q0CC Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x112D to 0x1135		These registers mimic the Distribution Divider Q0A registers (Register 0x1100 through Register 0x1108), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 55. Distribution Divider Q0A Registers Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1100	Divide ratio	[7:0]	Q0A divide ratio [7:0]		Q0A divide ratio. This 32-bit bit field is the divide ratio for the Q0A divider. The default value of 0x00000000 equals a divide ratio of 1, resulting in an output frequency that exceeds the maximum frequency for the AD9543.	0x0	R/W
0x1101		[7:0]	Q0A divide ratio [15:8]			0x0	R/W
0x1102		[7:0]	Q0A divide ratio [23:16]			0x0	R/W
0x1103		[7:0]	Q0A divide ratio [31:24]			0x0	R/W
0x1104	Phase offset	[7:0]	Q0A phase [7:0]		Q0A phase control. This bit field controls the Q0A phase in two ways: the bit field sets the initial phase offset after divider sync (reset); and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q0A distribution input clock half cycles.	0x0	R/W
0x1105		[7:0]	Q0A phase [15:8]			0x0	R/W
0x1106		[7:0]	Q0A phase [23:16]			0x0	R/W
0x1107		[7:0]	Q0A phase [31:24]			0x0	R/W
0x1108	Phase slew configuration	7	Reserved		Reserved.	0x0	R
		6	Q0A phase [32]		Q0A phase control. This bit field controls the Q0A phase in two ways: the bit field sets the initial phase offset after divider sync (reset); and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q0A distribution input clock half cycles.	0x0	R/W
		5	Enable Q0A half divide		Enable Q0A half divide. Setting this bit to Logic 1 adds 0.5 to the divide ratio programmed into the corresponding 32-bit Q0A divide ratio bit field.	0x0	R/W
		4	Enable Q0A pulse width control		Enable pulse width control mode. This bit controls whether the Q0A phase bit field adjusts the phase offset or the pulse width.	0x0	R/W
				0	The Q0A phase bit field controls the phase offset.		
				1	The Q0A phase bit field controls the pulse width.		
		3	Q0A phase slew mode		Q0A phase slew mode.	0x0	R/W
				0	Lag only (always slows down frequency). The phase controller slews the phase in the direction that always reduces the output frequency.		
				1	Lead or lag (quickest is automatically calculated). The phase controller slews the phase in the direction requiring the fewest steps. This means the output frequency can increase or decrease during a stepwise phase adjustment sequence.		
		[2:0]	Maximum phase slew step		Maximum phase slew step. This 3-bit bit field controls the maximum allowable phase step while adjusting the phase in the Q0A divider. Each step occurs every output clock cycle.	0x0	R/W
				0	One input clock half-cycle. The phase slew step size is half of the Q divider input period.		
				1	Two input clock half-cycles. The maximum phase slew step size equals the Q divider input period.		
				10	11°. The maximum phase slew step size equals 1/32 (~11.25°) of the output clock period.		
				11	23°. The maximum phase slew step size equals 1/16 (~22.5°) of the output clock period.		
				100	45°. The maximum phase slew step size equals 1/8 (~45°) of the output clock period.		
				101	90°. The maximum phase slew step size equals 1/4 (~90°) of the output clock period.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				110	180°. The maximum phase slew step size equals half (~180°) of the output clock period.		
				111	Maximum. The maximum phase slew step size equals the output clock period.		

DPLL TRANSLATION PROFILE 0.0 REGISTERS—REGISTER 0x1200 TO REGISTER 0x1217

Table 56. DPLL Translation Profile 0.0 Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1200	Priority and enable	Reserved		Profile 0.0 selection priority					Enable Profile 0.0	0x00	R/W
0x1201	Source	Reserved			Profile 0.0 reference source selection					0x00	R/W
0x1202	Zero delay feedback path	Reserved			Internal/external zero delay feedback path					0x00	R/W
0x1203	Feedback mode	Profile 0.0 loop filter base	Reserved		Profile 0.0 tag mode			Enable Profile 0.0 external zero delay	Enable Profile 0.0 hitless	0x00	R/W
0x1204	Loop bandwidth	Profile 0.0 loop bandwidth [7:0]								0x00	R/W
0x1205		Profile 0.0 loop bandwidth [15:8]								0x00	R/W
0x1206		Profile 0.0 loop bandwidth [23:16]								0x00	R/W
0x1207		Profile 0.0 loop bandwidth [31:24]								0x00	R/W
0x1208	Hitless feedback divider	Profile 0.0 hitless N-divider [7:0]								0xA0	R/W
0x1209		Profile 0.0 hitless N-divider [15:8]								0x0F	R/W
0x120A		Profile 0.0 hitless N-divider [23:16]								0x00	R/W
0x120B		Profile 0.0 hitless N-divider [31:24]								0x00	R/W
0x120C	Buildout feedback divider	Profile 0.0 buildout N-divider [7:0]								0xA0	R/W
0x120D		Profile 0.0 buildout N-divider [15:8]								0x0F	R/W
0x120E		Profile 0.0 buildout N-divider [23:16]								0x00	R/W
0x120F		Profile 0.0 buildout N-divider [31:24]								0x00	R/W
0x1210	Buildout feedback fraction	Profile 0.0 buildout fraction [7:0]								0x00	R/W
0x1211		Profile 0.0 buildout fraction [15:8]								0x00	R/W
0x1212		Profile 0.0 buildout fraction [23:16]								0x00	R/W
0x1213	Buildout feedback modulus	Profile 0.0 buildout modulus [7:0]								0x00	R/W
0x1214		Profile 0.0 buildout modulus [15:8]								0x00	R/W
0x1215		Profile 0.0 buildout modulus [23:16]								0x00	R/W
0x1216	Fast lock	Reserved				Profile 0.0 fast acquisition excess bandwidth				0x00	R/W
0x1217		Reserved	Profile 0.0 fast acquisition timeout			Reserved	Profile 0.0 fast acquisition lock settle time			0x00	R/W

Table 57. DPLL Translation Profile 0.1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1220 to 0x1237		These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 58. DPLL Translation Profile 0.2 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1240 to 0x1257		These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 59. DPLL Translation Profile 0.3 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1260 to 0x1277		These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 60. DPLL Translation Profile 0. 4 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1280 to 0x1297		These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 61. DPLL Translation Profile 0.5 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x12A0 to 0x12B7		These registers mimic the DPLL Translation Profile 0.0 registers (Register 0x1200 through Register 0x1217), but the register addresses are offset by 0x0020. All default values are identical.									R/W

Table 62. DPLL Translation Profile 0.0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1200	Priority and enable	[7:6]	Reserved		Reserved.	0x0	R
		[5:1]	Profile 0.0 selection priority		Profile 0 (Profile 0.0) selection priority. This 5-bit bit field contains the priority of the translation profile. This allows the user to assign different priorities to different reference inputs. 0x00 is the highest priority, and 0x1F is the lowest priority. The choice of priority level for a given translation profile is important. If the priority difference between the active profile, and a valid, but inactive higher priority profile is >7, the DPLL state machine alwayses switch to the higher priority profile. This is called revertive reference switching. Therefore, if revertive switching is desired, ensure that the higher priority profile has a priority that is at least 8 greater than a lower priority profile. If the difference between the priorities of the active profile and a valid, but inactive higher priority profile is 0 to 7, the DPLL state machine remains on the lower priority profile. This is called nonrevertive reference switching.	0x0	R/W
		0	Enable Profile 0.0		Enable DPLL0 Profile 0.0. Setting this bit to Logic 1 enables DPLL0 Profile 0. If this bit is Logic 0, DPLL0 never uses this profile.	0x0	R/W
0x1201	Source	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Profile 0.0 reference source selection		Profile 0.0 reference source selection. This 5-bit bit field contains the input source of the translation profile.	0x0	R/W
				0	Reference A.		
				1	Reference AA.		
				2	Reference B.		
				3	Reference BB.		
				5	Feedback from DPLL1.		
				8	Auxiliary NCO 0.		
				9	Auxiliary NCO 1.		
0x1202	Zero delay feedback path	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	External zero delay feed-back path		Profile 0.0 external zero delay feedback path. This 5-bit bit field configures the Profile 0.0 feedback path in hitless external zero delay mode.	0x0	R/W
				0	Reference A. Select this mode if REFA is single-ended or in differential mode.		
				1	Reference AA.		
				2	Reference B. Select this mode if REFB is single-ended or in differential mode.		
				3	Reference BB.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:0]	Internal zero delay feed-back path		Profile 0.0 internal zero delay feedback path. This 5-bit bit field configures the Profile 0.0 feedback path in hitless internal zero delay mode.	0x0	R/W
				0	OUT0AP. Select this mode if OUT0A is single-ended or in differential mode.		
				1	OUT0AN.		
				2	OUT0BP. Select this mode if OUT0B is single-ended or in differential mode.		
				3	OUT0BN.		
				4	OUT0CP. Select this mode if OUT0C is single-ended or in differential mode.		
				5	OUT0CN.		
0x1203	Feedback mode	7	Profile 0.0 loop filter base		Profile 0.0 loop filter base coefficients. This bit controls the set of loop filter coefficients used for DPLL0 Profile 0.	0x0	R/W
				0	Nominal phase margin (~70°).		
				1	High phase margin (~88.5°). Use this setting for applications that require no more than 0.1 dB of peaking in the DPLL closed-loop transfer function.		
		[6:5]	Reserved		Reserved.	0x0	R/W
		[4:2]	Profile 0.0 tag mode		Profile 0.0 tag mode. This 3-bit bit field configures the Profile 0.0 tag mode.	0x0	R/W
				0	Neither the reference nor feedback path contains tagged events.		
				1	Only the reference path is tagged.		
				2	Only the feedback path is tagged.		
				3	Both reference and feedback paths are tagged, but the untagged rates are unequal.		
				4	Both reference and feedback paths are tagged, and the untagged rates are equal.		
		1	Enable Profile 0.0 external zero delay		Enable DPLL0 Profile 0 external zero delay mode. Setting this bit to Logic 1 enables the DPLL0 Profile 0 external zero delay path for hitless mode.	0x0	R/W
		0	Enable Profile 0.0 hitless		Enable Profile 0.0 hitless operation.	0x0	R/W
				0	Selects the default phase buildout mode for DPLL0 Profile 0.		
				1	Enables hitless mode for DPLL0 Profile 0. Enable this bit for zero delay operation.		
0x1204	Loop bandwidth	[7:0]	Profile 0.0 loop bandwidth [7:0]		DPLL0 Profile 0 loop bandwidth. This 32-bit bit field is the DPLL loop bandwidth scaling factor. The default units for this bit field are microseconds (10 sec to 6 sec).	0x0	R/W
0x1205		[7:0]	Profile 0.0 loop bandwidth [15:8]			0x0	R/W
0x1206		[7:0]	Profile 0.0 loop bandwidth [23:16]			0x0	R/W
0x1207		[7:0]	Profile 0.0 loop bandwidth [31:24]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1208	Hitless feedback divider	[7:0]	Profile 0.0 hitless N-divider [7:0]		Profile 0.0 feedback divider in hitless mode. This 32-bit bit field is the DPLL0 feedback divide ratio while DPLL0 is in hitless mode. The feedback divide ratio is the value stored in this bit field plus one.	0xA0	R/W
0x1209		[7:0]	Profile 0.0 hitless N-divider [15:8]			0xF	R/W
0x120A		[7:0]	Profile 0.0 hitless N-divider [23:16]			0x0	R/W
0x120B		[7:0]	Profile 0.0 hitless N-divider [31:24]			0x0	R/W
0x120C	Buildout feedback divider	[7:0]	Profile 0.0 buildout N-divider [7:0]		DPLL0 Profile 0 buildout N-divide ratio. This 32-bit bit field is the integer portion of the DPLL feedback divide ratio while DPLL0 is in phase buildout mode. It is also referred to as the N-divider in the AD9543 data sheet.	0xA0	R/W
0x120D		[7:0]	Profile 0.0 buildout N-divider [15:8]			0xF	R/W
0x120E		[7:0]	Profile 0.0 buildout N-divider [23:16]			0x0	R/W
0x120F		[7:0]	Profile 0.0 buildout N-divider [31:24]			0x0	R/W
0x1210	Buildout feedback fraction	[7:0]	Profile 0.0 buildout fraction [7:0]		DPLL0 Profile 0 feedback divider fraction in buildout mode. This 24-bit bit field is the numerator of the DPLL fractional feedback divider while DPLL0 is in phase buildout mode. It is also referred to as FRAC in the AD9543 data sheet.	0x0	R/W
0x1211		[7:0]	Profile 0.0 buildout fraction [15:8]			0x0	R/W
0x1212		[7:0]	Profile 0.0 buildout fraction [23:16]			0x0	R/W
0x1213	Buildout feedback modulus	[7:0]	Profile 0.0 buildout modulus [7:0]		DPLL0 Profile 0 feedback divider modulus in buildout mode. This 24-bit bit field is the denominator of the DPLL fractional feedback divider while DPLL0 is in phase buildout mode. It is also referred to as MOD in the AD9543 data sheet.	0x0	R/W
0x1214		[7:0]	Profile 0.0 buildout modulus [15:8]			0x0	R/W
0x1215		[7:0]	Profile 0.0 buildout modulus [23:16]			0x0	R/W
0x1216	Fast lock	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Profile 0.0 fast acquisition excess bandwidth		DPLL0 Profile 0 fast acquisition excess bandwidth. This 4-bit bit field controls the DPLL0 loop bandwidth scaling factor (relative to the programmed DPLL loop bandwidth) while in fast acquisition mode. The DPLL automatically reduces the loop bandwidth by successive factors of 2 while the loop is acquiring. Setting this bit field to 0000b disables the feature.	0x0	R/W
				0	Feature disabled.		
				1	2×. The initial loop bandwidth is 2× the programmed value.		
				10	4×. The initial loop bandwidth is 4× the programmed value.		
				11	8×. The initial loop bandwidth is 8× the programmed value.		
				100	16×. The initial loop bandwidth is 16× the programmed value.		
				101	32×. The initial loop bandwidth is 32× the programmed value.		
				110	64×. The initial loop bandwidth is 64× the programmed value.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				111	128×. The initial loop bandwidth is 128× the programmed value.		
				1000	256×. The initial loop bandwidth is 256× the programmed value.		
				1001	512×. The initial loop bandwidth is 512× the programmed value.		
				1010	1024×. The initial loop bandwidth is 1024× the programmed value.		
0x1217		7	Reserved		Reserved.	0x0	R
		[6:4]	Profile 0.0 fast acquisition timeout		DPLL0 Profile 0 fast acquisition timeout. This 3-bit bit field controls the maximum amount of time that DPLL0 waits to achieve phase lock (without chatter) before reducing the loop bandwidth by a factor of two while in fast acquisition mode. This feature prevents the fast acquisition algorithm from stalling in the event that lock is not achieved during the fast acquisition process.	0x0	R/W
				0	1 ms.		
				1	10 ms.		
				10	50 ms.		
				11	100 ms.		
				100	500 ms.		
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Profile 0.0 fast acquisition lock settle time		DPLL0 Profile 0 fast acquisition lock settle time. This 3-bit bit field controls how long DPLL0 must wait after achieving phase lock (without chatter) before reducing the loop bandwidth by a factor of 2 while in fast acquisition mode. If the lock detector chatters, this timer is reset.	0x0	R/W
				0	1 ms.		
				1	10 ms.		
				10	50 ms.		
				11	100 ms.		
				100	500 ms.		
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		

DPLL CHANNEL 1 REGISTERS—REGISTER 0x1400 TO REGISTER 0x142A

Table 63. DPLL Channel 1 Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1400	Freerun tuning word	DPLL1 freerun tuning word [7:0]								0x00	R/W
0x1401		DPLL1 freerun tuning word [15:8]								0x00	R/W
0x1402		DPLL1 freerun tuning word [23:16]								0x00	R/W
0x1403		DPLL1 freerun tuning word [31:24]								0x00	R/W
0x1404		DPLL1 freerun tuning word [39:32]								0x00	R/W
0x1405		Reserved		DPLL1 freerun tuning word [45:40]						0x00	R/W
0x1406	Tuning word clamp	DPLL1 freerun tuning word offset clamp [7:0]								0xFF	R/W
0x1407		DPLL1 freerun tuning word offset clamp [15:8]								0xFF	R/W
0x1408		DPLL1 freerun tuning word offset clamp [23:16]								0xFF	R/W
0x1409	NCO gain	Reserved				DPLL1 NCO gain filter bandwidth				0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x140A	History accumulation timer	DPLL1 history accumulation timer [7:0]								0x0A	R/W
0x140B		DPLL1 history accumulation timer [15:8]								0x00	R/W
0x140C		DPLL1 history accumulation timer [23:16]								0x00	R/W
0x140D		Reserved				DPLL1 history accumulation timer [27:24]				0x00	R/W
0x140E		Reserved		DPLL1 delay history while not phase slew limiting	DPLL1 delay history frequency lock	DPLL1 delay history phase lock	DPLL1 quick start history	DPLL1 single sample history	DPLL1 persistent history	0x38	R/W
0x140F		Reserved					DPLL1 pause history while phase slew limiting	DPLL1 pause history frequency unlocked	DPLL1 pause history phase unlocked	0x00	R/W
0x1410	History accumulation hold off	DPLL1 history hold off time								0x00	R/W
0x1411	Phase slew limit	DPLL1 phase slew limit rate [7:0]								0x00	R/W
0x1412		DPLL1 phase slew limit rate [15:8]								0x00	R/W
0x1413		DPLL1 phase slew limit rate [23:16]								0x00	R/W
0x1414		DPLL1 phase slew limit rate [31:24]								0x06	R/W
0x1415	Phase offset	DPLL1 phase offset [7:0]								0x00	R/W
0x1416		DPLL1 phase offset [15:8]								0x00	R/W
0x1417		DPLL1 phase offset [23:16]								0x00	R/W
0x1418		DPLL1 phase offset [31:24]								0x00	R/W
0x1419		DPLL1 phase offset [39:32]								0x00	R/W
0x141A	Phase temperature compensation polynomial	DPLL1 phase temperature compensation C_1 significand [7:0]								0x00	R/W
0x141B		DPLL1 phase temperature compensation C_1 significand [15:8]								0x00	R/W
0x141C		DPLL1 phase temperature compensation C_1 exponent								0x00	R/W
0x141D		DPLL1 phase temperature compensation C_2 significand [7:0]								0x00	R/W
0x141E		DPLL1 phase temperature compensation C_2 significand [15:8]								0x00	R/W
0x141F		DPLL1 phase temperature compensation C_2 exponent								0x00	R/W
0x1420		DPLL1 phase temperature compensation C_3 significand [7:0]								0x00	R/W
0x1421		DPLL1 phase temperature compensation C_3 significand [15:8]								0x00	R/W
0x1422		DPLL1 phase temperature compensation C_3 exponent								0x00	R/W
0x1423		DPLL1 phase temperature compensation C_4 significand [7:0]								0x00	R/W
0x1424		DPLL1 phase temperature compensation C_4 significand [15:8]								0x00	R/W
0x1425		DPLL1 phase temperature compensation C_4 exponent								0x00	R/W
0x1426		DPLL1 phase temperature compensation C_5 significand [7:0]								0x00	R/W
0x1427		DPLL1 phase temperature compensation C_5 significand [15:8]								0x00	R/W
0x1428		DPLL1 phase temperature compensation C_5 exponent								0x00	R/W
0x1429	Phase adjust filter bandwidth	Reserved					DPLL1 phase temperature compensation filter bandwidth			0x00	R/W
0x142A	Inactive profile	Reserved					DPLL1 inactive profile index			0x00	R/W

Table 64. DPLL Channel 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1400	Freerun tuning word	[7:0]	DPLL1 freerun tuning word [7:0]		DPLL1 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL1 while it is in freerun mode.	0x0	R/W
0x1401		[7:0]	DPLL1 freerun tuning word [15:8]			0x0	R/W
0x1402		[7:0]	DPLL1 freerun tuning word [23:16]			0x0	R/W
0x1403		[7:0]	DPLL1 freerun tuning word [31:24]			0x0	R/W
0x1404		[7:0]	DPLL1 freerun tuning word [39:32]			0x0	R/W
0x1405		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL1 freerun tuning word [45:40]		DPLL1 freerun tuning word. This 46-bit bit field is the frequency tuning word used by DPLL1 while it is in freerun mode.	0x0	R/W
0x1406	Tuning word clamp	[7:0]	DPLL1 freerun tuning word offset clamp [7:0]		DPLL1 freerun tuning word offset clamp. This 24-bit bit field sets the DPLL1 tuning word offset clamp, f_{CLAMP}. The formula is f_{CLAMP} = DPLL1 freerun tuning word offset clamp × ($f_S/2^{36}$), where f_S is the system clock frequency.	0xFF	R/W
0x1407		[7:0]	DPLL1 freerun tuning word offset clamp [15:8]			0xFF	R/W
0x1408		[7:0]	DPLL1 freerun tuning word offset clamp [23:16]			0xFF	R/W
0x1409	NCO gain	[7:4]	Reserved		Reserved.	0x0	R/W
		[3:0]	DPLL1 NCO gain filter bandwidth		DPLL1 NCO gain freerun tuning word filter bandwidth. This 4-bit bit field controls the low-pass filter −3 dB cutoff frequency of the DPLL1 NCO.	0x0	R/W
				0x0	250 kHz (maximum).		
				0x1	120 kHz.		
				0x2	62 kHz.		
				0x3	31 kHz.		
				0x4	16 kHz.		
				0x5	7.8 kHz.		
				0x6	3.9 kHz.		
				0x7	1.9 kHz.		
				0x8	970 Hz.		
				0x9	490 Hz.		
				0xA	240 Hz.		
				0xB	120 Hz.		
				0xC	61 Hz.		
				0xD	30 Hz.		
				0xE	15 Hz.		
				0xF	7.6 Hz (minimum).		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x140A	History accumulation timer	[7:0]	DPLL1 history accumulation timer [7:0]		DPLL1 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the AD9543 data sheet. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and behavior is undefined for a timer value of 0x0000.	0xA	R/W
0x140B	History accumulation timer	[7:0]	DPLL1 history accumulation timer [15:8]			0x0	R/W
0x140C	History accumulation timer	[7:0]	DPLL1 history accumulation timer [23:16]			0x0	R/W
0x140D		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 history accumulation timer [27:24]		DPLL1 history accumulation timer. This 28-bit bit field is the duration of the averaging period (in milliseconds) and calculates the holdover tuning word value. It is referred to as t_{HAT} in the AD9543 data sheet. The allowable range is 1 ms to 268,435.455 sec (approximately 74.5 hours), and behavior is undefined for a timer value of 0x0000.	0x0	R/W
0x140E		[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 delay history while not phase slew limiting		DPLL1 delay history while not phase slew limiting. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL1 phase slew limiter is inactive. At that point, the tuning word averaging is further delayed by the value in the DPLL1 history hold off time. This bit is intended to ensure that holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase slew limiter.	0x1	R/W
		4	DPLL1 delay history frequency lock		DPLL1 delay history until frequency lock. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL1 is frequency locked. At that point, the tuning word averaging is further delayed by the value in the DPLL1 history hold off time. This bit is intended to ensure that holdover history accumulation begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the frequency lock detector.	0x1	R/W
		3	DPLL1 delay history phase lock		DPLL1 delay history until phase lock. Setting this bit to Logic 1 delays the tuning word history averaging during acquisition until the DPLL1 is phase locked. At that point, the tuning word averaging is further delayed by the value in the DPLL1 history hold off time. This bit is intended to ensure that holdover history averaging begins only when the DPLL is fully settled. When this bit is Logic 0, the history averaging is not contingent on the state of the phase lock detector.	0x1	R/W
		2	DPLL1 quick start history		DPLL1 quick start history. Setting this bit to Logic 1 allows the DPLL1 tuning word history to be available in 1/4 of the time specified in the DPLL1 history accumulation timer. This bit is intended to ensure that there is sufficient holdover history in cases where the DPLL has been locked to a reference for a short period.	0x0	R/W
		1	DPLL1 single sample history		DPLL1 single sample history. Setting this bit to Logic 1 allows DPLL1 to use the most recent tuning word for holdover in the event that the tuning word history is not available. This bit can be used in conjunction with the quick start history bit in this register. This bit is intended to ensure that there is a minimal holdover history available in cases where the DPLL has been locked to a reference for a short period.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	DPLL1 persistent history		DPLL1 persistent history. Setting this bit to Logic 1 allows the DPLL1 tuning word history to not be reset if there is an interruption in the tuning word averaging. This bit is intended to ensure that there is sufficient holdover history in cases where the DPLL has been locked to a reference for a short period. When this bit is Logic 0, the history accumulation resets when the DPLL exits holdover and reacquires.	0x0	R/W
0x140F	History accumulation timer	[7:3]	Reserved		Reserved.	0x0	R
		2	DPLL1 pause history while phase slew limiting		DPLL1 pause history while phase slew limiting. Setting this bit to Logic 1 pauses the tuning word history averaging when DPLL1 is phase slewing. The tuning word history is reset when the DPLL regains phase lock if the persistent history bit is Logic 0. This bit is intended to ensure that tuning word history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase slewing.	0x0	R/W
		1	DPLL1 pause history frequency unlocked		DPLL1 pause history while frequency unlocked. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when DPLL1 is frequency unlocked. The holdover history is reset when the DPLL regains frequency lock if the persistent history bit is Logic 0. This bit is intended to ensure that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of frequency lock status.	0x0	R/W
		0	DPLL1 pause history phase unlocked		DPLL1 pause history while phase unlocked. Setting this bit to Logic 1 pauses the holdover tuning word history averaging when DPLL1 phase slew limiter is active. The holdover history is reset when the DPLL is no longer phase slew limited if the persistent history bit is Logic 0. This bit is intended to ensure that holdover history averaging occurs only when the DPLL is fully settled. When this bit is Logic 0, the history averaging occurs regardless of phase lock status.	0x0	R/W
0x1410	History accumulation hold off	[7:0]	DPLL1 history hold off time		DPLL1 history hold off time. This 8-bit bit field is the amount of time (in milliseconds) that the DPLL tuning word history accumulation is delayed. Hold off is disabled if this bit field is 0x00.	0x0	R/W
0x1411	Phase slew limit	[7:0]	DPLL1 phase slew limit rate [7:0]		DPLL1 phase slew limit rate. This 28-bit bit field is the DPLL1 phase slew limit rate (in picoseconds/second). It is referred to as t_{OFST} in the AD9543 data sheet.	0x0	R/W
0x1412		[7:0]	DPLL1 phase slew limit rate [15:8]			0x0	R/W
0x1413		[7:0]	DPLL1 phase slew limit rate [23:16]			0x0	R/W
0x1414		[7:0]	DPLL1 phase slew limit rate [31:24]			0x6	R/W
0x1415	Phase offset	[7:0]	DPLL1 phase offset [7:0]		DPLL1 closed-loop phase offset. This signed, 40-bit bit field is the DPLL1 closed-loop phase offset (in picoseconds). It is referred to as t_{OFST} in the AD9543 data sheet	0x0	R/W
0x1416		[7:0]	DPLL1 phase offset [15:8]			0x0	R/W
0x1417		[7:0]	DPLL1 phase offset [23:16]			0x0	R/W
0x1418		[7:0]	DPLL1 phase offset [31:24]			0x0	R/W
0x1419		[7:0]	DPLL1 phase offset [39:32]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x141A	Phase temperature compensation polynomial	[7:0]	DPLL1 phase temperature compensation C_1 significand [7:0]		DPLL1 temperature compensation C_1 significand. This 10-bit bit field is the significand for the C_1 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x141B		[7:0]	DPLL1 phase temperature compensation C_1 significand [15:8]			0x0	R/W
0x141C		[7:0]	DPLL1 phase temperature compensation C_1 exponent		DPLL1 temperature compensation C_1 exponent. This 6-bit bit field is the exponent for the C_1 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x141D		[7:0]	DPLL1 phase temperature compensation C_2 significand [7:0]		DPLL1 temperature compensation C_2 significand. This 10-bit bit field is the significand for the C_2 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x141E		[7:0]	DPLL1 phase temperature compensation C_2 significand [15:8]			0x0	R/W
0x141F		[7:0]	DPLL1 phase temperature compensation C_2 exponent		DPLL1 temperature compensation C_2 exponent. This 6-bit bit field is the exponent for the C_2 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1420		[7:0]	DPLL1 phase temperature compensation C_3 significand [7:0]		DPLL1 temperature compensation C_3 significand. This 10-bit bit field is the significand for the C_3 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1421		[7:0]	DPLL1 phase temperature compensation C_3 significand [15:8]			0x0	R/W
0x1422		[7:0]	DPLL1 phase temperature compensation C_3 exponent		DPLL1 temperature compensation C_3 exponent. This 6-bit bit field is the exponent for the C_3 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1423		[7:0]	DPLL1 phase temperature compensation C_4 significand [7:0]		DPLL1 temperature compensation C_4 significand. This 10-bit bit field is the significand for the C_4 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1424		[7:0]	DPLL1 phase temperature compensation C_4 significand [15:8]			0x0	R/W
0x1425		[7:0]	DPLL1 phase temperature compensation C_4 exponent		DPLL1 temperature compensation C_4 exponent. This 6-bit bit field is the exponent for the C_4 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1426		[7:0]	DPLL1 phase temperature compensation C_5 significand [7:0]		DPLL1 temperature compensation C_5 significand. This 10-bit bit field is the significand for the C_5 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W
0x1427		[7:0]	DPLL1 phase temperature compensation C_5 significand [15:8]			0x0	R/W
0x1428		[7:0]	DPLL1 phase temperature compensation C_5 exponent		DPLL1 temperature compensation C_5 exponent. This 6-bit bit field is the exponent for the C_5 coefficient of the DPLL1 temperature compensation polynomial.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1429	Phase adjust filter bandwidth	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL1 phase temperature compensation filter bandwidth		DPLL1 temperature compensation low-pass filter bandwidth. This 3-bit bit field controls the low-pass filter −3 dB cutoff frequency of the DPLL1 delay compensation block.	0x0	R/W
				0x0	240 Hz (maximum).		
				0x1	120 Hz.		
				0x2	60 Hz.		
				0x3	30 Hz.		
				0x4	15 Hz.		
				0x5	7.6 Hz.		
				0x6	3.8 Hz.		
				0x7	1.9 Hz (minimum).		
0x142A	Inactive profile	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	DPLL1 inactive profile index		DPLL1 inactive profile index. The inactive profile index is used while DPLL1 is in holdover to retain the exact DPLL configuration, including the desired input/output phase relationship.	0x0	R/W

APLL CHANNEL 1 REGISTERS—REGISTER 0x1480 TO REGISTER 0x1483

Table 65. APLL Channel 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1480	Charge pump current	Enable APLL1 manual charge pump current	APLL1 manual charge pump current							0x90	R/W
0x1481	M1 divider	APLL1 M1 feedback divider								0x00	R/W
0x1482	Loop filter control	APLL1 loop filter zero resistor (R1)			APLL1 loop filter pole capacitor (C2)			APLL1 loop filter second pole resistor (R3)		0xE0	R/W
0x1483	DC offset current	Reserved				APLL1 dc offset current direction	APLL1 dc offset current value		Enable APLL1 dc offset current	0x03	R/W

Table 66. APLL Channel 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1480	Charge pump current	7	Enable APLL1 manual charge pump current		Enables manual control of the APLL 1 charge pump current.	0x0	R/W
				0	Disable manual charge pump current control. Disables manual control of the APLL1 charge pump current.		
				1	Enable manual charge pump current control. Enables manual control of the APLL1 charge pump current.		
		[6:0]	APLL1 manual charge pump current		APLL1 manual charge pump current. LSB = 3.5 μA. The user must set the enable manual charge pump current control bit in this register for this setting to be enabled.	0x0	R/W
				0000001b	1 × LSB.		
				0000010b	2 × LSB.		
				1111111b	127 × LSB.		
0x1481	M1 divider	[7:0]	APLL1 M1 feedback divider		APLL multiplication ratio. APLL1 M1 feedback divide ratio. Allowable values are 14 to 255.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1482	Loop filter control	[7:5]	APLL1 loop filter zero resistor (R1)		Loop Filter R1. APLL1 Loop Filter R1 (zero resistor) value.	0x0	R/W
				000	0 Ω (short).		
				001	250 Ω.		
				010	500 Ω.		
				011	750 Ω.		
				100	1.00 kΩ.		
				101	1.25 kΩ.		
				110	1.50 kΩ.		
				111	1.75 kΩ.		
		[4:2]	APLL1 loop filter pole capacitor (C2)		Loop Filter C2. APLL1 Loop Filter C2 (pole capacitor) value.	0x0	R/W
				000	8 pF.		
				001	24 pF.		
				010	40 pF.		
				011	56 pF.		
				100	72 pF.		
				101	88 pF.		
				110	104 pF.		
				111	120 pF.		
		[1:0]	APLL1 loop filter second pole resistor (R3)		Loop Filter R3. APLL1 Loop Filter R3 (second pole resistor) value.	0x0	R/W
				00	200 Ω.		
				01	250 Ω.		
				10	333 Ω.		
				11	500 Ω.		
0x1483	DC offset current	[7:4]	Reserved		Reserved.	0x0	R
		3	APLL1 dc offset current direction		DC offset current direction. This bit sets the direction of the APLL1 dc offset current.	0x0	R/W
				0	Up. DC offset current offset is positive.		
				1	Down. DC offset current offset is negative.		
		[2:1]	APLL1 dc offset current value		DC offset current. magnitude of the APLL1 charge pump dc offset current value.	0x0	R/W
				00	50% offset current. Offset current is 50% of the programmed APLL1 charge pump current (default).		
				01	25% offset current. Offset current is 25% of the programmed APLL1 charge pump current.		
				10	12.5% offset current. Offset current is 12.5% of the programmed APLL1 charge pump current.		
				11	6.25% offset current. Offset current is 6.25% of the programmed APLL1 charge pump current.		
		0	Enable APLL1 dc offset current		DC offset current enable. Setting this bit enables the APLL1 dc offset current.	0x0	R/W

DISTRIBUTION GENERAL 1 REGISTERS—REGISTER 0x14C0 TO REGISTER 0x14DC

Table 67. Distribution General 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x14C0	Modulation step	Modulation step [7:0]								0x00	R/W
0x14C1		Modulation step [15:8]								0x00	R/W
0x14C2	Modulation Counter A	Q1A modulation counter [7:0]								0x00	R/W
0x14C3		Q1A modulation counter [15:8]								0x00	R/W
0x14C4		Q1A modulation counter [23:16]								0x00	R/W
0x14C5		Reserved				Q1A modulation counter [27:24]				0x00	R/W
0x14C6	Modulation Counter B	Q1B modulation counter [7:0]								0x00	R/W
0x14C7		Q1B modulation counter [15:8]								0x00	R/W
0x14C8		Q1B modulation counter [23:16]								0x00	R/W
0x14C9		Reserved				Q1B modulation counter [27:24]				0x00	R/W
0x14CE	FB clock sync edge	Reserved						Feedback divider sync edge		0x00	R/W
0x14CF	Modulator A settings	Reserved				Enable Q1A N-shot modulator	Enable Q1A single-pulse modulator	Q1A modulator polarity	Enable Q1A modulator	0x00	R/W
0x14D0	Modulator B settings	Reserved				Enable Q1B N-shot modulator	Enable Q1B single-pulse modulator	Q1B modulator polarity	Enable Q1B modulator	0x00	R/W
0x14D2	N-shot gaps	N-shot gap								0x00	R/W
0x14D3	N-shot request	Reserved	N-shot request mode	N-shot						0x00	R/W
0x14D4	N-shot enable	Enable PRBS Q1BB	Enable Q1BB N-shot	Enable PRBS Q1B	Enable Q1B N-shot	Enable PRBS Q0AA	Enable Q1AA N-shot	Enable PRBS Q1A	Enable Q1A N-shot	0x00	R/W
0x14D6	N-shot retime	Reserved							Enable N-shot retime	0x00	R/W
0x14D7	Driver A configuration	Reserved		Bypass mute retiming Channel A	OUT1A driver mode		OUT1A driver current		Enable OUT1A HCSL	0x01	R/W
0x14D8	Driver B configuration	Reserved		Bypass mute retiming Channel B	OUT1B driver mode		OUT1B driver current		Enable OUT1B HCSL	0x01	R/W
0x14DA	Secondary clock path	Reserved					Enable SYSCLK Q0B	Enable SYSCLK Q0A	Enable SYSCLK Sync Mask	0x00	R/W
0x14DB	Sync control	Reserved					Enable DPLL1 reference sync	Autosync mode		0x00	R/W
0x14DC	Automute control	Reserved		Mask OUT1BB autounmute	Mask OUT1B autounmute	Mask OUT1AA autounmute	Mask OUT1A autounmute	DPLL1 autounmute mode		0x00	R/W

Table 68. Distribution General 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x14C0	Modulation step	[7:0]	Modulation step [7:0]		Modulation step. This 16-bit bit field controls the duty cycle step, which is the duty cycle deviation of a modulation event. The unit is the number of distribution clock half cycles.	0x0	R/W
0x14C1		[7:0]	Modulation step [15:8]			0x0	R/W
0x14C2	Modulation Counter A	[7:0]	Q1A modulation counter [7:0]		Q1A modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x14C3		[7:0]	Q1A modulation counter [15:8]			0x0	R/W
0x14C4		[7:0]	Q1A modulation counter [23:16]			0x0	R/W
0x14C5		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Q1A modulation counter [27:24]		Q1A modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x14C6	Modulation Counter B	[7:0]	Q1B modulation counter [7:0]		Q1B modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x14C7		[7:0]	Q1B modulation counter [15:8]			0x0	R/W
0x14C8		[7:0]	Q1B modulation counter [23:16]			0x0	R/W
0x14C9		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Q1B modulation counter [27:24]		Q1B modulation counter. This bit field sets the embedded clock frequency by controlling the count between modulation events on the modulation enabled dividers. The unit is Q divider cycles.	0x0	R/W
0x14CE	Feedback clock sync edge	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Feedback divider sync edge		Feedback divider sync edge. This bit field is only used when embedded output clock modulation is turned on, and allows the user to delay the synchronization edge (relative to the modulation base edge) of the feedback divider. Allowable values (in decimal) are 0, 1, 2, or 3 clock edges.	0x0	R/W
0x14CF	Modulator A settings	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable Q1A N-shot modulator		Enable Q1A modulator N-shot. Setting this bit to Logic 1 enables the embedded clock modulator controller to use the N-shot request signal to trigger five modulation events when N-shot request mode bit is Logic 0 (edge triggered) or continuously when the N-shot request mode bit is Logic 1 (level sensitive).	0x0	R/W
		2	Enable Q1A single-pulse modulation		Single-pulse modulation.	0x0	R/W
				0	dc balanced duty cycle modulation.		
				1	Single-pulse modulation.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	Q1A modulation polarity		Modulation polarity. This bit sets the type of (duty cycle) modulation event.	0x0	R/W
				0	The first modulated falling edge occurs earlier than nominal. In dc balanced mode, the second modulated falling edge occurs later than nominal.		
				1	The first modulated falling edge occurs later than nominal. In dc balanced mode, the second modulated falling edge occurs earlier than nominal.		
		0	Enable Q1A modulator		Enable embedded clock modulator. Setting this bit to Logic 1 enables the embedded clock (pulse width/duty cycle) modulation.	0x0	R/W
0x14D0	Modulator B settings	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable Q1B N-shot modulator		Enable Q1B modulator N-shot. Setting this bit to Logic 1 enables the embedded clock modulator controller to use the N-shot request signal to trigger five modulation events when N-shot request mode bit is Logic 0 (edge triggered) or continuously when the N-shot request mode bit is Logic 1 (level sensitive).	0x0	R/W
		2	Enable Q1B single-pulse modulation		Single-pulse modulation.	0x0	R/W
				0	DC balanced duty cycle modulation.		
				1	Single-pulse modulation.		
		1	Q1B modulation polarity		Modulation polarity. This bit sets the type of (duty cycle) modulation event.	0x0	R/W
				0	The first modulated falling edge occurs earlier than nominal. In dc balanced mode, the second modulated falling edge occurs later than nominal.		
				1	The first modulated falling edge occurs later than nominal. In dc balanced mode, the second modulated falling edge occurs earlier than nominal.		
		0	Enable Q1B modulator		Enable embedded clock modulator. Setting this bit to Logic 1 enables the embedded clock (pulse width/duty cycle) modulator.	0x0	R/W
0x14D2	N-shot gaps	[7:0]	N-shot gap		N-shot gap. This unsigned, 8-bit bit field contains the length (measured in Q divider output cycles) of the gap in a JESD204B N-shot pattern generation.	0x0	R/W
0x14D3	N-shot request	7	Reserved		Reserved.	0x0	R
		6	N-shot request mode		Channel 0 N-shot request mode.	0x0	R/W
				1	The N-shot generators operate in burst mode, and the rising edge of the trigger signal initiates the burst.		
				0	The N-shot generators operate in period gapped mode. In this mode, N-shot bursts occur as long as the trigger is in a Logic 1 state; for this reason, it is referred to as a level sensitive trigger mode.		
		[5:0]	N-shot		Number of clock pulses in an N-shot burst. This unsigned, 6-bit bit field contains the number of clock cycles in an N-shot burst.	0x0	R/W
0x14D4	N-shot enable	7	Enable Q1BB PRBS		Q1BB JESD204B PRBS Enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at divider output rate.	0x0	R/W
		6	Enable Q1BB N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
		5	Enable Q1B PRBS		Q1B JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	Enable Q1B N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
		3	Enable Q1AA PRBS		Q1AA JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		2	Enable Q1AA N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
		1	Enable Q1A PRBS		Q1A JESD204B PRBS enable. Setting this bit to Logic 1 enables the pseudorandom bit sequence clocked at the divider output rate.	0x0	R/W
		0	Enable Q1A N-shot		N-shot enable.	0x0	R/W
				0	JESD204B N-shot mode disabled.		
				1	JESD204B N-shot mode enabled. The output is muted until a user programmed N-shot burst is requested, which can be periodic. The associated Q divider must be ≥8.		
0x14D6	N-shot retime	[7:1]	Reserved		Reserved.	0x0	R
		0	Enable N-shot retime		Enable N-shot retiming.	0x0	R/W
				0	Mx pins or registers (user-selectable) provide the JESD204B N-shot retiming source.		
				1	The N short retiming block provides the JESD204B N-shot retiming source.		
0x14D7	Driver A configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel A		Removes retiming from Channel A mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function, and mutes the channel immediately.	0x0	R/W
		[4:3]	OUT1A driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q0A determines the divide ratio.		
				1	Dual- or single-ended output driven by Divider Q0A. Divider Q0A determines the divide ratio.		
				10	Dual- or single-ended output driven by separate Q dividers. Both Divider Q0A and Divider Q0AA are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT1A driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT1A HCSL		Selects HCSL or CML mode.	0x0	R/W
				0	CML mode. An external pull-up resistor is required.		
				1	HCSL mode. An external pull-down resistor is required.		
0x14D8	Driver B configuration	[7:6]	Reserved		Reserved.	0x0	R
		5	Bypass mute retiming Channel B		Removes retiming from Channel B mute. In normal operation, this bit is Logic 0, and the signal to mute an output channel is retimed so that runt pulses are avoided. Setting this bit to Logic 1 removes the retiming function and mutes the channel immediately.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:3]	OUT1B driver mode		Selects single-ended or differential output mode.	0x0	R/W
				0	Differential output. Divider Q1B determines the divide ratio.		
				1	Dual-, single-ended output driven by Divider Q1A. Divider Q1B determines the divide ratio.		
				10	Dual-, single-ended output driven by separate Q dividers. Both Divider Q1B and Divider Q1BB are enabled, although it is recommended that they have the same divide ratio.		
		[2:1]	OUT1B driver current		Output driver current. This current setting applies to both the normal and complementary output pins.	0x0	R/W
				0	7.5 mA.		
				1	12.5 mA.		
				10	15 mA.		
		0	Enable OUT1B HCSL		Selects HCSL or CML mode.	0x0	R/W
				0	CML mode. An external pull-up resistor is required.		
				1	HCSL mode. An external pull-down resistor is required.		
0x14DA	Secondary clock path	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable SYSCLK Q1B		Enable SYSCLK to Divider Q1B. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q1B.	0x0	R/W
		1	Enable SYSCLK Q1A		Enable SYSCLK to Divider Q1A. Setting this bit to Logic 1 enables a buffered copy of the system clock to Divider Q1A.	0x0	R/W
		0	Enable SYSCLK sync mask		Enable SYSCLK sync mask. Setting this bit to Logic 1 ensures that no sync events occur on outputs that are assigned to outputting the SYSCLK. This purpose of this feature is to ensure that no runt pulses or stalled clocks occur when a SYSCLK output clocks a microprocessor. Set this bit to Logic 1 only when the SYSCLK is fully configured and stable, because runt pulses can occur while configuring the SYSCLK.	0x0	R/W
0x14DB	Sync control	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable DPLL1 reference sync		DPLL1 reference sync enable. Setting this bit to Logic 1 enables automatic reference synchronization on DPLL1. Reference sync works only when a hitless translation profile is active. Reference sync does not occur when a phase buildout profile is active.	0x0	R/W
		[1:0]	Autosync mode		Autosync mode. This bit field controls when the clock distribution block receives a synchronization event. The output drivers do not toggle until there is a synchronization event.	0x0	R/W
				0	Manual sync. Automatic output synchronization disabled. In this mode, the user must issue a clock distribution synchronization command manually.		
				1	Immediate. Output synchronization occurs immediately after APLL lock.		
				10	DPLL phase lock. Output synchronization occurs when the DPLL phase locks.		
				11	DPLL frequency lock. Output synchronization occurs when the DPLL frequency locks.		
0x14DC	Automute control	[7:6]	Reserved		Reserved	0x0	R/W
		5	Mask OUT1BB autounmute		Mask OUT1BB autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	Mask OUT1B autounmute		Mask OUT1B autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		3	Mask OUT1AA autounmute		Mask OUT1AA autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		2	Mask OUT1A autounmute		Mask OUT1A autounmute.	0x0	R/W
				0	Normal operation. Automatic unmuting of the driver works in conjunction with the autounmute mode.		
				1	The automatic unmuting conditions are ignored and the driver is unmuted immediately.		
		[1:0]	DPLL1 autounmute mode		DPLL1 autounmute mode. This bit field controls at which point the output drivers start to toggle during acquisition while DPLL1 is in hitless mode.	0x0	R/W
				0	Disabled. Automatic unmuting is disabled and the output driver starts toggling immediately.		
				1	Hitless acquisition. Automatic driver unmuting occurs upon activation of a hitless profile.		
				10	Phase lock detect (PLD) (hitless mode only). Automatic driver unmuting occurs when phase lock is detected and the DPLL is in hitless mode.		
				11	Frequency lock detect (FLD) (hitless mode only). Automatic driver unmuting occurs when frequency lock is detected and the DPLL is in hitless mode.		

DISTRIBUTION DIVIDER 1 A REGISTERS—REGISTER 0x1500 TO REGISTER 0x1508

Table 69. Distribution Divider 1 A Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1500	Divider ratio	Q1A divider ratio [7:0]								0x00	R/W
0x1501		Q1A divider ratio [15:8]								0x00	R/W
0x1502		Q1A divider ratio [23:16]								0x00	R/W
0x1503		Q1A divider ratio [31:24]								0x00	R/W
0x1504	Phase offset	Q1A phase [7:0]								0x00	R/W
0x1505		Q1A phase [15:8]								0x00	R/W
0x1506		Q1A phase [23:16]								0x00	R/W
0x1507		Q1A phase [31:24]								0x00	R/W
0x1508	Phase slew configuration	Reserved	Q1A phase[32]	Enable Q1A half divide	Enable Q1A pulse width control	Q1A phase slew mode	Maximum phase slew step			0x07	R/W

Table 70. Distribution Divider 1 AA Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1509 to 0x1511		These registers mimic the Distribution Divider 1A registers (Register 0x1500 through Register 0x1508), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 71. Distribution Divider 1 B Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1512 to 0x151A		These registers mimic the Distribution Divider 1A registers (Register 0x1500 through Register 0x1508), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 72. Distribution Divider 1 BB Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x151B to 0x1523		These registers mimic the Distribution Divider 1A registers (Register 0x1500 through Register 0x1508), but the register addresses are offset by 0x0009. All default values are identical.									R/W

Table 73. Distribution Divider 1 A Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1500	Divider ratio	[7:0]	Q1A divider ratio [7:0]		Q1A divide ratio. This 32-bit bit field is the divide ratio for the Q1A divider. The default value of 0x00000000 equals a divide ratio of 1, which is invalid because it results in an output frequency that exceeds the maximum for the AD9543.	0x0	R/W
0x1501		[7:0]	Q1A divider ratio [15:8]			0x0	R/W
0x1502		[7:0]	Q1A divider ratio [23:16]			0x0	R/W
0x1503		[7:0]	Q1A divider ratio [31:24]			0x0	R/W
0x1504	Phase offset	[7:0]	Q1A phase [7:0]		Q1A phase control. This bit field controls the Q1A phase in two ways: the bit field sets the initial phase offset after divider sync (reset) and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q1A distribution input clock half cycles.	0x0	R/W
0x1505		[7:0]	Q1A phase [15:8]			0x0	R/W
0x1506		[7:0]	Q1A phase [23:16]			0x0	R/W
0x1507		[7:0]	Q1A phase [31:24]			0x0	R/W
0x1508	Phase slew config-uration	7	Reserved		Reserved.	0x0	R
		6	Q1A phase [32]		Q1A phase control. This bit field controls the Q1A phase in two ways: the bit field sets the initial phase offset after divider sync (reset); and subsequent changes to this bit field automatically initiate a phase slew event until the programmed phase is reached. The range is 0 to (2 × (divide ratio) − 1) in units of Q1A distribution input clock half cycles.	0x0	R/W
		5	Enable Q1A half divide		Enable Q1A half divide. Setting this bit to Logic 1 adds 0.5 to the divide ratio programmed into the corresponding 32-bit Q1A divide ratio bit field.	0x0	R/W
		4	Enable Q1A pulse width control		Enable pulse width control mode. This bit controls whether the Q1A Phase bit field adjusts the phase offset or the pulse width.	0x0	R/W
				0	The Q1A phase bit field controls the phase offset.		
				1	The Q1A phase bit field controls the pulse width.		
		3	Q1A phase slew mode		Q1A phase slew mode.	0x0	R/W
				0	Lag only (always slows down frequency). The phase controller slews the phase in the direction that always reduces the output frequency.		
				1	Lead or lag; quickest is automatically calculated. The phase controller slews the phase in the direction requiring the fewest steps, which means that the output frequency can increase or decrease during a stepwise phase adjustment sequence.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[2:0]	Maximum phase slew step		Maximum phase slew step.	0x0	R/W
				0	Maximum phase slew step. This 3-bit bit field controls the maximum allowable phase step while adjusting the phase in the Q1A divider. Each step occurs every output clock cycle.		
				1	One input clock half-cycle. The phase slew step size is half of the Q divider input period.		
				10	Two input clock half-cycles. The maximum phase slew step size equals the Q divider input period.		
				11	1°. The maximum phase slew step size equals 1/32 (~11.25°) of the output clock period.		
				100	23°. The maximum phase slew step size equals 1/16 (~22.5°) of the output clock period.		
				101	45°. The maximum phase slew step size equals 1/8 (~45°) of the output clock period.		
				110	90°. The maximum phase slew step size equals 1/4 (~90°) of the output clock period.		
				111	180°. The maximum phase slew step size equals half (~180°) of the output clock period.		

DPLL TRANSLATION PROFILE 1.0 REGISTERS—REGISTER 0x1600 TO REGISTER 0x1617

Table 74. DPLL Translation Profile 1.0 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1600	Priority and enable	Reserved		Profile 1.0 selection priority					Enable Profile 1.0	0x00	R/W
0x1601	Source	Reserved			Profile 1.0 reference source selection					0x00	R/W
0x1602	Zero delay feedback path	Reserved			Internal/external zero delay feedback path					0x00	R/W
0x1603	Feedback mode	Profile 1.0 loop filter base	Reserved		Profile 1.0 tag mode			Enable Profile 1.0 external zero delay	Enable Profile 1.0 hitless	0x00	R/W
0x1604	Loop bandwidth	Profile 1.0 loop bandwidth [7:0]								0x00	R/W
0x1605		Profile 1.0 loop bandwidth [15:8]								0x00	R/W
0x1606		Profile 1.0 loop bandwidth [23:16]								0x00	R/W
0x1607		Profile 1.0 loop bandwidth [31:24]								0x00	R/W
0x1608	Hitless feedback divider	Profile 1.0 hitless N-divider [7:0]								0xA0	R/W
0x1609		Profile 1.0 hitless N-divider [15:8]								0x0F	R/W
0x160A		Profile 1.0 hitless N-divider [23:16]								0x00	R/W
0x160B		Profile 1.0 hitless N-divider [31:24]								0x00	R/W
0x160C	Buildout feedback divider	Profile 1.0 buildout N-divider [7:0]								0xA0	R/W
0x160D		Profile 1.0 buildout N-divider [15:8]								0x0F	R/W
0x160E		Profile 1.0 buildout N-divider [23:16]								0x00	R/W
0x160F		Profile 1.0 buildout N-divider [31:24]								0x00	R/W
0x1610	Buildout feedback fraction	Profile 1.0 buildout fraction [7:0]								0x00	R/W
0x1611		Profile 1.0 buildout fraction [15:8]								0x00	R/W
0x1612		Profile 1.0 buildout fraction [23:16]								0x00	R/W
0x1613	Buildout feedback fraction	Profile 1.0 buildout modulus [7:0]								0x00	R/W
0x1614		Profile 1.0 buildout modulus [15:8]								0x00	R/W
0x1615		Profile 1.0 buildout modulus [23:16]								0x00	R/W
0x1616	Fast lock	Reserved				Profile 1.0 fast acquisition excess bandwidth				0x00	R/W
0x1617	Fast lock	Reserved	Profile 1.0 fast acquisition timeout			Reserved	Profile 1.0 fast acquisition lock settle time			0x00	R/W

Table 75. DPLL Translation Profile 1.1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1620 to 0x1637		These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 76. DPLL_ Translation Profile 1.2 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1640 to 0x1657		These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 77. DPLL Translation Profile 1.3 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1660 to 0x1677		These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 78. DPLL Translation Profile 1.4 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1680 to 0x1697		These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 79. DPLL Translation Profile 1.5 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x16A0 to 0x16B7		These registers mimic the DPLL Translation Profile 1.0 registers (Register 0x1600 through Register 0x1617), but the register addresses are offset by 0x0020. All default values are identical.								0x00	R/W

Table 80. DPLL Translation Profile 1.0 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1600	Priority and enable	[7:6]	Reserved		Reserved.	0x0	R
		[5:1]	Profile 1.0 selection priority		Profile 1.0 selection priority. This 5-bit bit field contains the priority of the translation profile. This allows the user to assign different priorities to different reference inputs. 0x00 is the highest priority, and 0x1F is the lowest priority.	0x0	R/W
					The choice of priority level for a given translation profile is important. If the priority difference between the active profile, and a valid, but inactive higher priority profile is >7, the DPLL state machine always switches to the higher priority profile. This is called revertive reference switching. Therefore, if revertive switching is desired, ensure the higher priority profile has a priority that is at least 8 greater than a lower priority profile.		
					If the difference between the priorities of the active profile and a valid, but inactive higher priority profile is 0 to 7, the DPLL state machine remains on the lower priority profile. This is called nonrevertive reference switching.		
		0	Enable Profile 1.0		Enable DPLL1 Profile 0 (Profile 1.0). Setting this bit to Logic 1 enables DPLL1 Profile 0. If this bit is Logic 0, DPLL1 never uses this profile.	0x0	R/W
0x1601	Source	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Profile 1.0 reference source selection		Profile 1.0 reference source selection. This 5-bit bit field contains the input source of the translation profile.	0x0	R/W
				0	Reference A.		
				1	Reference AA.		
				2	Reference B.		
				3	Reference BB.		
				4	Feedback from DPLL1.		
				8	Auxiliary NCO 0.		
				9	Auxiliary NCO 1.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1602	Zero delay feedback path	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	External zero delay feedback path		Profile 1.0 external zero delay feedback path. This 5-bit bit field configures the Profile1.0 feedback path in hitless external zero delay mode. Setting the Enable Profile 1.0 external zero delay bit to Logic 1 enables external zero delay mode for Prolife 1.0.	0x0	R/W
				0	Reference A. Select this mode if REFA is single-ended or in differential mode.		
				1	Reference AA.		
				2	Reference B. Select this mode if REFB is single-ended or in differential mode.		
				3	Reference BB.		
		[4:0]	Internal zero delay feedback path		Profile 1.0 internal zero delay feedback path. This 5-bit bit field configures the Profile 1.0 feedback path in hitless internal zero-delay mode. Setting the Enable Profile 1.0 internal zero delay bit to Logic 1 enables internal zero delay mode for Prolife 1.0.	0x0	R/W
				0	OUT1AP. Select this mode if OUT1A is single-ended or in differential mode.		
				1	OUT1AN.		
				2	OUT1BP. Select this mode if OUT1B is single-ended or in differential mode.		
				3	OUT1BN.		
0x1603	Feedback mode	7	Profile 1.0 loop filter base		Profile 1.0 loop filter base coefficients. This bit controls which set of loop filter coefficients are used for DPLL1 Profile 0.	0x0	R/W
				0	Nominal phase margin (~70°).		
				1	High phase margin (~88.5°) Use this setting for applications that require no more than 0.1 dB of peaking in the DPLL closed-loop transfer function.		
		[6:5]	Reserved		Reserved.	0x0	R/W
		[4:2]	Profile 1.0 tag mode		Profile 1.0 tag mode. This 3-bit bit field configures the Profile1.0 tag mode.	0x0	R/W
				0	Neither the reference nor feedback path contains tagged events.		
				1	Only the reference path is tagged.		
				2	Only the feedback path is tagged.		
				3	Both reference and feedback paths are tagged, but the untagged rates are unequal.		
				4	Both reference and feedback paths are tagged, and the untagged rates are equal.		
		1	Enable Profile 1.0 external zero delay		Enable DPLL1 Profile 0 external zero delay mode. Setting this bit to Logic 1 enables the DPLL1 Profile 0 external zero delay path for hitless mode.	0x0	R/W
		0	Enable Profile 1.0 hitless		Enable Profile 1.0 hitless operation.	0x0	R/W
				0	Selects the default phase buildout mode for the DPLL1 Profile 0		
				1	Enables hitless mode for DPLL1 Profile 0. This bit must also be enabled for zero delay operation.		
0x1604	Loop band-width	[7:0]	Profile 1.0 loop bandwidth [7:0]		DPLL1 Profile 0 loop bandwidth. This 32-bit bit field is the DPLL loop bandwidth scaling factor. The default units for this bit field are microseconds (10^{-6} seconds).	0x0	R/W
0x1605		[7:0]	Profile 1.0 loop bandwidth [15:8]			0x0	R/W
0x1606		[7:0]	Profile 1.0 loop bandwidth [23:16]			0x0	R/W
0x1607		[7:0]	Profile 1.0 loop bandwidth [31:24]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1608	Hitless feedback divider	[7:0]	Profile 1.0 hitless N-divider [7:0]		Profile 1.0 feedback divider in hitless mode. This 32-bit bit field is the DPLL1 feedback divide ratio while DPLL1 is in hitless mode. The feedback divide ratio is the value stored in this bit field plus one.	0xA0	R/W
0x1609		[7:0]	Profile 1.0 hitless N-divider [15:8]			0xF	R/W
0x160A		[7:0]	Profile 1.0 hitless N-divider [23:16]			0x0	R/W
0x160B		[7:0]	Profile 1.0 hitless N-divider [31:24]			0x0	R/W
0x160C	Buildout feedback divider	[7:0]	Profile 1.0 buildout N-divider [7:0]		DPLL1 Profile 0 buildout N-divide ratio. This 32-bit bit field is the integer portion of the DPLL feedback divide ratio while DPLL1 is in phase buildout mode. It is also referred to as the N-divider in the AD9543 data sheet.	0xA0	R/W
0x160D		[7:0]	Profile 1.0 buildout N-divider [15:8]			0xF	R/W
0x160E		[7:0]	Profile 1.0 buildout N-divider [23:16]			0x0	R/W
0x160F		[7:0]	Profile 1.0 buildout N-divider [31:24]			0x0	R/W
0x1610	Buildout feedback fraction	[7:0]	Profile 1.0 buildout fraction [7:0]		DPLL1 Profile 0 feedback divider fraction in buildout mode. This 24-bit bit field is the numerator of the DPLL fractional feedback divider while DPLL1 is in phase buildout mode. It is also referred to as FRAC in the AD9543 data sheet.	0x0	R/W
0x1611		[7:0]	Profile 1.0 buildout fraction [15:8]			0x0	R/W
0x1612		[7:0]	Profile 1.0 buildout fraction [23:16]			0x0	R/W
0x1613	Buildout feedback modulus	[7:0]	Profile 1.0 buildout modulus [7:0]		DPLL1 Profile 0 feedback divider modulus in buildout mode. This 24-bit bit field is the denominator of the DPLL fractional feedback divider while DPLL1 is in phase buildout mode. It is also referred to as MOD in the AD9543 data sheet.	0x0	R/W
0x1614		[7:0]	Profile 1.0 buildout modulus [15:8]			0x0	R/W
0x1615		[7:0]	Profile 1.0 buildout modulus [23:16]			0x0	R/W
0x1616	Fast lock	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Profile 1.0 fast acquisition excess bandwidth		DPLL1 Profile 0 fast acquisition excess bandwidth. This 4-bit bit field controls the DPLL1 loop bandwidth scaling factor (relative to the programmed DPLL loop bandwidth) while in fast acquisition mode. The DPLL automatically reduces its loop bandwidth by successive factors of 2 while the loop is acquiring. Setting this bit field to x'b0000 disables the feature.	0x0	R/W
				0	Feature disabled.		
				1	2×. The initial loop bandwidth is 2× the programmed value.		
				10	4×. The initial loop bandwidth is 4× the programmed value.		
				11	8×. The initial loop bandwidth is 8× the programmed value.		
				100	16×. The initial loop bandwidth is 16× the programmed value.		
				101	32×. The initial loop bandwidth is 32× the programmed value.		
				110	64×. The initial loop bandwidth is 64× the programmed value.		
				111	128×. The initial loop bandwidth is 128× the programmed value.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1000	256×. The initial loop bandwidth is 256× the programmed value.		
				1001	512×. The initial loop bandwidth is 512× the programmed value.		
				1010	1024×. The initial loop bandwidth is 1024× the programmed value.		
0x1617	Fast lock	7	Reserved		Reserved.	0x0	R
		[6:4]	Profile 1.0 fast acquisition timeout		DPLL1 Profile 0 fast acquisition timeout. This 3-bit bit field controls the maximum amount of time that DPLL1 waits to achieve phase lock (without chatter) before reducing the loop bandwidth by a factor of 2 while in fast acquisition mode. This feature prevents the fast acquisition algorithm from stalling in the event that lock is not achieved during the fast acquisition process.	0x0	R/W
				0	1 ms.		
				1	10 ms.		
				10	50 ms.		
				11	100 ms.		
				100	500 ms.		
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Profile 1.0 fast acquisition lock settle time		DPLL1 Profile 0 fast acquisition lock settle time. This 3-bit bit field controls how long DPLL1 must wait after achieving phase lock (without chatter) before reducing the loop bandwidth by a factor of 2 while in fast acquisition mode. If the lock detector chatters, this timer is reset.	0x0	R/W
				0	1 ms.		
				1	10 ms.		
				10	50 ms.		
				11	100 ms.		
				100	500 ms.		
				101	1 sec.		
				110	10 sec.		
				111	50 sec.		

OPERATIONAL CONTROLS GENERAL REGISTERS—REGISTER 0x2000 TO REGISTER 0x2005

Table 81. Operational Controls General Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2000	Global	Reserved				Sync all	Calibrate SYSCLK	Calibrate all	Power down all	0x00	R/W
0x2001	Power-down reference	Reserved				Power-down REFBB	Power-down REFB	Power-down REFAA	Power-down REFA	0x00	R/W
0x2002	Timeout reference	Reserved				Timeout Reference Monitor BB	Timeout Reference Monitor B	Timeout Reference Monitor AA	Timeout Reference Monitor A	0x00	R/W
0x2003	Fault reference	Reserved				Fault REFBB	Fault REFB	Fault REFAA	Fault REFA	0x00	R/W
0x2004	Bypass reference monitor	Reserved				Bypass Reference Monitor BB	Bypass Reference Monitor B	Bypass Reference Monitor AA	Bypass Reference Monitor A	0x00	R/W
0x2005	Clear IRQ	Clear watchdog timer	Reserved			IRQ clear PLL1	IRQ clear PLL0	IRQ clear common	IRQ clear all	0x00	R/W

Table 82. Operational Controls General Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2000	Global	[7:4]	Reserved		Reserved.	0x0	R/W
		3	Sync all		Synchronize all distribution dividers. The proper sequence for synchronizing the output dividers manually is to set this bit to Logic 1, write 0x01 to the IO_UPDATE register, set this bit to Logic 0, and write 0x01 to the IO_UPDATE register a second time.	0x0	R/W
				0	Normal operation.		
				1	Hold all distribution dividers in RESET with the divider outputs static.		
		2	Calibrate SYSCLK		Calibrate system clock PLL. Setting this bit to Logic 1 calibrates the system clock PLL. Because calibration occurs on the Logic 0 to Logic 1 transition, it is recommended to clear this bit after setting it. The system clock PLL must be calibrated during initial programming of the AD9543. Because the calibration signal is a logical OR of this bit and the calibrate all bit, this calibration bit is ineffective if the calibrate all bit is Logic 1 at the time this bit is set to Logic 1.	0x0	R/W
		1	Calibrate all		Calibrate all PLLs. Setting this bit to Logic 1 calibrates all PLLs, including the system clock PLL. Because calibration occurs on the Logic 0 to Logic 1 transition, it is recommended to clear this bit after setting it; this recommendation applies to all calibration bits on the AD9543. The system clock PLL and both APLLs must be calibrated during initial programming of the AD9543 for both PLL0 and PLL1 to function normally.	0x0	R/W
		0	Power down all		Power down entire chip. Setting this bit to Logic 1 puts the entire chip into a lower power mode. The serial port is still active in this state.	0x0	R/W
0x2001	Power-down reference	[7:4]	Reserved		Reserved.	0x0	R/W
		3	Power-down REFBB		Power-down REFBB. Setting this bit to Logic 1 powers down the REFBB input receiver.	0x0	R/W
		2	Power-down REFB		Power-down REFB. Setting this bit to Logic 1 powers down the REFB input receiver.	0x0	R/W
		1	Power-down REFAA		Power-down REFAA. Setting this bit to Logic 1 powers down the REFAA input receiver.	0x0	R/W
		0	Power-down REFA		Power-down REFA. Setting this bit to Logic 1 powers down the REFA input receiver.	0x0	R/W
0x2002	Timeout reference	[7:4]	Reserved		Reserved.	0x0	R/W
		3	Timeout Reference Monitor BB		Timeout REFBB validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE command) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following settings force REFBB valid: Set the Bypass Reference Monitor BB bit to Logic 1. Set the Fault REFBB bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	Timeout Reference Monitor B		Timeout REFB validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE command) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following settings force REFB valid: Set the Bypass Reference Monitor B bit to Logic 1. Set the Fault REFB bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.		
		1	Timeout Reference Monitor AA		Timeout REFAA validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE command) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following settings force REFAA valid: Set the Bypass Reference Monitor AA bit to Logic 1. Set the Fault REFAA bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.	0x0	R/W
		0	Timeout Reference Monitor A		Timeout REFA validation. Setting this autoclearing bit to Logic 1 (and issuing an IO_UPDATE command) while the input reference is unfaulted and validation timer counts down immediately validates the reference input. Setting this bit to Logic 1 at other times has no effect. The following settings force REFA valid: Set the Bypass Reference Monitor A bit to Logic 1. Set the Fault REFA bit to Logic 0. Issue IO_UPDATE command. Set this bit to Logic 1. Issue IO_UPDATE command.	0x0	R/W
0x2003	Fault reference	[7:4]	Reserved		Reserved.	0x0	R
		3	Fault REFBB		Force REFBB invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFBB is not available as long as this bit is Logic 1.	0x0	R/W
		2	Fault REFB		Force REFB I invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFB is not available as long as this bit is Logic 1.	0x0	R/W
		1	Fault REFAA		Force REFAA invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFAA is not available as long as this bit is Logic 1.	0x0	R/W
		0	Fault REFA		Force REFA invalid. Setting this bit to Logic 1 invalidates the REFBB input and guarantees REFA is not available as long as this bit is Logic 1.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2004	Bypass reference monitor	[7:4]	Reserved		Reserved.	0x0	R
		3	Bypass Reference Monitor BB		Bypass REFBB frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declares the reference unfaulted. See the register description for the Timeout Reference Monitor BB bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
		2	Bypass Reference Monitor B		Bypass REFB frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declare that reference unfaulted. See the register description for Timeout Reference Monitor B bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
		1	Bypass Reference Monitor AA		Bypass REFAA frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declare that reference unfaulted. See the register description for Timeout Reference Monitor AA bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
		0	Bypass Reference Monitor A		Bypass REFA frequency monitor. Setting this bit to Logic 1 bypasses the reference input monitor and declare that reference unfaulted. See the register description for Timeout Reference Monitor A bit for the additional steps needed to force a reference input to be valid.	0x0	R/W
0x2005	Clear IRQ	7	Clear watchdog		Clear watchdog timer. Setting this write-only bit to Logic 1 immediately clears the watchdog timer.	0x0	R
		[6:4]	Reserved		Reserved.	0x0	R/W
		3	IRQ clear PLL1		Clear all PLL1 IRQ. Setting this write-only bit to Logic 1 clears all PLL1 IRQs. This bit always reads back as Logic 0.	0x0	R/W
		2	IRQ clear PLL0		Clear all PLL0 IRQ. Setting this write-only bit to Logic 1 clears all PLL0 IRQs. This bit always reads back as Logic 0.	0x0	R/W
		1	IRQ clear common		Clear common IRQ. Setting this write-only bit to Logic 1 clears all PLL1 IRQs. This bit always reads back as Logic 0.	0x0	R/W
		0	IRQ clear all		Clear all IRQs. Setting this write-only bit to Logic 1 clears all PLL1 IRQs. This bit always reads back as Logic 0.	0x0	R/W

IRQ MAP COMMON CLEAR REGISTERS—REGISTER 0x2006 TO REGISTER 0x200A

Table 83. IRQ Map Common Clear Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2006	SYSCLK	SYSCLK unlocked	SYSCLK stabilized	SYSCLK locked	SYSCLK calibration completed	SYSCLK calibration started	Watchdog timeout occurred	EEPROM faulted	EEPROM completed	0x00	R/W
0x2007	Auxiliary DPLL	Reserved		Skew limit exceeded	Temperature warning occurred	Auxiliary DPLL unfaulted	Auxiliary DPLL faulted	Auxiliary DPLL unlocked	Auxiliary DPLL locked	0x00	R/W
0x2008	REFA	REFAA R divider resynced	REFAA validated	REFAA unfaulted	REFAA faulted	REFA R divider resynced	REFA validated	REFA unfaulted	REFA faulted	0x00	R/W
0x2009	REFB	REFBB R divider resynced	REFBB validated	REFBB unfaulted	REFBB faulted	REFB R divider resynced	REFB validated	REFB unfaulted	REFB faulted	0x00	R/W
0x200A	Timestamp	Reserved			Skew updated	Timestamp 1 event	Timestamp 0 event	Auxiliary NCO 1 event occurred	Auxiliary NCO 0 event occurred	0x00	R/W

Table 84. IRQ Map Common Clear Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2006	SYSCLK	7	SYSCLK unlocked		System clock unlocked. Set this bit to Logic 1 to clear the SYSCLK unlocked IRQ.	0x0	R/W
		6	SYSCLK stabilized		System clock stabilized. Set this bit to Logic 1 to clear the SYSCLK stabilized IRQ.	0x0	R/W
		5	SYSCLK locked		System clock locked. Set this bit to Logic 1 to clear the SYSCLK locked IRQ.	0x0	R/W
		4	SYSCLK calibration completed		System clock calibration ended. Set this bit to Logic 1 to clear the SYSCLK calibration ended IRQ.	0x0	R/W
		3	SYSCLK calibration started		System clock calibration activated. Set this bit to Logic 1 to clear the SYSCLK calibration started IRQ.	0x0	R/W
		2	Watchdog timeout occurred		Watchdog timeout. Set this bit to Logic 1 to clear the watchdog timer timeout IRQ.	0x0	R/W
		1	EEPROM faulted		EEPROM faulted. Set this bit to Logic 1 to clear the EEPROM faulted IRQ.	0x0	R/W
		0	EEPROM completed		EEPROM operation completed. Set this bit to Logic 1 to clear the EEPROM operation completed IRQ.	0x0	R/W
0x2007	Auxiliary DPLL	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew limit exceeded		Skew limit exceeded. Set this bit to Logic 1 to clear the reference input skew measurement limit exceeded IRQ.	0x0	R/W
		4	Temperature warning occurred		Temperature range warning. Set to Logic 1 to clear the temperature warning IRQ.	0x0	R/W
		3	Auxiliary DPLL unfaulted		Closed-loop SYSCLK compensation DPLL unfaulted. Set this bit to Logic 1 to clear the auxiliary DPLL unfaulted IRQ.	0x0	R/W
		2	Auxiliary DPLL faulted		Closed-loop SYSCLK compensation DPLL faulted. Set this bit to Logic 1 to clear the auxiliary DPLL faulted IRQ.	0x0	R/W
		1	Auxiliary DPLL unlocked		Closed-loop SYSCLK compensation DPLL unlocked. Set this bit to Logic 1 to clear the auxiliary DPLL unlocked IRQ.	0x0	R/W
		0	Auxiliary DPLL locked		Closed-loop SYSCLK compensation DPLL locked. Set this bit to Logic 1 to clear the auxiliary DPLL locked IRQ.	0x0	R/W
0x2008	REFA	7	REFAA R divider resynced		REFAA R divider resynced. Set this bit to Logic 1 to clear the REFAA R divider resynced IRQ.	0x0	R/W
		6	REFAA validated		REFAA validated. Set this bit to Logic 1 to clear the REFAA validated IRQ.	0x0	R/W
		5	REFAA unfaulted		REFAA unfaulted. Set this bit to Logic 1 to clear the REFAA unfaulted IRQ	0x0	R/W
		4	REFAA faulted		REFAA faulted. Set this bit to Logic 1 to clear the REFAA faulted IRQ.	0x0	R/W
		3	REFA R divider resynced		REFA R divider resynced. Set this bit to Logic 1 to clear the REFA R divider resynced IRQ	0x0	R/W
		2	REFA validated		REFA validated. Set this bit to Logic 1 to clear the REFA validated IRQ.	0x0	R/W
		1	REFA unfaulted		REFA unfaulted. Set this bit to Logic 1 to clear the REFA unfaulted IRQ.	0x0	R/W
		0	REFA faulted		REFA faulted. Set this bit to Logic 1 to clear the REFA faulted IRQ.	0x0	R/W
0x2009	REFB	7	REFBB R divider resynced		REFBB R divider resynced. Set this bit to Logic 1 to clear the REFBB R divider resynced IRQ.	0x0	R/W
		6	REFBB validated		REFBB validated. Set this bit to Logic 1 to clear the REFBB validated IRQ.	0x0	R/W
		5	REFBB unfaulted		REFBB unfaulted. Set this bit to Logic 1 to clear the REFBB unfaulted IRQ.	0x0	R/W
		4	REFBB faulted		REFBB faulted. Set this bit to Logic 1 to clear the REFBB faulted IRQ.	0x0	R/W
		3	REFB R divider resynced		REFB R divider resynced. Set this bit to Logic 1 to clear the REFB R divider resynced IRQ.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	REFB validated		REFB validated. Set this bit to Logic 1 to clear the REFB validated IRQ.	0x0	R/W
		1	REFB unfaulted		REFB unfaulted. Set to this bit Logic 1 to clear the REFB unfaulted IRQ.	0x0	R/W
		0	REFB faulted		REFB faulted. Set this bit to Logic 1 to clear the REFB faulted IRQ.	0x0	R/W
0x200A	Timestamp	[7:5]	Reserved		Reserved.	0x0	R
		4	Skew updated		Skew measurement updated. Set this bit to Logic 1 to clear the reference input skew measurement updated IRQ.	0x0	R/W
		3	Timestamp 1 event		Timestamp 1 time code available. Set this bit to Logic 1 to clear the Timestamp 1 IRQ.	0x0	R/W
		2	Timestamp 0 event		Timestamp 0 time code available. Set this bit to Logic 1 to clear the Timestamp 0 IRQ.	0x0	R/W
		1	Auxiliary NCO 1 event occurred		Auxiliary NCO 1 event occurred. Set this bit to Logic 1 to clear the auxiliary NCO 1 IRQ.	0x0	R/W
		0	Auxiliary NCO 0 event occurred		Auxiliary NCO 0 event occurred. Set this bit to Logic 1 to clear the auxiliary NCO 0 IRQ.	0x0	R/W

IRQ MAP DPLL0 CLEAR REGISTERS—REGISTER 0x200B TO REGISTER 0x200F

Table 85. IRQ Map DPLL0 Clear Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x200B	Lock	DPLL0 frequency clamp deactivated	DPLL0 frequency clamp activated	DPLL0 phase slew limiter deactivated	DPLL0 phase slew limiter activated	DPLL0 frequency unlocked	DPLL0 frequency locked	DPLL0 phase unlocked	DPLL0 phase locked	0x00	R/W
0x200C	State	DPLL0 reference switching	DPLL0 freerun entered	DPLL0 holdover entered	DPLL0 hitless entered	DPLL0 hitless exited	DPLL0 history updated	Reserved	DPLL0 phase step detected	0x00	R/W
0x200D	Fast acquisition	Reserved			DPLL0 N-divider resynced	DPLL0 fast acquisition completed	DPLL0 fast acquisition started	Reserved		0x00	R/W
0x200E	Activated profile	Reserved		DPLL0 Profile 5 activated	DPLL0 Profile 4 activated	DPLL0 Profile 3 activated	DPLL0 Profile 2 activated	DPLL0 Profile 1 activated	DPLL0 Profile 0 activated	0x00	R/W
0x200F	APLL	Reserved			DPLL0 distrib-ution synced	APLL0 unlocked	APLL0 locked	APLL0 calibration completed	APLL0 calibration started	0x00	R/W

Table 86. IRQ Map DPLL1 Clear Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2010 to 0x2014		These registers mimic the IRQ Map DPLL0 registers (Register 0x200B through Register 0x200F), but the register addresses are offset by 0x0005. All default values are identical.								0x00	R/W

Table 87. IRQ Map DPLL0 Clear Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x200B	Lock	7	DPLL0 frequency clamp deactivated		Frequency clamp deactivated. Set this bit to Logic 1 to clear IRQ for DPLL0 frequency clamp deactivated.	0x0	R/W
		6	DPLL0 frequency clamp activated		Frequency clamp activated. Set this bit to Logic 1 to clear IRQ for DPLL0 frequency clamp activated.	0x0	R/W
		5	DPLL0 phase slew limiter deactivated		Phase slew limiter deactivated. Set this bit to Logic 1 to clear IRQ for DPLL0 phase slew limiter deactivated.	0x0	R/W
		4	DPLL0 phase slew limiter activated		Phase slew limiter activated. Set this bit to Logic 1 to clear IRQ for DPLL0 phase slew limiter activated.	0x0	R/W
		3	DPLL0 frequency unlocked		Frequency unlocked. Set this bit to Logic 1 to clear IRQ for DPLL0 FLD (locked to unlocked transition).	0x0	R/W
		2	DPLL0 frequency locked		Frequency locked. Set this bit to Logic 1 to clear IRQ for DPLL0 frequency unlocked detect (unlocked to locked transition).	0x0	R/W
		1	DPLL0 phase unlocked		Phase unlocked. Set this bit to Logic 1 to clear IRQ for DPLL0 PLD (locked to unlocked transition).	0x0	R/W
		0	DPLL0 phase locked		Phase locked. Set this bit to Logic 1 to clear IRQ for DPLL0 phase unlocked detect (unlocked to locked transition).	0x0	R/W
0x200C	State	7	DPLL0 reference switching		Reference switching. Set this bit to Logic 1 to clear IRQ for DPLL0 reference input switching.	0x0	R/W
		6	DPLL0 freerun entered		Freerun mode entered. Set this bit to Logic 1 to clear IRQ for DPLL0 freerun mode entered.	0x0	R/W
		5	DPLL0 holdover entered		Holdover mode entered. Set this bit to Logic 1 to clear IRQ for DPLL0 holdover mode entered.	0x0	R/W
		4	DPLL0 hitless entered		Hitless mode entered. Set this bit to Logic 1 to clear IRQ for DPLL0 hitless mode entered.	0x0	R/W
		3	DPLL0 hitless exited		Hitless mode exited. Set this bit to Logic 1 to clear IRQ for DPLL0 hitless mode exited.	0x0	R/W
		2	DPLL0 history updated		Holdover history updated. Set this bit to Logic 1 to clear IRQ for DPLL0 tuning word holdover history updated.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DPLL0 phase step detected		Phase step detected. Set to Logic 1 to clear IRQ for DPLL0 reference input phase step detected.	0x0	R/W
0x200D	Fast acqui-sition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 N-divider resynced		N-divider resynchronized. Set this bit to Logic 1 to clear IRQ for DPLL0 N-divider resynced.	0x0	R/W
		3	DPLL0 fast acquisition completed		Fast acquisition completed. Set this bit to Logic 1 to clear IRQ for DPLL0 fast acquisition completed.	0x0	R/W
		2	DPLL0 fast acquisition started		Fast acquisition started. Set this bit to Logic 1 to clear IRQ for DPLL0 fast acquisition started.	0x0	R/W
		[1:0]	Reserved		Reserved.	0x0	R/W
0x200E	Activated profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 Profile 5 activated		Profile 5 activated. Set this bit to Logic 1 to clear IRQ for DPLL0 Profile 5 activated.	0x0	R/W
		4	DPLL0 Profile 4 activated		Profile 4 activated. Set this bit to Logic 1 to clear IRQ for DPLL0 Profile 4 activated.	0x0	R/W
		3	DPLL0 Profile 3 activated		Profile 3 activated. Set this bit to Logic 1 to clear IRQ for DPLL0 Profile 3 activated.	0x0	R/W
		2	DPLL0 Profile 2 activated		Profile 2 activated. Set this bit to Logic 1 to clear IRQ for DPLL0 Profile 2 activated.	0x0	R/W
		1	DPLL0 Profile 1 activated		Profile 1 activated. Set this bit to Logic 1 to clear IRQ for DPLL0 Profile 1 activated.	0x0	R/W
		0	DPLL0 Profile 0 activated		Profile 0 activated. Set this bit to Logic 1 to clear IRQ for DPLL0 Profile 0 activated.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x200F	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 distribution synced		Clock distribution synced. Set this bit to Logic 1 to clear IRQ for DPLL0 clock distribution synced.	0x0	R/W
		3	APLL0 unlocked		Unlock detected. Set this bit to Logic 1 to clear IRQ for APLL0 unlock detected (lock to unlock transition).	0x0	R/W
		2	APLL0 locked		Lock detected. Set this bit to Logic 1 to clear IRQ for APLL0 lock detected (unlock to lock transition).	0x0	R/W
		1	APLL0 calibration completed		Calibration completed. Set this bit to Logic 1 to clear IRQ for APLL0 calibration completed.	0x0	R/W
		0	APLL0 calibration started		Calibration started. Set this bit to Logic 1 to clear IRQ for APLL0 calibration started.	0x0	R/W

OPERATIONAL CONTROL CHANNEL 0 REGISTERS—REGISTER 0x2100 TO REGISTER 0x2107

Table 88. Operational Control Channel 0 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2100	Power down and calibration	Reserved						Calibrate APLL0	Power down Channel 0	0x00	R/W
0x2101	All Channel 0 control	Reserved				Sync all Channel 0 dividers	Reset all Channel 0 drivers	Mute all Channel 0 drivers	N-shot request Channel 0	0x00	R/W
0x2102	Divider Q0A	Reserved		Reset OUT0A/OUT0AA	Power down OUT0A/OUT0AA	Mute OUT0AA	Mute OUT0A	Reset Q0AA	Reset Q0A	0x00	R/W
0x2103	Divider Q0B	Reserved		Reset OUT0B/OUT0BB	Power down OUT0B/OUT0BB	Mute OUT0BB	Mute OUT0B	Reset Q0BB	Reset Q0B	0x00	R/W
0x2104	Divider Q0C	Reserved		Reset OUT0C/OUT0CC	Power down OUT0C/OUT0CC	Mute OUT0CC	Mute OUT0C	Reset Q0CC	Reset Q0C	0x00	R/W
0x2105	DPLL0 mode	Enable step detect reference fault	DPLL0 assign translation profile			DPLL0 translation profile select mode		DPLL0 force holdover	DPLL0 force freerun	0x00	R/W
0x2106	DPLL0 fast acquisition mode	Reserved				Enable DPLL0 fast acquisition no output	Enable DPLL0 fast acquisition first	Enable DPLL0 fast acquisition from holdover	Enable DPLL0 fast acquisition from freerun	0x00	R/W
0x2107	Clear state	Reserved			Channel 0 automute clear	Clear DPLL0 fast acquisition done	Reserved	DPLL0 clear history	Channel 0 autosync one-shot	0x00	R/W

Table 89. Operational Control Channel 0 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2100	Power down and calibration	[7:2]	Reserved		Reserved.	0x0	R
		1	Calibrate APLL0		APLL0 voltage controlled oscillator (VCO) calibration. Setting this bit from Logic 0 to Logic 1 performs the APLL VCO calibration on the next IO_UPDATE command. VCO calibration must be done during initial configuration and any time the nominal APLL VCO frequency changes. VCO calibration must be performed after the APLL dividers are configured and the desired APLL input frequency is present. This bit field is not self clearing, and it is recommended that the user write a Logic 0 to this bit field after performing the VCO calibration.	0x0	R/W
		0	Power down Channel 0		Power down Channel 0. Setting this bit to Logic 1 powers all blocks in Channel 0. All Channel 0 outputs are tristated.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2101	All Channel 0 control	[7:4]	Reserved		Reserved.	0x0	R
		3	Sync all Channel 0 drivers		Synchronize all Channel 0 dividers. If making the output driver static without resetting the corresponding Q Divider, use the mute bit in this register instead. The driver power-down bit must tristate the output driver.	0x0	R/W
				0	Normal operation.		
				1	All Channel 0 output drivers are held in a static state at the corresponding Q dividers are held in reset. In the sync state, differential drivers are held in a muted state. Releasing from Logic 1 to Logic 0 initializes all outputs synchronously.		
		2	Reset all Channel 0 drivers		Reset all Channel 0 drivers. The reset function is identical to the Mute All Channel 0 drivers bit in this register, except the mute function delays muting an output driver to avoid a runt pulse, whereas the reset function mutes the output driver immediately. Both the reset and mute functions contain logic to prevent runt pulses while unmuting an output driver.	0x0	R/W
		1	Mute all Channel 0 drivers		Mute all Channel 0 drivers. The driver power-down bit must tristate the output driver.	0x0	R/W
				0	Channel 0 drivers are unmuted. The output drivers contain logic to prevent runt pulses while transitioning from a mute to unmute state.		
				1	Channel 0 drivers are muted. In the muted state, differential drivers are held in a state in which the positive leg of the differential driver is static low, while the complementary output is static high.		
		0	N-shot request Channel 0		Channel 0 JESD204B N-shot request. In most cases, return this bit to zero to avoid unwanted retriggering of the N-shot generators.	0x0	R/W
				0	Normal operation (JESD204B N-shot not requested).		
				1	Channel 0 JESD204B N-shot request. This bit is in a buffered register, meaning an IO_UPDATE command must follow this register write.		
0x2102	Divider Q0A	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT0A/OUT0AA		Reset OUT0A and OUT0AA drivers. Use the driver power-down bits instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT0A/OUT0AA are OUT0AP/OUT0AN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT0A/AA is put immediately into reset and driven static low/high. In differential mode, OUT0AA is static high.		
		4	Power down OUT0A/OUT0AA		Power down OUT0A/OUT0AA.	0x0	R/W
				0	Normal Operation		
				1	OUT0A/OUT0AA are powered down and tristated. OUT0A/OUT0AA correspond to Pins OUT0AP/OUT0AN, respectively.		
		3	Mute OUT0AA		Mute OUT0AA. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0AA is OUT0AN.	0x0	R/W
				0	Normal operation. OUT0AA is unmuted.		
				1	OUT0AA is muted and driven static low. Use the driver power-down bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT0A is in differential mode.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	Mute OUT0A		Mute OUT0A. Use the driver power-down bit of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0A is OUT0AP.	0x0	R/W
				0	Normal operation. OUT0A is unmuted.		
				1	OUT0A is muted and driven static low. In differential mode, OUT0AA is static high.		
		1	Reset Q0AA		Reset Divider Q0AA. Setting this bit to Logic 1 immediately puts the Q0AA divider into reset.	0x0	R/W
		0	Reset Q0A		Reset Divider Q0A. Setting this bit to Logic 1 immediately puts the Q0A divider into reset.	0x0	R/W
0x2103	Divider Q0B	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT0B/OUT0BB		Reset OUT0B and OUT0BB drivers. Use the driver power-down bit of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT0B/OUT0BB are OUT0BP/OUT0BN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT0B/OUT0BB is put immediately into reset and driven static low/high. In differential mode, OUT0BB is static high.		
		4	Power down OUT0B/OUT0BB		Power down OUT0B/OUT0BB.	0x0	R/W
				0	Normal operation.		
				1	OUT0B/OUT0BB are powered down and tristated. OUT0B/OUT0BB correspond to Pins OUT0BP/OUT0BN, respectively.		
		3	Mute OUT0BB		Mute OUT0BB. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0BB is OUT0BN.	0x0	R/W
				0	Normal operation. OUT0BB is unmuted.		
				1	OUT0BB is muted and driven static low. Use the driver power-down bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT0B is in differential mode.		
		2	Mute OUT0B		Mute OUT0B. Use the driver power-down bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0B is OUT0BP.	0x0	R/W
				0	Normal operation. OUT0B is unmuted.		
				1	OUT0B is muted and driven static low. In differential mode, OUT0BB is static high.		
		1	Reset Q0BB		Reset Divider Q0BB. Setting this bit to Logic 1 immediately puts the Q0BB divider into reset.	0x0	R/W
		0	Reset Q0B		Reset Divider Q0B. Setting this bit to Logic 1 immediately puts the Q0B divider into reset.	0x0	R/W
0x2104	Divider Q0C	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT0C/OUT0CC		Reset OUT0C and CC drivers. Use the driver power-down bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT0C/OUT0CC is OUT0CP/OUT0CCN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT0C/OUT0CC is put immediately into reset and driven static low/high. In differential mode, OUT0CC is static high.		
		4	Power down OUT0C/OUT0CC		Power down OUT0C/OUT0CC.	0x0	R/W
				0	Normal operation		
				1	OUT0C/OUT0CC are powered down and tristated. OUT0C/OUT0CC correspond to Pins OUT0CP/OUT0CN, respectively.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		3	Mute OUT0CC		Mute OUT0CC. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0CC is OUT0CN	0x0	R/W
				0	Normal operation. OUT0CC is unmuted.		
				1	OUT0CC is muted and driven static low. Use the driver power-down bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT0C is in differential mode.		
		2	Mute OUT0C		Mute OUT0C. Use the driver power-down bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT0C is OUT0CP.	0x0	R/W
				0	Normal operation. OUT0C is unmuted.		
				1	OUT0C is muted and driven static low. In differential mode, OUT0CC is static high.		
		1	Reset Q0CC		Reset Divider Q0CC. Setting this bit to Logic 1 immediately puts the Q0CC divider into reset.	0x0	R/W
		0	Reset Q0C		Reset Divider Q0C. Setting this bit to Logic 1 immediately puts the Q0C divider into reset.	0x0	R/W
0x2105	DPLL0 mode	7	Enable step detect reference fault		Enable step detect reference fault.	0x0	R/W
				0	In the event that the phase step detector activates, DPLL0 ignores the clock edge that activated the step detector and initiates a new reference acquisition.		
				1	Similar to Logic 0, but the input reference monitor is reset. In this case, validate the input reference prior to DPLL00 beginning a new reference input acquisition.		
		[6:4]	DPLL0 assign translation profile		DPLL0 manual translation profile assign. This 3-bit bit field controls which DPLL0 translation profile is selected when DPLL0 is in manual mode. Manual mode is selected in the DPLL0 profile selection mode bit field.	0x0	R/W
				000	DPLL Translation Profile 0.0.		
				001	DPLL Translation Profile 0.1.		
				010	DPLL Translation Profile 0.2.		
				011	DPLL Translation Profile 0.3.		
				100	DPLL Translation Profile 0.4.		
				101	DPLL Translation Profile 0.5.		
				110, 111	Do not use.		
		[3:2]	DPLL0 translation profile select mode		DPLL0 translation profile selection mode. This 2-bit bit field controls how DPLL0 selects which translation profile to use.	0x0	R/W
				0	Fully automatic-based on priority-based selection. In this fully automatic mode, the DPLL state machine chooses the highest priority translation profile. If the DPLL is unable to find a profile per the selection process, it reverts to either holdover mode (if there is sufficient tuning word history) or freerun mode. In the case of a tie, the lowest numbered profile is chosen.		
				1	Manual profile selection with fallback to autoprofile selection. In this mode, the user chooses the profile to use. The DPLL uses the selected profile until it becomes invalid. At that time, the DPLL reverts to normal, priority-based profile selection.		
				2	Manual profile selection with fallback to holdover mode. In this mode, the user chooses the profile to use. The DPLL uses this profile until it becomes invalid. At that time, the DPLL reverts to holdover mode.		
				3	The user controls all operation.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	DPLL0 force holdover		Force DPLL0 into holdover mode.	0x0	R/W
				0	Normal operation.		
				1	DPLL0 is forced into holdover mode. In this mode, DPLL0 does not lock to any input references and behaves like a frequency synthesizer. If the DPLL0 history available bit is Logic 0, there is insufficient tuning word history, and DPLL0 uses its freerun tuning word instead of its accumulated tuning word history.		
		0	DPLL0 force freerun		Force DPLL0 into freerun mode.	0x0	R/W
				0	Normal operation.		
				1	DPLL0 is forced into freerun mode. In this mode, DPLL0 does not lock to any input references and behaves like a frequency synthesizer.		
0x2106	DPLL0 fast acquisition mode	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable DPLL0 fast acquisition no output		Enable DPLL0 fast acquisition if no outputs.	0x0	R/W
				0	Normal operation. A fast acquisition event on DPLL0 is permitted to occur regardless of whether or not the Channel 0 outputs receive a sync signal or not. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is enabled only if the none of the DPLL0 outputs receive a sync signal. The purpose of this bit is to ensure that none of the outputs are toggling during a fast acquisition sequence.		
		2	Enable DPLL0 fast acquisition first		Enable DPLL0 fast acquisition only during first acquisition.	0x0	R/W
				0	DPLL0 fast acquisition mode is not dependent the status of the DPLL0 fast acquisition done bit. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is not enabled if the DPLL0 fast acquisition done bit is Logic 1. The purpose of this bit is to execute a fast acquisition sequence only once.		
		1	Enable DPLL0 fast acquisition from holdover		Enable_DPLL0 fast acquisition from holdover mode.	0x0	R/W
				0	DPLL0 fast acquisition mode is not enabled when exiting holdover mode.When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is enabled when exiting holdover mode.		
		0	Enable DPLL0 fast acquisition from freerun		Enable_DPLL0 fast acquisition from freerun mode.	0x0	R/W
				0	DPLL0 fast acquisition mode is not enabled when exiting freerun mode. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL0 fast acquisition is enabled when exiting freerun mode.		
0x2107	Clear state	[7:5]	Reserved		Reserved.	0x0	R
		4	Channel 0 automute clear		Clear automute state. Setting this bit to Logic 1 allows the user to manually clear the automatic muting of Channel 0. This reinitializes the muting of outputs until the currently programmed condition in the DPLL0 autounmute mode bit field is satisfied.	0x0	R/W
		3	Clear DPLL0 fast acquisition done		Clear the DPLL0 fast acquisition done bit. Setting this autoclearing bit to Logic 1 clears the DPLL0 fast acquisition done bit.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	Reserved		Reserved.	0x0	R/W
		1	DPLL0 clear history		Clear DPLL0 tuning word history. Setting this bit to Logic 1 sets DPLL0 history available bit to Logic 0 and clears the internal tuning word history values for DPLL0. However, the DPLL0 tuning work history bit field remains intact until the processor calculates a new average and sets the DPLL0 history available bit to Logic 1, indicating a new average is available.	0x0	R/W
		0	Channel 0 clear autosync one-shot		Channel 0 clear autosync one-shot. This autoclearing bit rearms the autosync state machine for Channel 00. When used in conjunction with autosync mode = 01 binary, it is a convenient way to sync or resync the outputs.	0x0	R/W
				0	Normal operation. A clock distribution autosync event only occurs once per channel when an autosync condition is met. The autosync mode bit field controls when this happens. For example, the output sync on DPLL frequency lock.		
				1	Clock distribution autosync is rearmed, and an output resync occurs when the next autosync event occurs. If the autosync mode bit field is set to 01b, setting this bit to Logic 1 triggers an immediate sync event provided that APLL0 is locked.		

OPERATIONAL CONTROL CHANNEL 1 REGISTERS—REGISTER 0x2200 TO REGISTER 0x2207

Table 90. Operational Control Channel 1 Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2200	Power down and calibration	Reserved						Calibrate APLL1	Power down Channel 1	0x00	R/W
0x2201	All Channel 1 control	Reserved				Sync all Channel 1 dividers	Reset all Channel 1 drivers	Mute all Channel 1 drivers	N-shot request Channel 1	0x00	R/W
0x2202	Divider Q1A	Reserved		Reset OUT1A/ OUT1AA	Power down OUT1A/OUT1AA	Mute OUT1AA	Mute OUT1A	Reset Q1AA	Reset Q1A	0x00	R/W
0x2203	Divider Q1B	Reserved		Reset OUT1B/OUT1BB	Power down OUT1B/OUT1BB	Mute OUT1BB	Mute OUT1B	Reset Q1BB	Reset Q1B	0x00	R/W
0x2204	Reserved	Reserved								0x00	R/W
0x2205	DPLL1 Mode	Enable step detect reference fault	DPLL1 assign translation profile			DPLL1 translation profile select mode		DPLL1 force holdover	DPLL1 force freerun	0x00	R/W
0x2206	DPLL1 fast acquisition mode	Reserved				Enable DPLL1 fast acquisition no output	Enable DPLL1 fast acquisition first	Enable DPLL1 fast acquisition from holdover	Enable DPLL1 fast acquisition from freerun	0x00	R/W
0x2207	Clear state	Reserved			Channel 1 automute clear	Clear DPLL1 fast acquisition done	Reserved	DPLL1 clear history	Channel 1 autosync one-shot	0x00	R/W

Table 91. Operational Control Channel 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2200	Power down and calibration	[7:2]	Reserved		Reserved.	0x0	R
		1	Calibrate APLL1		APLL1 VCO calibration. Setting this bit from Logic 0 to Logic 1 performs the APLL VCO calibration on the next IO_UPDATE command. VCO calibration must be done during initial configuration and any time the nominal APLL VCO frequency changes. Perform VCO calibration after the APLL dividers are configured and the desired APLL input frequency is present. This bit field is not self clearing, and it is recommended that the user write a Logic 0 to this bit field after performing the VCO calibration.	0x0	R/W
		0	Power down Channel 1		Power down Channel 1. Setting this bit to Logic 1 powers all blocks in Channel 1. All Channel 1 outputs are tristated.	0x0	R/W
0x2201	All Channel 1 control	[7:4]	Reserved		Reserved.	0x0	R
		3	Sync all Channel 1 drivers		Synchronize all Channel 1 dividers. To make the output driver static without resetting the corresponding Q divider, use the mute bit in this register. Use the driver power-down bit to tristate the output driver.	0x0	R/W
				0	Normal operation.		
				1	All Channel 1 output drivers are held in a static state at the corresponding Q dividers (held in reset). In the sync state, differential drivers are held in a muted state. Releasing from Logic 1 to Logic 0 initializes all outputs synchronously.		
		2	Reset all Channel 1 drivers		Reset all channel 1 drivers. The reset function is identical to the Mute All Channel 1 drivers bit in this register, except the mute function delays muting an output driver to avoid a runt pulse, whereas the reset function mutes the output driver immediately. Both the reset and mute functions contain logic to prevent runt pulses while unmuting an output driver.	0x0	R/W
		1	Mute all Channel 1 drivers		Mute all Channel 1 drivers. Use the driver power-down bit to tristate the output driver.	0x0	R/W
				0	Channel 1 drivers are unmuted. The output drivers contain logic to prevent runt pulses while transitioning from a mute to unmute state.		
				1	Channel 1 drivers are muted. In the muted state, differential drivers are held in a state in which the positive leg of the differential driver is static low, while the complementary output is static high.		
		0	N-shot request Channel 1		Channel 1 JESD204B N-shot request. In most cases, return this bit to zero to avoid unwanted retriggering of the N-shot generators.	0x0	R/W
				0	Normal operation (JESD204B N-shot not requested).		
				1	Channel 1 JESD204B N-Shot request. This bit is in a buffered register, meaning that an IO_UPDATE command must follow this register write.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2202	Divider Q1A	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT1A/OUT1AA		Reset OUT1A and OUT1AA drivers. Use the driver power-down bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT1A/OUT1AA are OUT1AP/OUT1AN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT1A/OUT1AA is put immediately into reset and driven static low/high. In differential mode, OUT1AA is static high.		
		4	Power down OUT1A/OUT1AA		Power down OUT1A/OUT1AA.	0x0	R/W
				0	Normal operation.		
				1	OUT1A/OUT1AA are powered down and tristated. OUT1A/OUT1AA correspond to Pins OUT1AP/OUT1AN, respectively.		
		3	Mute OUT1AA		Mute OUT1AA. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1AA is OUT1AN.	0x0	R/W
				0	Normal operation. OUT1AA is unmuted.		
				1	OUT1AA is muted and driven static low. Use the driver power-down bit instead of this bit to tristate the output driver. Setting this bit has no effect if OUT1A is in differential mode.		
		2	Mute OUT1A		Mute OUT1A. Use the driver power-down bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1A is OUT1AP.	0x0	R/W
				0	Normal operation. OUT1A is unmuted.		
				1	OUT1A is muted and driven static low. In differential mode, OUT1AA is be static high.		
		1	Reset Q1AA		Reset Divider Q1AA. Setting this bit to Logic 1 immediately puts the Q1AA divider into reset.	0x0	R/W
		0	Reset Q1A		Reset Divider Q1A. Setting this bit to Logic 1 immediately puts the Q1A divider into reset.	0x0	R/W
0x2203	Divider Q1B	[7:6]	Reserved		Reserved.	0x0	R
		5	Reset OUT1B/OUT1BB		Reset OUT1B and OUT1BB drivers. Use the driver power-down bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning from a reset condition. The pin names for OUT1B/OUT1BB are OUT1BP/OUT1BN, respectively.	0x0	R/W
				0	Normal operation.		
				1	OUT1B/OUT1BB is put immediately into reset and driven static low/high. In differential mode, OUT1BB is static high.		
		4	Power down OUT1B/OUT1BB		Power down OUT1B/OUT1BB.	0x0	R/W
				0	Normal operation.		
				1	OUT1B/OUT1BB are powered down and tristated. OUT1B/OUT1BB correspond to Pins OUT1BP/OUT1BN, respectively.		
		3	Mute OUT1BB		Mute OUT1BB. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1BB is OUT1BN	0x0	R/W
				0	Normal operation. OUT1BB is unmuted.		
				1	OUT1BB is muted and driven static low. Use the driver power-down bit instead of this bit in order to tristate the output driver. Setting this bit has no effect if OUT1B is in differential mode.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	Mute OUT1B		Mute OUT1B. Use the driver power-down bit instead of this bit to tristate the output driver. The output drivers contain logic to prevent runt pulses while transitioning both to and from a mute condition. The pin name for OUT1B is OUT1BP	0x0	R/W
				0	Normal operation. OUT1B is unmuted.		
				1	OUT0B is muted and driven static low. In differential mode, OUT1BB is static high.		
		1	Reset Q1BB		Reset Divider Q1BB. Setting this bit to Logic 1 immediately puts the Q1BB divider into reset.	0x0	R/W
		0	Reset Q1B		Reset Divider Q1B. Setting this bit to Logic 1 immediately puts the Q1B divider into reset.	0x0	R/W
0x2205	DPLL1 mode	7	Enable step detect reference fault		Enable step detect reference fault.	0x0	R/W
				0	In the event that the phase step detector activates, DPLL1 ignores the clock edge that activates the step detector and initiates a new reference acquisition.		
				1	Similar to Logic 0, but the input reference monitor is reset. In this case, the input reference must be validated prior to DPLL1 beginning a new reference input acquisition.		
		[6:4]	DPLL1 assign translation profile		DPLL1 manual translation profile assign. This 3-bit bit field controls which DPLL1 translation profile is selected when DPLL1 is in manual mode. Manual mode is selected in the DPLL1 profile selection mode bit field.	0x0	R/W
				000	DPLL Translation Profile 1.0.		
				001	DPLL Translation Profile 1.1.		
				010	DPLL Translation Profile 1.2.		
				011	DPLL Translation Profile 1.3.		
				100	DPLL Translation Profile 1.4.		
				101	DPLL Translation Profile 1.5.		
				110, 111	Do not use.		
		[3:2]	DPLL1 translation profile select mode		DPLL1 translation profile selection mode. This 2-bit bit field controls how DPLL1 selects which translation profile to use.	0x0	R/W
				0	Fully automatic-based on priority-based selection. In this fully automatic mode, the DPLL state machine chooses the highest priority translation profile. If the DPLL is unable to find a profile per the selection process, it reverts to either holdover (if there is sufficient tuning word history) or freerun mode. In the case of a tie, the lowest numbered profile is chosen.		
				1	Manual profile selection with fallback to autoprofile selection. In this mode, the user chooses the profile to use. The DPLL uses the selected profile until it becomes invalid. At that time, the DPLL reverts to normal, priority-based profile selection.		
				2	Manual profile selection with fallback to holdover mode. In this mode, the user chooses the profile to use. The DPLL uses this profile until it becomes invalid. At that time, the DPLL reverts to holdover mode.		
				3	The user controls all operation.		
		1	DPLL1 force holdover		Force DPLL1 into holdover mode.	0x0	R/W
				0	Normal operation.		
				1	DPLL1 is forced into holdover mode. In this mode, DPLL1 does not lock to any input references and behaves like a frequency synthesizer. If the DPLL1 history available bit is Logic 0, there is insufficient tuning word history, and DPLL1 uses its freerun tuning word instead of its accumulated tuning word history.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	DPLL1 force freerun		Force DPLL1 into freerun mode.	0x0	R/W
				0	Normal operation.		
				1	DPLL1 is forced into freerun mode. In this mode, DPLL1 does not lock to any input references and behaves like a frequency synthesizer.		
0x2206	DPLL1 fast acquisition mode	[7:4]	Reserved		Reserved.	0x0	R
		3	Enable DPLL1 fast acquisition if no output		Enable DPLL1 fast acquisition if no outputs.	0x0	R/W
				0	Normal operation. A fast acquisition event on DPLL1 is permitted to occur regardless of whether or not the Channel 1 outputs receive a sync signal or not. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is enabled only if the none of the DPLL1 outputs receive a sync signal. The purpose of this bit is to ensure that none of the outputs are toggling during a fast acquisition sequence.		
		2	Enable DPLL1 fast acquisition first		Enable DPLL1 fast acquisition only during first acquisition.	0x0	R/W
				0	DPLL1 fast acquisition mode is not dependent the status of the DPLL1 fast acquisition done bit. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is not enabled if the DPLL1 fast acquisition done bit is Logic 1. The purpose of this bit is to execute a fast acquisition sequence only once.		
		1	Enable DPLL1 fast acquisition from holdover		Enable DPLL1 fast acquisition from holdover mode.	0x0	R/W
				0	DPLL1 fast acquisition mode is not enabled when exiting holdover mode. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is enabled when exiting holdover mode.		
		0	Enable DPLL1 fast acquisition from freerun		Enable DPLL1 fast acquisition from freerun mode.	0x0	R/W
				0	DPLL1 fast acquisition mode is not enabled when exiting freerun mode. When all four fast acquisition bits in this register are Logic 0, all four fast acquisition modes are enabled as though these four bits are all Logic 1.		
				1	DPLL1 fast acquisition is enabled when exiting freerun mode.		
0x2207	Clear state	[7:5]	Reserved		Reserved.	0x0	R
		4	Channel 1 automute clear		Clear automute state. Setting this bit to Logic 1 allows the user to manually clear the automatic muting of Channel 1. This reinitializes the muting of outputs until the currently programmed condition in the DPLL1 autounmute mode bit field is satisfied.	0x0	R/W
		3	Clear DPLL1 fast acquisition done		Clear the DPLL1 fast acquisition done bit. Setting this autoclearing bit to Logic 1 clears the DPLL1 fast acquisition done bit.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	Reserved		Reserved.	0x0	R/W
		1	DPLL1 clear history		Clear DPLL1 tuning word history. Setting this bit to Logic 1 sets the DPLL1 history available bit to Logic 0 and clears the internal tuning word history values for DPLL1. However, the DPLL1 tuning work history bit field remains intact until the processor calculates a new average and sets the DPLL1 history available bit to Logic 1, indicating that a new average is available.	0x0	R/W
		0	Channel 1 clear autosync one-shot		Channel 1 clear autosync one-shot. This autoclearing bit rearms the autosync state machine for Channel 1. When used in conjunction with autosync mode = 01 binary, it is a convenient way to sync (or resync) the outputs.	0x0	R/W
				0	Normal operation. A clock distribution autosync event only occurs once per channel when an autosync condition is met. The autosync mode bit field controls when this happens. For example, output sync on DPLL frequency lock.		
				1	Clock distribution autosync is rearmed, and an output resync occurs when the next autosync event occurs. If the autosync mode bit field is set to 01b, setting this bit to Logic 1 triggers an immediate sync event provided that APLL1 is locked.		

AUXILIARY NCO 0 REGISTERS—REGISTER 0x2800 TO REGISTER 0x281E

Table 92. Auxiliary NCO 0 Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2800	Center frequency	Auxiliary NCO 0 center frequency [7:0]								0x00	R/W
0x2801		Auxiliary NCO 0 center frequency [15:8]								0x00	R/W
0x2802		Auxiliary NCO 0 center frequency [23:16]								0x00	R/W
0x2803		Auxiliary NCO 0 center frequency [31:24]								0x00	R/W
0x2804		Auxiliary NCO 0 center frequency [39:32]								0x00	R/W
0x2805		Auxiliary NCO 0 center frequency [47:40]								0x00	R/W
0x2806		Auxiliary NCO 0 center frequency [55:48]								0x00	R/W
0x2807	Offset frequency	Auxiliary NCO 0 offset frequency [7:0]								0x00	R/W
0x2808		Auxiliary NCO 0 offset frequency [15:8]								0x00	R/W
0x2809		Auxiliary NCO 0 offset frequency [23:16]								0x00	R/W
0x280A		Auxiliary NCO 0 offset frequency [31:24]								0x00	R/W
0x280B	Tag ratio	Auxiliary NCO 0 tag ratio [7:0]								0x00	R/W
0x280C		Auxiliary NCO 0 tag ratio [15:8]								0x00	R/W
0x280D	Tag delta	Auxiliary NCO 0 tag delta [7:0]								0x00	R/W
0x280E		Auxiliary NCO 0 tag delta [15:8]								0x00	R/W
0x280F	Type adjust	Reserved						Auxiliary NCO 0 cycle type	Auxiliary NCO 0 delta type	0x00	R/W
0x2810	Delta rate limit	Auxiliary NCO 0 delta rate limit [7:0]								0x00	R/W
0x2811		Auxiliary NCO 0 delta rate limit [15:8]								0x00	R/W
0x2812		Auxiliary NCO 0 delta rate limit [23:16]								0x00	R/W
0x2813		Auxiliary NCO 0 delta rate limit [31:24]								0x00	R/W
0x2814	Delta adjust	Auxiliary NCO 0 delta [7:0]								0x00	R/W
0x2815		Auxiliary NCO 0 delta T [15:8]								0x00	R/W
0x2816		Auxiliary NCO 0 delta UI [23:16]								0x00	R/W
0x2817		Auxiliary NCO 0 delta [31:24]								0x00	R/W
0x2818		Auxiliary NCO 0 delta T [39:32]								0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2819	Cycle adjust	Auxiliary NCO 0 cycle absolute UI [7:0]								0x00	R/W
0x281A		Auxiliary NCO 0 cycle absolute [15:8]								0x00	R/W
0x281B		Auxiliary NCO 0 cycle absolute [23:16]								0x00	R/W
0x281C		Auxiliary NCO 0 cycle absolute [31:24]								0x00	R/W
0x281D		Auxiliary NCO 0 cycle absolute [39:32]								0x00	R/W
0x281E	Pulse width	Auxiliary NCO 0 pulse width exponent				Auxiliary NCO 0 pulse width significand				0x00	R/W

Table 93. Auxiliary NCO 0 Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2800	Center frequency	[7:0]	Auxiliary NCO 0 center frequency [7:0]		Auxiliary NCO 0 center frequency. This 56-bit integer bit field contains the auxiliary NCO 0 center frequency. The units are in 2 Hz to 40 Hz. For example, program this bit field to 0x00010000000000 to achieve a 1 Hz center frequency. The maximum center frequency is approximately 65 kHz.	0x0	R/W
0x2801		[7:0]	Auxiliary NCO 0 center frequency [15:8]			0x0	R/W
0x2802		[7:0]	Auxiliary NCO 0 center frequency [23:16]			0x0	R/W
0x2803		[7:0]	Auxiliary NCO 0 center frequency [31:24]			0x0	R/W
0x2804		[7:0]	Auxiliary NCO 0 center frequency [39:32]			0x0	R/W
0x2805		[7:0]	Auxiliary NCO 0 center frequency [47:40]			0x0	R/W
0x2806		[7:0]	Auxiliary NCO 0 center frequency [55:48]			0x0	R/W
0x2807	Offset frequency	[7:0]	Auxiliary NCO 0 offset frequency [7:0]		Auxiliary NCO 0 offset frequency. This 32-bit unsigned integer bit field contains the auxiliary NCO 0 offset frequency. The units are in 2 Hz to 24 Hz. The upper 8 bits form the integer portion, and the lower 24 bits form the fractional portion. For example, program this bit field to 0x01000000 to achieve a 1 Hz center frequency. The maximum offset frequency is approximately 256 Hz.	0x0	R/W
0x2808		[7:0]	Auxiliary NCO 0 offset frequency [15:8]			0x0	R/W
0x2809		[7:0]	Auxiliary NCO 0 offset frequency [23:16]			0x0	R/W
0x280A		[7:0]	Auxiliary NCO 0 offset frequency [31:24]			0x0	R/W
0x280B	Tag ratio	[7:0]	Auxiliary NCO 0 tag ratio [7:0]		Auxiliary NCO 0 tag ratio. This unsigned integer 16-bit bit field specifies the interval between tagged and untagged timestamps. The units are the period of the timestamp interval. A value of 0x0000 in this bit field disables the feature. A value of 0x0002 specifies that every third timestamp is tagged, for example.	0x0	R/W
0x280C		[7:0]	Auxiliary NCO 0 tag ratio [15:8]		Auxiliary NCO 0 tag ratio. This unsigned integer 16-bit bit field specifies the interval between tagged and untagged timestamps. The units are the period of the timestamp interval. A value of 0x0000 in this bit field disables the feature. A value of 0x0002 specifies that every third timestamp is tagged, for example.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x280D	Tag delta	[7:0]	Auxiliary NCO 0 tag delta [7:0]		Auxiliary NCO 0 tag delta. This autoclearing, signed integer 16-bit bit field shifts the phase of tagged timestamps. The units are the period of the timestamp interval.	0x0	R/W
0x280E		[7:0]	Auxiliary NCO 0 tag delta [15:8]			0x0	R/W
0x280F	Type adjust	[7:2]	Reserved		Reserved.	0x0	R
		1	Auxiliary NCO 0 cycle type		Auxiliary NCO 0 cycle type. This bit controls the operation of the auxiliary NCO 0 cycle bit field.	0x0	R/W
				0	Absolute value. The unsigned, 40-bit auxiliary NCO 0 cycle bit field directly replaces the integer portion of the auxiliary NCO 0 time bit field.		
				1	Relative change. The signed, 40-bit auxiliary NCO 0 cycle bit field increments or decrements the integer portion of the auxiliary NCO 0 time bit field relative to its current value.		
		0	Auxiliary NCO 0 delta type		Auxiliary NCO 0 delta type. This bit specifies the units when programming the size of the phase offset of the auxiliary NCO (using the auxiliary NCO 0 delta register).	0x0	R/W
				0	Delta T. The absolute time offset specified in units of picoseconds.		
				1	Delta UI. The relative phase offset specified as a fraction of the auxiliary NCO period and with a total range of −½ UI to approximately +½ UI.		
	Delta rate limit	[7:0]	Auxiliary NCO 0 delta rate limit [7:0]		Auxiliary NCO 0 delta rate limit. This unsigned, 32-bit bit field controls the slew rate limit of Auxiliary NCO 0 while phase slewing due to a phase offset change. The units are 2 UI to 36 UI. For example, for a slew limit of 1 μs/s, the required value is 10^6 divided by 2^{36}, which equals 68,719 decimal (0x00010C6F).This feature is disabled when this bit field is set to all zeros (0x00000000).	0x0	R/W
0x2811		[7:0]	Auxiliary NCO 0 delta rate limit [15:8]			0x0	R/W
0x2812		[7:0]	Auxiliary NCO 0 delta rate limit [23:16]			0x0	R/W
0x2813		[7:0]	Auxiliary NCO 0 delta rate limit [31:24]			0x0	R/W
0x2814	Delta adjust	[7:0]	Auxiliary NCO 0 Delta [7:0]		Auxiliary NCO 0 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of auxiliary NCO 0. The units of this bit field depend on the setting of the Auxiliary NCO 0 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 0 Delta T [7:0]		Auxiliary NCO 0 Delta T. When the Auxiliary NCO 0 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 0.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta UI [7:0]		Auxiliary NCO 0 delta UI. When the Auxiliary NCO 0 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 0 relative to 360°. The allowable range is from −½ UI to approximately +½ UI.	0x0	R/W
0x2815		[7:0]	Auxiliary NCO 0 delta [15:8]		Auxiliary NCO 0 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of auxiliary NCO 0. The units of this bit field depend on the setting of the Auxiliary NCO 0 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta T [15:8]		Auxiliary NCO 0 delta T. When the Auxiliary NCO 0 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 0.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta UI [15:8]		Auxiliary NCO 0 delta UI. When the Auxiliary NCO 0 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 0 relative to 360°. The allowable range is from −½ UI to approximately +½ UI.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2816		[7:0]	Auxiliary NCO 0 delta [23:16]		Auxiliary NCO 0 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of Auxiliary NCO 0. The units of this bit field depend on the setting of the Auxiliary NCO 0 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta T [23:16]		Auxiliary NCO 0 delta T. When the Auxiliary NCO 0 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 0.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta UI [23:16]		Auxiliary NCO 0 delta UI. When the Auxiliary NCO 0 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 0 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W
0x2817		[7:0]	Auxiliary NCO 0 delta [31:24]		Auxiliary NCO 0 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of auxiliary NCO 0. The units of this bit field depend on the setting of the Auxiliary NCO 0 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta T [31:24]		Auxiliary NCO 0 delta T. When the Auxiliary NCO 0 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 0.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta UI [31:24]		Auxiliary NCO 0 Delta UI. When the Auxiliary NCO 0 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 0 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W
0x2818		[7:0]	Auxiliary NCO 0 delta [39:32]		Auxiliary NCO 0 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of Auxiliary NCO 0. The units of this bit field depend on the setting of the Auxiliary NCO 0 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta T [39:32]		Auxiliary NCO 0 delta T. When the Auxiliary NCO 0 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 0.	0x0	R/W
		[7:0]	Auxiliary NCO 0 delta UI [39:32]		Auxiliary NCO 0 delta UI. When the Auxiliary NCO 0 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of auxiliary NCO 0 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W
0x2819	Cycle adjust	[7:0]	Auxiliary NCO 0 cycle absolute [7:0]		Auxiliary NCO 0 cycle absolute value. When the Auxiliary NCO 0 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 0 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 0 cycle relative change [7:0]		Auxiliary NCO 0 cycle relative change. When the Auxiliary NCO 0 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 0 time bit field relative to its current value.	0x0	R/W
0x281A		[7:0]	Auxiliary NCO 0 cycle absolute [7:0]		Auxiliary NCO 0 cycle absolute value. When the Auxiliary NCO 0 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 0 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 0 cycle relative change [7:0]		Auxiliary NCO 0 cycle relative change. When the Auxiliary NCO 0 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 0 time bit field relative to its current value.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x281B		[7:0]	Auxiliary NCO 0 cycle absolute [7:0]		Auxiliary NCO 0 cycle absolute value. When the Auxiliary NCO 0 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 0 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 0 cycle relative change [7:0]		Auxiliary NCO 0 cycle relative change. When the Auxiliary NCO 0 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 0 time bit field relative to its current value.	0x0	R/W
0x281C		[7:0]	Auxiliary NCO 0 cycle absolute [7:0]		Auxiliary NCO 0 cycle absolute value. When the Auxiliary NCO 0 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 0 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 0 cycle relative change [7:0]		Auxiliary NCO 0 cycle relative change. When the Auxiliary NCO 0 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 0 time bit field relative to its current value.	0x0	R/W
0x281D		[7:0]	Auxiliary NCO 0 cycle absolute [7:0]		Auxiliary NCO 0 cycle absolute value. When the Auxiliary NCO 0 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 0 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 0 cycle relative change [7:0]		Auxiliary NCO 0 cycle relative change. When the Auxiliary NCO 0 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 0 time bit field relative to its current value.	0x0	R/W
0x281E	Pulse width	[7:4]	Auxiliary NCO 0 pulse width exponent		Auxiliary NCO 0 pulse width exponent. This 4-bit bit field allows the user to adjust the duration of the auxiliary NCO pulse generator. The pulse width is determined by the following formula: Pulse width = $(96/f_S) \times (1 + S + 2(E + 5))$, where E is the value of this register, f_S is the system clock frequency, and S is the value of the Auxiliary NCO 0 pulse width significand bit field.	0x0	R/W
		[3:0]	Auxiliary NCO 0 pulse width significand		Auxiliary NCO 0 pulse width significand. This 4-bit bit field allows the user to adjust the duration of the Auxiliary NCO pulse generator. The pulse width is determined by the following formula:Pulse width = $(96/f_S) \times (1 + S + 2(E + 5))$, where E is the value of this register, f_S is the system clock frequency, and S is the value of the Auxiliary NCO 0 pulse width exponent bit field.	0x0	R/W

AUXILIARY NCO 1 REGISTERS—REGISTER 0x2840 TO REGISTER 0x285E

Table 94. Auxiliary NCO 1 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2840	Center frequency	Auxiliary NCO 1 center frequency [7:0]								0x00	R/W
0x2841		Auxiliary NCO 1 center frequency [15:8]								0x00	R/W
0x2842		Auxiliary NCO 1 center frequency [23:16]								0x00	R/W
0x2843		Auxiliary NCO 1 center frequency [31:24]								0x00	R/W
0x2844		Auxiliary NCO 1 center frequency [39:32]								0x00	R/W
0x2845		Auxiliary NCO 1 center frequency [47:40]								0x00	R/W
0x2846		Auxiliary NCO 1 center frequency [55:48]								0x00	R/W
0x2847		Auxiliary NCO 1 offset frequency [7:0]								0x00	R/W
0x2848		Auxiliary NCO 1 offset frequency [15:8]								0x00	R/W
0x2849		Auxiliary NCO 1 offset frequency [23:16]								0x00	R/W
0x284A		Auxiliary NCO 1 offset frequency [31:24]								0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x284B	Tag ratio	Auxiliary NCO 1 tag ratio [7:0]								0x00	R/W
0x284C		Auxiliary NCO 1 tag ratio [15:8]								0x00	R/W
0x284D	Tag delta	Auxiliary NCO 1 tag delta [7:0]								0x00	R/W
0x284E		Auxiliary NCO 1 tag delta [15:8]								0x00	R/W
0x284F	Type adjust	Reserved						Auxiliary NCO 1 cycle type	Auxiliary NCO 1 delta type	0x00	R/W
0x2850	Delta rate limit	Auxiliary NCO 1 delta rate limit [7:0]								0x00	R/W
0x2851		Auxiliary NCO 1 delta rate limit [15:8]								0x00	R/W
0x2852		Auxiliary NCO 1 delta rate limit [23:16]								0x00	R/W
0x2853		Auxiliary NCO 1 delta rate limit [31:24]								0x00	R/W
0x2854	Delta adjust	Auxiliary NCO 1 delta [7:0]								0x00	R/W
0x2855		Auxiliary NCO 1 delta [15:8]								0x00	R/W
0x2856		Auxiliary NCO 1 delta [23:16]								0x00	R/W
0x2857		Auxiliary NCO 1 delta [31:24]								0x00	R/W
0x2858		Auxiliary NCO 1 delta [39:32]								0x00	R/W
0x2859	Cycle adjust	Auxiliary NCO 1 cycle absolute [7:0]								0x00	R/W
0x285A		Auxiliary NCO 1 cycle absolute [15:8]								0x00	R/W
0x285B		Auxiliary NCO 1 cycle absolute [23:16]								0x00	R/W
0x285C		Auxiliary NCO 1 cycle absolute [31:24]								0x00	R/W
0x285D		Auxiliary NCO 1 cycle absolute [39:32]								0x00	R/W
0x285E	Pulse width	Auxiliary NCO 1 pulse width exponent				Auxiliary NCO 1 pulse width significand				0x00	R/W

Table 95. Auxiliary NCO 1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2800	Center frequency	[7:0]	Auxiliary NCO 1 center frequency [7:0]		Auxiliary NCO 1 center frequency. This 56-bit integer bit field contains the auxiliary NCO 1 center frequency. The units are in 2 Hz to 40 Hz. For example, program this bit field to 0x00010000000000 to achieve a 1 Hz center frequency. The maximum center frequency is approximately 65 kHz.	0x0	R/W
0x2801		[7:0]	Auxiliary NCO 1 center frequency [15:8]			0x0	R/W
0x2802		[7:0]	Auxiliary NCO 1 center frequency [23:16]			0x0	R/W
0x2803		[7:0]	Auxiliary NCO 1 center frequency [31:24]			0x0	R/W
0x2804		[7:0]	Auxiliary NCO 1 center frequency [39:32]			0x0	R/W
0x2805		[7:0]	Auxiliary NCO 1 center frequency [47:40]			0x0	R/W
0x2806		[7:0]	Auxiliary NCO 1 center frequency [55:48]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2807	Offset frequency	[7:0]	Auxiliary NCO 1 offset frequency [7:0]		Auxiliary NCO 1 offset frequency. This 32-bit unsigned integer bit field contains the auxiliary NCO 1 offset frequency. The units are in 2 Hz to 24 Hz. The upper 8 bits form the integer portion, and the lower 24 bits form the fractional portion. For example, program this bit field to 0x01000000 to achieve a 1 Hz center frequency. The maximum offset frequency is approximately 256 Hz.	0x0	R/W
0x2808		[7:0]	Auxiliary NCO 1 offset frequency [15:8]			0x0	R/W
0x2809		[7:0]	Auxiliary NCO 1 offset frequency [23:16]			0x0	R/W
0x280A		[7:0]	Auxiliary NCO 1 offset frequency [31:24]			0x0	R/W
0x280B	Tag ratio	[7:0]	Auxiliary NCO 1 tag ratio [7:0]		Auxiliary NCO 1 tag ratio. This unsigned integer 16-bit bit field specifies the interval between tagged and untagged timestamps. The units are the period of the timestamp interval. A value of 0x0000 in this bit field disables the feature. A value of 0x0002 specifies that every third timestamp is tagged, for example.	0x0	R/W
0x280C		[7:0]	Auxiliary NCO 1 tag ratio [15:8]			0x0	R/W
0x280D	Tag delta	[7:0]	Auxiliary NCO 1 tag delta [7:0]		Auxiliary NCO 1 tag delta. This autoclearing, signed integer 16-bit bit field shifts the phase of tagged timestamps. The units are the period of the timestamp interval.	0x0	R/W
0x280E		[7:0]	Auxiliary NCO 1 tag delta [15:8]			0x0	R/W
0x280F	Type adjust	[7:2]	Reserved		Reserved.	0x0	R
		1	Auxiliary NCO 1 cycle type		Auxiliary NCO 1 cycle type. This bit controls the operation of the auxiliary NCO 1 cycle bit field.	0x0	R/W
				0	Absolute value. The unsigned, 40-bit auxiliary NCO 1 cycle bit field directly replaces the integer portion of the auxiliary NCO 1 time bit field.		
				1	Relative change. The signed, 40-bit auxiliary NCO 1 cycle bit field increments or decrements the integer portion of the auxiliary NCO 1 time bit field relative to its current value.		
		0	Auxiliary NCO 1 delta type		Auxiliary NCO 1 delta type. This bit specifies the units when programming the size of the phase offset of the auxiliary NCO (using the auxiliary NCO 1 delta register).	0x0	R/W
				0	Delta T. The absolute time offset specified in units of picoseconds.		
				1	Delta UI. The relative phase offset specified as a fraction of the auxiliary NCO period and with a total range of −½ UI to approximately +½ UI.		
0x2810	Delta rate limit	[7:0]	Auxiliary NCO 1 delta rate limit [7:0]		Auxiliary NCO 1 delta rate limit. This unsigned, 32-bit bit field controls the slew rate limit of Auxiliary NCO 0 while phase slewing due to a phase offset change. The units are 2 UI to 36 UI. For example, for a slew limit of 1 µs/s, the required value is 10^6 divided by 2^{36}, which equals 68,719 decimal (0x00010C6F).This feature is disabled when this bit field is set to all zeros (0x00000000).	0x0	R/W
0x2811		[7:0]	Auxiliary NCO 1 delta rate limit [15:8]			0x0	R/W
0x2812		[7:0]	Auxiliary NCO 1 delta rate limit [23:16]			0x0	R/W
0x2813		[7:0]	Auxiliary NCO 1 delta rate limit [31:24]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2814	Delta adjust	[7:0]	Auxiliary NCO 1 Delta [7:0]		Auxiliary NCO 1 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of auxiliary NCO 1. The units of this bit field depend on the setting of the Auxiliary NCO 1 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta T [7:0]		Auxiliary NCO 1 Delta T. When the Auxiliary NCO 1 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 1.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta UI [7:0]		Auxiliary NCO 1 delta UI. When the Auxiliary NCO 1 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 1 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W
0x2815	Delta adjust	[7:0]	Auxiliary NCO 1 delta [15:8]		Auxiliary NCO 1 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of auxiliary NCO 1. The units of this bit field depend on the setting of the Auxiliary NCO 1 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta T [15:8]		Auxiliary NCO 1 delta T. When the Auxiliary NCO 1 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 1.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta UI [15:8]		Auxiliary NCO 1 delta UI. When the Auxiliary NCO 1 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 1 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W
0x2816	Delta adjust	[7:0]	Auxiliary NCO 1 delta [23:16]		Auxiliary NCO 1 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of Auxiliary NCO 1. The units of this bit field depend on the setting of the Auxiliary NCO 1 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta T [23:16]		Auxiliary NCO 1 delta T. When the Auxiliary NCO 1 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 1.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta UI [23:16]		Auxiliary NCO 1 delta UI. When the Auxiliary NCO 1 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 1 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W
0x2817	Delta adjust	[7:0]	Auxiliary NCO 1 delta [31:24]		Auxiliary NCO 1 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of auxiliary NCO 1. The units of this bit field depend on the setting of the Auxiliary NCO 1 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta T [31:24]		Auxiliary NCO 1 delta T. When the Auxiliary NCO 1 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 1.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta UI [31:24]		Auxiliary NCO 1 Delta UI. When the Auxiliary NCO 1 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of Auxiliary NCO 1 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2818		[7:0]	Auxiliary NCO 1 delta [39:32]		Auxiliary NCO 1 delta. This signed, twos compliment, 40-bit integer bit field is the amount of phase shift of Auxiliary NCO 1. The units of this bit field depend on the setting of the Auxiliary NCO 1 delta type register.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta T [39:32]		Auxiliary NCO 1 delta T. When the Auxiliary NCO 1 delta type bit is Logic 0, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in picoseconds) of Auxiliary NCO 1.	0x0	R/W
		[7:0]	Auxiliary NCO 1 delta UI [39:32]		Auxiliary NCO 1 delta UI. When the Auxiliary NCO 1 delta type bit is Logic 1, this signed, twos compliment, 40-bit integer bit field is the amount of phase shift (in unit intervals) of auxiliary NCO 1 relative to 360°. The allowable range is from −1/2 UI to approximately +1/2 UI.	0x0	R/W
0x2819		[7:0]	Auxiliary NCO 1 cycle absolute [7:0]		Auxiliary NCO 1 cycle absolute value. When the Auxiliary NCO 1 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 1 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 1 cycle relative change [7:0]		Auxiliary NCO 1 cycle relative change. When the Auxiliary NCO 1 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 1 time bit field relative to its current value.	0x0	R/W
0x281A		[7:0]	Auxiliary NCO 1 cycle absolute [7:0]		Auxiliary NCO 1 cycle absolute value. When the Auxiliary NCO 1 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 1 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 1 cycle relative change [7:0]		Auxiliary NCO 1 cycle relative change. When the Auxiliary NCO 1 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 1 time bit field relative to its current value.	0x0	R/W
0x281B		[7:0]	Auxiliary NCO 1 cycle absolute [7:0]		Auxiliary NCO 1 cycle absolute value. When the Auxiliary NCO 1 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 1 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 1 cycle relative change [7:0]		Auxiliary NCO 1 cycle relative change. When the Auxiliary NCO 1 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 1 time bit field relative to its current value.	0x0	R/W
0x281C		[7:0]	Auxiliary NCO 1 cycle absolute [7:0]		Auxiliary NCO 1 cycle absolute value. When the Auxiliary NCO 1 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 1 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 1 cycle relative change [7:0]		Auxiliary NCO 1 cycle relative change. When the Auxiliary NCO 1 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 1 time bit field relative to its current value.	0x0	R/W
0x281D		[7:0]	Auxiliary NCO 1 cycle absolute [7:0]		Auxiliary NCO 1 cycle absolute value. When the Auxiliary NCO 1 cycle type bit is Logic 0, this unsigned, 40-bit bit field allows the user to update the integer portion of the Auxiliary NCO 1 time bit field directly.	0x0	R/W
		[7:0]	Auxiliary NCO 1 cycle relative change [7:0]		Auxiliary NCO 1 cycle relative change. When the Auxiliary NCO 1 cycle type bit is Logic 1, this signed, 40-bit bit field allows the user to increment or decrement the integer portion of the Auxiliary NCO 1 time bit field relative to its current value.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x281E	Pulse width	[7:4]	Auxiliary NCO 1 pulse width exponent		Auxiliary NCO 1 pulse width exponent. This 4-bit bit field allows the user to adjust the duration of the auxiliary NCO pulse generator. The pulse width is determined by the following formula: Pulse width = $(96/f_S) \times (1 + S + 2(E + 5))$, where E is the value of this register, f_S is the system clock frequency, and S is the value of the Auxiliary NCO 1 pulse width significand bit field.	0x0	R/W
		[3:0]	Auxiliary NCO 1 pulse width significand		Auxiliary NCO 1 pulse width significand. This 4-bit bit field allows the user to adjust the duration of the Auxiliary NCO pulse generator. The pulse width is determined by the following formula: Pulse width = $(96/f_S) \times (1 + S + 2(E + 5))$, where E is the value of this register, f_S is the system clock frequency, and S is the value of the Auxiliary NCO 1 pulse width exponent bit field.	0x0	R/W

TEMPERATURE SENSOR REGISTERS—REGISTER 0x2900 TO REGISTER 0x2906

Table 96. Temperature Sensor Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2900	External temperature	External temperature [7:0]								0x00	R/W
0x2901		External temperature [15:8]								0x00	R/W
0x2902	Temperature source	Reserved					Select DPLL0 delay temperature compensation source	Select DPLL1 delay temperature compensation source	Select SYSCLK temperature compensation source	0x00	R/W
0x2903	Low temperature alarm	Low temperature threshold [7:0]								0x00	R/W
0x2904		Low temperature threshold [15:8]								0x00	R/W
0x2905	High temperature alarm	High temperature threshold [7:0]								0x00	R/W
0x2906		High temperature threshold [15:8]								0x00	R/W

Table 97. Temperature Sensor Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2900	External temp-erature	[7:0]	External temperature [7:0]		External temperature. This signed, 16-bit bit field is where the user inputs the temperature of a remote temperature sensor. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The value in this bit field is computed by multiplying the temperature (in degrees Celsius) by 128. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required after writing for the newly programmed value to take effect. For example, to enter a temperature of −15.6°C, T = −15.6 × 128 = −1997 (decimal) = 0xF833. To enter a temperature of 35.1°C, T = 35.1 × 128 = 4493 (decimal) = 0x118D.	0x0	R/W
0x2901		[7:0]	External temperature [15:8]			0x0	R/W
0x2902	Temp-erature source	[7:3]	Reserved		Reserved.	0x0	R
		2	Select DPLL1 delay temperature comp-ensation source		DPLL1 delay compensation source. This bit allows the user to choose which temperature reading to use when compensating the temperature variation of the DPLL1 static phase offset.	0x0	R/W
				0	Use the internal temperature sensor.		
				1	Use the external temperature bit field.		
		1	Select DPLL0 Delay temperature compensation source		DPLL0 delay compensation source. This bit allows the user to choose which temperature reading to use when compensating the temperature variation of the DPLL0 static phase offset.	0x0	R/W
				0	Use the internal temperature sensor.		
				1	Use the external temperature bit field.		
		0	Select SYSCLK temperature compensation source		SYSCLK temperature compensation source. This bit allows the user to choose which temperature reading to use when compensating the system clock frequency temperature variation.	0x0	R/W
				0	Use the internal temperature sensor.		
				1	Use the external temperature bit field.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2903	Low temp-erature alarm	[7:0]	Low temperature threshold [7:0]		Low temperature threshold. This signed, 16-bit bit field contains the lower threshold of the internal temperature of the device before the temperature alarm is activated. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The value in this bit field is computed by multiplying the desired temperature setting (in degrees Celsius) by 128. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required after writing for the newly programmed value to take effect. The temp-erature sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, to enter a temperature of −15.6°C, T = −15.6 × 128 = −1997 (decimal) = 0xF833. To enter a temperature of 35.1°C, T = 35.1 × 128 = 4493 (decimal) = 0x118D.	0x0	R/W
0x2904		[7:0]	Low temperature threshold [15:8]			0x0	R/W
0x2905	High temp-erature alarm	[7:0]	High temperature threshold [7:0]		High temperature threshold. This signed, 16-bit bit field contains the upper threshold of the internal temperature of the device before the temperature alarm is activated. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The value in this bit field is computed by multiplying the desired temperature setting (in degrees Celsius) by 128. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required after writing for the newly programmed value to take effect. The temp-erature sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, to enter a temperature of −15.6°C, T = −15.6 × 128 = −1997 (decimal) = 0xF833. To enter a temperature of 35.1°C, T = 35.1 × 128 = 4493 (decimal) = 0x118D.	0x0	R/W
0x2906		[7:0]	High temperature threshold [15:8]			0x0	R/W

TDC AUXILIARY REGISTERS—REGISTER 0x2A00 TO REGISTER 0x2A16

Table 98. TDC_AUXILIARY Register Summary

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2A00	AUXTDC0 divide	Auxiliary 0 divide								0x00	R/W
0x2A01	AUXTDC0 Period	Auxiliary 0 period [7:0]								0x00	R/W
0x2A02		Auxiliary 0 period [15:8]								0x00	R/W
0x2A03		Auxiliary 0 period [23:16]								0x00	R/W
0x2A04		Auxiliary 0 period [31:24]								0x00	R/W
0x2A05		Auxiliary 0 period [39:32]								0x00	R/W
0x2A06		Auxiliary 0 period [47:40]								0x00	R/W
0x2A07		Auxiliary 0 period [55:48]								0x00	R/W
0x2A08		Reserved				Auxiliary 0 period [59:56]				0x00	R/W
0x2A09	AUXTDC1 divide	Auxiliary 1 divide								0x00	R/W
0x2A0A	AUXTDC1 Period	Auxiliary 1 period [7:0]								0x00	R/W
0x2A0B		Auxiliary 1 period [15:8]								0x00	R/W
0x2A0C		Auxiliary 1 period [23:16]								0x00	R/W
0x2A0D		Auxiliary 1 period [31:24]								0x00	R/W
0x2A0E		Auxiliary 1 period [39:32]								0x00	R/W
0x2A0F		Auxiliary 1 period [47:40]								0x00	R/W
0x2A10		Auxiliary 1 period [55:48]								0x00	R/W
0x2A11		Reserved				Auxiliary 1 period [59:56]				0x00	R/W
0x2A12	Timestamp 0 settings	Timebase Source 0	Reserved	Timestamp Only Tags 0	Timestamp Source 0					0x06	R/W
0x2A13	Timestamp 1 settings	Timebase Source 1	Reserved	Timestamp Only Tags 1	Timestamp Source 1					0x07	R/W
0x2A14	Skew window	Reserved				Skew window size				0x00	R/W

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2A15	Skew reference source	Reserved		Skew reference tags only	Select skew reference					0x00	R/W
0x2A16	Skew measurement source	Reserved		Skew measure tags only	Select skew measure					0x00	R/W

Table 99. TDC_AUXILIARY Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A00	AUXTDC0 divide	[7:0]	Auxiliary 0 divide		AUXTDC0 divide ratio. This 8-bit bit field is the AUXTDC0 divide ratio, and allows the user to input a clock that is higher than the 200 kHz maximum TDC input frequency. The actual divide ratio is the programmed value plus 1. Therefore, programming this bit field to 0x00 results in a divide ratio of 1.	0x0	R/W
0x2A01	AUXTDC0 period	[7:0]	Auxiliary 0 period [7:0]		AUXTDC0 input period. This 60-bit bit field contains the AUXTDC0 input period specified in attoseconds. For example, if the AUXTDC0 input clock is 2.048 MHz, the period is 488,281,250,000 as (1/(2.048 MHz)). The corresponding 60-bit hexadecimal value is 0x0000071AFD498D0, which is the input period of the AUXTDC0 clock before it is divided by the Auxiliary 0 divider block.	0x0	R/W
0x2A02		[7:0]	Auxiliary 0 period [15:8]			0x0	R/W
0x2A03		[7:0]	Auxiliary 0 period [23:16]			0x0	R/W
0x2A04		[7:0]	Auxiliary 0 period [31:24]			0x0	R/W
0x2A05		[7:0]	Auxiliary 0 period [39:32]			0x0	R/W
0x2A06		[7:0]	Auxiliary 0 period [47:40]			0x0	R/W
0x2A07		[7:0]	Auxiliary 0 period [55:48]			0x0	R/W
0x2A08		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Auxiliary 0 period [59:56]		AUXTDC0 input period. This 60-bit bit field contains the AUXTDC0 input period specified in attoseconds. For example, if the AUXTDC0 input clock is 2.048 MHz, the period is 488,281,250,000 as (1/(2.048 MHz)). The corresponding 60-bit hexadecimal value is 0x0000071AFD498D0. This is the input period of the AUXTDC0 clock before it is divided by the Auxiliary 0 divider block.	0x0	R/W
0x2A09	AUXTDC1 divide	[7:0]	Auxiliary 1 divide		AUXTDC1 divide ratio. This 8-bit bit field is the AUXTDC1 divide ratio, and allows the user to input a clock that is higher than the 200 kHz maximum TDC input frequency. The actual divide ratio is the programmed value plus 1. Therefore, programming this bit field to 0x00 results in a divide ratio of 1.	0x0	R/W
0x2A0A	AUXTDC1 period	[7:0]	Auxiliary 1 period [7:0]		AUXTDC1 input period. This 60-bit bit field contains the AUXTDC1 input period specified in attoseconds. For example, if the AUXTDC1 input clock is 2.048 MHz, the period is 488,281,250,000 as (1/(2.048 MHz)). The corresponding 60-bit hexadecimal value is 0x000 0071 AFD4 98D0. This is the input period of the AUXTDC1 clock before it is divided by the Auxiliary 1 divider block.	0x0	R/W
0x2A0B		[7:0]	Auxiliary 1 period [15:8]			0x0	R/W
0x2A0C		[7:0]	Auxiliary 1 period [23:16]			0x0	R/W
0x2A0D		[7:0]	Auxiliary 1 period [31:24]			0x0	R/W
0x2A0E		[7:0]	Auxiliary 1 period [39:32]			0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A0F		[7:0]	Auxiliary 1 period [47:40]			0x0	R/W
0x2A10		[7:0]	Auxiliary 1 period [55:48]			0x0	R/W
0x2A11		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Auxiliary 1 period [59:56]		AUXTDC0 input period. This 60-bit bit field contains the AUXTDC1 input period specified in attoseconds. For example, if the AUXTDC1 input clock is 2.048 MHz, the period is 488,281,250,000 as (1/(2.048 MHz)). The corresponding 60-bit hexadecimal value is 0x0000071AFD498D0, which is the input period of the AUXTDC1 clock before it is divided by the Auxiliary 1 divider block.	0x0	R/W
0x2A12	Timestamp 0 settings	7	Timebase Source 0		Timebase Source 0. This bit selects the reference time base for User Timestamp Processor 0. An increment of one user stamp corresponds to the period of the reference time base.	0x0	R/W
				0	Use Auxiliary NCO 0 as the reference time base for User Timestamp Processor 0.		
				1	Use Auxiliary NCO 1 as the reference time base for User Timestamp Processor 0.		
		6	Reserved		Reserved.		
		5	Timestamp Only Tags 0		Timestamp only tagged events (Timestamper 0).		
				0	All rising edges detected by the selected TDC create a user timestamp event on Timestamper 0.		
				1	Only tagged rising edges detected by the selected TDC create a user timestamp event on Timestamper 0.		
		[4:0]	Timestamp Source 0		Timestamp Source 0. This 5-bit bit field selects the TDC timestamp source for the User Timestamp 0 processor.		
				0	REFA.		
				1	REFAA.		
				2	REFB.		
				3	REFBB.		
				6	AUXTDC0 (default).		
				7	AUXTDC1.		
				8	AUXNCO0.		
				9	AUXNCO1.		
				10	Alternate between auxiliary TDCs (ping pong mode).		
0x2A13	Timestamp 1 settings	7	Timebase Source 1		Timebase Source 1. This bit selects the reference time base for User Timestamp Processor 1. An increment of one of user stamp corresponds to the period of the reference time base.	0x0	R/W
				0	Use Auxiliary NCO 0 as the reference time base for User Timestamp Processor 1.		
				1	Use Auxiliary NCO 1 as the reference time base for User Timestamp Processor 1.		
		6	Reserved		Reserved.		
		5	Timestamp Only Tags 1		Timestamp only tagged events (Timestamper 1)		
				0	All rising edges detected by the selected TDC create a user timestamp event on Timestamper 1.		
				1	Only tagged rising edges detected by the selected TDC create a user timestamp event on Timestamper 1.		
		[4:0]	Timestamp Source 1		Timestamp Source 1. This 5-bit bit field selects the TDC timestamp source for User Timestamp 0 processor.	0x7	R/W
				0	REFA.		
				1	REFAA.		
				2	REFB.		
				3	REFBB.		
				6	AUXTDC0 (default).		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				7	AUXTDC1.		
				8	AUXNCO0.		
				9	AUXNCO1.		
				10	Alternate between auxiliary TDCs (ping pong mode).		
0x2A14	Skew window size	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Skew window size		Skew measurement window size. This 4-bit bit field controls the amount of averaging for both the skew offset and skew drift measurements. The skew offset full window and skew drift full window bits are Logic 1, and the specified number of averages are compiled for the skew offset and skew drift measurements, respectively. The values in the table below are in the form of M/N, where M is the number of averages for skew offset measurement, and N is the number of averages for skew drift measurement.	0x0	R/W
				0	2/2.		
				1	4/4.		
				10	8/8.		
				11	16/16.		
				100	32/16.		
				101	64/16.		
				110	128/16.		
				111	256/16.		
				1000	512/16.		
				1001	1024/16.		
				1010	2048/16.		
				1011	4096/16.		
				1100	8192/16.		
				1101	16384/16.		
				1110	32768/16.		
				1111	65536/16.		
0x2A15	Skew reference source	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew reference tags only		Use tagged events only for skew reference.	0x0	R/W
				0	All rising edges detected by the selected TDC create a skew reference edge.		
				1	Only tagged rising edges detected by the selected TDC create a skew reference edge.		
		[4:0]	Select skew reference		Skew Reference Source. This 5-bit bit field selects the TDC source for skew measurement processor.	0x0	R/W
				0	REFA.		
				1	REFAA.		
				2	REFB.		
				3	REFBB.		
				6	AUXTDC0 (default).		
				7	AUXTDC1.		
				8	AUXNCO0.		
				9	AUXNCO1.		
0x2A16	Skew measurement source	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew measure tags only		Use tagged events only for skew measurements.	0	R/W
				0	All rising edges detected by the selected TDC create a skew measurement edge.		
				1	Only tagged rising edges detected by the selected TDC create a skew measurement edge.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[4:0]	Select skew measure		Skew measurement source. This 5-bit bit field selects the TDC (time to digital converter) for the edge to be measured by skew measurement processor. The skew measurement processor measures the time difference between the rising edge of the skew reference source to the rising edge of the skew measurement source. The result is stored in the skew offset and skew drift bit fields.	0x0	R/W
				0	REFA.		
				1	REFAA.		
				2	REFB.		
				3	REFBB.		
				6	AUXTDC0 (default).		
				7	AUXTDC1.		
				8	AUXNCO0.		
				9	AUXNCO1.		

EEPROM REGISTERS—REGISTER 0x2E00 TO REGISTER 0x2E1E

Table 100. EEPROM Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2E00	EEPROM options	Reserved					Verify EEPROM CRC	EEPROM fast mode	EEPROM write enable	0x00	R/W
0x2E01	EEPROM condition	Reserved				EEPROM load condition				0x00	R/W
0x2E02	EEPROM save	Reserved							EEPROM save	0x00	R/W
0x2E03	EEPROM load	Reserved							EEPROM load	0x00	R/W
0x2E10 to 0x2E1E	EEPROM sequence	EEPROM sequence								0xFF	R/W

Table 101. EEPROM Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2E00	EEPROM options	[7:3]	Reserved		Reserved.	0x0	R
		2	Verify EEPROM CRC		Verify EEPROM cyclic redundancy check (CRC). Setting this autoclearing bit to Logic 1 immediately starts a register loading from the EEPROM into the device to verify the EEPROM contents, and requires the same amount of time as a load from EEPROM operation. The key difference between this command and load from EEPROM is that the current AD9543 register settings are not overwritten using this command. An IO_UPDATE command is not required.	0x0	R/W
		1	EEPROM fast mode		EEPROM I^2C fast mode.	0x0	R/W
				0	100 kHz I^2C mode.		
				1	Fast I^2C (400 kHz) mode.		
					These clock rates are the maximum internally generated SCL frequencies. The nominal frequency of the internally generated I^2C SCL clock is typically 30% slower than these values.		
		0	EEPROM write enable		EEPROM write enable. This bit must be set to Logic 1 before performing a save to EEPROM operation. This bit is not autoclearing, and is in a live register. Live registers do not require an IO_UPDATE command to take effect.	0x0	R/W
				0	Writing to EEPROM disabled.		
				1	Writing to EEPROM enabled.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2E01	EEPROM condition	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	EEPROM condition		EEPROM condition map. This 4-bit bit field contains the EEPROM condition map, which allows conditional processing of EEPROM commands. Conditional processing allows users to store multiple configurations in the AD9543 EEPROM and select them at EEPROM loading time. Conditional processing is disabled by setting this bit field to 0x0 during an EEPROM write; this is called condition zero, and EEPROM instructions that are stored with condition zero are executed unconditionally during a load from EEPROM operation. Refer to the AD9543 data sheet for details on conditional EEPROM instructions.	0x0	R/W
0x2E02	EEPROM save	[7:1]	Reserved		Reserved.	0x0	R
		0	EEPROM save		Save to EEPROM. Setting this autoclearing bit to Logic 1 immediately starts a register save to the EEPROM from the AD9543. The user must write a Logic 1 to the EEPROM write enable bit in this register prior to writing a Logic 1 to this bit. This bit is in a live register and an IO_UPDATE command is not required after writing this bit.	0x0	R/W
0x2E03	EEPROM load	[7:1]	Reserved		Reserved.	0x0	R
		0	EEPROM load		Load from EEPROM. Setting this autoclearing bit to Logic 1 immediately starts a register loading from the EEPROM into the device. An IO_UPDATE command is not required.	0x0	R/W
0x2E10 to 0x2E1E	EEPROM sequence	[7:0]	EEPROM sequence		EEPROM storage sequence. This group of 15 registers contain the EEPROM storage sequence instructions for the AD9543 EEPROM controller. These instructions include operational codes (such as input/output update or APLL calibration), as well as the sequence of AD9543 register values that are to be stored in the EEPROM. Refer to the AD9543 data sheet for the list operational controls and programming sequence details.	0xFF	R/W

STATUS READBACK REGISTERS—REGISTER 0x3000 TO REGISTER 0x300A

Table 102. Status Readback Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3000	EEPROM status	Reserved				EEPROM CRC error	EEPROM fault	EEPROM load in progress	EEPROM save in progress	0x0X	R
0x3001	SYSCLK and PLL status	Reserved		PLL1 locked	PLL0 locked	Reserved	SYSCLK calibration busy	SYSCLK stable	SYSCLK locked	0xXX	R
0x3002	Miscellaneous status	Auxiliary NCO 1 delta overflow	Auxiliary NCO 1 delta slewing	Auxiliary NCO 0 delta overflow	Auxiliary NCO 0 delta slewing	Reserved	Auxiliary DPLL reference fault	Auxiliary DPLL lock detect	Temperature alarm	0xXX	R
0x3003	Temperature readback	Internal temperature [7:0]								0xXX	R
0x3004	Temperature readback	Internal temperature [15:8]								0xXX	R
0x3005	REFA status	Reserved		REFA LOS	REFA valid	REFA fault	REFA excess jitter	REFA fast	REFA slow	0xXX	R
0x3006	REFAA status	Reserved		REFAA LOS	REFAA valid	REFAA fault	REFAA excess jitter	REFAA fast	REFAA slow	0xXX	R
0x3007	REFB status	Reserved		REFB LOS	REFB valid	REFB fault	REFB excess jitter	REFB fast	REFB slow	0xXX	R
0x3008	REFBB status	Reserved		REFBB LOS	REFBB valid	REFBB fault	REFBB excess jitter	REFBB fast	REFBB slow	0xXX	R
0x3009	DPLL0 active profile	Reserved		DPLL0 Profile 5 active	DPLL0 Profile 4 active	DPLL0 Profile 3 active	DPLL0 Profile 2 active	DPLL0 Profile 1 active	DPLL0 Profile 0 active	0xXX	R
0x300A	DPLL1 active profile	Reserved		DPLL1 Profile 5 active	DPLL1 Profile 4 active	DPLL1 Profile 3 active	DPLL1 Profile 2 active	DPLL1 Profile 1 active	DPLL1 Profile 0 active	0xXX	R

Table 103. Status Readback Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3000	EEPROM status	[7:4]	Reserved		Reserved.	0x0	R
		3	EEPROM CRC error		EEPROM CRC error detected. A Logic 1 indicates a CRC error occurred during an EEPROM operation. This bit is in a live register, meaning an IO_UPDATE command is not needed while polling this register. If an EEPROM fault is detected, this bit remains Logic 1 until the next EEPROM operation.	0x0	R
		2	EEPROM fault		EEPROM general fault detected. A Logic 1 indicates that a general EEPROM error occurred during an EEPROM operation. This bit is in a live register, meaning an IO_UPDATE command is not needed while polling this register. If an EEPROM fault is detected, this bit remains Logic 1 until the next EEPROM operation.	0x0	R
		1	EEPROM load in progress		EEPROM load in progress. A Logic 1 indicates that a load from EEPROM operation is in progress. This bit is in a live register, meaning an IO_UPDATE command is not needed while polling this register.	0x0	R
		0	EEPROM save in progress		EEPROM save in progress. A Logic 1 indicates that a save to EEPROM operation is in progress. This bit is in a live register, meaning that an IO_UPDATE command is not needed while polling this register.	0x0	R
0x3001	SYSCLK and PLL status	[7:6]	Reserved		Reserved.	0x0	R
		5	PLL1 locked		DPLL1 and APLL1 locked. A Logic 1 indicates that both Channel 1 PLLs (DPLL1 and APLL0) are locked. This bit is the logical AND of system clock lock detect, APLL1 lock detect, DPLL1 frequency, and DPLL1 PLD. This bit is in a live register, meaning that an IO_UPDATE command is not needed prior to reading.	Prog	RP
		4	PLL0 locked		DPLL0 and APLL0 locked. A Logic 1 indicates that both Channel 0 PLLs (DPLL0 and APLL0) are locked. This bit is the logical AND of system clock lock detect, APLL0 lock detect, DPLL0 frequency, and DPLL0 PLD. This bit is in a live register, meaning that an IO_UPDATE command is not needed prior to reading.	Prog	RP
		3	Reserved		Reserved.	0x0	R
		2	SYSCLK calibration busy		System clock calibration in progress. A Logic 1 indicates that the system clock VCO is calibrating. This status bit is in a live register, meaning that an IO_UPDATE command is not required prior to reading.	Prog	RP
		1	SYSCLK stable		System clock stable. A Logic 1 indicates that the system clock PLL is stable, meaning that the system clock PLL has been locked for at least as long as the value programmed into the system clock stability timer bit field. This status bit is in a live register, meaning that an IO_UPDATE command is not required prior to reading.	Prog	RP
		0	SYSCLK locked		System clock PLL locked. A Logic 1 indicates that the system clock PLL is locked. This status bit is in a live register, meaning that an IO_UPDATE command is not required prior to reading.	Prog	RP
0x3002	Miscel-laneous status	7	Auxiliary NCO 1 delta overflow		Auxiliary NCO 1 delta overflow error. A Logic 1 indicates that an Auxiliary NCO 1 delta overflow occurred. If the Auxiliary NCO 1 delta type = 0, this error can occur if the user specifies an Auxiliary NCO 1 delta value that is greater than one Auxiliary NCO 1 period. If the Auxiliary NCO 1 delta type = 1, this error can occur if the user specifies an Auxiliary NCO 1 delta value with an absolute value greater than 1/2 of the Auxiliary NCO 1 period. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command immediately prior to reading to ensure that the latest status is read.	Prog	RP
		6	Auxiliary NCO 1 delta slewing		Auxiliary NCO 1 delta slewing. A Logic 1 indicates that Auxiliary NCO 1 is phase slewing. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command immediately prior to reading to ensure that the latest status is read.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		5	Auxiliary NCO 0 delta overflow		Auxiliary NCO 0 delta overflow error. A Logic 1 indicates that an Auxiliary NCO 0 delta overflow occurred. If the Auxiliary NCO 0 delta type = 0, this error can occur if the user specifies an Auxiliary NCO 0 delta value that is greater than one Auxiliary NCO 0 period. If the Auxiliary NCO 0 delta type = 1, this error can occur if the user specifies an Auxiliary NCO 0 delta value with an absolute value greater than 1/2 of the Auxiliary NCO 0 period. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command immediately prior to reading to ensure that the latest status is read.	Prog	RP
		4	Auxiliary NCO0 delta slewing		Auxiliary NCO 0 delta slewing. A Logic 1 indicates that Auxiliary NCO 0 is phase slewing. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command immediately prior to reading to ensure that the latest status is read.	Prog	RP
		3	Reserved		Reserved.	0x0	R
		2	Auxiliary DPLL reference fault		Auxiliary DPLL reference fault. This bit indicates an out of range reference fault of the auxiliary DPLL.	Prog	RP
				0	Auxiliary DPLL reference fault is not detected.		
				1	Auxiliary DPLL reference fault is detected.		
		1	Auxiliary DPLL lock detect		Auxiliary DPLL lock detect. This bit indicates the status of the auxiliary DPLL, which calculates an offset to compensate for any frequency error in the system clock PLL.	Prog	RP
				0	Auxiliary DPLL is not locked.		
				1	Auxiliary DPLL is locked.		
		0	Temperature alarm		Temperature alarm. A Logic 1 indicates that the temperature sensor detected a temperature that is outside of the range programmed into the high temperature threshold and low temperature threshold. This status bit is a buffered register, meaning that an IO_UPDATE command is required prior to reading to read back the latest value.	Prog	RP
0x3003	Temperature readback	[7:0]	Internal temperature [7:0]		Internal temperature. This signed, 16-bit bit field contains the internal temperature of the device. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The temperature reading is computed by multiplying the value in this bit field by 2^{-7} and is in degrees Celsius. The sensor samples at approximately 6.1 kHz. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required prior to reading to read back the latest value. The sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, if the internal temperature reads 0xF833 (−1997 decimal), $T = -1997 \times 2^{-7}$°C = −15.6°C.	Prog	RP
0x3004	Temperature readback	[7:0]	Internal temperature [15:8]		Internal temperature. This signed, 16-bit bit field contains the internal temperature of the device. Bits[6:0] contain the fractional part and Bits[14:7] contain the integer part. The temperature reading is computed by multiplying the value in this bit field by 2^{-7} and is in degrees Celsius. The sensor samples at approximately 6.1 kHz. This bit field is contained in two buffered registers, meaning that an IO_UPDATE command is required prior to reading to read back the latest value. The sensor is intended to provide an indication of relative (but not necessarily absolute) temperature. For example, if the internal temperature reads 0xF833 (−1997 decimal), $T = -1997 \times 2^{-7}$°C = −15.6°C.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3005	REFA status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFA LOS		REFA loss of signal (LOS). A Logic 1 indicates a REFA LOS. This bit is in a buffered register, meaning the user must issue an IO_UPDATE command prior to reading to read back the latest value. The value of this bit can change dynamically, so instead of monitoring this bit, monitor the REFA fault bit in this register which remains high whenever REFA is faulted (due to any type of fault).	0x0	R
		4	REFA valid		REFA frequency valid. A Logic 1 indicates that the period of the REFA clock is within the range allowed by the REFA nominal period and REFA offset limit settings for at least as long as the REFA validation timer setting. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFA fault		REFA fault. A Logic 1 indicates that the REFA clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFA LOS, REFA fast, REFA slow, and REFA excess jitter bits. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFA excess jitter		Excess jitter detected on REFA. A Logic 1 indicates that the jitter of the REFA clock is higher than allowed by its profile settings as specified in the REFA jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		1	REFA fast		REFA frequency is above upper limit. A Logic 1 indicates that the frequency of the REFA clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading. If the REFA clock is missing, the REFA fast and REFA slow bits in this register can both be Logic 1.	0x0	R
		0	REFA slow		REFA frequency is below lower limit. A Logic 1 indicates that the frequency of the REFA clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFA clock is missing, the REFA fast and REFA slow bits in this register can both be Logic 1.	0x0	R
0x3006	REFAA status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFAA LOS		REFAA LOS. A Logic 1 indicates a REFAA LOS. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command prior to reading in order to read back the latest value. The value of this bit can change dynamically, so instead of monitoring this bit, monitor the REFAA fault bit in this register which remains high whenever REFAA is faulted (due to any type of fault).	0x0	R
		4	REFAA valid		REFAA frequency valid. A Logic 1 indicates that the period of the REFAA clock is within the range allowed by the REFAA nominal period and REFAA offset limit settings for at least as long as the REFAA validation timer setting. This status bit is in a buffered register, meaning an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFAA fault		Reference AA fault. A Logic 1 indicates that the REFAA clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFAA LOS, REFAA fast, REFAA slow, and REFAA excess jitter bits. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFAA excess jitter		Excess jitter detected on REFAA. A Logic 1 indicates that the jitter of the REFAA clock is higher than allowed by its profile settings as specified in the REFAA jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		1	REFAA fast		REFAA frequency is above upper limit. A Logic 1 indicates that the frequency of the REFAA clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFAA clock is missing, the REFAA fast and REFAA slow bits in this register can both be Logic 1.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	REFAA slow		REFAA frequency is below lower limit. A Logic 1 indicates the frequency of the REFAA clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFAA clock is missing, the REFAA fast and REFAA slow bits in this register can both be Logic 1.	0x0	R
0x3007	REFB status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFB LOS		REFB LOS. A Logic 1 indicates a REFB LOS. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command prior to reading to read back the latest value. The value of this bit can change dynamically, so instead of monitoring this bit, monitor the REFB fault bit in this register which remains high whenever REFB is faulted (due to any type of fault).	0x0	R
		4	REFB valid		REFB frequency valid. A Logic 1 indicates that the period of the REFB clock is within the range allowed by the REFB nominal period and REFB offset limit settings for at least as long as the REFB validation timer setting. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFB fault		REFB fault. A Logic 1 indicates that the REFB clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFB LOS, REFB fast, REFB slow, and REFB excess jitter bits. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFB excess jitter		Excess jitter detected on REFB. A Logic 1 indicates that the jitter of the REFB clock is higher than allowed by its profile settings as specified in the REFB jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		1	REFB fast		REFB frequency is above upper limit. A Logic 1 indicates that the frequency of the REFB clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFB clock is missing, the REFB fast and REFB slow bits in this register can both be Logic 1.	0x0	R
		0	REFB slow		REFB frequency is below lower limit. A Logic 1 indicates the frequency of the REFB clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFB clock is missing, the REFB fast and REFB slow bits in this register can both be Logic 1.	0x0	R
0x3008	REFBB status	[7:6]	Reserved		Reserved.	0x0	R
		5	REFBB LOS		REFBB LOS. A Logic 1 indicates a REFBB LOS. This bit is in a buffered register, meaning that the user must issue an IO_UPDATE command prior to reading to read back the latest value. The value of this bit can change dynamically, so instead of monitoring this bit, monitor the REFB fault bit in this register which remains high whenever REFBB is faulted (due to any type of fault).	0x0	R
		4	REFBB valid		REFBB frequency valid. A Logic 1 indicates that the period of the REFBB clock is within the range allowed by the REFBB nominal period and REFBB offset limit settings for at least as long as the REFBB validation timer setting. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		3	REFBB fault		REFBB fault. A Logic 1 indicates that the REFBB clock is either missing, has excess jitter, or its frequency is outside of the range allowed by its profile settings. It is the logical OR of the REFBB LOS, REFBB fast, REFBB slow, and REFBB excess jitter bits. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R
		2	REFBB excess jitter		Excess jitter detected on REFBB. A Logic 1 indicates that the jitter of the REFBB clock is higher than allowed by its profile settings as specified in the REFBB jitter tolerance bit field. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	REFBB fast		REFBB frequency is above upper limit. A Logic 1 indicates that the frequency of the REFBB clock is higher than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFBB clock is missing, the REFBB fast and REFBB slow bits in this register can both be Logic 1.	0x0	R
		0	REFBB slow		REFBB frequency is below lower limit. A Logic 1 indicates the frequency of the REFBB clock is lower than allowed by its profile settings. This status bit is in a buffered register, meaning that an IO_UPDATE command is needed prior to reading. If the REFBB clock is missing, the REFBB fast and REFBB slow bits in this register can both be Logic 1.	0x0	R
0x3009	DPLL0 active profile	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 active profile		Active translation profile for DPLL0.	0x0	R
				000000	DPLL0 does not have an active translation profile.		
				000001	DPLL0 Translation Profile 0.0 is active.		
				000010	DPLL0 Translation Profile 0.1 is active.		
				000100	DPLL0 Translation Profile 0.2 is active.		
				001000	DPLL0 Translation Profile 0.3 is active.		
				010000	DPLL0 Translation Profile 0.4 is active.		
				100000	DPLL0 Translation Profile 0.5 is active.		
0x300A	DPLL1 active profile	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL1 active profile		Active translation profile for DPLL1.	0x0	R
				000000	DPLL1 does not have an active translation profile.		
				000001	DPLL1 Translation Profile 1.0 is active.		
				000010	DPLL1 Translation Profile 1.1 is active.		
				000100	DPLL1 Translation Profile 1.2 is active.		
				001000	DPLL1 Translation Profile 1.3 is active.		
				010000	DPLL1 Translation Profile 1.4 is active.		
				100000	DPLL1 Translation Profile 1.5 is active.		

IRQ MAP COMMON READ REGISTERS—REGISTER 0x300B TO REGISTER 0x300F

Table 104. IRQ Map Common Read Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x300B	SYSCLK	SYSCLK unlocked	SYSCLK stabilized	SYSCLK locked	SYSCLK calibration completed	SYSCLK calibration started	Watchdog timeout	EEPROM faulted	EEPROM completed	0x00	R
0x300C	Auxiliary DPLL	Reserved		Skew limit exceeded	Temperature warning	Auxiliary DPLL unfaulted	Auxiliary DPLL faulted	Auxiliary DPLL unlocked	Auxiliary DPLL locked	0x00	R
0x300D	REFA	REFAA R divider resynced	REFAA validated	REFAA unfaulted	REFAA faulted	REFA R divider resynced	REFA validated	REFA unfaulted	REFA faulted	0x00	R
0x300E	REFB	REFBB R divider resynced	REFBB validated	REFBB unfaulted	REFBB faulted	REFB R divider resynced	REFB valid	REFB unfaulted	REFB faulted	0x00	R
0x300F	Timestamp	Reserved			Skew updated	Timestamp 1 event	Timestamp 0 event	Auxiliary NCO 1 event	Auxiliary NCO 0 event	0x00	R

Table 105. IRQ Map Common Read Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x300B	SYSCLK	7	SYSCLK unlocked		System clock unlocked. Read-only status of the SYSCLK unlocked IRQ.	0x0	R
		6	SYSCLK stabilized		System clock stabilized. Read-only status of the SYSCLK stabilized IRQ.	0x0	R
		5	SYSCLK locked		System clock locked. Read-only status of the SYSCLK locked IRQ.	0x0	R
		4	SYSCLK calibration completed		System clock calibration is completed. Read-only status of the SYSCLK calibration completed IRQ.	0x0	R
		3	SYSCLK calibration started		System clock calibration started. Read-only status of the SYSCLK calibration started IRQ.	0x0	R
		2	Watchdog timeout		Watchdog timeout. Read-only status of the watchdog timer timeout IRQ.	0x0	R
		1	EEPROM faulted		EEPROM faulted. Read-only status of the EEPROM faulted IRQ.	0x0	R
		0	EEPROM completed		EEPROM operation completed. Read-only status of the EEPROM operation completed IRQ.	0x0	R
0x300C	Auxiliary DPLL	[7:6]	Reserved		Reserved.	0x0	R
		5	Skew limit exceeded		Skew limit exceeded. Read-only status of the reference input skew measurement limit exceeded IRQ.	0x0	R
		4	Temperature warning		Temperature range warning.	0x0	R
		3	Auxiliary DPLL unfaulted		Closed-loop SYSCLK compensation DPLL unfaulted. Read-only status of the auxiliary DPLL unfaulted IRQ.	0x0	R
		2	Auxiliary DPLL faulted		Closed-loop SYSCLK compensation DPLL faulted. Read-only status of the auxiliary DPLL faulted IRQ.	0x0	R
		1	Auxiliary DPLL unlocked		Closed-loop SYSCLK compensation DPLL unlocked. Read-only status of the auxiliary DPLL unlocked IRQ.	0x0	R
		0	DPLL locked		Closed-loop SYSCLK compensation DPLL locked. Read-only status of the auxiliary DPLL locked IRQ.	0x0	R
0x300D	REFA	7	REFAA R divider resynced		REFAA R divider resynced. Read-only status of the REFAA R divider resynced IRQ.	0x0	R
		6	REFAA validated		REFAA validated. Read-only status of the REFAA validated IRQ.	0x0	R
		5	REFAA unfaulted		REFAA unfaulted. Read-only status of the REFAA unfaulted IRQ.	0x0	R
		4	REFAA faulted		REFAA faulted. Read-only status of the REFAA faulted IRQ.	0x0	R
		3	REFA R divider resynced		REFA R divider resynced. Read-only status of the REFA R divider resynced IRQ.	0x0	R
		2	REFA validated		REFA validated. Read-only status of the REFA validated IRQ.	0x0	R
		1	REFA unfaulted		REFA unfaulted. Read-only status of the REFA unfaulted IRQ.	0x0	R
		0	REFA faulted		REFA faulted. Read-only status of the REFA faulted IRQ.	0x0	R
0x300E	REFB	7	REFBB R divider resynced		REFBB R divider resynced. Read-only status of the REFBB R divider resynced IRQ.	0x0	R
		6	REFBB validated		REFBB validated. Read-only status of the REFBB validated IRQ.	0x0	R
		5	REFBB unfaulted		REFBB unfaulted. Read-only status of the REFBB unfaulted IRQ.	0x0	R
		4	REFBB faulted		REFBB faulted. Read-only status of the REFBB faulted IRQ.	0x0	R
		3	REFB R divider resynced		REFB R divider resynced. Read-only status of the REFB R divider resynced IRQ.	0x0	R
		2	REFB valid		REFB validated. Read-only status of the REFB valid IRQ.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	REFB unfaulted		REFB unfaulted. Read-only status of the REFB unfaulted IRQ.	0x0	R
		0	REFB faulted		REFB faulted. Read-only status of the REFB faulted IRQ.	0x0	R
0x300F	Timestamp	[7:5]	Reserved		Reserved.	0x0	R
		4	Skew updated		Skew measurement updated. Read-only status of the ref input skew measurement updated IRQ.	0x0	R
		3	Timestamp 1 event		Timestamp 1 time code available. Read-only status of the Timestamp 1 event IRQ.	0x0	R
		2	Timestamp 0 event		Timestamp 0 time code available. Read-only status of the Timestamp 0 event IRQ.	0x0	R
		1	Auxiliary NCO 1 event		Auxiliary NCO 1 event. Read-only status of the Auxiliary NCO 1 event IRQ.	0x0	R
		0	Auxiliary NCO 0 event		Auxiliary NCO 0 event. Read-only status of the Auxiliary NCO 0 event IRQ.	0x0	R

IRQ MAP DPLL0 READ REGISTERS—REGISTER 0x3010 TO REGISTER 0x3014

Table 106. IRQ Map DPLL0 Read Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3010	Lock	DPLL0 frequency clamp deactivated	DPLL0 frequency clamp activated	DPLL0 phase slew limiter deactivated	DPLL0 phase slew limiter activated	DPLL0 frequency unlocked	DPLL0 frequency locked	DPLL0 phase unlocked	DPLL0 phase locked	0x00	R
0x3011	State	DPLL0 reference switching	DPLL0 freerun entered	DPLL0 holdover entered	DPLL0 hitless entered	DPLL0 hitless exited	DPLL0 history updated	Reserved	DPLL0 phase step detecteded	0x00	R
0x3012	Fast acqui-sition	Reserved			DPLL0 N-divider resynced	DPLL0 fast acquisition completed	DPLL0 fast acquisition started	Reserved		0x00	R
0x3013	Activated profile	Reserved		DPLL0 Profile 5 activated	DPLL0 Profile 4 activated	DPLL0 Profile 3 activated	DPLL0 Profile 2 activated	DPLL0 Profile 1 activated	DPLL0 Profile 0 activated	0x00	R
0x3014	APLL	Reserved			DPLL0 distribution synced	APLL0 unlocked	APLL0 locked	APLL0 calibration completed	APLL0 calibration started	0x00	R

Table 107. IRQ Map DPLL0 Read Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3010	Lock	7	DPLL0 frequency clamp deactivated		Frequency clamp deactivated. Read-only status of IRQ for DPLL0 frequency clamp deactivated.	0x0	R
		6	DPLL0 frequency clamp activated		Frequency clamp activated. Read-only status of IRQ for DPLL0 frequency clamp activated.	0x0	R
		5	DPLL0 phase slew limiter deactivated		Phase slew limiter deactivated. Read-only status of IRQ for DPLL0 phase slew limiter deactivated.	0x0	R
		4	DPLL0 phase slew limiter activated		Phase slew limiter activated. Read-only status of IRQ for DPLL0 phase slew limiter activated.	0x0	R
		3	DPLL0 frequency unlocked		Frequency unlocked. Read-only status of IRQ for DPLL0 FLD (locked to unlocked transition).	0x0	R
		2	DPLL0 frequency locked		Frequency locked. Read-only status of IRQ for DPLL0 FLD (unlocked to locked transition).	0x0	R
		1	DPLL0 phase unlocked		Phase unlocked. Read-only status of IRQ for DPLL0 PLD (locked to unlocked transition).	0x0	R
		0	DPLL0 phase locked		Phase locked. Read-only status of IRQ for DPLL0 PLD (unlocked to locked transition).	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3011	State	7	DPLL0 reference switching		Reference switching. Read-only status of IRQ for DPLL0 reference input switching.	0x0	R
		6	DPLL0 freerun entered		Freerun mode entered. Read-only status of IRQ for DPLL0 freerun mode entered.	0x0	R
		5	DPLL0 holdover entered		Holdover mode entered. Read-only status of IRQ for DPLL0 holdover mode entered.	0x0	R
		4	DPLL0 hitless entered		Hitless mode entered. Read-only status of IRQ for DPLL0 hitless mode entered.	0x0	R
		3	DPLL0 hitless exited		Hitless mode exited. Read-only status of IRQ for DPLL0 hitless mode exited.	0x0	R
		2	DPLL0 history updated		Holdover history updated. Read-only status of IRQ for DPLL0 tuning word holdover history updated.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DPLL0 phase step detected		Phase step detected. Read-only status of IRQ for DPLL0 reference input phase step detected.	0x0	R
0x3012	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 N-divider resynced		N-divider resynchronized. Read-only status of IRQ for DPLL0 N-divider resynced.	0x0	R
		3	DPLL0 fast acquisition completed		Fast acquisition completed. Read-only status of IRQ for DPLL0 fast acquisition completed.	0x0	R
		2	DPLL0 fast acquisition started		Fast acquisition started. Read-only status of IRQ for DPLL0 fast acquisition started.	0x0	R
		[1:0]	Reserved		Reserved.	0x0	R
0x3013	Activated profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 Profile 5 activated		Profile 5 activated. Read-only status of IRQ for DPLL0 Profile 5 activated.	0x0	R
		4	DPLL0 Profile 4 activated		Profile 4 activated. Read-only status of IRQ for DPLL0 Profile 4 activated.	0x0	R
		3	DPLL0 Profile 3 activated		Profile 3 activated. Read-only status of IRQ for DPLL0 Profile 3 activated.	0x0	R
		2	DPLL0 Profile 2 activated		Profile 2 activated. Read-only status of IRQ for DPLL0 Profile 2 activated.	0x0	R
		1	DPLL0 Profile 1 activated		Profile 1 activated. Read-only status of IRQ for DPLL0 Profile 1 activated.	0x0	R
		0	DPLL0 Profile 0 activated		Profile 0 activated. Read-only status of IRQ for DPLL0 Profile 0 activated.	0x0	R
0x3014	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL0 distribution synced		Clock distribution synced. Read-only status of IRQ for DPLL0 clock distribution synced.	0x0	R
		3	APLL0 unlocked		Unlock detected. Read-only status of IRQ for APLL0 unlock detected (lock to unlock transition).	0x0	R
		2	APLL0 locked		Lock detected. Read-only status of IRQ for APLL0 lock detected (unlock to lock transition).	0x0	R
		1	APLL0 calibration completed		Calibration completed. Read-only status of IRQ for APLL0 calibration completed.	0x0	R
		0	APLL0 calibration started		Calibration started. Read-only status of IRQ for APLL0 calibration started.	0x0	R

IRQ MAP DPLL1 READ REGISTERS—REGISTER 0x3015 TO REGISTER 0x3019

Table 108. IRQ Map DPLL1 Read Registers Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3015	Lock	DPLL1 frequency clamp deactivated	DPLL1 frequency clamp activated	DPLL1 phase slew limiter deactivated	DPLL1 phase slew limiter activated	DPLL1 frequency unlocked	DPLL1 frequency locked	DPLL1 phase unlocked	DPLL1 phase locked	0x00	R
0x3016	State	DPLL1 reference switching	DPLL1 freerun entered	DPLL1 holdover entered	DPLL1 hitless entered	DPLL1 hitless exited	DPLL1 history updated	Reserved	DPLL1 phase step detected	0x00	R
0x3017	Fast acquisition	Reserved			DPLL1 N-divider resynced	DPLL1 Fast acquisition completed	DPLL1 Fast acquisition started	Reserved		0x00	R
0x3018	Activated profile	Reserved		DPLL1 Profile 5 activated	DPLL1 Profile 4 activated	DPLL1 Profile 3 activated	DPLL1 Profile 2 activated	DPLL1 Profile 1 activated	DPLL1 Profile 0 activated	0x00	R
0x3019	APLL	Reserved			DPLL1 distribution synced	APLL1 unlocked	APLL1 locked	APLL1 calibration completed	APLL1 calibration started	0x00	R

Table 109. IRQ Map DPLL1 Read Registers Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3015	Lock	7	DPLL1 frequency clamp deactivated		Frequency clamp deactivated. Read-only status of IRQ for DPLL1 frequency clamp deactivated.	0x0	R
		6	DPLL1 frequency clamp activated		Frequency clamp activated. Read-only status of IRQ for DPLL1 frequency clamp activated.	0x0	R
		5	DPLL1 phase slew limiter deactivated		Phase slew limiter deactivated. Read-only status of IRQ for DPLL1 phase slew limiter deactivated.	0x0	R
		4	DPLL1 phase slew limiter activated		Phase slew limiter activated. Read-only status of IRQ for DPLL1 phase slew limiter activated.	0x0	R
		3	DPLL1 frequency unlocked		Frequency unlocked. Read-only status of IRQ for DPLL1 FLD (locked to unlocked transition).	0x0	R
		2	DPLL1 frequency locked		Frequency locked. Read-only status of IRQ for DPLL1 FLD (unlocked to locked transition).	0x0	R
		1	DPLL1 phase unlocked		Phase unlocked. Read-only status of IRQ for DPLL1 PLD (locked to unlocked transition).	0x0	R
		0	DPLL1 phase locked		Phase locked. Read-only status of IRQ for DPLL1 PLD (unlocked to locked transition).	0x0	R
0x3016	State	7	DPLL1 reference switching		Reference switching. Read-only status of IRQ for DPLL1 reference input switching.	0x0	R
		6	DPLL1 freerun entered		Freerun mode entered. Read-only status of IRQ for DPLL1 freerun mode entered.	0x0	R
		5	DPLL1 holdover entered		Holdover mode entered. Read-only status of IRQ for DPLL1 holdover mode entered.	0x0	R
		4	DPLL1 hitless entered		Hitless mode entered. Read-only status of IRQ for DPLL1 hitless mode entered.	0x0	R
		3	DPLL1 hitless exited		Hitless mode exited. Read-only status of IRQ for DPLL1 hitless mode exited.	0x0	R
		2	DPLL1 history updated		Holdover history updated. Read-only status of IRQ for DPLL1 tuning word holdover history updated.	0x0	R
		1	Reserved		Reserved.	0x0	R
		0	DPLL1 phase step detect		Phase step detected. Read-only status of IRQ for DPLL1 reference input phase step detected	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3017	Fast acquisition	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 N-divider resynced		N-divider resynchronized. Read-only status of IRQ for DPLL1 N-divider resynchronization.	0x0	R
		3	DPLL1 fast acquisition completed		Fast acquisition completed. Read-only status of IRQ for DPLL1 fast acquisition completed.	0x0	R
		2	DPLL1 Fast acquisition started		Fast acquisition started. Read-only status of IRQ for DPLL1 fast acquisition started.	0x0	R
		[1:0]	Reserved		Reserved.	0x0	R
0x3018	Activated profile	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 Profile 5 activated		Profile 5 activated. Read-only status of IRQ for DPLL1 Profile 5 activated	0x0	R
		4	DPLL1 Profile 4 activated		Profile 4 activated. Read-only status of IRQ for DPLL1 Profile 4 activated	0x0	R
		3	DPLL1 Profile 3 activated		Profile 3 activated. Read-only status of IRQ for DPLL1 Profile 3 activated	0x0	R
		2	DPLL1 Profile 2 activated		Profile 2 activated. Read-only status of IRQ for DPLL1 Profile 2 activated	0x0	R
		1	DPLL1 Profile 1 activated		Profile 1 activated. Read-only status of IRQ for DPLL1 Profile 1 activated	0x0	R
		0	DPLL1 Profile 0 activated		Profile 0 activated. Read-only status of IRQ for DPLL1 Profile 0 activated	0x0	R
0x3019	APLL	[7:5]	Reserved		Reserved.	0x0	R
		4	DPLL1 distribution synced		Clock distribution synchronized. Read-only status of IRQ for DPLL1 clock distribution synchronized.	0x0	R
		3	APLL1 unlocked		Unlock detected. Read-only status of IRQ for APLL1 unlock detected (lock to unlock transition).	0x0	R
		2	APLL1 lock		Lock detected. Read-only status of IRQ for APLL1 lock detected (unlock to lock transition).	0x0	R
		1	APLL1 calibration completed		Calibration completed. Read-only status of IRQ for APLL1 calibration completed.	0x0	R
		0	APLL1 calibration started		Calibration started. Read-only status of IRQ for APLL1 calibration started.	0x0	R

STATUS READBACK PLL0 REGISTERS—REGISTER 0x3100 TO REGISTER 0x310E

Table 110. STATUS_READBACK_PLL_0 Register Summary

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3100	DPLL0 lock status	Reserved		APLL0 calibration done	APLL0 calibration busy	APLL0 Lock	DPLL0 frequency lock	DPLL0 phase lock	Channel 0 all lock	0xXX	R
0x3101	DPLL0 operation	Reserved	DPLL0 active profile			DPLL0 active	DPLL0 reference switch	DPLL0 Holdover	DPLL0 freerun	0xXX	R
0x3102	DPLL0 state	Reserved		DPLL0 FACQ done	DPLL0 FACQ active	Reserved	DPLL0 phase slew limit	DPLL0 frequency clamp	DPLL0 history available	0xXX	R
0x3103	DPLL0 tuning word history	DPLL0 tuning word history [7:0]								0xXX	R
0x3104		DPLL0 tuning word history [15:8]								0xXX	R
0x3105		DPLL0 tuning word history [23:16]								0xXX	R
0x3106		DPLL0 tuning word history [31:24]								0xXX	R
0x3107		DPLL0 tuning word history [39:32]								0xXX	R
0x3108		Reserved		DPLL0 tuning word history [45:40]						0xXX	R
0x3109	DPLL0 PLD Tub	DPLL0 PLD tub [7:0]								0xXX	R
0x310A		Reserved				DPLL0 PLD tub [11:8]				0x0X	R

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x310B	DPLL0 FLD Tub	DPLL0 FLD tub[7:0]								0xXX	R
0x310C		Reserved			DPLL0 FLD tub [11:8]					0x0X	R
0x310D	DPLL0 distribution phase slew active	Reserved		Channel 0 phase slew active						0xXX	R
0x310E	DPLL0 distribution phase slew error	Reserved		Channel 0 phase control error						0xXX	R

Table 111. STATUS_READBACK_PLL_0 Register Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3100	DPLL0 lock status	[7:6]	Reserved		Reserved.	0x0	R
		5	APLL0 calibration done		APLL0 calibration complete. This read-only bit is Logic 1 when APLL0 calibration is complete. This bit remains Logic 1 until another APLL0 calibration is issued. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		4	APLL0 calibration busy		APLL0 calibration in progress. This read-only bit is Logic 1 when APLL0 calibration is in progress. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		3	APLL0 lock		APLL0 lock. This read-only bit is Logic 1 when APLL0 is locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		2	DPLL0 frequency lock		DPLL0 frequency lock. This read-only bit is Logic 1 when DPLL0 is frequency locked. All of the bits in this register are live, meaning that their status is dynamically updated with needing an IO_UPDATE command before reading.	Prog	RP
		1	DPLL0 phase lock		DPLL0 phase lock. This read-only bit is Logic 1 when DPLL0 is phase locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		0	Channel 0 all lock		Channel 0 all lock. This read-only bit is the logical AND of the APLL0 lock and the DPLL0 phase lock bits in this register. It is Logic 1 when both PLLs are locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
0x3101	DPLL0 operation	7	Reserved		Reserved.	0x0	R
		[6:4]	DPLL0 active profile		DPLL0 active profile. This 3-bit bit field contains the active profile for DPLL0. If DPLL0 is not active, this bit field contains the last active profile. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		3	DPLL0 active		DPLL0 active. This read-only bit is Logic 1 when DPLL0 is actively tracking an input reference. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	DPLL0 reference switch		DPLL0 input reference switching. This read-only bit is Logic 1 when DPLL0 is switching input references. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL0 holdover		DPLL0 is in holdover mode. This read-only bit is Logic 1 when DPLL0 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL0 freerun		DPLL0 is in freerun mode. This read-only bit is Logic 1 when DPLL0 is in freerun mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3102	DPLL0 state	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL0 FACQ done		DPLL0 fast acquisition done. This read-only bit is Logic 1 when the DPLL0 fast acquisition is completed is complete. It is cleared by writing Logic 1 to the clear DPLL0 fast acquisition (FACQ) done bit. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		4	DPLL0 FACQ active		DPLL0 fast acquisition active. This read-only bit is Logic 1 when the DPLL0 fast acquisition logic is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		3	Reserved		Reserved.	Prog	RP
		2	DPLL0 phase slew limit		DPLL0 phase slew limiter active. This read-only bit is Logic 1 when the DPLL0 phase slew limiter is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL0 frequency clamp		DPLL0 frequency clamp is active. This read-only bit is Logic 1 when the DPLL0 frequency clamp is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL0 history available		DPLL0 history available. This read-only bit is Logic 1 when the DPLL0 holdover history is available. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3103	DPLL0 tuning word history	[7:0]	DPLL0 tuning word history [7:0]		DPLL0 tuning word history. This 46-bit bit field contains the DPLL0 tuning word history that is used while DPLL0 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3104		[7:0]	DPLL0 tuning word history [15:8]			Prog	RP
0x3105		[7:0]	DPLL0 tuning word history [23:16]			Prog	RP
0x3106		[7:0]	DPLL0 tuning word history [31:24]			Prog	RP
0x3107		[7:0]	DPLL0 tuning word history [39:32]			Prog	RP
0x3108		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL0 tuning word history [45:40]		DPLL0 tuning word history. This 46-bit bit field contains the DPLL0 tuning word history that is used while DPLL0 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3109	DPLL0 PLD tub	[7:0]	DPLL0 PLD tub [7:0]		DPLL0 PLD tub level. This 12-bit bit field contains the DPLL0 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310A		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL0 PLD tub [11:8]		DPLL0 PLD tub level. This 12-bit bit field contains the DPLL0 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310B	DPLL0 FLD tub	[7:0]	DPLL0 FLD tub [7:0]		DPLL0 FLD tub level. This 12-bit bit field contains the DPLL0 FLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310C		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL0 FLD tub [11:8]		DPLL0 FLD tub level. This 12-bit bit field contains the DPLL0 FLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x310D	DPLL0 distribution phase slew active	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Channel 0 phase slew active		Channel 0 phase slewing active. This 6-bit bit field contains read-only bits that are Logic 1 when phase slewing is active on the DPLL0 Q0x Dividers, where x is A, AA, B, BB, C, and CC. An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows: Bit 0 is Logic 1 when phase slewing is active on Divider Q0A. Bit 1 is Logic 1 when phase slewing is active on Divider Q0AA. Bit 2 is Logic 1 when phase slewing is active on Divider Q0B. Bit 3 is Logic 1 when phase slewing is active on Divider Q0BB. Bit 4is Logic 1 when phase slewing is active on Divider Q0C. Bit 5 is Logic 1 when phase slewing is active on Divider Q0CC.	Prog	RP
0x310E	DPLL0 distribution phase slew error	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Channel 0 phase control error		Channel 0 Phase Control Error. This 6-bit bit field contains read-only bits that are Logic 1 when phase slewing is active on the DPLL0 Q0x Dividers, where x is A, AA, B, BB, C, and CC. An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows: Bit 0 is Logic 1 when phase slewing is active on Divider Q0A. Bit 1 is Logic 1 when phase slewing is active on Divider Q0AA. Bit 2 is Logic 1 when phase slewing is active on Divider Q0B. Bit 3 is Logic 1 when phase slewing is active on Divider Q0BB. Bit 4 is Logic 1 when phase slewing is active on Divider Q0C. Bit 5 is Logic 1 when phase slewing is active on Divider Q0CC.	Prog	RP

STATUS READBACK PLL1 REGISTERS—REGISTER 0x3200 TO REGISTER 0x320E

Table 112. STATUS_READBACK_PLL_1 Register Summary

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3200	DPLL1 lock status	Reserved		APLL1 calibration done	APLL1 calibration busy	APLL1 lock	DPLL1 frequency lock	DPLL1 phase lock	Ch1 all lock	0xXX	R
0x3201	DPLL1 operation	Reserved	DPLL1 active profile			DPLL1 active	DPLL1 reference switch	DPLL1 holdover	DPLL1 freerun	0xXX	R
0x3202	DPLL1 state	Reserved		DPLL1 FACQ done	DPLL1 FACQ active	RESERVED	DPLL1 phase slew limit	DPLL1 frequency clamp	DPLL1 history available	0xXX	R
0x3203	DPLL1 tuning word history	DPLL1 tuning word history [7:0]								0xXX	R
0x3204		DPLL1 tuning word history [15:8]								0xXX	R
0x3205		DPLL1 tuning word history [23:16]								0xXX	R
0x3206		DPLL1 tuning word history [31:24]								0xXX	R
0x3207		DPLL1 tuning word history [39:32]								0xXX	R
0x3208		Reserved		DPLL1 tuning word history [45:40]						0xXX	R
0x3209	DPLL1 PLD tub	DPLL1 PLD Tub [7:0]								0xXX	R
0x320A		Reserved				DPLL1 PLD Tub [11:8]				0x0X	R
0x320B	DPLL1 FLD tub	DPLL1 FLD Tub [7:0]								0xXX	R
0x320C		Reserved				DPLL1 FLD Tub [11:8]				0x0X	R
0x320D	DPLL1 distribution phase slew active	Reserved				Channel 1 phase slew active				0x0X	R
0x320E	DPLL1 distribution phase slew error	Reserved				Channel 1 phase control error				0x0X	R

Table 113. STATUS_READBACK_PLL_1 Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3200	DPLL1 lock status	[7:6]	Reserved		Reserved.	0x0	R
		5	APLL1 calibration done		APLL1 calibration complete. This read-only bit is Logic 1 when APLL1 calibration is complete. This bit remains Logic 1 until another APLL1 calibration is issued. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		4	APLL1 calibration busy		APLL1 calibration in progress. This read-only bit is Logic 1 when APLL1 calibration is in progress. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		3	APLL1 lock		APLL1 lock. This read-only bit is Logic 1 when APLL1 is locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	DPLL1 frequency lock		DPLL1 frequency lock. This read-only bit is Logic 1 when DPLL1 is frequency locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		1	DPLL1 phase lock		DPLL1 phase lock. This read-only bit is Logic 1 when DPLL1 is phase locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
		0	Channel 1 all lock		Channel 1 all lock. This read-only bit is the logical AND of the APLL1 lock and the DPLL1 phase lock bits in this register. It is Logic 1 when both PLLs are locked. All of the bits in this register are live, meaning their status is dynamically updated without needing an IO_UPDATE command before reading.	Prog	RP
0x3201	DPLL1 operation	7	Reserved		Reserved.	0x0	R
		[6:4]	DPLL1 active profile		DPLL1 active profile. This 3-bit bit field contains the active profile for DPLL1. If DPLL1 is not active, this bit field contains the last active profile. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		3	DPLL1 active		DPLL1 active. This read-only bit is Logic 1 when DPLL1 is actively tracking an input reference. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		2	DPLL1 reference switch		DPLL1 input reference switching. This read-only bit is Logic 1 when DPLL1 is switching input references. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL1 holdover		DPLL1 is in holdover mode. This read-only bit is Logic 1 when DPLL1 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL1 freerun		DPLL1 is in freerun mode. This read-only bit is Logic 1 when DPLL1 is in freerun mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3202	DPLL1 state	[7:6]	Reserved		Reserved.	0x0	R
		5	DPLL1 FACQ done		DPLL1 fast acquisition done. This read-only bit is Logic 1 when the DPLL1 fast acquisition is completed is complete. It is cleared by writing Logic 1 to the clear DPLL1 FACQ done bit. An input/output update is needed immediately before reading this register to read its latest value.	Prog	RP
		4	DPLL1 FACQ active		DPLL1 fast acquisition active. This read-only bit is Logic 1 when the DPLL1 fast acquisition logic is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		3	Reserved		Reserved.	Prog	RP
		2	DPLL1 phase slew limit		DPLL1 phase slew limiter active. This read-only bit is Logic 1 when the DPLL1 phase slew limiter is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		1	DPLL1 frequency clamp		DPLL1 frequency clamp is active. This read-only bit is Logic 1 when the DPLL1 frequency clamp is active. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
		0	DPLL1 turning world history		DPLL1 history available. This read-only bit is Logic 1 when the DPLL0 holdover history is available. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3203	DPLL1 tuning word history	[7:0]	DPLL1 turning world history [7:0]		DPLL1 tuning word history. This 46-bit bit field contains the DPLL1 tuning word history that is used while DPLL1 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3204		[7:0]	DPLL1 turning world history [15:8]			Prog	RP
0x3205		[7:0]	DPLL1 turning world history [23:16]			Prog	RP
0x3206		[7:0]	DPLL1 turning world history [31:24]			Prog	RP
0x3207		[7:0]	DPLL1 turning world history [39:32]			Prog	RP
0x3208		[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	DPLL1 turning world history [45:40]		DPLL1 tuning word history. This 46-bit bit field contains the DPLL1 tuning word history that is used while DPLL1 is in holdover mode. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x3209	DPLL1 PLD tub	[7:0]	DPLL1 PLD tub [7:0]		DPLL1 PLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x320A		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 PLD tub [11:8]		DPLL1 PLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x320B	DPLL1 FLD tub	[7:0]	DPLL1 FLD tub [7:0]		DPLL1 FLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x320C		[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DPLL1 FLD tub [11:8]		DPLL1 FLD tub level. This 12-bit bit field contains the DPLL1 PLD tub level. An IO_UPDATE command is needed immediately before reading this register to read its latest value.	Prog	RP
0x320D	DPLL1 distribution phase slew active	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Channel 1 phase slew active		Channel 1 phase slewing active. This 4-bit bit field contains read-only bits that are Logic 1 when phase slewing is active on the DPLL1 Q1x Dividers, where x is A, AA, B, BB. An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows: Bit 0 is Logic 1 when phase slewing is active on Divider Q1A. Bit 1 is Logic 1 when phase slewing is active on Divider Q1AA. Bit 2 is Logic 1 when phase slewing is active on Divider Q1B. Bit 3 is Logic 1 when phase slewing is active on Divider Q1BB.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x320E	DPLL1 distribution phase slew error	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Channel 1 phase control error		Channel 1 phase control error. This 4-bit bit field contains read-only bits that are Logic 1 when phase slewing is active on the DPLL1 Q1x Dividers, where x is A, AA, B, BB. An IO_UPDATE command is needed immediately before reading this register to read its latest value. The bit mapping is as follows: Bit 0 is Logic 1 when phase slewing is active on Divider Q1A. Bit 1 is Logic 1 when phase slewing is active on Divider Q1AA. Bit 2 is Logic 1 when phase slewing is active on Divider Q1B. Bit 3 is Logic 1 when phase slewing is active on Divider Q1BB.	Prog	RP

AUXILIARY TDC READ REGISTERS—REGISTER 0x3A00 TO REGISTER 0x3A3B

Table 114. TDC_AUXILIARY_READ Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3A00	AUXNCO0 time	Auxiliary NCO 0 time clock [7:0]								0xXX	R
0x3A01		Auxiliary NCO 0 time clock [15:8]								0xXX	R
0x3A02		Auxiliary NCO 0 time clock [23:16]								0xXX	R
0x3A03		Auxiliary NCO 0 time clock [31:24]								0xXX	R
0x3A04		Auxiliary NCO 0 time clock [39:32]								0xXX	R
0x3A05		Auxiliary NCO 0 time clock [47:40]								0xXX	R
0x3A06		Auxiliary NCO 0 time clock [55:48]								0xXX	R
0x3A07		Auxiliary NCO 0 time clock [63:56]								0xXX	R
0x3A08		Auxiliary NCO 0 time clock [71:64]								0xXX	R
0x3A09		Auxiliary NCO 0 time clock [79:72]								0xXX	R
0x3A0A	AUXNCO1 time	Auxiliary NCO 1 time clock [7:0]								0xXX	R
0x3A0B		Auxiliary NCO 1 time clock [15:8]								0xXX	R
0x3A0C		Auxiliary NCO 1 time clock [23:16]								0xXX	R
0x3A0D		Auxiliary NCO 1 time clock [31:24]								0xXX	R
0x3A0E		Auxiliary NCO 1 time clock [39:32]								0xXX	R
0x3A0F		Auxiliary NCO 1 time clock [47:40]								0xXX	R
0x3A10		Auxiliary NCO 1 time clock [55:48]								0xXX	R
0x3A11		Auxiliary NCO 1 time clock [63:56]								0xXX	R
0x3A12		Auxiliary NCO 1 time clock [71:64]								0xXX	R
0x3A13		Auxiliary NCO 1 time clock [79:72]								0xXX	R
0x3A14	Timestamp 0 event time	Event 0 time [7:0]								0xXX	R
0x3A15		Event 0 time [15:8]								0xXX	R
0x3A16		Event 0 time [23:16]								0xXX	R
0x3A17		Event 0 time [31:24]								0xXX	R
0x3A18		Event 0 time [39:32]								0xXX	R
0x3A19		Event 0 time [47:40]								0xXX	R
0x3A1A		Event 0 time [55:48]								0xXX	R
0x3A1B		Event 0 time [63:56]								0xXX	R
0x3A1C		Event 0 time [71:64]								0xXX	R
0x3A1D		Event 0 time [79:72]								0xXX	R
0x3A1E		User Timestamp 0 missed count								0xXX	R
0x3A1F		Reserved							User Timestamp 0 low resolution	0x0X	R

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x3A20	Timestamp 1 event time	Event 1 time [7:0]								0xXX	R
0x3A21		Event 1 time [15:8]								0xXX	R
0x3A22		Event 1 time [23:16]								0xXX	R
0x3A23		Event 1 time [31:24]								0xXX	R
0x3A24		Event 1 time [39:32]								0xXX	R
0x3A25		Event 1 time [47:40]								0xXX	R
0x3A26		Event 1 time [55:48]								0xXX	R
0x3A27		Event 1 time [63:56]								0xXX	R
0x3A28		Event 1 time [71:64]								0xXX	R
0x3A29		Event 1 time [79:72]								0xXX	R
0x3A2A		User Timestamp 1 missed count								0xXX	R
0x3A2B		Reserved							User Timestamp 1 low resolution	0x0X	R
0x3A2C	Skew offset	Skew offset [7:0]								0xXX	R
0x3A2D		Skew offset [15:8]								0xXX	R
0x3A2E		Skew offset [23:16]								0xXX	R
0x3A2F		Skew offset [31:24]								0xXX	R
0x3A30		Skew offset [39:32]								0xXX	R
0x3A31		Skew offset [47:40]								0xXX	R
0x3A32		Skew offset [55:48]								0xXX	R
0x3A33		Skew offset full window	Reserved	Skew offset [61:56]						0xXX	R
0x3A34	Skew drift	Skew drift [7:0]								0xXX	R
0x3A35		Skew drift [15:8]								0xXX	R
0x3A36		Skew drift [23:16]								0xXX	R
0x3A37		Skew drift [31:24]								0xXX	R
0x3A38		Skew drift [39:32]								0xXX	R
0x3A39		Skew drift [47:40]								0xXX	R
0x3A3A		Skew drift [55:48]								0xXX	R
0x3A3B		Skew drift full window	Reserved	Skew drift [61:56]						0xXX	R

Table 115. TDC_AUXILIARY_READ Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3A00	AUXNCO0 time	[7:0]	Auxiliary NCO 0 time clock [7:0]		Auxiliary NCO 0 time clock. This 80-bit read-only bit field contains the value of the NCO 0 time clock at the time the last IO_UPDATE command was latched by the digital logic. It is useful in two ways: the user can compare the relative phases of NCO 0 and NCO 1. In addition, the integer portion of this bit field can determined how many NCO events occur in a given time interval.	Prog	RP
0x3A01		[7:0]	Auxiliary NCO 0 time clock [15:8]			Prog	RP
0x3A02		[7:0]	Auxiliary NCO 0 time clock [23:16]			Prog	RP
0x3A03		[7:0]	Auxiliary NCO 0 time clock [31:24]			Prog	RP
0x3A04		[7:0]	Auxiliary NCO 0 time clock [39:32]			Prog	RP
0x3A05		[7:0]	Auxiliary NCO 0 time clock [47:40]			Prog	RP
0x3A06		[7:0]	Auxiliary NCO 0 time clock [55:48]			Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3A07		[7:0]	Auxiliary NCO 0 time clock [63:56]			Prog	RP
0x3A08		[7:0]	Auxiliary NCO 0 time clock [71:64]			Prog	RP
0x3A09		[7:0]	Auxiliary NCO 0 time clock [79:72]			Prog	RP
0x3A0A		[7:0]	Auxiliary NCO 1 time clock [7:0]			Prog	RP
0x3A0B	AUXNCO1 time	[7:0]	Auxiliary NCO 1 time clock [15:8]		Auxiliary NCO 1 time clock. This 80-bit read-only bit field contains the value of the NCO 1 time clock at the time the last IO_UPDATE command was latched by the digital logic. It is useful in two ways: the user can compare the relative phases of NCO 0 and NCO 1. In addition, the integer portion of this bit field can determined how many NCO events occur in a given time interval.	Prog	RP
0x3A0C		[7:0]	Auxiliary NCO 1 time clock [23:16]			Prog	RP
0x3A0D		[7:0]	Auxiliary NCO 1 time clock [31:24]			Prog	RP
0x3A0E		[7:0]	Auxiliary NCO 1 time clock [39:32]			Prog	RP
0x3A0F		[7:0]	Auxiliary NCO 1 time clock [47:40]			Prog	RP
0x3A10		[7:0]	Auxiliary NCO 1 time clock [55:48]			Prog	RP
0x3A11		[7:0]	Auxiliary NCO 1 time clock [63:56]			Prog	RP
0x3A12		[7:0]	Auxiliary NCO 1 time clock [71:64]			Prog	RP
0x3A13		[7:0]	Auxiliary NCO 1 time clock [79:72]			Prog	RP
0x3A14	Timestamp 0 event time	[7:0]	Event 0 Time [7:0]		User Timestamp Event 0 time. This 80-bit read-only bit field contains the User Timestamp 0 event time.	Prog	RP
0x3A15		[7:0]	Event 0 Time [15:8]			Prog	RP
0x3A16		[7:0]	Event 0 Time [23:16]			Prog	RP
0x3A17		[7:0]	Event 0 Time [31:24]			Prog	RP
0x3A18		[7:0]	Event 0 time [39:32]			Prog	RP
0x3A19		[7:0]	Event 0 time [47:40]			Prog	RP
0x3A1A		[7:0]	Event 0 time [55:48]			Prog	RP
0x3A1B		[7:0]	Event 0 time [63:56]			Prog	RP
0x3A1C		[7:0]	Event 0 time [71:64]			Prog	RP
0x3A1D		[7:0]	Event 0 time [79:72]			Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3A1E		[7:0]	User Timestamp 0 missed count		User Timestamp 0 missed count. This unsigned 8-bit bit field contains the number of user timestamps that have been lost in User Timestamp 0. There are two ways to lose a user timestamp: two user timestamps can arrive with no intervening IO_UPDATE command. In that case, the user timestamp in the active register space is overwritten. Or two user timestamps arrive with an IO_UPDATE command after each stamp, but the first user timestamp is not read before issuing another IO_UPDATE command. In that case, the user timestamp in the active register space is overwritten.	Prog	RP
0x3A1F		[7:1]	Reserved		Reserved.	0x0	R
		0	User Timestamp 0 low resolution		User Timestamp 0 low resolution flag. This bit is Logic 1 if the User Timestamp 0 processor detects an event edge that is outside of the expected event period. Discard the associated user timestamp if this bit is Logic 1.	Prog	RP
0x3A20	Timestamp 1 event time	[7:0]	Event 1 time [7:0]		User Timestamp Event 1 time. This 80-bit read-only bit field contains the User Timestamp 0 event time.	Prog	RP
0x3A21		[7:0]	Event 1 time [15:8]			Prog	RP
0x3A22		[7:0]	Event 1 time [23:16]			Prog	RP
0x3A23		[7:0]	Event 1 time [31:24]			Prog	RP
0x3A24		[7:0]	Event 1 time [39:32]			Prog	RP
0x3A25		[7:0]	Event 1 time [47:40]			Prog	RP
0x3A26		[7:0]	Event 1 time [55:48]			Prog	RP
0x3A27		[7:0]	Event 1 time [63:56]			Prog	RP
0x3A28		[7:0]	Event 1 time [71:64]			Prog	RP
0x3A29		[7:0]	Event 1 time [79:72]			Prog	RP
0x3A2A		[7:0]	User Timestamp 1 missed count		User Timestamp 1 missed count. This unsigned 8-bit bit field contains the number of user timestamps that have been lost in User Timestamp 1. There are two ways to lose a user timestamp: two user timestamps can arrive with no intervening IO_UPDATE command. In that case, the user timestamp in the active register space is overwritten. Or two user timestamps arrive with an IO_UPDATE command after each stamp, but the first user timestamp is not read before issuing another IO_UPDATE command. In that case, the user timestamp in the active register space is overwritten.	Prog	RP
0x3A2B		[7:1]	Reserved		Reserved.	0x0	R
		0	User Timestamp 1 low resolution		User Timestamp 1 low resolution flag. This bit is Logic 1 if the User Timestamp 1 processor detects an event edge that is outside of the expected event period. Discard the associated user timestamp if this bit is Logic 1.	Prog	RP

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x3A2C	Skew offset	[7:0]	Skew offset [7:0]		Skew offset. This signed, 62-bit bit field contains the result of a skew offset measurement between the rising edge of the skew reference source to the rising edge of the skew measurement source. If the skew offset calculation is fully averaged, the skew offset full window bit is Logic 1: the value in this bit field must be multiplied by 2^{-16} and the result is the measured skew in units of picoseconds. For example, a skew offset of 0x3FFFFFF8A67324B5 equals −31,567,174,475 decimal. Therefore, $-31,567,174,475 \times 2^{-16} = -481676.8$ ps (approximately), meaning the skew measurement edge leads the skew reference edge by ~482 ns.	Prog	RP
0x3A2D		[7:0]	Skew offset [15:8]			Prog	RP
0x3A2E		[7:0]	Skew offset [23:16]			Prog	RP
0x3A2F		[7:0]	Skew offset [31:24]			Prog	RP
0x3A30		[7:0]	Skew offset [39:32]			Prog	RP
0x3A31		[7:0]	Skew offset [47:40]			Prog	RP
0x3A32		[7:0]	Skew offset [55:48]			Prog	RP
0x3A33		7	Skew offset full window		Skew offset over full window. This bit is Logic 1 when the skew offset calculation is fully averaged over the window size determined by the skew window size bit field. It is Logic 0 if this condition is been met. There is an additional diagnostic bit associated with this measurement; the skew limit exceeded IRQ activates if the limits of the skew measurement processor are exceeded.	Prog	RP
		6	Reserved		Reserved.	0x0	R
		[5:0]	Skew offset [61:56]		Skew offset. This signed, 62-bit bit field contains the result of a skew offset measurement between the rising edge of the skew reference source to the rising edge of the skew measurement source. If the skew offset calculation is fully averaged, the skew offset full window bit is Logic 1: the value in this bit field must be multiplied by 2^{-16} and the result is the measured skew in units of picoseconds. For example, a skew offset of 0x3FFFFFF8A67324B5 equals −31,567,174,475 decimal. Therefore, $-31,567,174,475 \times 2^{-16} = -481676.8$ ps (approximately), meaning the skew measurement edge leads the skew reference edge by ~482 ns.	Prog	RP
0x3A34	Skew drift	[7:0]	Skew drift [7:0]		Skew drift. This signed, 62-bit bit field contains the result of a skew drift measurement between the successive periods of the skew reference source. Skew drift is a measure of the rate at which the unaveraged skew offset varies cycle by cycle. The value in this bit field must be must be multiplied by 2^{-16} and the result is in picoseconds per unit interval. The unit interval is the period of the reference source. For example, assume that the reference source has a frequency of 100 Hz, and a skew drift of 0x3FFFFFF8A67324B5 (−31,567,174,475 decimal) is read. Then, $-31,567,174,475 \times 2^{-16} = -481676.8$ ps (approximately). Because the reference period is 10 ms, this result indicates the reference measurement period is decreasing 482 ns every 10 ms relative to the reference source period, implying a frequency offset of −48.2 ppm. If the skew drift calculation is fully averaged, the skew drift over full window bit is Logic 1.	Prog	RP
0x3A35		[7:0]	Skew drift [15:8]			Prog	RP
0x3A36		[7:0]	Skew drift [23:16]			Prog	RP
0x3A37		[7:0]	Skew drift [31:24]			Prog	RP
0x3A38		[7:0]	Skew drift [39:32]			Prog	RP
0x3A39		[7:0]	Skew drift [47:40]			Prog	RP
0x3A3A		[7:0]	Skew drift [55:48]			Prog	RP
0x3A3B		7	Skew drift full window		Skew drift over full window. This bit is Logic 1 when the skew drift calculation is fully averaged over the window size determined by the skew window size bit field. It is Logic 0 if this condition is been met. There is an additional diagnostic bit associated with this measurement; the skew limit exceeded IRQ activates if the limits of the skew measurement processor is exceeded.	Prog	RP
		6	Reserved		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[5:0]	Skew drift [61:56]		Skew drift. This signed, 62-bit bit field contains the result of a skew drift measurement between the successive periods of the skew reference source. Skew drift is a measure of the rate at which the unaveraged skew offset varies cycle by cycle. The value in this bit field must be multiplied by 2^{-16} and the result is in picoseconds per unit interval. The unit interval is the period of the reference source. For example, assume that the reference source has a frequency of 100 Hz, and a skew drift of 0x 3FFFFFF8A67324B5 (−31,567,174,475 decimal) is read. Then, $-31,567,174,475 \times 2^{-16} =$ −481676.8 ps (approximately). Because the reference period is 10 ms, this result indicates the reference measurement period is decreasing 482 ns every 10 ms relative to the reference source period, implying a frequency offset of −48.2 ppm. If the skew drift calculation is fully averaged, the skew drift over full window bit is Logic 1.	Prog	RP

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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