VMK180 Evaluation Board

User Guide

UG1411 (v1.1) March 7, 2022

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Table of Contents

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Chapter 1

Introduction

Overview

The VMK180 evaluation board features the Xilinx® Versal® ACAP XCVM1802 device. The VMK180 board enables the demonstration, evaluation, and development of the applications listed here, as well as other customer applications.

- Storage acceleration
- Data center network acceleration
- Passive optical network
- Automotive
- Aerospace and defense
- Industrial, scientific, and medical
- Test and measurement
- Embedded vision
- Machine learning
- Audio video broadcast
- Wired and wireless

The VMK180 evaluation board is equipped with many of the common board-level features needed for design development, including:

- SFP28 and QSFP28 optical transceiver support
- LPDDR4 component and DDR4 UDIMM memory
- HDMI
- USB
- PMOD connectors
- CAN and Ethernet networking interfaces
- Two FMC+ expansion ports

- PCIe® (up to Gen4x8)

Models of Boards

The following table lists the models for the VMK180 evaluation board. See the VMK180 Evaluation Board product page for details.

Table 1: **Models of VMK180 Evaluation Boards**

Kit	Description
EK-VMK180-G	Versal ACAP VMK180 evaluation kit.
EK-VMK180-G-ED	Xilinx Versal ACAP VMK180 evaluation kit, encryption disabled, no secure boot support, China/Russia specific.
EK-VMK180-G-ED-J	Xilinx Versal ACAP VMK180 evaluation kit, Japan specific.

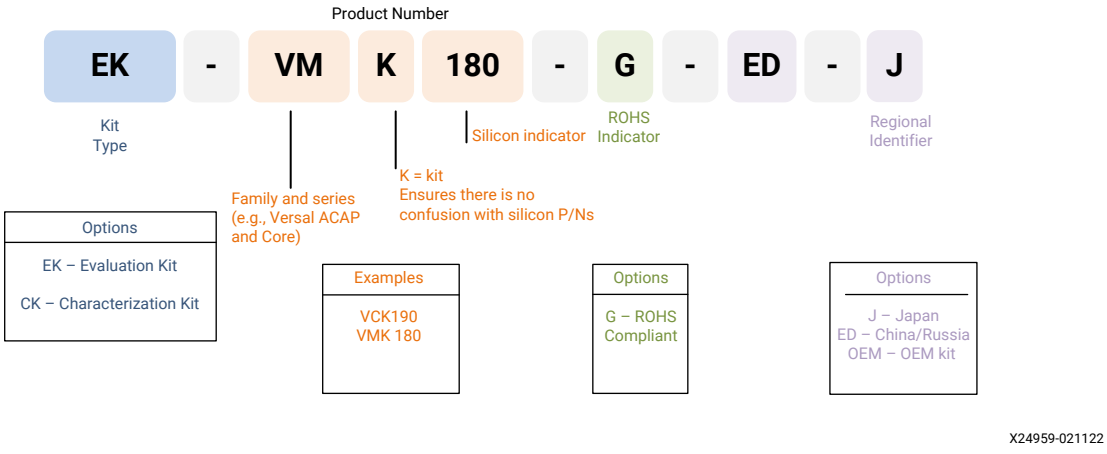
Notes:

1. Users of encryption-disabled kits will not be able to access the following features:
   - Secure boot
   - Secure key storage/management
   - Crypto HW acceleration (PS and APU crypto accelerators)
   - Encrypted bitstream loading
   - Encrypted BOOT.BIN partitions
   - PUF operation

Versal ACAP Kit Numbering

The Versal ACAP kit numbering is illustrated in the following figure.

Figure 1: **Kit Numbering**



Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. All Versal® ACAP design process Design Hubs and the Design Flow Assistant materials can be found on the Xilinx.com website. This document covers the following design processes:

- **Board System Design:** Designing a PCB through schematics and board layout. Also involves power, thermal, and signal integrity considerations. For more information, see Versal ACAP Design Process Documentation Board System Design.

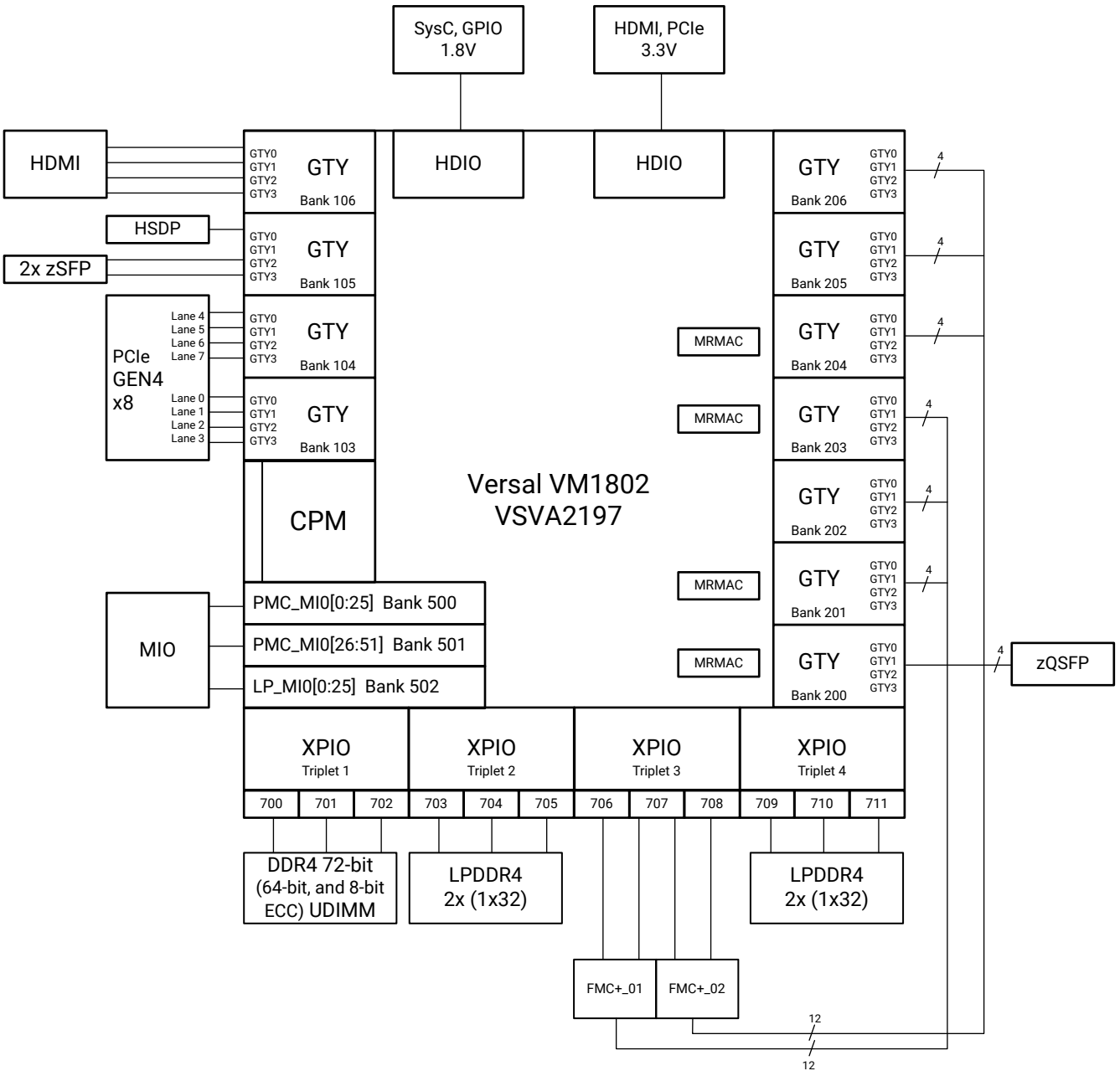
Additional Resources

See Appendix E: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the VMK180 evaluation board.

Block Diagram

The VMK180 block diagram is shown in the following figure.

Figure 2: **VMK180 Block Diagram**



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Board Features

The VMK180 evaluation board features are listed here. Detailed information for each feature is provided in Chapter 3: Board Component Descriptions.

- XCVM1802, VSVA2197 package
- Form factor: extended height PCIe®, double-slot (heatsink clearance)
- Onboard configuration from:
  - USB-to-JTAG bridge
  - JTAG pod 2 mm 2x7 flat cable connector
  - microSD card (PS MIO I/F)
  - microSD card (System Controller I/F)
- External boot module (EBM) configuration option
  - X-EBM-01 dual quad SPI (QSPI)
- Clocks
  - ACAP Bank 406 HDMI_REC_CLK_OUT 148.50 MHz
  - ACAP Bank 503 RTC Xtal 32.768 kHz
  - ACAP Bank 503 Si570 REF_CLK 33.3333 MHz
  - ACAP Bank 700 Si570 DDR4_CLK (DIMM) 200 MHz
  - ACAP Bank 705 Si570 DDR4_CLK2 (LPDDR4) 200 MHz
  - ACAP Bank 711 Si570 DDR4_CLK1 (LPDDR4) 200 MHz
  - ACAP Bank GTY103/4 (REFCLK0) PCIe_CLK0/1 100 MHz
  - ACAP Bank GTY105 (REFCLK0) Si570 zSFP_SI570_CLK 156.250 MHz
  - ACAP Bank GTY105 (REFCLK1) Si570 HSDP_SI570_CLK 156.250 MHz
  - ACAP Bank GTY200 (REFCLK0) 8A34001_CLK1_IN 100 MHz
  - IEEE-1588 eCPRI 8A34001 clocks (various)
- DDR4 8 GB 72-bit (64-bit, and 8-bit ECC) UDIMM
  - XPIO triplet 1 (banks 700, 701, 702)
- Two LPDDR4 interfaces (2x32-bit 4 GB components each)
  - XPIO triplets 2 (banks 703, 704, 705) and 4 (banks 709, 710, 711)

- PL FMCP HSCP (FMC+) connectivity
  - XPIO triplet 3 (banks 706, 707, 708)
  - FMCP1 HSCP full LA[00:33] bus
  - FMCP2 HSCP full LA[00:33] bus
- PL GPIO connections
  - PL UART1 to FTDI
  - PL GPIO DIP switch (4-position)
  - PL GPIO pushbuttons (two)
  - PL GPIO LEDs (four)
  - PL GPIO DC configuration header
  - PL SYSCTLR_GPIO[0:5]
- 44 PL GTY transceivers (11 quads)
  - PCIe 8-lane edge connector (8, banks GTY103, GTY104)
  - HSDP USB3.1 TYPE C (1, bank GTY105)
  - zSFP28 (2, bank GTY105)
  - HDMI (3, bank GTY106)
  - HDMI TX only, RX not used (1, bank GTY106)
  - zQSFP28 (4, bank GTY200)
  - FMCP1 HSCP DP (12, banks GTY201-GTY203)
  - FMCP2 HSCP DP (12, banks GTY204-GTY206)
  - Not used (1, bank GTY105)
- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)
  - Gen3 8-lane (x8)
  - Gen4 8-lane (x8)
- PS PMC MIO connectivity
  - PS MIO[0:12]: boot configuration header
    - DC QSPI support

    - PS MIO[13:25]: USB2.0
    - PS MIO[26:36, 50:51]: SD1 I/F
    - PS MIO[37]: ZU4_TRIGGER
    - PS MIO[38:39]: PCIe_WAKE_B, PCIe_PERST_B
    - PS MIO[40:41]: CAN1
    - PS MIO[42:43]: UART0 to FTDI
    - PS MIO[44:47]: I2C1, I2C0
    - PS MIO[48:49], PS LPD MIO[0:25]: dual GEM0/1 RGMII Ethernet with stacked RJ-45
- Security: PSBATT button battery backup
- SYSMON header
- Operational switches (power on/off, PROG_B, boot mode DIP switch)
- Operational status LEDs (INIT, DONE, PS STATUS, PGOOD)
- Power management
- System Controller (XCZU4EG)

The VMK180 provides a rapid prototyping platform using the XCVM1802-2MSEVSVA2197 device. See the *Versal Architecture and Product Data Sheet: Overview* (DS950) for a feature set overview, description, and ordering information.

Board Specifications

Dimensions (Extended Height PCIe Form-Factor)

Height: 7.477 inches (18.992 cm)

Length: 9.50 inches (24.13 cm) (¾ PCIe length)

Thickness: 66.87 mil ±10% (1.698 mm ±10%)

***Note*:** Reserve two adjacent PCIe slots to accommodate fan-sink height.

***Note*:** A 3D model of this board is not available.

See the VMK180 evaluation board website for the XDC listing and board schematics.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

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Chapter 2

Board Setup and Configuration

Standard ESD Measures

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

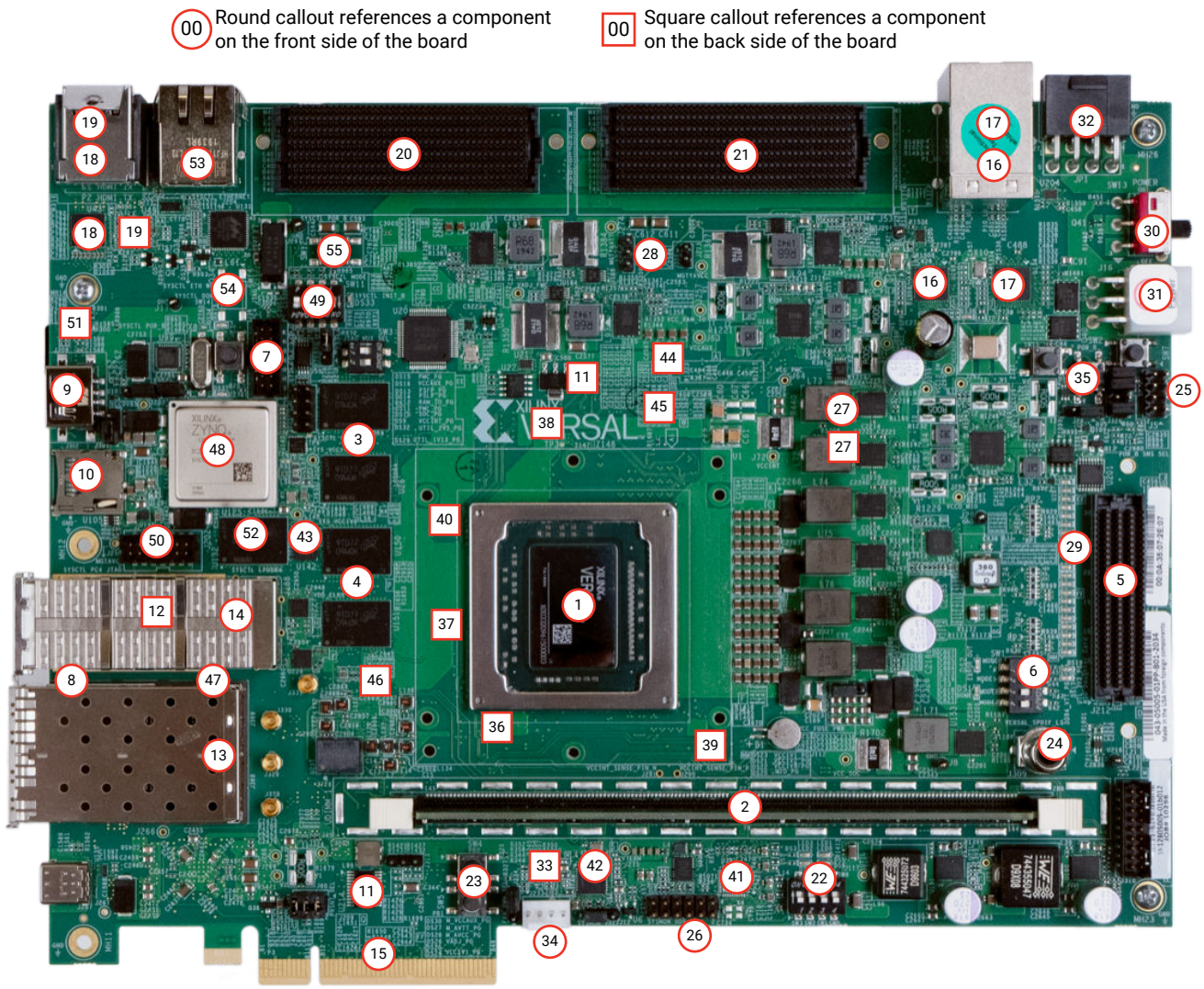
Board Component Location

The following figure shows the VMK180 board component locations. Each numbered component shown in the figure is keyed to the table in Board Component Descriptions.

IMPORTANT! *The following figure is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT! *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific VMK180 version of interest for such details.*

Figure 3: **Evaluation Board Component Locations**



Board Component Descriptions

The following table identifies the components and references the respective schematic (038-05005-01) page numbers.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the VMK180 board power connector J16. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VMK180 board and voids the board warranty.*

Table 2: **Board Component Locations**

Callout	Ref. Des.	Feature	Notes	Schematic Page
1	U1	Versal® ACAP	XCVM1802-2MSEVSVA2197 The heatsink is not shown in Figure 3[1]	
2	J45	DDR4 288-pin DIMM SOCKET/ DDR4 DIMM	FCI 10124677-000100ILF/Micron MTA9ADF1G72AZ-3G2E1	43
3	U25,U26	LPDDR4 16 GBIT comp. memory (B710/B711 IF)	Micron MT53D512M32D2DS-046	27,28
4	U150,U151	LPDDR4 16 GBIT comp. memory (B709/B710 IF)	Micron MT53D512M32D2DS-046	29, 30
5	J212	Fast-boot module daughter card connector	Samtec SEAF-30-05.0-L-08-1-A-K-TR	31
6	SW1	ACAP MODE 4-pole DIP switch, active-High	C&K SDA04H1SBD	12
7	J36	ACAP JTAG 2 mm 2x7 flat-cable connector	Molex 87832-1420	24
8	U20,J207	USB-UART bridge, USB Type-C connector (USB2.0)	FTDI FT4232HL-REEL, Amphenol 12401598E4#2A	25, 99
9	U99,J308	USB ULPI transceiver, USB 2.0 type A connector	SMSC USB3320C-EZK, WURTH 629104190121	24
10	U104,J302	Versal ACAP SD 3.0 level-translator circuit, SD card socket	Nexperia IP4856CX25/CZ, ALPS SCHA4B0419	76
11	U33,U35,U214	I2C bus switches	TI TCA9548APWR	44, 45
12	U233	I2C bus expander	TI TCA6416APWR	55
13	J287	zSFP/zSFP+ (1x2 stacked) connector	Tyco 2198318-6	45
14	J288	zQSFPConnector	TE 1551920-2	47
15	P3	PCIe EndPoint 8-lane edge connector	NA - PCB layout feature	46
16	U198,J307B(UPR)	GEM0 SGMII Ethernet PHY, `0x01`, RJ45 w/mag	TI DP83867ISRGZ, TE-AMP 2301997-7 dual port	77
17	U134,J307A(LWR)	GEM1 SGMII Ethernet PHY, `0x02`, RJ45 w/mag	TI DP83867ISRGZ, TE-AMP 2301997-7 dual port	78
18	U43,P2A(UPR)	HDMI XMT, TMDS to HDMI level shifter retimer, `0x22`, `0xBC`	TI SN65DP159RGZ, TE 1888811-1 dual port	50
19	U55,P2B(LWR)	HDMI RCV TMDS retimer, `0x0B`, `0xB8`	TI TMDS181IRGZT, TE 1888811-1 dual port	51

Table 2: **Board Component Locations** *(cont'd)*

Callout	Ref. Des.	Feature	Notes	Schematic Page
20	J51	FMCP1	Samtec ASP-184329-01	32-36
21	J53	FMCP2	Samtec ASP-184329-01	37-41
22	DS3-DS6,SW6	User LEDs and 4-pole DIP switch, active-High	Lumex SML-LX0603GW (green), C&K SDA04H1SBD	53
23	SW4,SW5	User pushbutton, active-High	E-switch TL3301EP100QG	53
24	U216,J309	SPDIF IF driver and RCA jack	TI SN74AVC1T45, CUI RCJ-021	79
25	U110,J5	CAN BUS transceiver, 2x4 CAN header	Nexperia TJA1057GT/3J, SULLINS PBC04DAAN	80
26	J11	SYSMON 2X6 vertical male pin header	SULLINS PBC06DAAN	12
27	Various	Power management system (top, [bottom])	Infineon regulators	47-60
28	J325	PMBus 3-pin header	SULLINS PBC03SAAN	26
29	DS9-DS17,DS19-DS32	Power good LEDs	Lumex SML-LX0603GW-TR, green	83
30	SW13	Power On/Off slide switch	C&K 1201M2S3AQE2	46
31	J16	Power connector, 2x3, for AC-DC power adapter	MOLEX 39-30-1060 (mini-fit)	46
32	JP1	Power connector, 2x4, for ATX PCIe power	Astron 6652208-T0003T-H-A	46
33	U64	Fan controller	Maxim MAX6643LBBAEE++	54
34	J233	Fan header (keyed 4-pin)	Molex 22-11-2032	54
35	U10,SW2	Power-on reset (POR) with pushbutton	TI TPS389001DSER, E-switch TL3301EP100QG	15
	U110,J326	Alternate POR source driver and 2x4 select header	TI SN74LVC07A, SULLINS PBC04DAAN	15
	SW15	GEM0 Ethernet PHY reset pushbutton, active-Low	E-switch TL3301EP100QG	77
	SW7	GEM1 Ethernet PHY reset pushbutton, active-Low	E-switch TL3301EP100QG	78
36	U2	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x60	Silicon Labs SI570BAB000299DG	4
37	U3	LPDDR4 CLK2, 200 MHz, 3.3V LVDS, 0x60	Silicon Labs SI570BAB000299DG	5
38	U4	LPDDR4 CLK1, 200 MHz, 3.3V LVDS, 0x60	Silicon Labs SI570BAB000299DG	7
39	U5	HSDP CLK, 156.25 MHz, 3.3V LVDS, 0x5D	Silicon Labs SI570BAB000544DG	8
40	U32	ACAP U1 REF CLK, 33.33 MHz, 1.8V CMOS, 0x5D	Silicon Labs SI570JAC000900DG	43
41	U39	PCIe 1:2 buffer, 100 MHz, 3.3V LVDS	IDT 85411AMLF	49
42	U62	HDMI jitter atten., 148.50 MHz, 3.3V LVDS, 0x6C	IDT 8T49N241-994NLGI	52

Table 2: **Board Component Locations** *(cont'd)*

Callout	Ref. Des.	Feature	Notes	Schematic Page
43	U142	SYSCTLR clocks 33.33 MHz & 125 MHz I2C 0x6A	Silicon Labs Si5332FD10259-GM1	101
44	U192	zSFP CLK, 156.25 MHz, 3.3V LVDS, 0x5D	Silicon Labs SI570BAB000544DG	8
45	U205	IEEE-1588 eCPRI input CLK, 100 MHz, 3.3V LVDS, 0x5F	Silicon Labs SI570BAC002038DG	48
46	U219	IEEE-1588 eCPRI CLK, various, 3.3V, 0x58	IDT 8A34001E-000AJG8	104
47	J328-J331	IEEE-1588 eCPRI 8A34001 CLK in and out SMA pairs	Rosenberger 32K10K-400L5	104
48	U125	XCZU4EG System Controller	TI MSP430F5342	85-91
49	SW11	System Controller MODE 4-pole DIP switch, active-High	C&K SDA04H1SBD	89
50	J202	System Controller JTAG 2 mm 2 x 7 flat-cable connector	Molex 87832-1420	89
51	J206	System Controller SD card socket	ALPS SCHA4B0419	96
52	U132	System Controller LPDDR4 16 GBIT comp. memory	Micron MT53D512M32D2DS-046	97
53	U131,J204	System Controller SGMII Ethernet, RJ45 w/magnetics	Marvell 88E1512-A0-NNP2C000, Halo HFJ11-1G01E-L12RL	95
54	SW16	System Controller pushbutton switch, active-High	E-switch TL3301EP100QG	88
55	U129,SW12	System Controller POR with pushbutton	TI TPS389001DSER, E-switch TL3301EP100QG	88

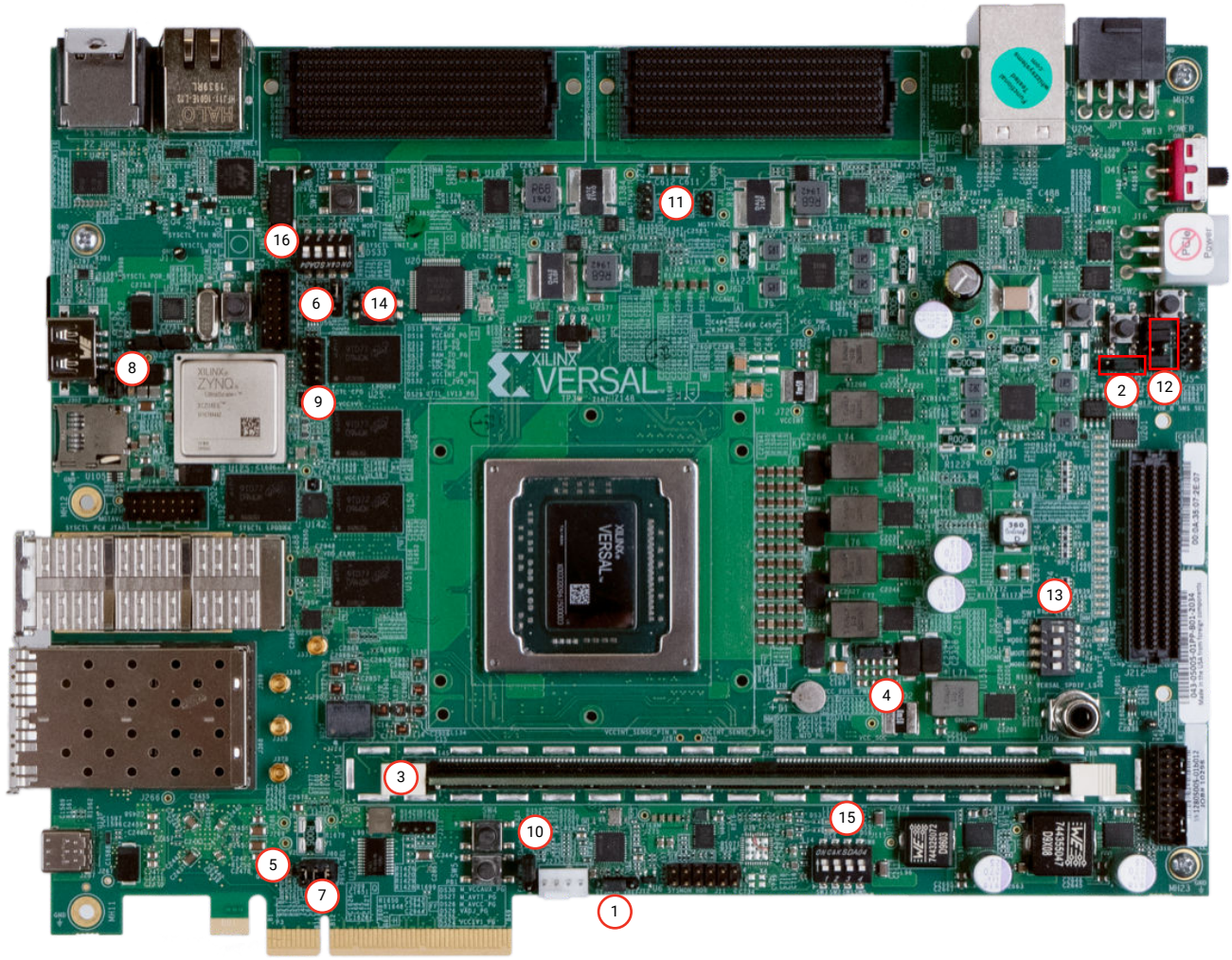
Notes:

1. The VMK180 evaluation board includes a Cofan USA 30-6156-06 heatsink with a thermal resistance of 0.27°C/W.

Default Jumper and Switch Settings

The following figure shows the VMK180 board jumper header and switch locations. Each numbered component shown in the figure is keyed to the applicable table in this section. Both tables reference the respective schematic page numbers.

Figure 4: **Board Jumper Header and Switch Locations**



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Jumpers

The following table lists the default jumper settings.

Table 3: **Default Jumper Settings**

Callout Number	Ref. Des.	Function	Default	Schematic Page
1	J12	SYSMON VREFP	1-2	12
		1-2: 1.024V VREFP connected to ACAP		
		2-3: VREFP connected to GND		

Table 3: **Default Jumper Settings** *(cont'd)*

Callout Number	Ref. Des.	Function	Default	Schematic Page
2	J26	POR_B sense select 1-2: VCCO_503 2-3: VCCAUX_PMC	1-2	15
3	J32	SFP1_TX_DISABLE select ON: enable always OFF: disable/allows ACAP U1 control	ON	45
4	J34	ACAP U1 bank VCC_FUSE select 1-2: VCC1V8 2-3: GND	2-3	17
5	J35	SFP0_TX_DISABLE select ON: enable always OFF: disable/allows ACAP U1 control	ON	17
6	J37	JTAG MUX U14/U15 OE_B 1-2: UTIL_3V3 disable 2-3: GND enable	2-3	24
7	J60	PCIe lane size select 1-2: x1 3-4: x4 5-6: x8	5-6	46
8	J203	SYSCTLR_POR_B enable ON: enable OFF: disable	ON	89
9	J205	System Controller M88E1512 EPHY U131 configuration 1:2: GND (5'b00000) 3:4: SYSCTLR_ETH_LED0 5:6: SYSCTLR_ETH_LED0 7:8: SYS_VCC1V8 (5'b00001)	7-8	95
10	J234	ACAP cooling fan control 1-2: MAX6643 U64 control is enabled 2-3: always on	2-3	54
8	J300	ULPI USB3320 U99 USB conn. J308 shield select 1-2: J308 shield directly to GND 2-3: J308 shield capacitor C2762 to GND	1-2	42
8	J301	IP4856 U104 VERSAL_SD1_REF voltage select 1-2: UTIL_3V3 2-3: GND	1-2	76

Table 3: **Default Jumper Settings** *(cont'd)*

Callout Number	Ref. Des.	Function	Default	Schematic Page
11	J306	Si53340 clock MUX U206 input select	OFF	48
		ON: CLK1 8a34001_Q2		
		OFF: U205 USER_SI570_1(100 MHz default)		
12	J326	POR_B source select (OR'd with POR_B)	1-2 3-4 7-8	15
		None: U10 TPS389001 POR only		
		1-2: U125 SYSCTLR_POR_B		
		3-4: J36 PC4_POR_B		
		5-6: J212(B) DC_PS_POR_B_OUT		
		7-8: U20 FTDI_POR_B		

Switches

The following table lists the default switch settings.

Table 4: **Default Switch Settings**

Callout Number	Ref. Des.	Function	Default	Schematic Page
13	SW1	ACAP U1 mode 4-pole DIP switch	0000	14
		Switch OFF = 1 = High; ON = 0 = Low		
		Mode = SW1[4:1] = Mode[3:0]		
		JTAG = ON,ON,ON,ON = 0000		
		QSPI32 = ON,ON,OFF,ON = 0010		
		SD = OFF,OFF,OFF,ON = 1110		
		Reserved for Xilinx® = OFF,OFF,OFF,OFF = 1111		
14	SW3	JTAG MUX select 2-pole DIP switch	01	24
		Switch OFF = 1 = High; ON = 0 = Low		
		SW3[1:2] = MUX[S0:S1]		
		SYSCTLR U125 BANK 44 = ON,ON = 00		
		FTDI BRIDGE U20 = ON,OFF = 01		
15	SW6	ACAP U1 BANK 306 GPIO 4-Pole DIP switch	0000	53
		SW6[4:1] = GPIO_DIP_SW[0:3]		
		Switch OFF = 0 = Low; ON = 1 = High		
16	SW11	ZU4 SYSCTLR U125 Mode 4-Pole DIP switch	0000	89
		Switch OFF = 1 = High; ON = 0 = Low		
		Mode = SW11[4:1] = Mode[3:0]		
		JTAG = ON,ON,ON,ON = 0000		
		QSPI32 = ON,ON,OFF,ON = 0010		
		SD = OFF,OFF,OFF,ON = 1110		

Versal ACAP Configuration

The Versal XCVM1802 ACAP boot process is described in the “Platform Boot, Control, and Status” section of the *Versal ACAP Technical Reference Manual* (AM011). The VMK180 board supports a subset of the modes documented in the technical reference manual via onboard and daughter card boot options. The mode DIP switch SW1 configuration option settings are listed in the following table.

Table 5: **Mode Switch SW1 Configuration Option Settings**

Boot Mode	Mode Pins [3:0][2]	Mode SW1 [4:1][2]	Comments
JTAG	0000[1, 3]	ON, ON, ON, ON	Supported with or without boot module attached
QSPI32	0010	ON, ON, OFF, ON	Supported only with boot module X-EBM-01 attached Supports x1, x2, x4, and dual-parallel x8
SD1_3.0	1110	OFF, OFF, OFF, ON	Supported with or without boot module attached

Notes:

1. Default switch setting.
2. Mode DIP SW1 poles [4:1] correspond to U1 XCVM1802 MODE[3:0].
3. Mode DIP SW1 individual switches ON=LOW (p/d to GND)=0, OFF=HIGH (p/u to VCCO)=1.

JTAG

The Vivado®, XilinxSDK, or third-party tools can establish a JTAG connection to the Versal ACAP in the two ways described here:

- FTDI FT4232 USB-to-JTAG/USB-UART device (U20) connected to USB 3.1 type-C connector (J207), which requires:
  - Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal ACAP Configuration
  - Set 2-pole DIP SW3[1:2] set to 01 (ON, OFF) for JTAG MUX channel 2 FT4232 U20 bridge
  - On the 3-pin JTAG MUX, enable header J37 (2-pin jumper block installed on pins 2-3) to enable the JTAG MUX
  - Power-cycle the VMK180 board or press the power-on reset (POR) pushbutton (SW2) (SW2 is callout 46 in the "Evaluation Board Component Locations" figure in Board Component Location)
- JTAG pod flat cable connector J36 (2 mm 2x7 shrouded/keyed), which requires:
  - Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal ACAP Configuration
  - On the 3-pin JTAG MUX, enable header J37 (2-pin jumper block installed on pins 1-2) to inhibit the JTAG MUX (hi-Z mode)

- 2-pole DIP SW3[1:2] setting is XX as the MUX is inhibited/turned off
- In this mode, the FT4232 device (U20) UART functionality continues to be available
- Power-cycle the VMK180 board or press the power-on reset pushbutton (SW2) (SW2 is callout 46 in the "Evaluation Board Component Locations" figure in Board Component Location)

QSPI32

This boot mode is supported only with boot module X-EBM-01 attached to the MIO connector (J212). J212 is a 240-pin (8 x 30) MIO connector wired to XCVM1802 U1 bank 500 PMC_MIO[0:12] pins. The supported QSPI configurations are x1, x2, x4, and dual-parallel x8. To boot from a QSPI X-EBM-01 boot module:

1. Store a valid XCVM1802 ACAP boot image file on the X-EBM-01 resident QSPI.
2. Set boot mode SW1 for QSPI32 as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal ACAP Configuration.
3. Power-cycle the VMK180 or press the POR pushbutton SW2. SW2 is callout 35 in the "Evaluation Board Component Locations" figure in Board Component Location.

SD1_3.0

To boot from a SD card installed in microSD card socket J302:

1. Store a valid XCVM1802 ACAP boot image file on a microSD card. Plug the SD card into the VMK180 board SD socket J302 connected to the XCVM1802 U1 bank 501 MIO SD interface.
2. Set boot MODE SW1 for SD1_3.0 as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal ACAP Configuration.
3. Power-cycle the VMK180 or press the POR pushbutton SW2. SW2 is callout 35 in the "Evaluation Board Component Locations" figure in Board Component Location.

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Chapter 3

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. The "Board Component Locations" table in Board Component Descriptions identifies the components and references the respective schematic page numbers. Component locations are shown in the "Evaluation Board Component Locations" figure in Board Component Location.

Component Descriptions

Versal ACAP

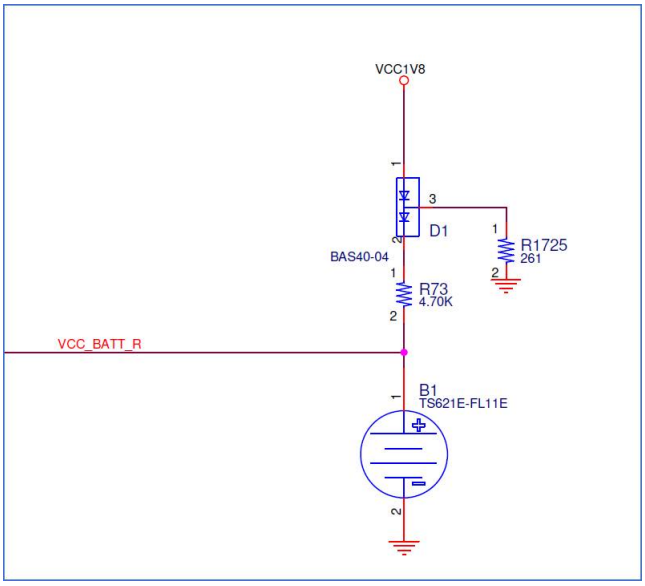
[Figure 3, callout 1]

The VMK180 board is populated with the Versal® XCVM1802-2MSEVSVA2197 ACAP, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Versal ACAP features the Arm® flagship Cortex®-A72 64-bit dual-core processor and Cortex®-R5F dual-core real-time processor. For additional information on the Versal XCVM1802-2MSEVSVA2197 ACAP, see the *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956). See the *Versal ACAP Technical Reference Manual* (AM011) for more information about Versal ACAP configuration options.

Encryption Key Battery Backup Circuit

The XCVM1802 ACAP U1 implements bitstream encryption key technology. The VMK180 board provides the encryption key backup battery circuit shown in the following figure.

Figure 5: **Encryption Key Backup Circuit**



The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCVM1802 ACAP U1 VCC_BATT bank pin AG33. The battery supply current IBATT specification is 150 nA maximum when board power is off. Battery B1 is charged from the VCC1V8 1.8V rail through a 2 series diode with the first forward drop to yield between 0.24V to 0.46V over temperature per fixed 5 mA load, R1725, and limiting 1.56V max at the ACAP pin, PSVBATT. The second diode and 4.7 kΩ current limit resistor allows the battery to trickle charge and prevent battery B1 from back powering R1725.

I/O Voltage Rails

The XCVM1802 ACAP PL I/O bank voltages on the VMK180 board are listed in the following table.

***Note*:** The VMK180 board is shipped with VADJ_FMC set to 1.5V by the ZU4 system controller.

Table 6: **I/O Voltage Rails**

ACAP (U1) Bank	Power Supply Rail Net Name	Voltage	Description
HDIO Bank 306	VCC1V8	1.8V	GPIO: PB[0:1], DIP_SW[0:3], LED[0:3]; DC_PL_GPIO[0:3]; SYSCTLR_GPIO[0:5]; UART1_TXD/RXD
HDIO Bank 406	VCC3V3	3.3V	HDMI status/ctrl(15)IF; HDIO_UART3_TX/RX; HDIO_UART4_TX/RX
XPIO Bank 700	VCC1V2_DDR4	1.2V	DDR4_DIMM1_DQ[32:63], CB[0:7], ADDR/CTRL; DDR4_DIMM1_CLK; Si570 U2 200 MHz
XPIO Bank 701	VCC1V2_DDR4	1.2V	DDR4_DIMM1_DQ[24:31], ADDR/CTRL
XPIO Bank 702	VCC1V2_DDR4	1.2V	DDR4_DIMM1_DQ[0:23], CB[0:7]

Table 6: **I/O Voltage Rails** *(cont'd)*

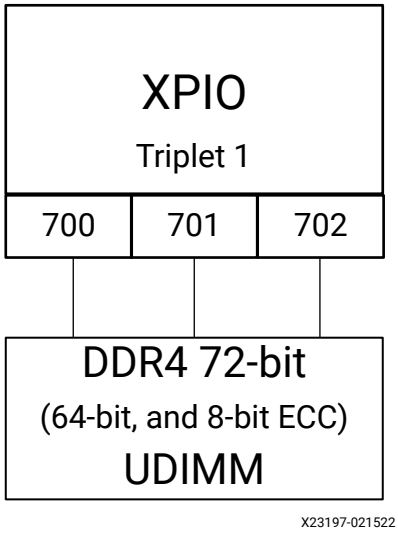
ACAP (U1) Bank	Power Supply Rail Net Name	Voltage	Description
XPIO Bank 703	VCC1V1_LP4	1.1V	LPDDR4_3_DQ[0:7, 16:23], ADDR/CTRL
XPIO Bank 704	VCC1V1_LP4	1.1V	LPDDR4_2_DQ[0:7, 16:23]; LPDDR4_3_DQ[8:15, 24:31]
XPIO Bank 705	VCC1V1_LP4	1.1V	LPDDR4_2_DQ[8:15, 24:31], ADDR/CTRL; Si570 U3 200 MHz
XPIO Bank 706	VADJ_FMC	1.5V	8A34001_GPIO_[0:15]; FMCP1_LA[00:16]
XPIO Bank 707	VADJ_FMC	1.5V	FMCP1_LA[17:33]; FMCP2_LA[26:33]
XPIO Bank 708	VADJ_FMC	1.5V	FMCP2_LA[00:25]
XPIO Bank 709	VCC1V1_LP4	1.1V	LPDDR4_1_DQ[0:7, 16:23], ADDR/CTRL
XPIO Bank 710	VCC1V1_LP4	1.1V	LPDDR4_0_DQ[0:7, 16:23]; LPDDR4_1_DQ[8:15, 24:31]
XPIO Bank 711	VCC1V1_LP4	1.1V	LPDDR4_0_DQ[8:15, 24:31], ADDR/CTRL; Si570 U4 200 MHz
PMC MIO 500	VCCO_500	3.3V	SYSMON IF; PMC_MIO[0:25]_500; ISL60002 U6 1.042V VREF; J1 2x6 SYSMON PIN HDR
PMC MIO 501	VCCO_501	3.3V	PMC_MIO[26:51]
LP MIO 502	VCCO_502	3.3V	LPD_MIO[0:25]

DDR4 UDIMM Socket

[Figure 3, callout 1]

The VMK180 board XPIO triplet 1 (banks 700/701/702) memory interface supports 288-pin 72-bit (64-bit, and 8-bit ECC) DDR4 DIMM socket J45.

Figure 6: **DDR4 DIMM Memory**



The VMK180 board is shipped with a DDR4 UDIMM installed:

- Manufacturer: Micron
- Part number: MTA9ADF1G72AZ-3G2E1
- Description
  - 8 GB 288-pin DDR UDIMM
  - Single rank
  - 8 Gb (1 Gig x 8), 16 banks
  - Supports up to 3200 Mb/s

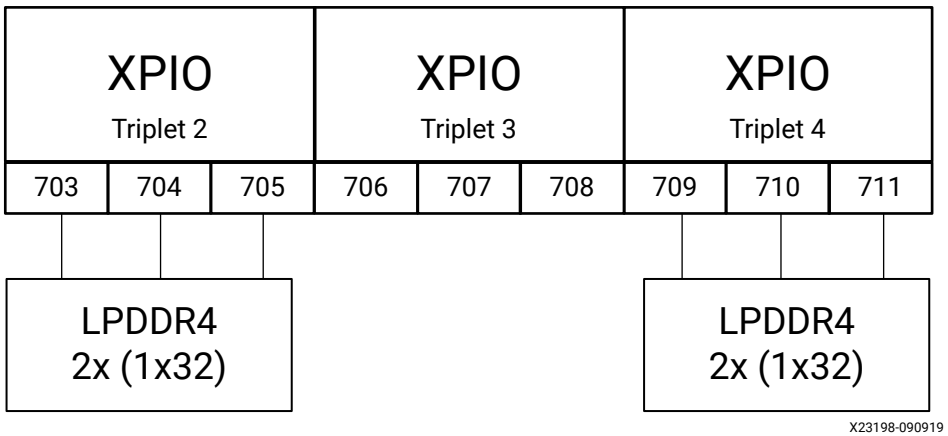
The VMK180 XCVM1802 ACAP DDR interface performance is documented in the *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956). The VMK180 DDR4 DIMM interface adheres to the constraints guidelines documented in the PCB guidelines for DDR4 section of the *Versal ACAP PCB Design User Guide* (UG863). The DDR4 DIMM interface is a 40Ω impedance implementation. Other memory interface details are also available in the *Versal ACAP Memory Resources Architecture Manual* (AM007). For more details, see the Micron MTA9ADF1G72AZ-3GE1 data sheet at the Micron website. The ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

LPDDR4 Component Memory

[Figure 3, callout 3 and 4]

The VMK180 board hosts two LPDDR4 memory systems, each with a component configuration of 2x (1x32-bit component).

Figure 7: **LPDDR4 Component Memory**



XCVM1802 U1 XPIO triplet 2 (banks 703/704/704) and triplet 4 (banks 709/710/711) each support two independent 32-bit 2 GB component interfaces (4 GB per triplet).

- Manufacturer: Micron
- Part number: MT53D512M32D2DS-046 WT:D (dual die LPDDR4 SRAM)
- Component description
  - 16 Gb (512 Mb x 32)
  - 1.1V 200-ball WFBGA
  - DDR4-2133

The VMK180 XCVM1802 ACAP PL DDR interface performance is documented in the *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956). The VMK180 board LPDDR4 component memory interfaces adhere to the constraints guidelines documented in the PCB guidelines for DDR4 section of *Versal ACAP PCB Design User Guide* (UG863). The VMK180 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *Versal ACAP Memory Resources Architecture Manual* (AM007). For more memory component details, see the Micron MT53D512M32D2DS data sheet at the Micron website. The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

System Reset POR_B

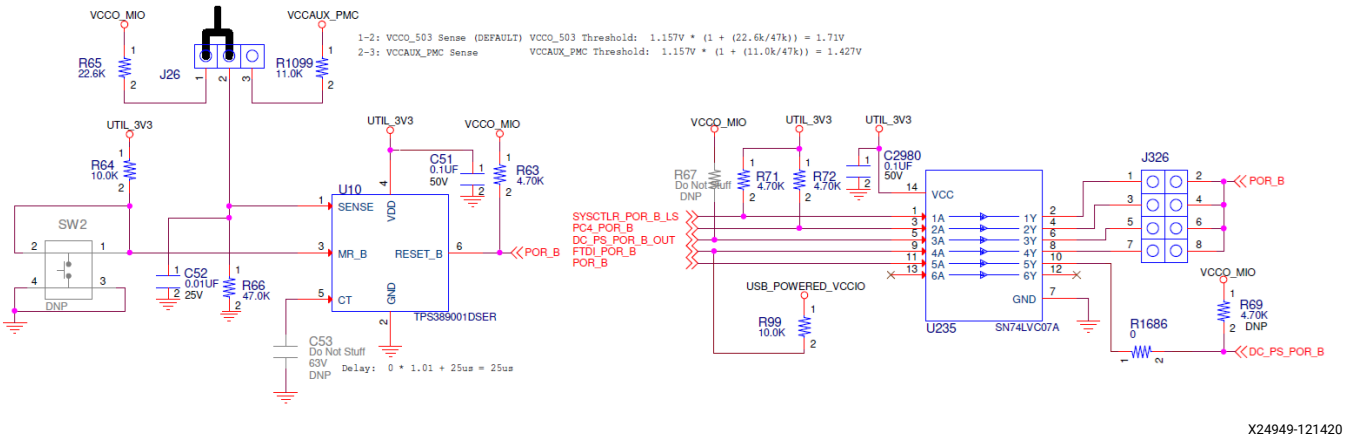
[Figure 3, callout 35]

POR_B is the Versal ACAP processor reset, which can be controlled by:

- SYSCTLR (U125)
- PC4 header (J36)
- MIO EBM (external boot module on J212)
- FTDI USB JTAG chip (U20)

In the following figure, U235 allows directional open drain level shifting for all of these masters, and J326 allows them to be bused together if desired. The fifth channel buffers POR_B out to the EBM (external boot module) as DC_PS_POR_B. The TPS389001 U10 supervisor chip holds POR_B off until power is valid. The VMK180 board POR circuit is shown in the figure.

Figure 8: **POR_B Reset Circuit**



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PMC and LPD MIO

The following table provides MIO peripheral mapping implemented on the VMK180 board. See the *Versal ACAP Technical Reference Manual* (AM011) for more information on MIO peripheral mapping. The XCVM1802 ACAP Bank 500, 501, and 502 mappings are listed in the table.

Table 7: **MIO Peripheral Mapping**

PMC MIO[0:25] Bank 500		PMC MIO[26:51] Bank 501		LPD MIO[0:25] Bank 502	
0	MIO CONN. J212	26	SD1	0	GEM0
1	MIO CONN. J212	27	SD1	1	GEM0
2	MIO CONN. J212	28	SD1	2	GEM0
3	MIO CONN. J212	29	SD1	3	GEM0
4	MIO CONN. J212	30	SD1	4	GEM0
5	MIO CONN. J212	31	SD1	5	GEM0
6	MIO CONN. J212	32	SD1	6	GEM0
7	MIO CONN. J212	33	SD1	7	GEM0
8	MIO CONN. J212	34	SD1	8	GEM0
9	MIO CONN. J212	35	SD1	9	GEM0
10	MIO CONN. J212	36	SD1	10	GEM0
11	MIO CONN. J212	37	ZU4_TRIGGER	11	GEM0
12	MIO CONN. J212	38	PCIE_PERST_B	12	GEM1
13	U103.6 USB3320 U99 reset gate	39	PCIE_PWRBRK_B	13	GEM1
14	USB3320 U99	40	CAN1_TXD	14	GEM1
15	USB3320 U99	41	CAN1_RXD	15	GEM1
16	USB3320 U99	42	UART0	16	GEM1
17	USB3320 U99	43	UART0	17	GEM1
18	USB3320 U99	44	I2C1	18	GEM1

Table 7: **MIO Peripheral Mapping** *(cont'd)*

PMC MIO[0:25] Bank 500		PMC MIO[26:51] Bank 501		LPD MIO[0:25] Bank 502	
19	USB3320 U99	45	I2C1	19	GEM1
20	USB3320 U99	46	I2C0	20	GEM1
21	USB3320 U99	47	I2C0	21	GEM1
22	USB3320 U99	48	GEM0	22	GEM1
23	USB3320 U99	49	GEM1	23	GEM1
24	USB3320 U99	50	PCIE_WAKE_B	24	GEM0, GEM1
25	USB3320 U99	51	SD1	25	GEM0, GEM1

PMC MIO[0–12] Bank 500: MIO Daughter Card (DC) Connector J212

[Figure 3, callout 5]

The VMK180 U1 XCVM1802 bank 500 PMC_MIO[0:12] pins are connected to the 240-pin (8 x 30) MIO connector J212. This interface enables high-speed XCVM1802 configuration using the X-EBM-01 QSPI external daughter card installed on J212.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints. The XCVM1802 MIO connector J212 pinout is listed in the following figure.

Figure 9: **MIO Connector J212 Pinout**

		VMK180 Config Daughter Cards					
H	G	F	E	D	C	B	A
	Reserved	UTIL_5V0	PMC_MIO0	VCCO_PMC0	PMC_MIO2	GND	
	GND	UTIL_5V0	PMC_MIO1	VCCO_PMC0	PMC_MIO3	GND	
GND		GND	GND	GND	GND		GND
GND		GND	PMC_MIO8	GND	PMC_MIO10		GND
	GND	PMC_MIO4	PMC_MIO9	PMC_MIO6	PMC_MIO11	GND	
		PMC_MIO5	GND	PMC_MIO7	GND	GND	
GND		GND		GND			GND
	GND	PMC_MIO12					GND
			GND		GND	GND	
GND		GND		GND		GND	
	GND						GND
			GND		GND		GND
GND		GND		GND		GND	
	GND					GND	
			GND		GND		GND
GND		GND		GND			GND
	GND					GND	
			GND		GND	GND	
GND		GND		GND			GND
	GND						GND
			GND		GND	GND	
GND		GND	SYS_CTRL0	GND		GND	
	GND	MODE0	SYS_CTRL1	DC_I2C_SCL			GND
		MODE1	GND	DC_I2C_SDA	GND		GND
		MODE2	SYS_CTRL2	DC_PRSNT		GND	
		MODE3	SYS_CTRL3	PS_POR_B		GND	
GND			GND		GND		GND
	GND		GND		GND		GND
			UTIL_3V3	GND			Reserved
Reserved			UTIL_3V3				Reserved

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PMC MIO[13:25] Bank 500: USB 2.0 ULPI PHY

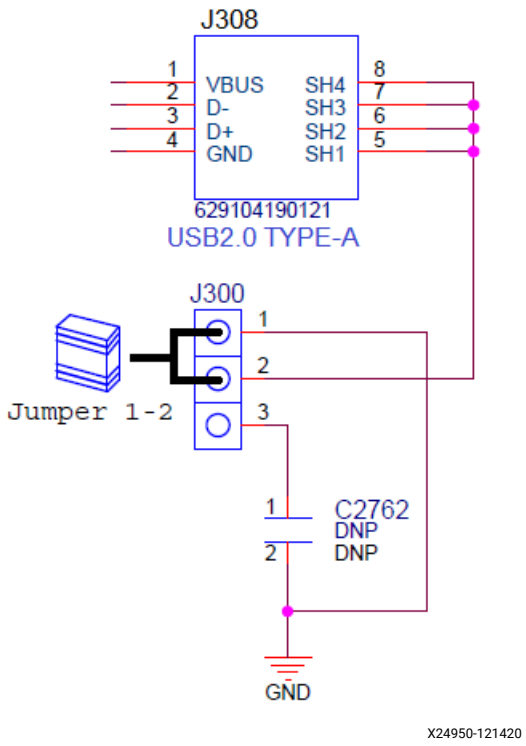
The VMK180 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI transceiver (U99) to support a USB 2.0 type-A connector (J308). A USB cable is supplied in the VMK180 evaluation kit (standard-A connector to host computer, USB 2.0 A connector to VMK180 board connector J308). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device, which drives the physical USB bus. Using the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal (X8). See the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details. The interface to the USB3320 PHY is implemented through the IP in the XCVM1802 ACAP PS.

The USB3320 ULPI transceiver circuit has a Micrel MIC2544 high-side programmable current limit switch (U100). This switch has an open-drain output fault flag on pin 2, which turns on red LED DS37 if over current or thermal shutdown conditions are detected. DS37 is located just above the U125 system controller component (callout 48 in the figure in Board Component Location).

***Note*:** As shown in the following figure, the shield for the USB 2.0 type-A connector (J308) can be tied to GND by a jumper on header J300 pins 1-2 (default). The USB shield can optionally be connected through a series capacitor to GND by installing a capacitor (body size 0402) at location C2762 and jumping pins 2-3 on header J300.

Figure 10: **USB3320 USB2.0 Connector J308 Shield Connection Options**



The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

PMC MIO[26:36, 51] Bank 501: Secure Digital (SD) Card IF (J302)

[Figure 3, callout 10]

A secure digital (SD) card connector is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD2.0 and SD3.0 access.

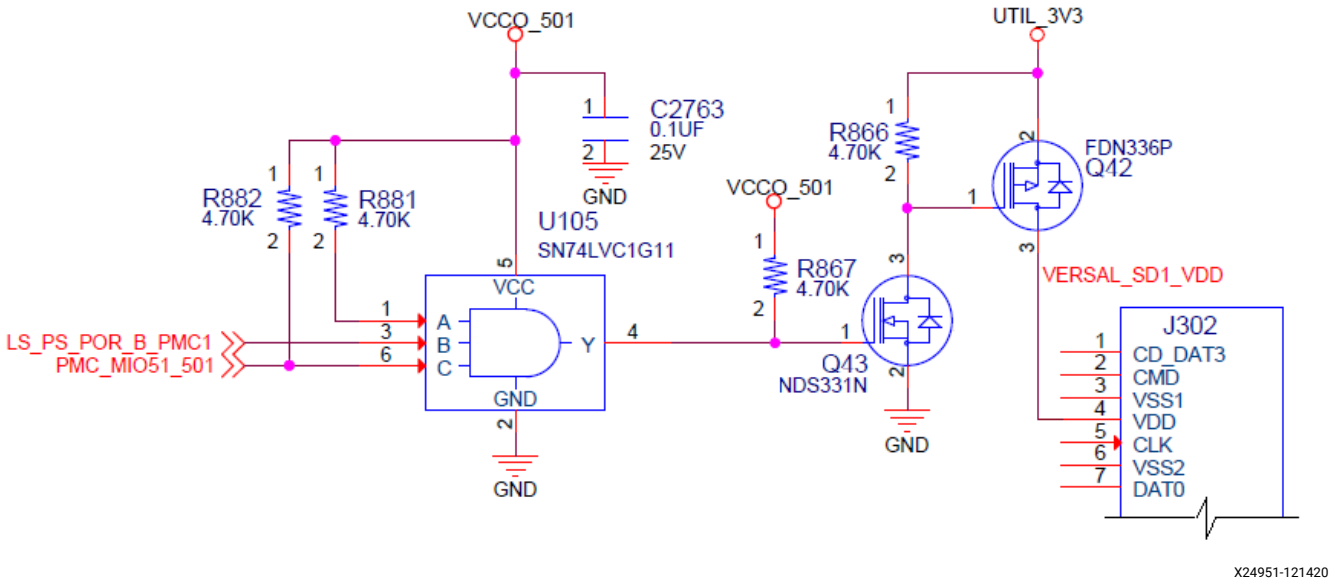
The SDIO interface signals PMC_MIO[26:36, 51] are connected to XCVM1802 ACAP bank 501, which has its VCCO set to 3.3V. Six SD interface nets PMC_MIO[26, 29, 30:33] are passed through a Nexperia IP4856CX25 SD 3.0-compliant voltage level-translator U104 (mounted on an Aries adapter), present between the XCVM1802 ACAP and the SD card connector (J302). The Nexperia IP4856CX25 U104 device provides SD3.0 capability with SDR104 performance. The Aries adapter schematic pinout to IP4856CX25 device pinout cross-reference table is shown in the following table and also on the VMK180 schematic page for this circuit.

The Nexperia SD3.0 level shifter is mounted on an Aries adapter board (located on the bottom of the board under SD socket J302) that has the pin mapping shown in the table.

Table 8: **IP4856CX25 U104 Adapter Pinout**

Aries Adapter Pin Number	IP4856CX25 Pin Number	IP4856CX25 Pin Name
1	C1	CLK_IN
2	C3	GND
3	D3	CD
4	D2	CMD_H
5	E2	CLK_FB
6	E4	WP
7	B4	VLDO
8	C4	VSD_REF
9	A3	DIR_0
10	A4	VSUPPLY
11	B3	VCCA
12	A2	DIR_CMD
13	D1	DATA0_H
14	B2	SEL
15	B1	DATA3_H
16	E1	DATA1_H
17	E3	DIR_1_3
18	A1	DATA2_H
19	E5	DATA1_SD
20	D5	DATA0_SD
21	C5	CLK_SD
22	D4	CMD_SD
23	B5	DATA3_SD
24	A5	DATA2_SD
25	C2	ENABLE

Figure 11: **SD Socket J302 Power Control**



Information for the SD I/O card specification can be found at the SanDisk Corporation or SD Association websites. The VMK180 SD card interface supports the SD1 (2.0) and SD2 (3.0) configuration boot modes documented in the *Versal ACAP Technical Reference Manual* (AM011).

For Nexperia IP4856CX25 component details, see the IP4856CX25 data sheet at the Nexperia website.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

PS MIO[37] ZU4 System Controller GPIO

The ACAP PS bank 501 MIO37 is connected to the ZU4 system controller U125 bank 500 MIO11 pin AE17.

PMC MIO[38:39] PCIe Status

The ACAP PS bank 501 MIO38 (PCIE_PERST_B) and MIO50 (PCIE_WAKE_B) are connected to the PCIe 8-lane edge connector P3 PERST# (pin A11) and WAKE# (pin B11), respectively.

PMC MIO[40:41] CAN1

[Figure 3, callout 25]

The ACAP PS bank 501 MIO40 (TX OUT) and MIO41 (RX IN) support the PS-side CAN bus TX and RX interface wired through the TI SN74AVC2T244 level-translators U107 and U109, respectively, to the NXP TJA1057GT/3J CAN-bus transceiver U110. This transceiver is connected to the 2x4 0.1-inch pitch 8-pin male header J5.

See the NXP TJA1057GT/3J data sheet at the Nexperia website for CAN-bus transceiver details.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

PMC MIO[42:43] UART0

[Figure 3, callout 8]

This is the primary Versal ACAP PS-side UART interface. The VMK180 USB Type-C connector J207 only supports USB2.0.

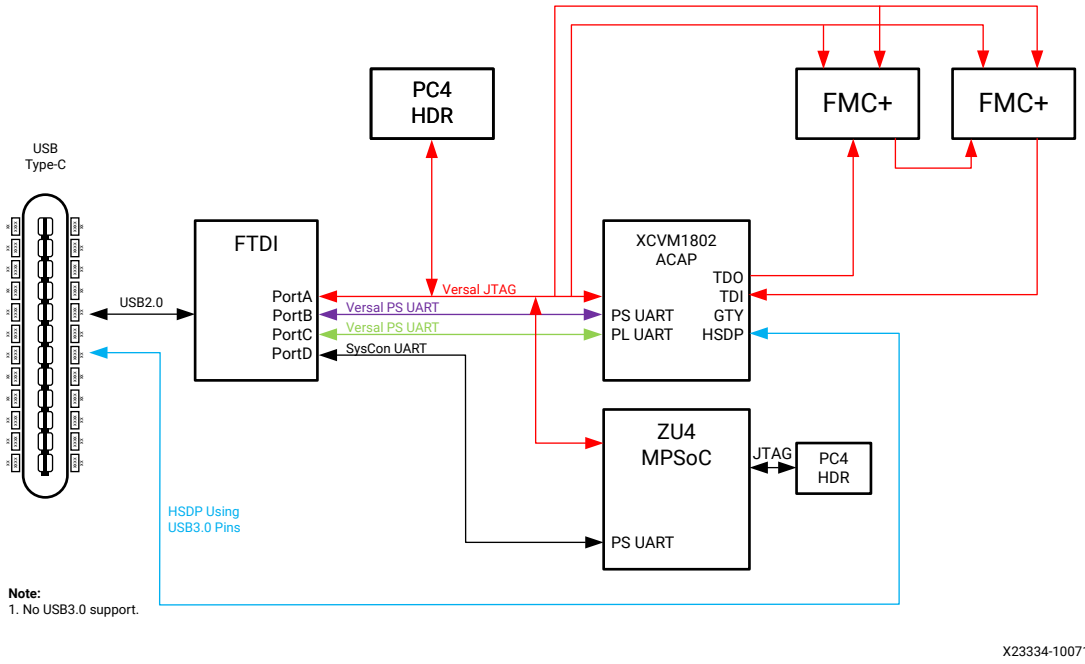
MIO42 (RX_IN) and MIO43 (TX_OUT) are connected to FTDI FT4232HL U20 USB-to-Quad-UART bridge port BD through TI SN74AVC4T245 level-shifters U18 and U21. The FT4232HL U20 port assignments are listed in the following table.

Table 9: **FT4232HL Port Assignments**

FT4232HL U34	Versal ACAP U1
Port AD JTAG	VMK180 JTAG chain
Port BD UART0	PS_UART0 (MIO 18-19)
Port CD UART1	PL_UART1 bank 306
Port DD UART2	U20 system controller UART

The FT4232HL UART interface connections are shown in the following figure.

Figure 12: **FT4232HL UART Connections**



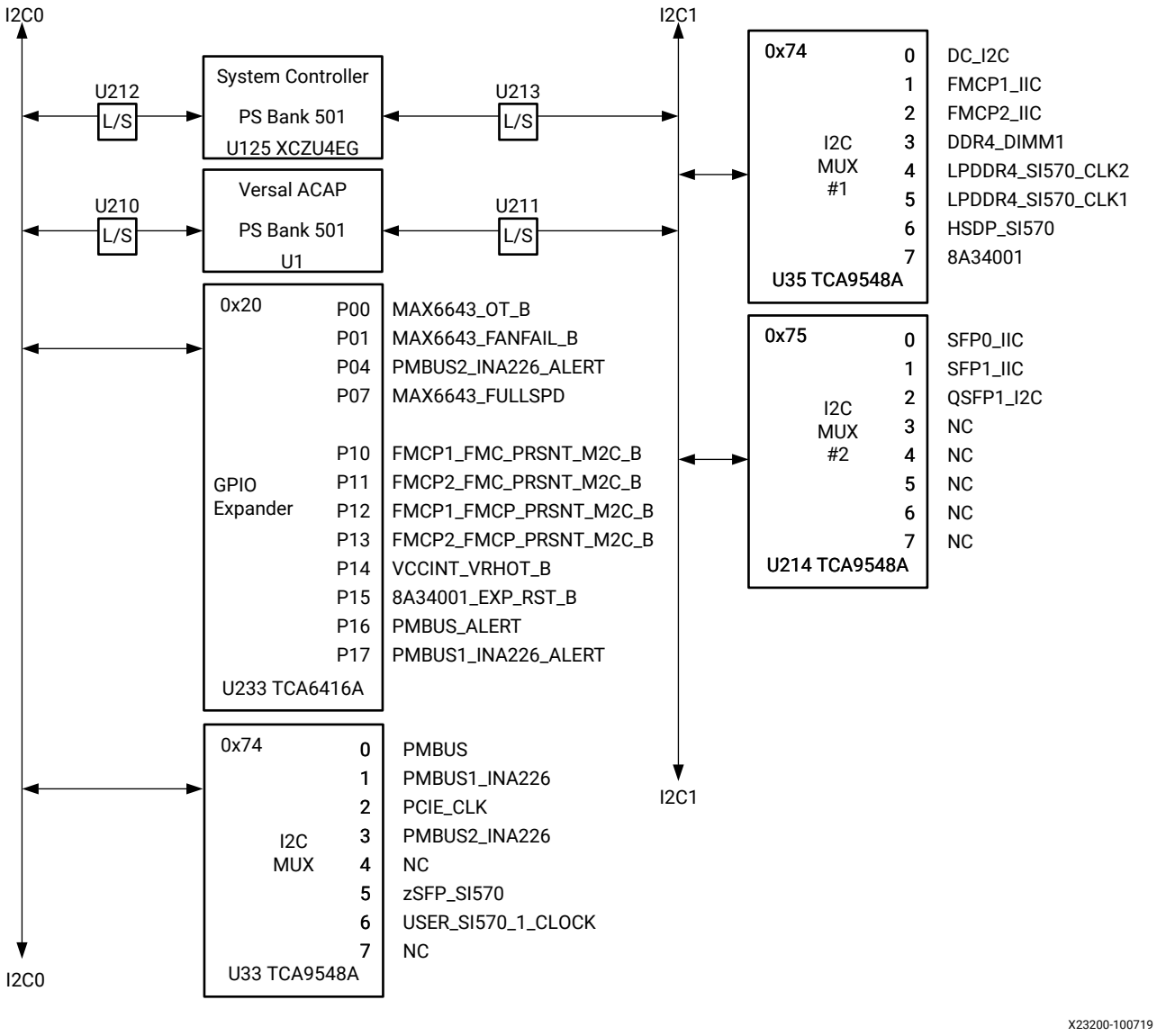
For more information on the FT4232HL, see the Future Technology Devices International Ltd website.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

PMC MIO[46:47] I2C0, PMC MIO[44:45] I2C1 I2C Bus Overview

The following figure shows an overview of the I2C0 and I2C1 bus connections.

Figure 13: **I2C0 and I2C1 Bus Connectivity Overview**



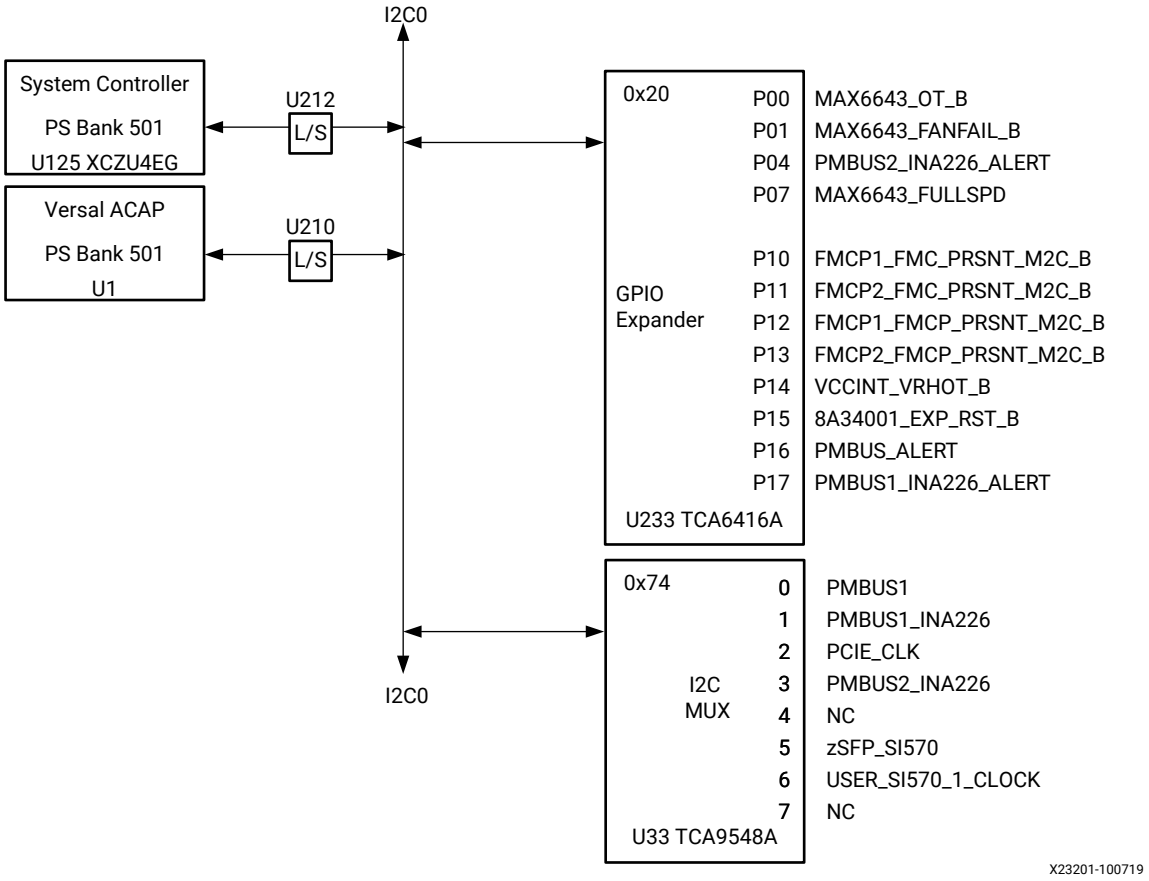
PMC MIO[46:47] I2C0 Bus

[Figure 3, callout 11]

Bus I2C0 connects the XCVM1802 U1 PS bank 501 and the XCZU4EG system controller U125 PS bank 501 to a GPIO 16-bit port expander (TCA6416A U233) and I2C switch (TCA9548A U33). The port expander enables accepting various fan controller, FMCP connector, and power system status inputs. Bus I2C0 also provides access to power system PMBus power controllers and INA226 power monitors, as well as three SI570 components via the U33 TCA9548A switch. TCA6416A U233 is pin-strapped to respond to I2C address `0x20`. The TCA9548A U33 switch is set to `0x74`.

The following figure shows the I2C0 bus connectivity.

Figure 14: **I2C0 Bus Topology**



The devices on each port of the I2C0 U233 TCA6416A port expander and on each bus of the I2C0 U33 PCA9548A switch are listed in the following two tables. The I2C0 target device I2C addresses are listed in the third table below.

Table 10: **I2C0 Port Expander TCA6416A U233 Address 0x20 Connections**

TCA6416A U233		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin No.	Pin Name	Reference Designator	Device
SDA	23	I2C0_SDA	See the "I2C0 Bus Topology" figure. TCA6416AU233 Addr. 0x20			
SCL	22	I2C0_SCL				
P00	4	MAX6643_OT_B (1)	9	OT_B	U64	MAX6643
P01	5	MAX6643_FANFAIL_B (1)	4	FANFAIL_B	U64	MAX6643
P04	8	PMBUS2_INA226_ALERT (1)	3	ALERT	14x INA226	INA226
P07	11	MAX6643_FULLSPD (1)	6	FULLSPD	U64	MAX6643
P10	13	FMCP1_FMC_PRSNT_M2C_B	H2	PRSNT_M2C_L	J51(H)	ASP_184329_01
P11	12	FMCP2_FMC_PRSNT_M2C_B	H2	PRSNT_M2C_L	J53(H)	ASP_184329_01

Table 10: **I2C0 Port Expander TCA6416A U233 Address 0x20 Connections** *(cont'd)*

TCA6416A U233		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin No.	Pin Name	Reference Designator	Device
P12	15	FMCP1_FMCP_PRSNT_M2C_B	Z1	HSPC_PRSNT_M2C_L	J51(N)	ASP_184329_01
P13	16	FMCP2_FMCP_PRSNT_M2C_B	Z1	HSPC_PRSNT_M2C_L	J53(N)	ASP_184329_01
P14	17	VCCINT_VRHOT_B	14	VRHOT_ICRIT#	U152	IR35215
P15	18	8A34001_EXP_RST_B	1	A	U221	SN74LVC1G08
P16	19	IRPS5401_ALERT_B	-	Not connected	In schematic	Delete
P17	20	PMBUS1_INA226_ALERT (1)	3	ALERT	5x INA226	INA226

Table 11: **I2C0 Multiplexer TCA9548A U33 Address 0x74 Connections**

TCA9548A U33		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin No.	Pin Name	Reference Designator	Device
SDA	19	I2C0_SDA	See the "I2C0 Bus Topology" figure; PCA9548A U33 Addr. `0x74`			
SCL	18	I2C0_SCL				
SD0/SC0	4/5	PMBUS_SDA/SCL	9,10	NA	J98	PMBUS HDR
			Miscellaneous power components; see Board Power System for details			
SD1/SC1	6/7	PMBUS1_INA226_SDA/SCL	4,5	SDA, SCL	5x INA226	INA226
SD2/SC2	8/9	PMBUS2_SDA/SCL	9,10	NA	J104	PMBUS HDR
			Miscellaneous power components see Board Power System for details			
SD3/SC3	10/11	PMBUS2_INA226_SDA/SCL	4,5	SDA, SCL	14x INA226	INA226
SD4/SC4	13/14	LP_I2C_SM_SDA/SCL	NA	Not connected	NA	NA
SD5/SC5	15/16	zSFP_SI570_SDA/SCL	7,8	SDA, SCL	U192	SI570
SD6/SC6	17/18	USER_SI570_1_CLOCK_SDA/SCL	7,8	SDA, SCL	U205	SI570
SD7/SC7	19/20	USER_SI570_2_CLOCK_SDA/SCL	NA	Not connected	NA	NA

Table 12: **I2C0 Port Expander TCA6416A U233 Address 0x20 Connections**

I2C Devices	I2C Switch Position	I2C Address		Device
I2C0 Bus				
TCA6416A 16-bit port expander	N/A	`0b1110101`	`0x20`	U233 TCA6416A
Function	**Port**	**Direction**		
MAX6643_OT_B	P00	IN	N/A	U64 MAX6643
MAX6643_FANFAIL_B	P01	IN	N/A	U64 MAX6643
N/A	P02-P03 NC	N/A	N/A	N/A
PMBUS2_INA226_ALERT	P04	IN	N/A	U166, U168, U172, U173, U174, U176, U177, U178, U180, U182, U184 ,U186, U188, U234 INA226, U125 ZU4EG
N/A	P05-P06 NC	N/A	N/A	N/A
MAX6643_FULLSPD	P07	OUT	N/A	U64 MAX6643
FMCP1_FMC_PRSNT_M2C_B	P10	IN	N/A	J51 FMCP HSPC

Table 12: **I2C0 Port Expander TCA6416A U233 Address 0x20 Connections** *(cont'd)*

I2C Devices	I2C Switch Position	I2C Address		Device
I2C0 Bus				
FMCP2_FMC_PRSNT_M2C_B	P11	IN	N/A	J53 FMCP HSPC
FMCP1_FMCP_PRSNT_M2C_B	P12	IN	N/A	J51 FMCP HSPC
FMCP2_FMCP_PRSNT_M2C_B	P13	IN	N/A	J53 FMCP HSPC
VCCINT_VRHOT_B	P14	IN	N/A	U152 IR35215
8A34001_EXP_RST_B	P15	IN	N/A	U221 SN74LVC1G08
PMBUS_ALERT	P16	IN	N/A	U152, U160, U167, U175, U179, U181, U183, U185, U187, U189, U194, U195 Various Vreg, U125 ZU4EG
PMBUS1_INA226_ALERT	P17	IN	N/A	U65,U161-U165 INA226, U125 ZU4EG
TCA9548A 8-Chan. bus switch	N/A	0b1110101	0x75	U33 TCA9548A
Function	Port	Binary Format	Hex Format	
PMBUS_SDA/SCL	0	0b00010011-0b00010100, 0b00010110-0b00010111, 0b00011001-0b00100000	0x13, 0x14, 0x16, 0x17, 0x19-0x20	See tables in Board Power System
PMBUS1_INA226_SDA/SCL	1	0b01000000-0b01000101	0x40-0x45	U65,U161-U165 INA226; see tables in Board Power System
PMBUS2_INA226_SDA/SCL	3	0b01000000-0b01000101	0x40-0x4D	U166, U168, U172, U173, U174, U176, U177, U178, U180, U182, U184, U186, U188, U234 INA226; see tables in Board Power System
No connect	4	NA	NA	NA
zSFP_SI570_SDA/SCL	5	0b1011101	0x5D	U192 SI570
USER_SI570_1_CLOCK_SDA/SCL	6	0b1011111	0x5F	U205 SI570
No Connect	7	NA	NA	NA

PMC MIO[44:45] I2C1 Bus

[Figure 3, callout 11]

Bus I2C1 connects the XCVM1802 U1 PS bank 501, and the XCZU4EG system controller U125 PS bank 501 to two I2C switches (TCA9548A U35 and U214). These I2C1 connections enable I2C communications with other I2C capable target devices. TCA9548A U35 is pin-strapped to respond to I2C address 0x74. TCA9548A U214 is pin-strapped to respond to I2C address 0x75. The following figure shows the I2C1 bus connectivity detailed in the first two tables below. The I2C0 target device I2C addresses are listed in the third table.

For more information on the TCA9548A and TCA6416A, see the Texas Instruments website.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Figure 15: **I2C1 Bus Topology**

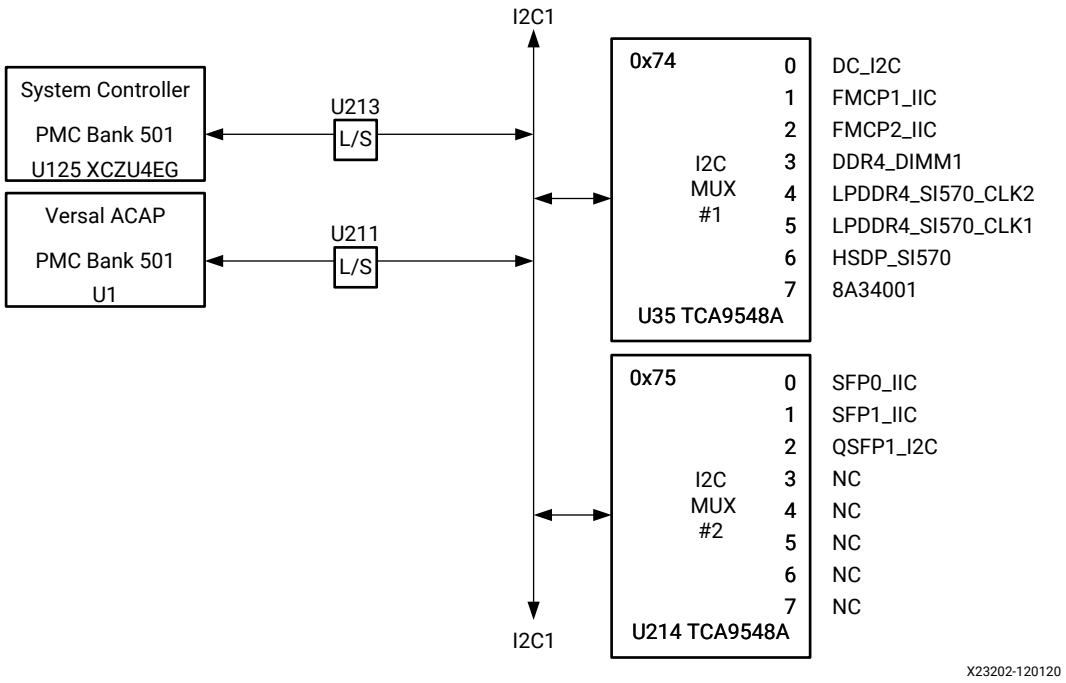


Table 13: **I2C1 TCA9548A U35 Address 0x74 Connections**

TCA9548A U35		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin No.	Pin Name	Reference Designator	Device
SDA	19	I2C0_SDA	See the connections shown in the "I2C1 Bus Topology" figure. TCA9548A U35 Addr. 0x74			
SCL	18	I2C0_SCL				
SD0/SC0	4/5	DC_I2C_SDA/SCL	D25,D24	D25,D24	J212	DC connector
			5,6	SDA,SCL	U34	M24128-BR
			7,8	SDA,SCL	U32	SI570
SD1/SC1	6/7	FMCP1_IIC_SDA/SCL	C31,C30	SDA, SCL	J51	ASP_184329_01
SD2/SC2	8/9	FMCP2_IIC_SDA/SCL	C31,C30	SDA, SCL	J53	ASP_184329_01
SD3/SC3	10/11	DDR4_DIMM1_SDA/SCL	285,141	SDA, SCL	J45	FCI 10124677
			7,8	SDA,SCL	U2	SI570
SD4/SC4	13/14	LPDDR4_SI570_CLK2_SDA/SCL	7,8	SDA,SCL	U3	SI570
SD5/SC5	15/16	LPDDR4_SI570_CLK1_SDA/SCL	7,8	SDA, SCL	U4	SI570
SD6/SC6	17/18	HSDP_SI570_SDA/SCL	7,8	SDA, SCL	U5	SI570
SD7/SC7	19/20	8A34001_SDA/SCL	L2,K2	SDIO, SCLK	U219	8A34001
			3,1&2	NA	J310	2x9 HDR

Table 14: **I2C1 TCA9548A U214 Address 0x75 Connections**

TCA9548A U214		Schematic Net Name	Connected To			
Pin Name	Pin No.		Pin No.	Pin Name	Reference Designator	Device
SDA	19	I2C0_SDA	See the connections shown in the "I2C1 Bus Topology" figure. TCA9548A U214 Addr. 0x75			
SCL	18	I2C0_SCL				
SD1/SC1	6/7	SFP0_IIC_SDA/SCL	T4,T5	SDA_T4,SCL_T5	J287(TOP)	2198318-6
SD2/SC2	8/9	SFP1_IIC_SDA/SCL	L4,L5	SDA_L4,SCL_L5	J287(BOT)	2198318-6
SD3/SC3	10/11	QSFP1_I2C_SDA/SCL	12,11	SDA, SCL	J288	1551920-2

Table 15: **I2C1 Bus Device I2C Addresses**

I2C Devices	I2C Switch Position	I2C Address		Device
I2C1 Bus				
TCA9548A 8-channel bus switch	N/A	0b1110100	0x74	U35 TCA9548A
Function	Port	Binary Format	Hex Format	
DC_I2C_SDA/ SCL	0	0b1010100	0x54	DC SE1 on J212
		0b1000010	0x42	DC SE2 on J212
		0b1011101	0x5D	U32 SI570
FMCP1_IIC_SDA/ SCL	1	0bXXXXXXX	0x##	J51 FMC HSPC
FMCP2_IIC_SDA/ SCL	2	0bXXXXXXX	0x##	J53 FMC HSPC
DDR4_DIMM1_SDA/ SCL	3	0b1010000	0x50	J45 FCI socket
		0b1100000	0x60	U2 SI570
LPDDR4_SI570_CLK2	4	0b1100000	0x60	U3 SI570
LPDDR4_SI570_CLK1	5	0b1100000	0x60	U4 SI570
HSDP_SI570_SDA/SCL	6	0b1011101	0x5D	U5 SI570
8A34001_SDA/SCL	7	0b1011000	0x58	U219 8A34001
		TBD	TBD	J310 2x9 HDR.
TCA9548 8-chan. bus switch	N/A	0b1110101	0x75	U214 TCA9548A
SFP0_IIC_SDA/SCL	0	0b1010000	0x50	J287 (BOT)
SFP1_IIC_SDA/SCL	1	0b1010000	0x50	J287 (TOP)
QSFP1_I2C_SDA/SCL	2	0b1010000	0x50	J288
No connect	3 - 7	NA	NA	NA

PMC MIO[48] and LPD_MIO[0:11, 24:25]: GEM0 Ethernet

[Figure 3, callout 16]

A PS Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface (see the figure in PMC MIO[49] and LPD_MIO[12:25]: GEM1 Ethernet), which connects to TI DP83867IRPAP U198 Ethernet RGMII PHY before being routed to a vertical dual-stacked RJ45 Ethernet connector J307 (upper receptacle). The RGMII Ethernet PHY is boot strapped to PHY address (`0x01`) and Auto Negotiation is set to *Enable*.

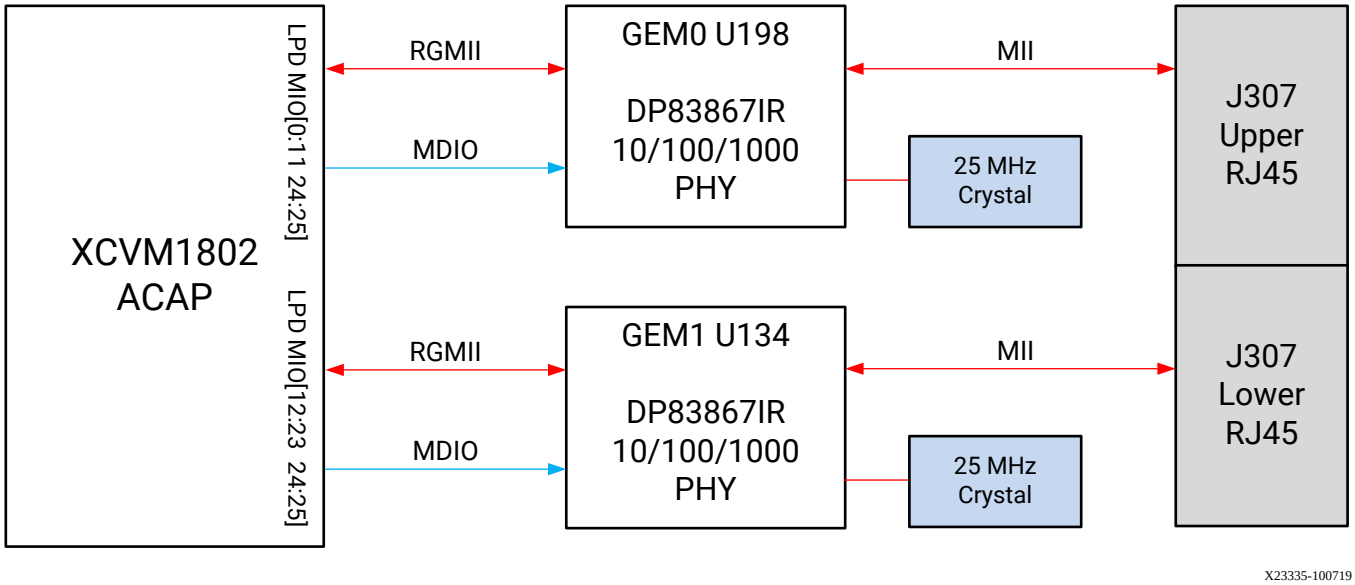
PMC MIO[49] and LPD_MIO[12:25]: GEM1 Ethernet

[Figure 3, callout 17]

A PS Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface (see the following figure), which connects to TI DP83867IRPAP U134 Ethernet RGMII PHY before being routed to a vertical dual-stacked RJ45 Ethernet connector J307 (lower receptacle). The RGMII Ethernet PHY is boot strapped to PHY address (`0x02`) and Auto Negotiation is set to *Enable*.

The following figure shows the dual Ethernet topology.

Figure 16: **Dual RGMII Ethernet**

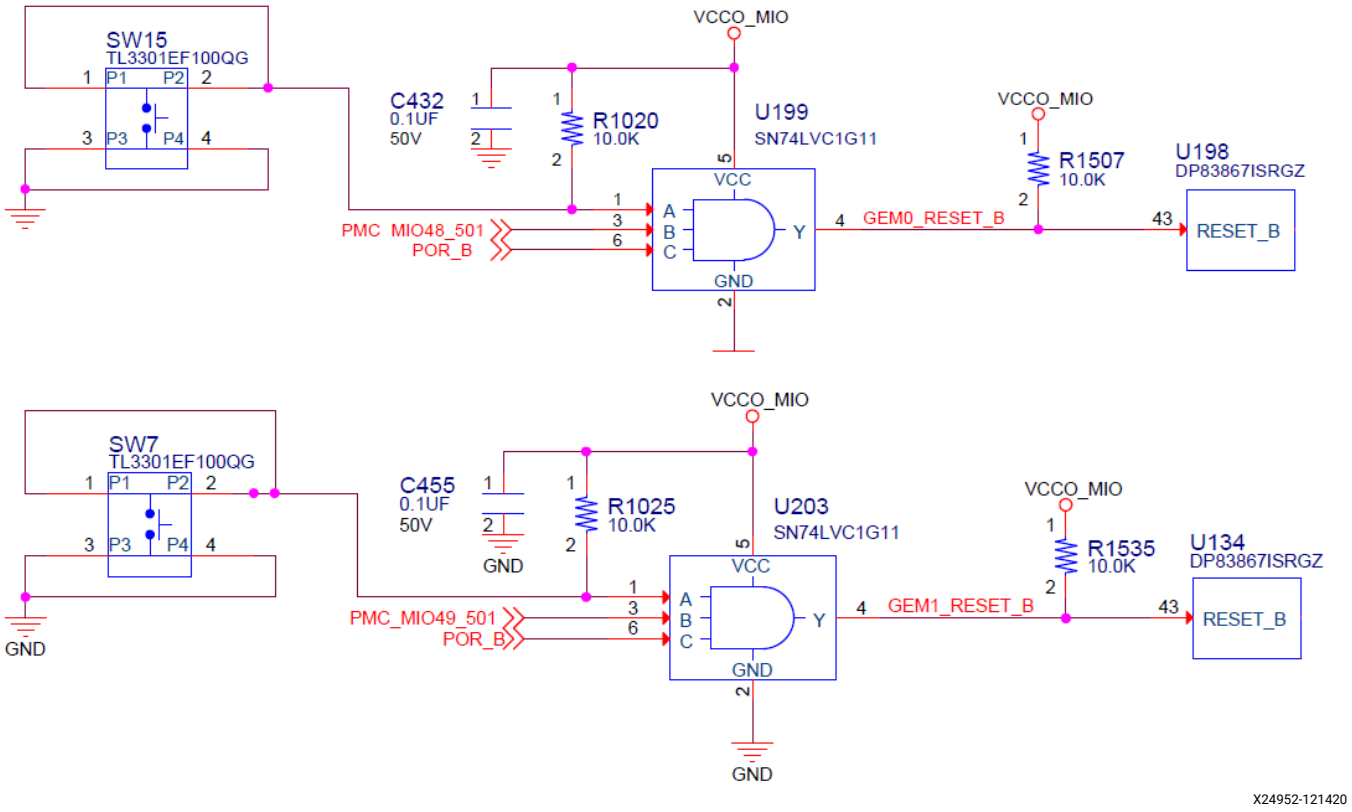


Ethernet PHY (Three Resets)

[Figure 3, callout 35]

Each DP83867ISRGZ PHY (GEM0 U198, GEM1 U134) is reset by its GEMx_RESET_B generated by dedicated pushbutton switches and PMC_MIO signals as shown in the following figure. The POR_B signal generated by the TPS389001DSER U10 POR device (activated by pushbutton SW2) is wired in parallel to each Ethernet PHY reset circuit.

Figure 17: **Ethernet PHY Reset Circuit**



Ethernet PHY LED Interface

[Figure 3, callout 16 and 17]

Each DP83867ISRGZ PHY (GEM0 U198, GEM1 U134) controls two LEDs in the J307 two port connector bezel. The upper port (GEM0) yellow and green LEDs are above the port, and the lower port (GEM1) LEDs are below the port. The PHY signal LED0 drives the green LED, and LED1 drives the yellow LED. The LED2 signal is not used.

The LED functional description is listed in the following table.

Table 16: **Ethernet PHY LED Functional Description**

DP83867IS PHY Pin		Type	Description
Name	Number		
LED_2	45	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits.
LED_1	46	S, I/O, PD	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be repurposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC.

See the TI DP83867 RGMII PHY data sheet at the Texas Instruments website for component details.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

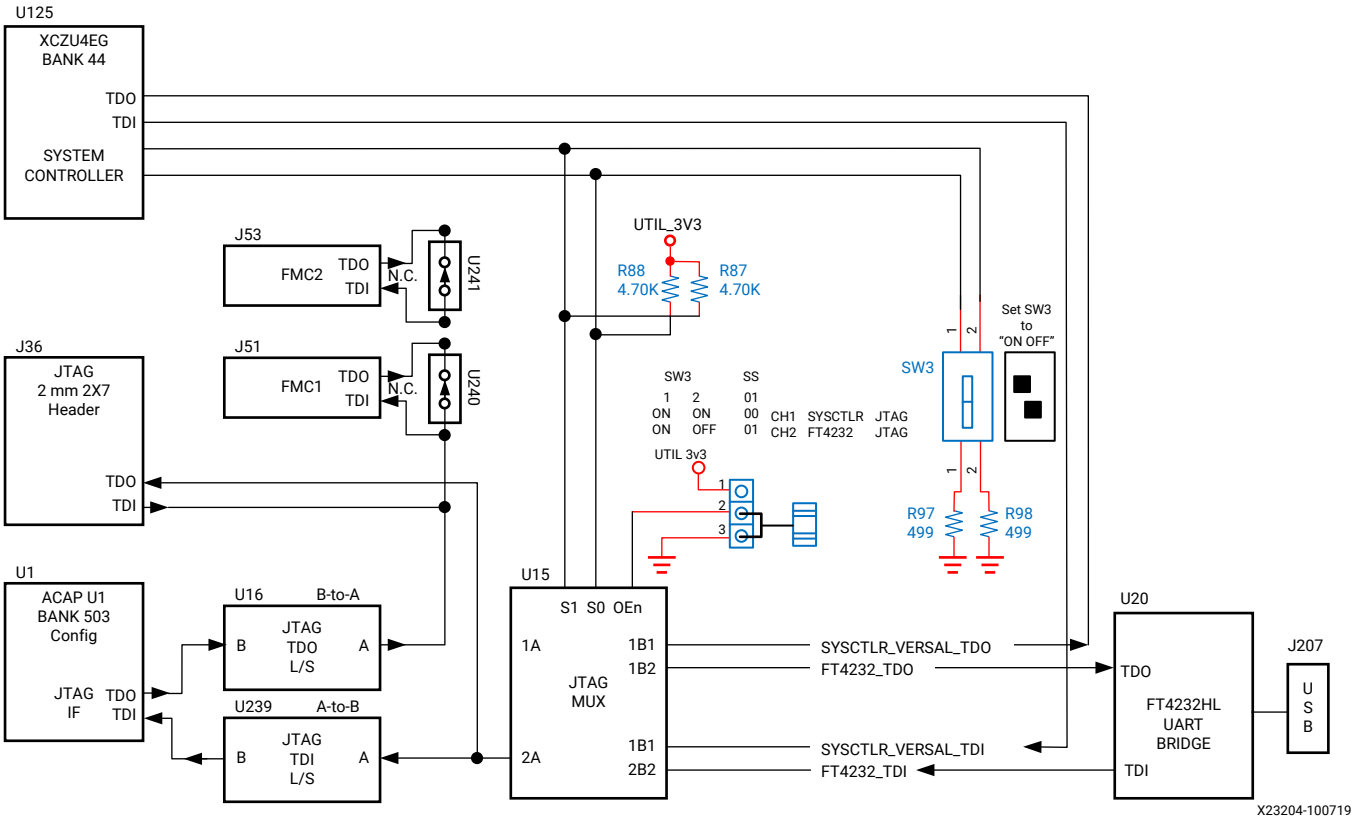
JTAG Chain

[Figure 3, callout 7, 8, and 48]

VMK180 JTAG chain

- J36 2x7 2 mm shrouded, keyed JTAG pod flat cable connector
- J207 USB-C connector connected to U20 FT4232HL USB-JTAG bridge
- U125 XCZU4EG System Controller bank 44

Figure 18: **JTAG Chain Block Diagram**



See Versal ACAP Configuration for information on JTAG programming via:

- FTDI FT4232 USB-to-JTAG/USB-UART device (U20) connected to USB 3.1 type-C connector (J207)
- JTAG pod flat cable connector J36 (2 mm 2x7 shrouded/keyed)

See the "FT4232HL UART Interface Connections" figure in PMC MIO[42:43] UART0 for an overview of FT4232 U20 JTAG and USB-UART connectivity.

Clock Generation

The VMK180 board provides fixed and variable clock sources for the XCVM1802 U1 ACAP and other function blocks. The following table lists the source devices for each clock.

Table 17: **Clock Sources**

Callout	Ref. Des.	Feature	Notes	Schematic Page
36	U2	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x60	Silicon Labs SI570BAB000299DG	4
37	U3	LPDDR4 CLK2, 200 MHz, 3.3V LVDS, 0x60	Silicon Labs SI570BAB000299DG	5
38	U4	LPDDR4 CLK1, 200 MHz, 3.3V LVDS, 0x60	Silicon Labs SI570BAB000299DG	7
39	U5	HSDP CLK, 156.25 MHz, 3.3V LVDS, 0x5D	Silicon Labs SI570BAB000544DG	8
40	U32	ACAP U1 REF CLK, 33.33 MHz, 1.8V CMOS, 0x5D	Silicon Labs SI570JAC000900DG	43
41	U39	PCIe jitter atten., 100 MHz, 3.3V LVDS	IDT 85411AMLF	49
42	U62	HDMI jitter atten., 148.50 MHz, 3.3V LVDS, 0x6C	IDT 8T49N241-994NLGI	52
43	U142	SYSCTLR clocks 33.33 MHz & 125 MHz I2C 0x6A	Silicon Labs Si5332FD10259-GM1	101
44	U192	zSFP CLK, 156.25 MHz, 3.3V LVDS, 0x5D	Silicon Labs SI570BAB000544DG	8
45	U205	FMCP MGT CLK, 100 MHz, 3.3V LVDS, 0x5F	Silicon Labs SI570BAC002038DG	48
46	U219	IEEE-1588 eCPRI CLK, various, 3.3V, 0x58	IDT 8A34001E-000AJG8	104
47	J328-J331	IEEE-1588 eCPRI 8A34001 CLK in and out SMA pairs	Rosenberger 32K10K-400L5	104

The connection details for ACAP U1 connected clocks described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Programmable DDR4 DIMM SI570 Clock

[Figure 3, callout 36]

The VMK180 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U2) connected to the GC inputs of U1 DDR4 DIMM interface bank 700. The DDR4_DIMM1_CLK_P and DDR4_DIMM1_CLK _N series capacitor coupled clock signals are connected to XCVM1802 ACAP U1 pins AE42 and AF43, respectively. At power-up, this clock defaults to an output frequency of 200.000 MHz. User applications or the System Controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VMK180 board reverts this user clock to the default frequency of 200.000 MHz.

- Programmable oscillator: Silicon Labs SI570BAB000299DG (10 MHz-945 MHz range, 200.000 MHz default)
- I2C address `0x60`
- LVDS differential output, total stability: 61.5 ppm

Programmable LPDDR4 SI570 Clock2

[Figure 3, callout 37]

The VMK180 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U3) connected to the GC inputs of U1 LPDDR4_2 interface bank 705. The LPDDR4_CLK2_P and LPDDR4_CLK2_N series capacitor coupled clock signals are connected to XCVM1802 ACAP U1 pins AW27 and AY27, respectively. At power-up, this clock defaults to an output frequency of 200.000 MHz. User applications or the System Controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VMK180 board reverts this user clock to the default frequency of 200.000 MHz.

- Programmable oscillator: Silicon Labs SI570BAB000299DG (10 MHz-945 MHz range, 200.000 MHz default)
- I2C address `0x60`
- LVDS differential output, total stability: 61.5 ppm

Programmable LPDDR4 SI570 Clock1

[Figure 3, callout 38]

The VMK180 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U4) connected to the GC inputs of U1 LPDDR4_1 interface bank 705. The LPDDR4_CLK1_P and LPDDR4_CLK1_N series capacitor coupled clock signals are connected to XCVM1802 ACAP U1 pins AK8 and AK7, respectively. At power-up, this clock defaults to an output frequency of 200.000 MHz. User applications or the System Controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VMK180 board reverts this user clock to the default frequency of 200.000 MHz.

- Programmable oscillator: Silicon Labs SI570BAB000299DG (10 MHz-945 MHz range, 200.000 MHz default)
- I2C address `0X60`
- LVDS differential output, total stability: 61.5 ppm

Programmable HSDP SI570 Clock

[Figure 3, callout 39]

The VMK180 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U5) connected to the GTY_REFCLK1 inputs of U1 GTY bank 105. The HSDP_SI570_CLK_P and HSDP_SI570_CLK _N series capacitor coupled clock signals are connected to XCVM1802 ACAP U1 pins J39 and J40, respectively. At power-up, this clock defaults to an output frequency of 156.250 MHz. User applications or the System Controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VMK180 board reverts this user clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs SI570BAB000544DG (10 MHz-945 MHz range, 156.250 MHz default)
- I2C address `0x5D`
- LVDS differential output, total stability: 61.5 ppm

Programmable zSFP SI570 Clock

[Figure 3, callout 44]

The VMK180 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U192) connected to the GTY_REFCLK0 inputs of U1 GTY bank 105. The zSFP_SI570_CLK_P and zSFP_SI570_CLK _N series capacitor coupled clock signals are connected to XCVM1802 ACAP U1 pins L39 and L40, respectively. At power-up, this clock defaults to an output frequency of 156.250 MHz. User applications or the System Controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VMK180 board reverts this user clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs SI570BAB000544DG (10 MHz-945 MHz range, 156.250 MHz default)
- I2C address `0x5D`
- LVDS differential output, total stability: 61.5 ppm

Programmable SI570 REF Clock

[Figure 3, callout 40]

The VMK180 board has an I2C programmable SI570 low-jitter 1.8V CMOS single-ended oscillator (U32). The 33.333 MHz REF_CLK clock signals is connected to XCVM1802 ACAP U1 configuration bank 503 pin AE32. At power-up, this clock defaults to an output frequency of 33.333 MHz. User applications or the System Controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VMK180 board reverts this user clock to the default frequency of 33.333 MHz.

- Programmable oscillator: Silicon Labs SI570JAC000900DG (10 MHz-945 MHz range, 33.333 MHz default)
- I2C address `0x5D`
- CMOS single-ended output, total stability: 61.5 ppm

Programmable SI5332 System Controller Clock

[Figure 3, callout 43]

The VMK180 board has an I2C programmable SI5332 low-jitter 6-differential-output clock generator (U142). Each output clock P/N pair has its own independent Vout pin. Two of the six output clocks are used on the VMK180.

OUT0 is a single-ended 33.333 MHz 1.8V LVCMOS clock SYSCTLR_PS_REF_CLK connected to the XCZU4EG System Controller (U125) configuration bank 503 pin R16.

OUT1 is a differential 125.000 MHz 3.3V LVDS clock. The SYSCTLR_GTR_CLK0_SGMII_P and SYSCTLR_GTR_CLK0_SGMII_N series capacitor coupled clock signals are connected to XCZU4EG U125 GTR bank 505 MGTREFCLK0 pins F23 and F24, respectively.

At power-up, OUT0 and OUT1 default the frequencies indicated above. User applications or the System Controller can change the output frequency within the range of 0 MHz to 333.333 MHz through the I2C bus interface. Power cycling the VMK180 board reverts the OUT0 and OUT1 frequencies to their defaults.

- Programmable clock generator: Silicon Labs Si5332FD10259-GM1 (0 MHz-333.333 MHz range)
- Outputs
  - OUT0: 33.3333... MHz [33 + 1/3 MHz] LVCMOS Single (+) 1.8V 50Ω [100/3 MHz]
  - OUT1: 125 MHz LVDS slow 3.3V
  - OUT2: 26 MHz LVDS slow 3.3V
  - OUT3: Unused
  - OUT4: Unused
  - OUT5: Unused

- I2C address `0x6A`

PCIe Clock

[Figure 3, callout 41]

The VMK180 board includes an IDT 85411 (U39) 1:2 clock buffer for the PCIe clock fan out to the Versal ACAP. The 100 MHz PCIE_CLK_P/N clock from the PCIe 8-lane edge connector (P3) drives the U39 clock input.

The U39's buffered outputs are used to create differential clock pairs to the ACAP U1 GTY103/GTY104 PCIe interface:

- U39's Q0 PCIE_CLK0_P/N are connected to PCIE_TX/RX[0:3] interface GTY103 GTY_REFCLK0 pins W39 (P) and W40 (N), which are A/C coupled
- U39's Q1 PCIE_CLK1_P/N are connected to PCIE_TX/RX[4:7] interface GTY104 GTY_REFCLK0 pins R39 (P) and R40 (N), which are A/C coupled
- 1:2 clock buffer
  - Q0: 100 MHz LVDS
  - Q1: 100 MHz LVDS

Programmable FMCP MGT SI570 Clock with Buffer

[Figure 3, callout 45]

The VMK180 board has an I2C programmable SI570 low-jitter 3.3V LVDS differential oscillator (U205) driving SI53340 (U206) 2-to-4 clock buffer input CLK0. The clock buffer generates four copies of the input clock. The SI53340 CLK1 second input is driven by 8A34001 (U219) output Q2. The SI53340 input clock select is controlled by 2-pin header J306 with default jumper off, selecting the CLK0 SI570 input. At power-up, SI570 (U205) defaults to an output frequency of 100.000 MHz. User applications or the System Controller can change the output frequency within the range of 10 MHz to 945 MHz through the I2C bus interface. Power cycling the VMK180 board reverts this user clock to the default frequency of 100.000 MHz.

- Programmable oscillator: Silicon Labs SI570BAB000299DG (10 MHz-945 MHz range, 100.000 MHz default)
- I2C address `0x5F`
- LVDS differential output, total stability: 61.5 ppm

The four SI53340 (U206) outputs are connected as follows:

- Outputs
  - Q0: SI570_8A34001_MUX_BUF0_P/N capacitor coupled to GTY201 FMCP1_DP[0:3]_C2M/M2C interface GTY_REFCLK0 pins AB11 (P) and AB10 (N)

- Q1: SI570_8A34001_MUX_BUF1_P/N capacitor coupled to GTY204 FMCP2_DP[0:3]_C2M/M2C interface GTY_REFCLK0 pins G13 (P) and G12 (N)
- Q2: SI570_8A34001_MUX_BUF2_P/N capacitor coupled to GTY205 FMCP2_DP[4:7]_C2M/M2C interface GTY_REFCLK0 pins E13 (P) and E12 (N)
- Q3: SI570_8A34001_MUX_BUF3_P/N capacitor coupled to GTY206 FMCP2_DP[8:11]_C2M/M2C interface GTY_REFCLK0 pins C13 (P) and C12 (N)

The connection details for ACAP U1 connected clocks described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

For more details on the Silicon Labs SI570, SI5332, and SI53340 devices, see the Silicon Labs website.

For more details on the IDT 85411AMLF, 8T49N241, and 8A34001 devices, see the Integrated Device Technology, Inc. website.

For Versal ACAP clocking information, see the *Versal ACAP Clocking Resources Architecture Manual* (AM003).

IEEE-1588 eCPRI Programmable Synchronization Management Unit

[Figure 3, callout 46]

GTY Transceivers

[Figure 3, callout 1]

The GTY transceivers in the XCVM1802 ACAP U1 are grouped into four channels or quads. The XCVM1802 has four GTY quads (GTYs 103-106) on the right side of the device and seven GTY quads (GTYs 200-206) on the left side of the device.

The VMK180 board provides access to 11 of the 11 GTY quads as shown in the GTY map in the following table.

The GTY connections are shown in the following figure.

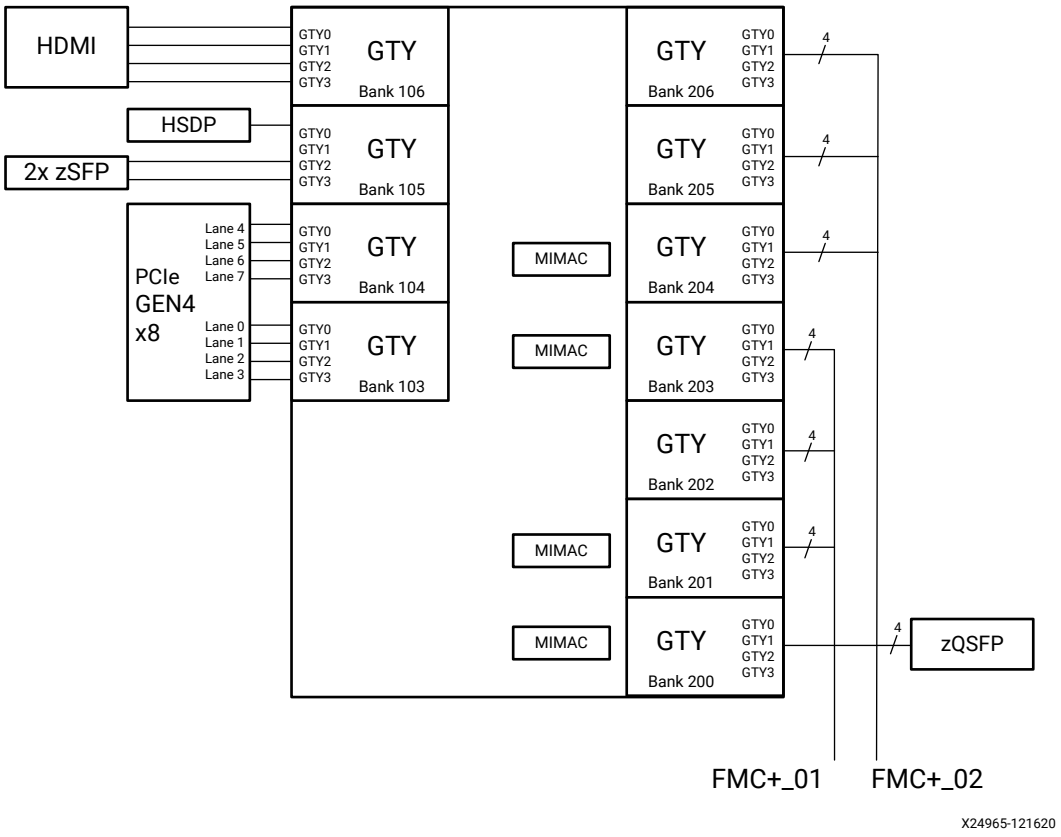
Table 18: **GTY Mapping**

VMK180 XC10S80 VSVA2197 GTY Mapping									
HDMI_TX_CLK_LVDS (TX only)	ch3	GTYT_S Quad 106					GTYT_S Quad 206	ch3	FMC2 DP11
HDMI Lane 2	ch2							ch2	FMC2 DP10
HDMI Lane 1	ch1							ch1	FMC2 DP9
HDMI Lane 0	ch0							ch0	FMC2 DP8
HDMI_9T49N241_CLK	refclk1							refclk1	FMC2_GBTCLK2
HDMI_RX_CLK	refclk0							refclk0	SI570_8A34001_MUX_BUF3

Table 18: **GTY Mapping** *(cont'd)*

VMK180 XC10S80 VSVA2197 GTY Mapping									
SFP1	ch3	GTYT_M Quad 105	PCIe			PCIe	GTYT_S Quad 205	ch3	FMC2 DP7
SFP0	ch2							ch2	FMC2 DP6
None	ch1							ch1	FMC2 DP5
HSDP (USB-C)	ch0							ch0	FMC2 DP4
HSDP SI570 CLK	refclk1							refclk1	FMC2_GBTCLK1
zSFP SI570 CLK	refclk0							refclk0	SI570_8A34001_MUX_BUF2
PCIe Lane 7	ch3	GTYB_M Quad 104	PCIe			MIMAC	GTYB_S Quad 204	ch3	FMC2 DP3
PCIe Lane 6	ch2							ch2	FMC2 DP2
PCIe Lane 5	ch1							ch1	FMC2 DP1
PCIe Lane 4	ch0							ch0	FMC2 DP0
None	refclk1							refclk1	FMC2_GBTCLK0
PCIe Slot Clock 0 (buffered)	refclk0							refclk0	SI570_8A34001_MUX_BUF1
PCIe Lane 3	ch3	GTYT_S Quad 103	CPMG4			MIMAC	GTYT_M Quad 203	ch3	FMC1 DP11
PCIe Lane 2	ch2							ch2	FMC1 DP10
PCIe Lane 1	ch1							ch1	FMC1 DP9
PCIe Lane 0	ch0							ch0	FMC1 DP8
NONE	refclk1							refclk1	FMC1_GBTCLK2
PCIe Slot Clock 0 (buffered)	refclk0							refclk0	None
			CPMG4			PCIe	GTYB_M Quad 202	ch3	FMC1 DP7
								ch2	FMC1 DP6
								ch1	FMC1 DP5
								ch0	FMC1 DP4
								refclk1	FMC1_GBTCLK1
								refclk0	None
						MIMAC	GTYT_S Quad 201	ch3	FMC1 DP3
								ch2	FMC1 DP2
								ch1	FMC1 DP1
								ch0	FMC1 DP0
								refclk1	FMC1_GBTCLK0
								refclk0	SI570_8A34001_MUX_BUF0
						MIMAC	GTYB_S Quad 200	ch3	QSFP4
								ch2	QSFP3
								ch1	QSFP2
								ch0	QSFP1
								refclk1	IEEE-1588 Clock
								refclk0	IEEE-1588 Clock

Figure 19: **VMK180 GTY Connections**



GTY103/104: PCI Express Card Edge Connectivity

[Figure 3, callout 15]

The 8-lane PCI Express card edge connector P3 supports operation up to Gen4 x8. P3 supports data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications, 8.0 GT/s for Gen3 applications, and 16.0 GT/s for Gen4 applications. The PCIe transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe_EP_REFCLK_P/N PCIe reference clock (routed as a 100Ω differential pair) received from J18 is routed to IDT 85411AMLF U39 1:2 buffer, which retransmits the clock as PCIe_CLK0 and PCIe_CLK1. U39 output Q0 PCIe_CLK0_P/N is routed to GTY103 (PCIe_EP_TX/RX[3:0]_P/N) and output Q1 PCIe_CLK1_P/N is routed to GTY104 (PCIe_TX/RX[7:4]_P/N).

For additional information about the Versal ACAP PCIe functionality, see the *Versal ACAP Integrated Block for PCI Express LogiCORE IP Product Guide* (PG343). Additional information about the PCI Express standard is available at the PCI-SIG website.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

GTY105: HSDP and 2x zSFP

GTY105 channel 1 is not used.

The GTY105 channel 0 high-speed debug port is a new feature that will be supported in the future. GTY105 REFCLK1 receives the HSDP_SI570_CLK from Si570 U5 (default frequency 156.25 MHz).

GTY105 channel 2 is wired to SFP0 and channel 3 is wired to SFP1. The two zSFPs are implemented in a dual-port stacked connector J287 (SFP0 lower, SFP1 upper). Each SFP has an I2C connection to the I2C1 bus through the I2C multiplexer (TCA9548PWR U214) as documented in PMC MIO[44:45] I2C1 Bus.

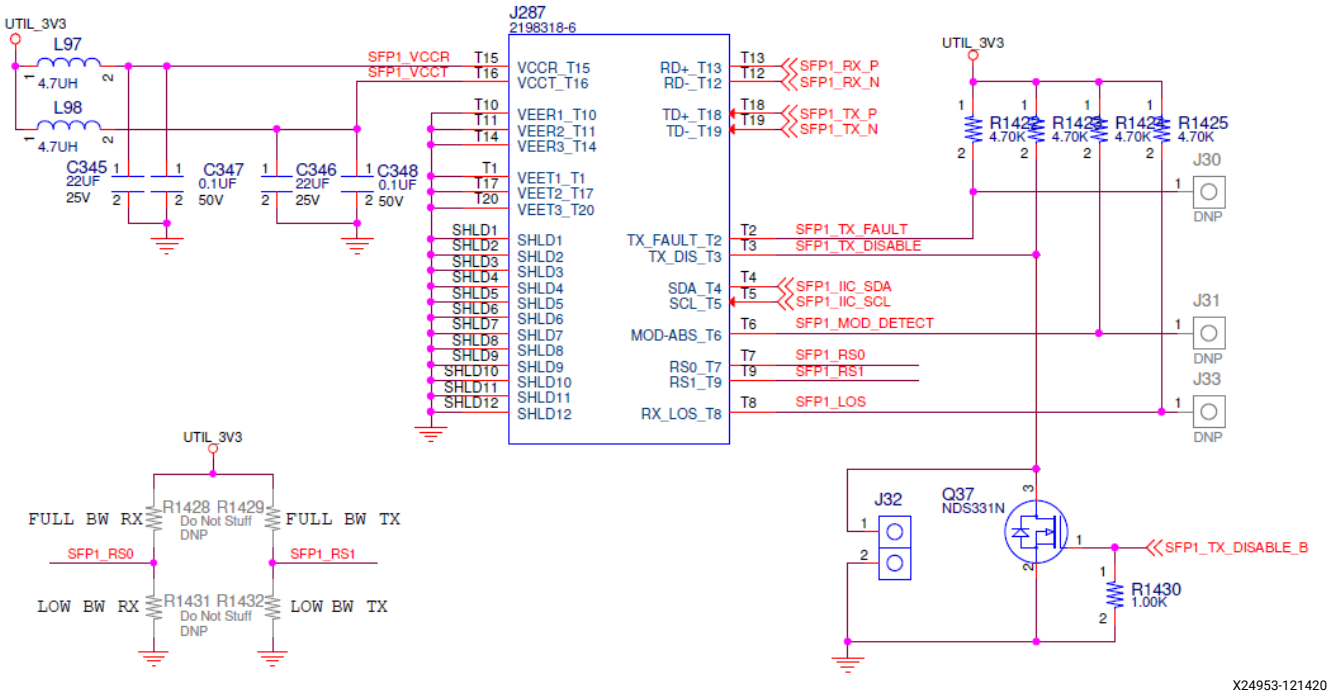
GTY105 REFCLK0 receives the zSFP_SI570_CLK from Si570 U192 (default frequency 156.25 MHz).

zSFP/zSFP+ Module Connector

[Figure 3, callout 13]

The VMK180 board hosts dual-port zSFP/zSFP+ J287, which accepts zSFP or zSFP+ modules. The following figure shows the zSFP/zSFP+ module connector circuitry typical of the two implementations.

Figure 20: **zSFP/zSFP+ Module Connector**



The following table lists the zSFP+ module control and status connections.

Table 19: **zSFP0- zSFP1 Module Control and Status Connections**

zSFP Control/ Status Signal	Board Connection		zSFP Module
SFP0_TX_FAULT	Test point J276	High = Fault	zSFP0 J287 lower
		Low = Normal operation	
SFP0_TX_DISABLE	Jumper J35	Off = SFP disabled	
		On = SFP enabled	
SFP0_MOD_DETECT	Test point J31	High = Module not present	
		Low = Module present	
SFP0_RS0[1]	PU R1420/PD R1426	PU R25 = Full RX bandwidth	
		PD R30 = Reduced RX bandwidth	
SFP0_RS1[1]	PU R1421/PD R1427	PU R227 = Full RX bandwidth	
		PD R142 = Reduced RX bandwidth	
SFP0_LOS	Test point J33	High = Loss of receiver signal	
		Low = Normal operation	
SFP1_TX_FAULT	Test point J30	High = Fault	zSFP1 J287 upper
		Low = Normal operation	
SFP1_TX_DISABLE	Jumper J32	Off = SFP disabled	
		On = SFP enabled	
SFP1_MOD_DETECT	Test point J277	High = Module not present	
		Low = Module present	
SFP1_RS0[1]	PU R1428/PD R1431	PU R182 = Full RX bandwidth	
		PD R190 = Reduced RX bandwidth	
SFP1_RS1[1]	PU R1429/PD R1432	PU R185 = Full RX bandwidth	
		PD R202 = Reduced RX bandwidth	
SFP1_LOS	Test point J278	High = Loss of receiver signal	
		Low = Normal operation	

Notes:

1. The RS0/RS1 PU/PD resistors are not populated. There are pull-down resistors built into the SFP/zSFP modules that select the lower bandwidth mode of the module.

For additional information about the enhanced SFP+ module, see the SFF-8431 specification at the SNIA website.

The zSFP connector I2C interfaces are connected to the I2C bus via the TCA9548 I2C multiplexer U214 (see PMC MIO[46:47] I2C0 Bus and PMC MIO[44:45] I2C1 Bus for more details).

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

GTY200: QSFP1

The GTY200 channels 0:3 are wired to QSFP1 J288.

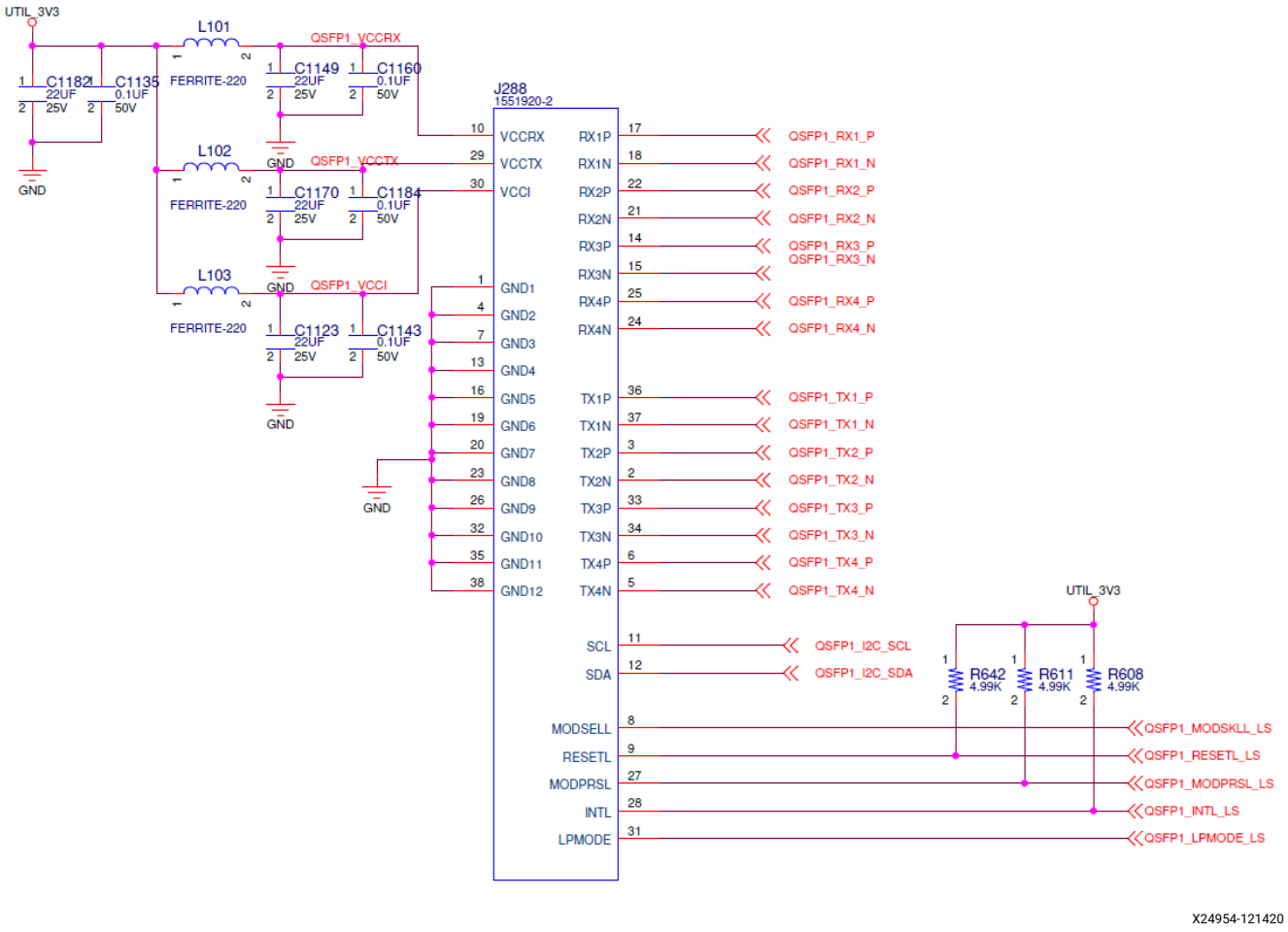
The GTY200 REFCLK0 drives 8A34001_CLK1_IN, and REFCLK1 receives the 8A34001_Q1_OUT to and from the 8A34001 clock device U219.

QSFP Module Connector

[Figure 3, callout 14]

The following figure shows the QSFP module connector circuitry implementation.

Figure 21: **QSFP Module Connector**



The QSFP connector 3.3V control nets are wired to ACAP U1 bank 406.

The QSFP connector I2C interface is connected to the I2C bus via the TCA9548 I2C multiplexer U214 (see PMC MIO[44:45] I2C1 Bus for more details).

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

GTY106: HDMI TX and RX

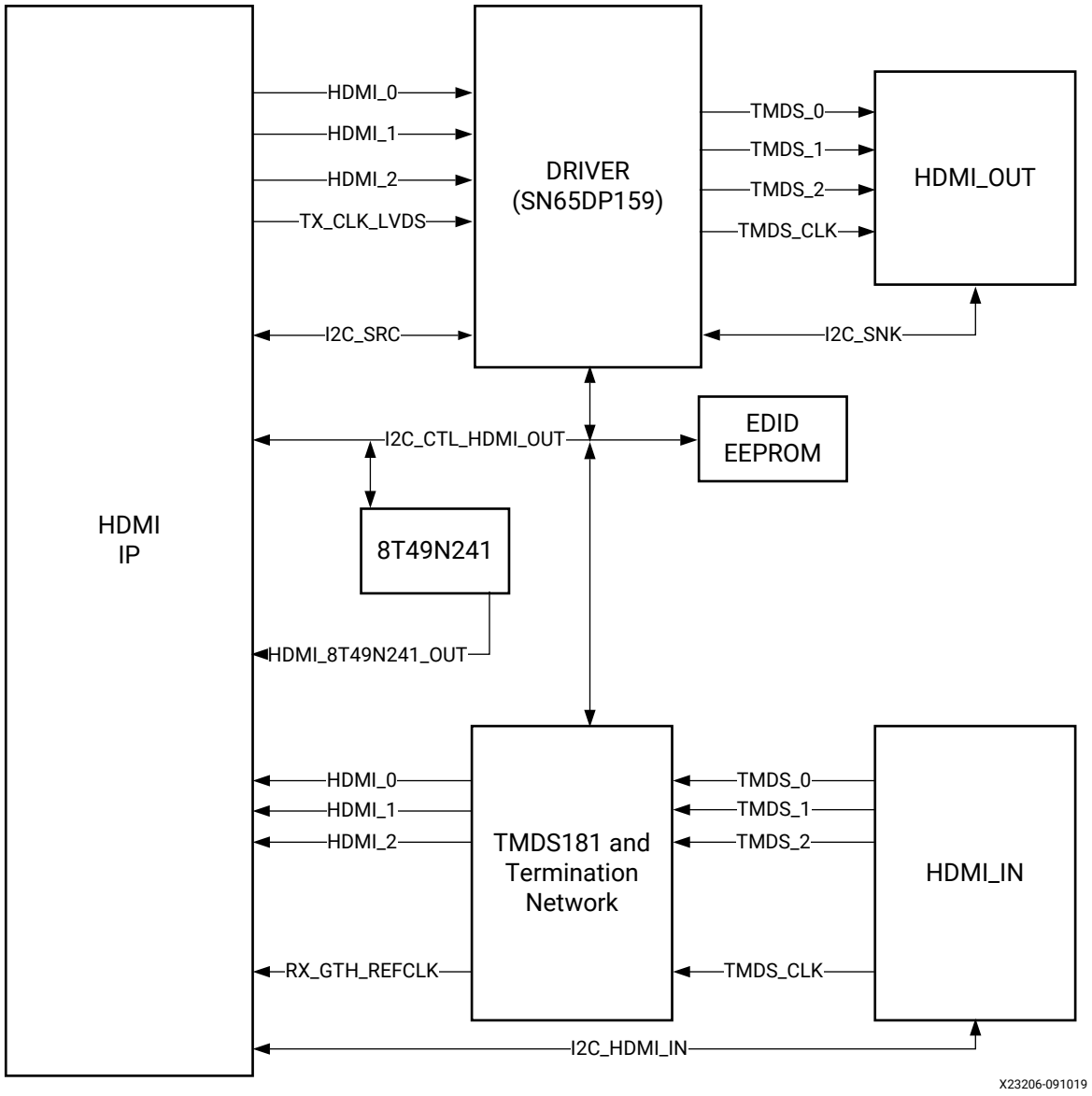
HDMI Video Output (TX)

[Figure 3, callout 18 and 19]

The VMK180 board provides an HDMI™ video output using a TI SN65DP159RGZ HDMI retimer at U43. The HDMI output is provided on a TE Connectivity 1888811-1 right-angle dual-stacked HDMI type A receptacle at P2 (upper port). The SN65DP159RGZ device is a dual mode DisplayPort to transition-minimized differential signal (TMDS) retimer supporting digital video interface (DVI) 1.0 and HDMI 1.4b and 2.0 output signals. The SN65DP159RGZ device supports the dual mode standard version 1.1 type 1 and type 2 through the DDC link or AUX channel. The SN65DP159RGZ device supports data rates up to 6 Gb/s per data lane to support Ultra HD (4K x 2K/60 Hz) 8-bits per color high-resolution video and HDTV with 16-bit color depth at 1080p (1920 x 1080/60 Hz). The SN65DP159RGZ device can automatically configure itself as a re-driver at data rates <1 Gb/s, or as a retimer at more than this data rate. This feature can be turned off through I2C programming. The HDMI video transmit/receive block diagram is shown in the following figure.

The ACAP U1 bank 406 user logic can implement a clock recovery circuit and output the series resistor coupled HDMI_REC_CLK_OUT (pin L19) for jitter attenuation. The jitter attenuated U62 Q2 HDMI_8T49N241_OUT_P/N series capacitor coupled output clock is connected to the HDMI_TX/RX[0:3] interface GTY106 GTY_REFCLK1 pins E39 (P) and E40 (N).

Figure 22: **HDMI Interface Block Diagram**



The VMK180 board accepts HDMI video input on the TE Connectivity 1888811-1 right-angle dual-stacked HDMI type-A receptacle P2 (lower port). The HDMI TMDS signals are input to TI TMDS181 retimer U55, which then drives the series capacitor coupled HDMI RX signals to U1 XCVM1802 GTY bank 106. The VMK180 HDMI RX interface supports up to 4K 60 Hz resolutions. See the Xilinx HDMI IP documentation for more details about resolutions, color spaces, and optional HDCP features supported by the U1 Versal ACAP.

The HDMI clock recovery is detailed in PCIe Clock.

For Xilinx HDMI IP details, see the *HDMI 1.4/2.0 Transmitter Subsystem Product Guide* (PG235) and the HDMI Transmitter and Receiver Subsystem Answer Record 70514.

See the HDMI Transmitter and Receiver Subsystem Answer Record 70514 for HDMI-compliant references.

For more details on the TI SN65DP159RGZ and TMDS181 HDMI retimers, see the component data sheets on the Texas Instruments website. For more details on the IDT 8T49N241, see the component data sheet on the Integrated Device Technology, Inc. website.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

GTY201 – GTY203: FMCP1 and GTY203 – GTY206: FMCP2 FPGA Mezzanine Card Interface

[Figure 3, callout 20 and 21]

The VMK180 evaluation board supports the VITA 57.4 FPGA mezzanine card (FMC+ or FMCP) specification by providing a subset implementation of the high pin count connectors at J51 (FMCP1) and J53 (FMCP2). FMC+ connectors use a 14 x 40 form factor, populated with 560 pins. The connector is keyed so that a mezzanine card, when installed on the VMK180 evaluation board, faces away from the board.

The FMCP1 DP[0:11] are connected across ACAP U1 GTY201-GTY203. The FMCP2 DP[0:11] are connected across ACAP U1 GTY204-GTY206. The FMCP1 and FMCP2 LA[0:33] bus and differential CLK pairs are connected across the banks 706, 707, and 708 triplet.

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

FMC+ Connector Type

The Samtec SEAF series, 1.27 mm (0.050 in) pitch mates with the SEAM series connector. For more information about the SEAF series connectors, see the Samtec, Inc. website.

The 560-pin FMC+ connector defined by the FMC specification (see Appendix A: VITA 57.4 FMCP Connector Pinouts) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 24 transceiver differential pairs
- 6 transceiver (GBTCLK) differential clocks
- 4 differential (CLK) clocks
- 1 differential (REFCLK) clock (both C2M and M2C pairs)
- 1 differential (SYNC) clock (both C2M and M2C pairs)

- 239 ground and 17 power connections

For more information about the VITA 57.4 FMC+ specification, see the VITA FMC Marketing Alliance website.

FMCP1 Connector J51

[Figure 3, callout 20]

The HSPC connector J51 implements a subset of the full FMCP connectivity:

- 68 single-ended or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 12 transceiver differential pairs
- 3 transceiver differential clocks
- 2 differential clocks
- 239 ground and 15 power connections

FMCP2 Connector J53

[Figure 3, callout 20]

The HSPC connector J53 implements a subset of the full FMCP connectivity:

- 68 single-ended or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 12 transceiver differential pairs
- 3 transceiver differential clocks
- 2 differential clocks
- 1 differential (REFCLK) clock C2M pair
- 1 differential (SYNC) clock C2M pair
- 239 ground and 15 power connections

See the FPGA Mezzanine Card (FMC) VITA 57.4 specification for additional information on the FMCP HSPC connector. The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

VADJ_FMC Power Rail

The VMK180 evaluation board implements the ANSI/VITA 57.4 IPMI support functionality. The power control of the VADJ_FMC power rail is managed by the ZU4 U125 System Controller. This rail powers both FMCP HSPC J51 and J53 VADJ pins, as well as the XCVM1802 U1 VCCO on the FMCP interface banks 706, 707, and 708. The valid values of the VADJ_FMC rail are 0, 1.2V, or 1.5V. At power on, the System Controller detects if an FMC module is installed on J51 or J53. The following sequence of actions then take place:

- If no card is attached to a FMCP connector, the VADJ_FMC voltage is set to 1.5V
- When an FMC card is attached, its IIC EEPROM is read to find a VADJ voltage supported by both the VMK180 board and the FMC module, within the available choices of 0, 1.2V, or 1.5V
- If no valid information is found in an attached FMC card IIC EEPROM, the VADJ_FMC rail is set to 0.0V

The System Controller user interface allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ_FMC rail. The override mode is useful for FMC mezzanine cards that do not contain valid IPMI EPROM data defined by the ANSI/VITA 57.4 specification.

User I/O

[Figure 3, callout 22 and 23]

The VMK180 board provides these GPIO bank 306 user and general purpose I/O capabilities:

- Four user LEDs (callout 22)
  - GPIO_LED[0:3]: DS6, DS5, DS4, DS3
- 4-position user DIP switch (callout 23)
  - GPIO_DIP_SW[0:3]: SW6
- Two user pushbuttons and CPU reset switch (callouts 24 and 25)
  - GPIO_PB[0:1]: SW4, SW5

The detailed ACAP connections for the feature described in this section are documented in the VMK180 board XDC file, referenced in Appendix B: Xilinx Design Constraints.

Power and Status LEDs

[Figure 3, callout 29]

The following table defines the power and status LEDs. For user-controlled GPIO LED details, see User I/O.

Table 20: **Power and Status LEDs**

Ref. Des.	Schematic Net Name	LED Color	Description
DS1	DONE	Green	ACAP U1 bit file download is complete
DS2	PS_ERR_OUT	Red	PS_ERR_OUT is asserted for accidental loss of power, an error in the PMU that holds the CSU in reset, or an exception in the PMU
DS3	GPIO_LED_3	Green	USER GPIO LED
DS4	GPIO_LED_2	Green	USER GPIO LED
DS5	GPIO_LED_1	Green	USER GPIO LED
DS6	GPIO_LED_0	Green	USER GPIO LED
DS9	VCCINT_PGOOD	Green	VCCINT 0.80 VDC power on
DS10	VCC_SOC_PGOOD	Green	VCC_SOC 0.80V power on
DS11	VCC_PMC_PGOOD	Green	VCC_PMC 0.80V power on
DS12	VCC_RAM_IO_PGOOD	Green	VCC_RAM_IO 0.80V power on
DS13	VCC_PSLP_PGOOD	Green	VCC_PSLP 0.80V power on
DS14	VCC_PSFP_PGOOD	Green	VCC_PSFP 0.80V power on
DS15	VCCAUX_PMC_PGOOD	Green	VCCAUX_PMC 1.5 VDC power on
DS16	VCCAUX_PGOOD	Green	VCCAUX 1.5 VDC power on
DS17	DIMM1_VTERM_0V60_PGOOD	Green	DDR4 DIMM VTERM 0.6 VDC power on
DS19	UTIL_3V3_PGOOD	Green	UTIL_3V3 3.3 VDC power on
DS20	VCCO_MIO_PGOOD	Green	VCCO_MIO 1.8 VDC power on
DS21	VCC3V3_PGOOD	Green	VCC3V3 3.3 VDC power on
DS22	VCC1V8_PGOOD	Green	VCC1V8 1.8 VDC power on
DS23	VCC1V2_DDR4_PGOOD	Green	VCC1V2_DDR4 1.2 VDC power on
DS24	VCC1V1_LP4_PGOOD	Green	VCC1V1_LP4 1.1 VDC power on
DS26	VADJ_FMC_PGOOD	Green	VADJ_FMC 1.5V (Nom.) power on
DS27	MGTYAVTT_PGOOD	Green	MGTYAVTT 1.2 VDC power on
DS28	MGTYAVCC_PGOOD	Green	MGTYAVCC 0.88 VDC power on
DS29	UTIL_1V13_PGOOD	Green	UTIL_1V13 1.13 VDC power on
DS30	MGTYVCCAUX_PGOOD	Green	MGTVCCAUX 1.5 VDC power on
DS32	UTIL_2V5_PGOOD	Green	UTIL_2V5 2.5 VDC power on
DS33	SYSCTLR_INIT_B	Red	
DS34	SYSCTLR_DONE	Green	
DS35	SYSCTLR_ETH_WOL	Green	
DS36	VCC12_SW	Green	12 VDC power on
DS37	USB3320 ERROR	Red	
DS39	MAX8869 RST_B	Green	GEM0/1 VDDA1P0 is 8% or lower

The following figure shows the board's power good LEDs.

Figure 23: **Power Good Indicator LEDs**

X24955-121420

Cooling Fan Connector

[Figure 3, callout 34]

The VMK180 cooling fan connector is shown in the following figure. The VMK180 uses the Maxim MAX6643 (U64) fan controller, which autonomously controls the fan speed by controlling the pulse width modulation (PWM) signal to the fan based on the die temperature sensed via the ACAP's DXP and DXN pins. The fan rotates slowly (acoustically quiet) when ACAP U1 is cool and rotates faster as the ACAP heats up (acoustically noisy).

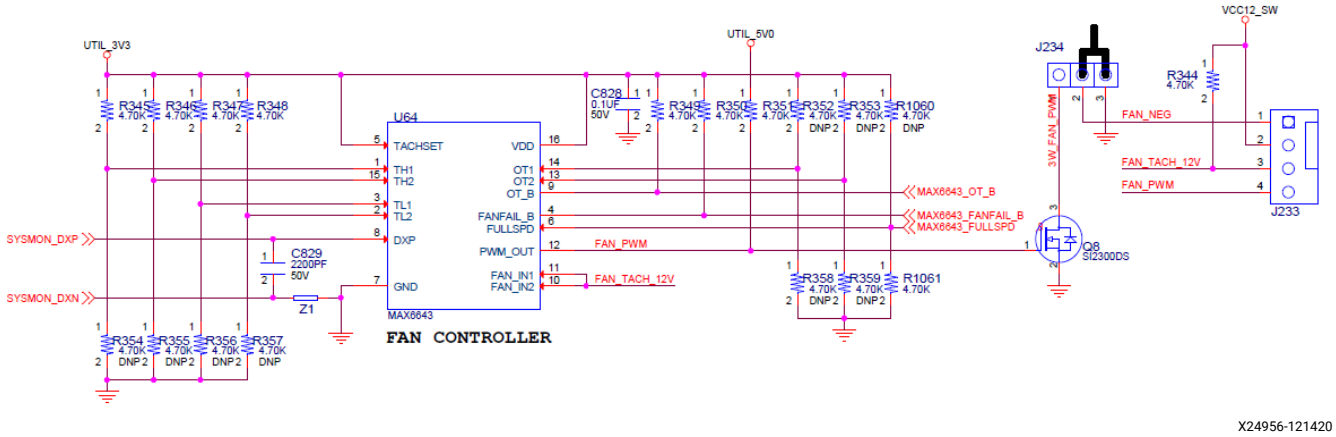
The fan speed (PWM) versus the ACAP die temperature algorithm along with the over temperature set point and fan failure alarm mechanisms are defined by the strapping resistors on the MAX6643 device.

The over temperature and fan failures alarms can be monitored either by any available processor in ACAP U1 by polling the I2C expander U233 on the I2C bus or via the ZU4 U125 System Controller.

The VMK180 board provides a fan controller bypass header J234 to permit the fan to be always on. Always on (J234 pins 2 and 3 jumpered) is the default jumper setting shown in the figure.

Note: When J234 pins 1 and 2 are jumpered to enable fan controller functionality, at initial board power on it is normal for the fan controller to energize the fan at full speed for a few seconds.

Figure 24: **12V Fan Header**



System Controller

[Figure 3, callout 48]

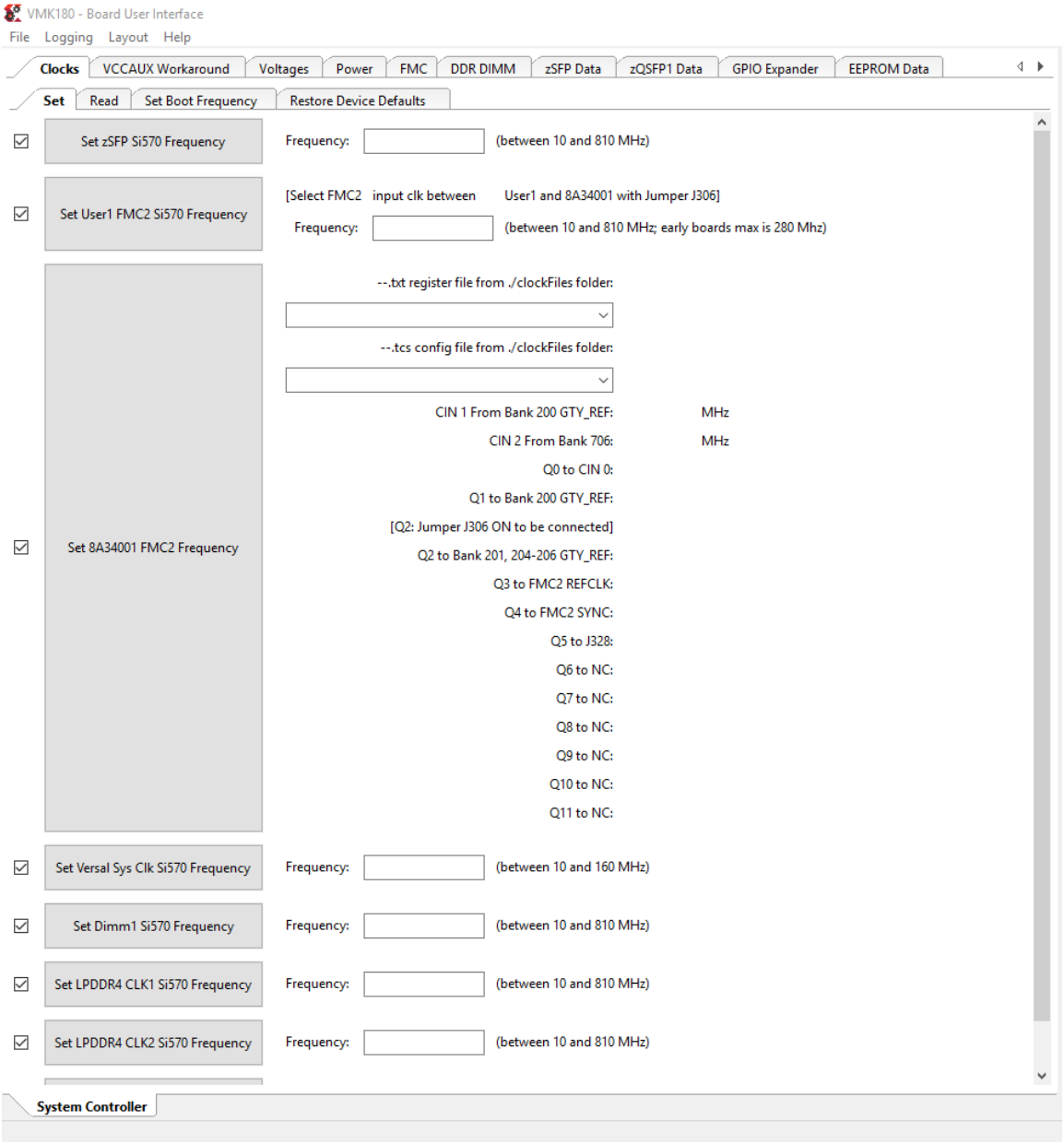
The VMK180 board includes an onboard System Controller. A host PC resident system controller board user interface application is provided on the VMK180 evaluation board website. This board user interface application enables the query and control of select programmable features such as clocks, FMC functionality, and power system parameters. The VMK180 website also includes a tutorial on the board user interface application and board setup instructions.

A brief summary of these instructions is provided here.

1. Ensure the Silicon Labs VCP USB-UART drivers are installed. See the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033).
2. Download the board user interface host PC application from the VMK180 evaluation board website.
3. Connect a USB cable to VMK180 USB-UART USB-C connector (J207).
4. Power-cycle the VMK180.
5. Launch the board user interface application.

The board user interface application UI is shown in the following figure.

Figure 25: **System Controller User Interface**



On first use of the SCUI, select **FMC → Set VADJ → Boot-up** tab and click **USE FMC EEPROM Voltage**. The SCUI buttons gray out during command execution and return to their original appearance when ready to accept a new command.

See the VMK180 Software Install and VMK180 Board Setup Tutorial (XTP629) and the System Controller Tutorial (XTP628) (which includes instructions for changing VMK180 clocks) for more information on installing and using the system controller UI.

Switches

[Figure 3, callout 6 and 30]

The VMK180 board includes power and configuration switches:

- SW13 power on/off slide switch
- SW1 U1 ACAP PS bank 503 4-pole mode DIP switch

Power On/Off Slide Switch

[Figure 3, callout 30]

The VMK180 board power switch is SW13. Sliding the switch actuator from the off to the on position applies 12VDC power from either the 2x3 6-pin Mini-Fit power input connector J16 (power from an external 120VAC-to-12VDC power adapter) or the 2x4 8-pin ATX power supply PCIe-type connector JP1.

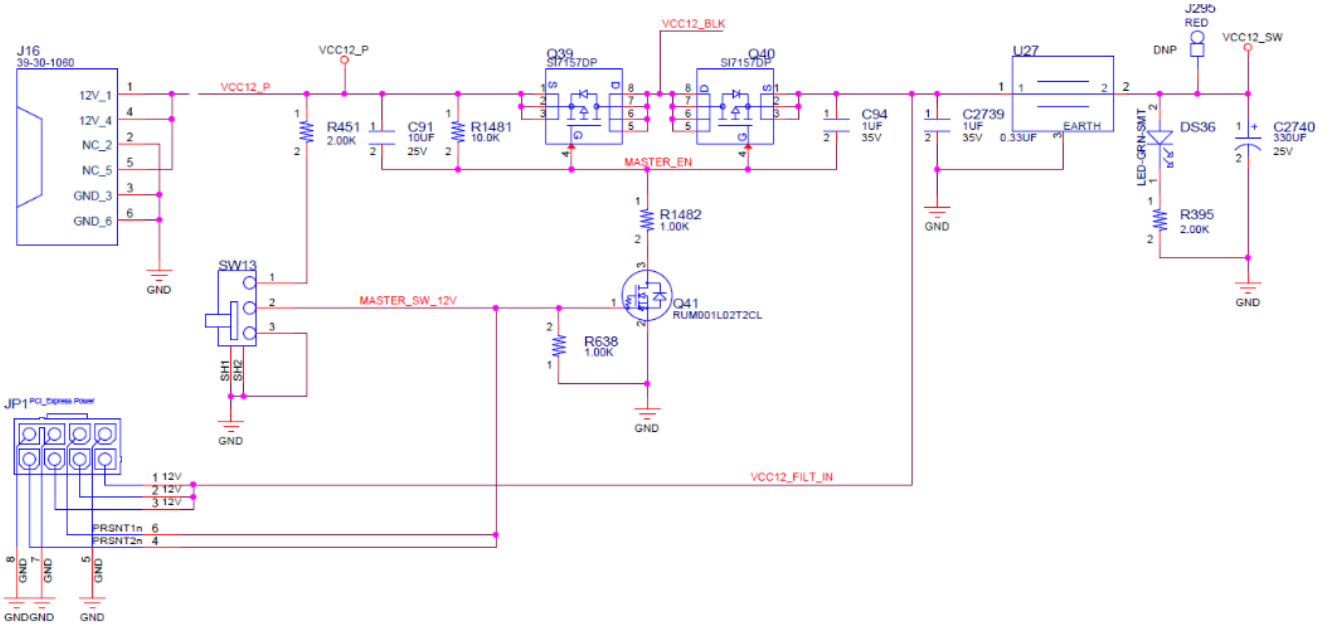
IMPORTANT! *Power to the VMK180 is mutually exclusive and only one of the two power connectors J16 or JP1 should be used to provide board power.*

The green LED DS36 illuminates when the VMK180 board power switch is on. See Board Power System for details on the onboard power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the VMK180 board power connector J16. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VMK180 board and voids the board warranty.*

The following figure shows the power connector J16, power switch SW13, and LED indicator DS36.

Figure 26: **Power Input**



X23276-100119

Board Power System

[Figure 3, callout 27]

The VMK180 evaluation board uses power management ICs (PMIC) and power regulators from Infineon (Integrated Circuits) to supply the core and auxiliary voltages listed in the following tables. See schematic 038-05005-01 in XTP620, available from the VMK180 product page.

Table 21: **Power System - PMBus Regulators and INA226 Map**

PMBus Regulators and INA226 Map								
Schematic Page	Rail Name	Regulator Type	U#	Vout (V)	Iout (A)	I2C Address	INA226 U#	INA226 I2C Address
							PMBUS1(1), PMBUS2(2)	
57	VCCINT	IR35215 PMIC (6 Phase)	U152	0.80	190	0x16	U65	0x40(1)
	VCC_SOC			0.80	18		U161	0x41(1)
61	VCC_PSLP	IRPS5401 (4 Phase + LDO)	U160	0.80	1	0x17	U165	0x44(1)
	VCC_PSFP			0.80	2		U164	0x45(1)
	VCCAUX			1.5	3		U166	0x40(2)
	VCC_RAM_IO			0.80	4		U162	0x43(1)
	VCCINT_PMC			0.80	0.5		U163	0x42(1)
63	VCCO_MIO	IRPS5401 (4 Phase + LDO)	U167	1.8	2	0x1C	U172	0x45(2)
	VCC3V3			3.3	0.5		U174	0x47(2)
	VCC1V8			1.8	6		U173	0x46(2)
	VCCAUX_PMC			1.5	0.5		U168	0x41(2)
65	UTIL_1V13	IRPS5401 (4 Phase + LDO)	U175	1.13	1	0x1D	NA	NA
	UTIL_2V5			2.5	1		NA	NA
	VCC1V2_DDR4			1.2	4		U176	0x48(2)
	VCC1V1_LP4			1.1	4		U177	0x49(2)
	MGTYVCCAUX			1.5	0.5		U234	0x4D(2)
69	VADJ_FMC	IR38164	U185	1.5	10	0x1E	U184	0x4A(2)
70	MGTYAVCC	IR38164	U187	0.88	6	0x1F	U186	0x4B(2)
71	MGTYAVTT	IR38164	U189	1.2	10	0x20	U188	0x4C(2)

RECOMMENDED: *To ensure reliable operation, Xilinx recommends running the report_power command in the Vivado tools for designs targeting this board. The reported rail current requirements should do not exceed the values listed in the following table.*

The total device power should remain under 125W. To assist the Vivado tools in reporting when power exceeds this amount, add this XDC constraint:

`set_operating_conditions-design_power_budget` 125 ;# (125W max power)

Table 22: **Device Rail Maximum Current**

Device Rail	Maximum Current (Amps)
VCCINT	190
VCC_SOC + VCC_IO	18
VCC_PSLP	1
VCC_PSFP	2
VCCAUX	1.5
VCC_RAM	4
VCC_PMC	0.5
VCCAUX_PMC	0.5
MGTYVCCAUX	0.5
MGTYAVCC	6
MGTYAVTT	10
VCCO 3.3V	0.5
VCCO 1.5V* (assuming VADJ_FMC programmed to 1.5V)	10
VCCO 1.1V	4
VCCO 1.8V + VCCO_501 + VCCO_502 + VCCO_503	2

Table 23: **Power System - Non-PMBus Regulators and INA226 Map**

Non-PMBus Regulators and INA226 Map								
Schematic Page	Rail Name	Regulator Type	U#	Vout (V)	Iout (A)	I2C Address	INA226 U#	INA226 I2C Address
72	DIMM1_VTERM	IR3897	U80	0.6	4	NA	NA	NA
73	UTIL_3V3	IR3889	U190	3.3	22	NA	NA	NA
74	UTIL_5V0	IR3889	U191	5	15	NA	NA	NA
102	SYS_VCC0V85	TPS62480RNCR	U143	0.85	6	NA	NA	NA
103	SYS_VCC1V8	TPS62097RWKR	U144	1.8	2	NA	NA	NA
	SYS_VCC1V1	TPS7A8300ARGRR	U145	1.1	2	NA	NA	NA
	SYS_MGTAVCC	TPS62097RWKR	U146	0.9	2	NA	NA	NA
	SYS_VCC1V2	TPS62097RWKR	U147	1.2	2	NA	NA	NA

Table 23: **Power System - Non-PMBus Regulators and INA226 Map** *(cont'd)*

Non-PMBus Regulators and INA226 Map								
106	8A34001_VCC_GPIO_DC	LP38798SD-ADJ/NOPB	U223	3.3	0.8	NA	NA	NA
	8A34001_VDDA	LP38798SD-ADJ/NOPB	U225	3.3	0.8	NA	NA	NA
	8A34001_VDDO_Q1_10_7	LP38798SD-ADJ/NOPB	U226	3.3	0.8	NA	NA	NA
	8A34001_VDD_CLK0	LP38798SD-ADJ/NOPB	U227	3.3	0.8	NA	NA	NA
	8A34001_VDDO_Q0_9_6	LP38798SD-ADJ/NOPB	U228	3.3	0.8	NA	NA	NA
	8A34001_VDD_CLK1	LP38798SD-ADJ/NOPB	U229	3.3	0.8	NA	NA	NA
	8A34001_VDDO_Q2_4_11	LP38798SD-ADJ/NOPB	U230	3.3	0.8	NA	NA	NA
	8A34001_VDDO_Q8_3_5	LP38798SD-ADJ/NOPB	U236	3.3	0.8	NA	NA	NA
107	8A34001_VDD_FOD	LP38798SD-ADJ/NOPB	U231	1.8	0.8	NA	NA	NA
	8A34001_VDDD	LP38798SD-ADJ/NOPB	U232	1.8	0.8	NA	NA	NA

More information about the power system regulator components can be found at the Infineon Integrated Circuits website.

The FMCP HSPC (J51 and J53) VADJ pins are wired to the programmable rail VADJ_FMC. The VADJ_FMC rail is programmed to 1.50V by default. The VADJ_FMC rail also powers the XCVM1802 FMCP interface banks 706, 707, and 708 (see the table in I/O Voltage Rails). Documentation describing PMBus programming for the Infineon power controllers is available at the Infineon Integrated Circuits website. The PCB layout and power system design meet the recommended criteria described in the *Versal ACAP PCB Design User Guide* (UG863).

Monitoring Voltage and Current

Twenty rails have a TI INA226 PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA226 to report the sensed parameters separately on the PMBus. The rails equipped with the INA226 power monitors are shown in the power system table in Board Power System.

As described in PMC MIO[46:47] I2C0 Bus, the I2C0 bus provides access to the PMBus power controllers and the INA226 power monitors via the U33 TCA9548A bus switch. All PMBus controlled Infineon regulators are tied to the PMBUS_SDA/SCL PMBus, while the INA226 power monitors are split across PMBUS1_INA226_SDA/SCL and PMBUS2_INA226_SDA/SCL.

The I2C0 bus topology figure and I2C0 port expander TCA6416A U233 address 0x20 connections table in PMC MIO[46:47] I2C0 Bus document the I2C0 bus access path to the Infineon PMBus controllers and INA226 power monitor op amps. Also, see schematic See schematic 038-05005-01 in XTP620, available from the VMK180 product page. These power system components are also accessible to the ZU4 U125 system controller (bank 501) and the ACAP U1 (bank 501).

VITA 57.4 FMCP Connector Pinouts

Overview

The following figure shows the pinout of the FPGA plus mezzanine card (FMCP) high pin count (HSPC) connector defined by the VITA 57.4 FMC specification. For a description of how the VMK180 evaluation board implements the FMCP specification, see FPGA Mezzanine Card Interface.

Figure 27: **FMCP HSPC Connector Pinout**

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

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Appendix B

Xilinx Design Constraints

Overview

The Xilinx® design constraints (XDC) file template for the VMK180 board provides for designs targeting the VMK180 evaluation board. Net names in the constraints listed correlate with net names on the latest VMK180 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.

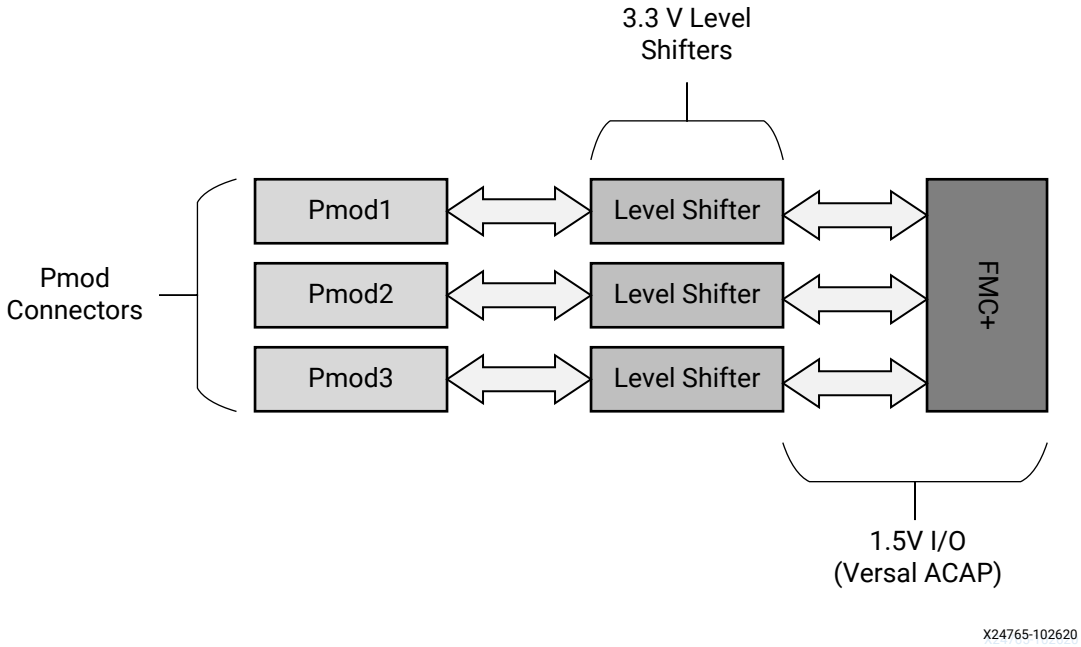
The HSPC FMCP connectors J51 and J53 are connected to ACAP U1 banks powered by the variable voltage VADJ_FMC. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT! *See the VMK180 board documentation ("Board Files" check box) for the XDC file.*

Pmod FMC

The Pmod FMC-XM119 board is for accessing Pmod standard devices or general purpose I/O from the base development board. The Pmod standard uses 100 mil space, 25 mil square, and pin header style connectors. The following figure shows a basic block diagram of the main components on the Pmod FMC. The basic function of this board is to provide a Pmod compatible standard connected to the PL I/O of the Versal® ACAP. For more information, see the Digilent Pmod Interface Specification.

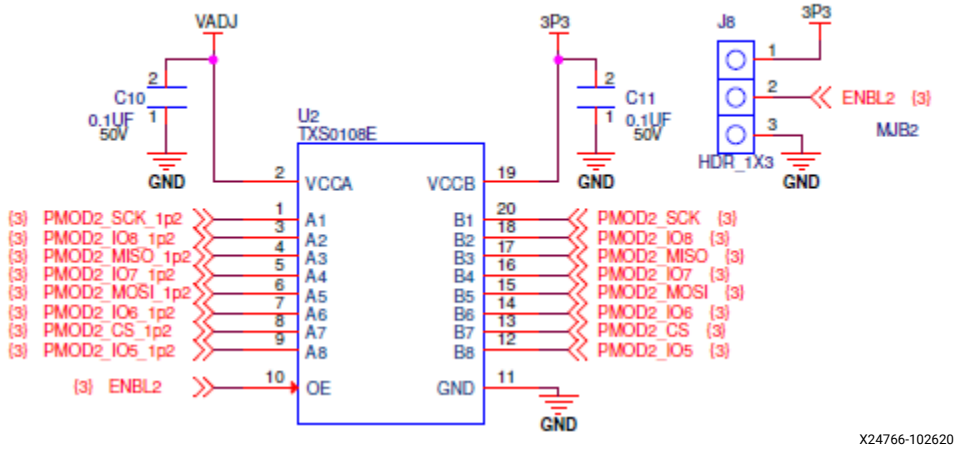
Figure 28: **Pmod FMC Block Diagram**



The FMC-XM119 board provides three Pmod 12 pin connectors. There are voltage level translators on the I/O side from the ACAP because of voltage compatibility with the bank fixed voltages. See the *Versal ACAP SelectIO Resources Architecture Manual* (AM010) for details on bank voltages.

The voltage translators shown in the figure are the TXS0108E 8-bit bidirectional level shifter voltage translators for open drain and push-pull applications. The input voltage for the I/O to the level translator is controlled from the VADJ, which operates in the range of 1.5V to 3.3V. With the Versal ACAP, the I/O voltage on the XPIO (which is the primary I/O of the FMC) is a maximum of 1.5V, so the default setting for using this FMC Pmod card is VADJ = 1.5V on the XPIO I/O. On the output side of the level translator, this is converted to a 3.3V signal because the Pmod specification is at 3.3V. 5V is also supported per the Pmod specification, but this voltage is not supported without modification to the output power supplies of the level translator, which are fixed at 3.3V for the XM119 FMC board.

Figure 29: **TXS0108E Bidirectional Voltage Level Translator**



***Note*:** This level translator was specifically chosen to allow bidirectional signaling at lower frequencies, such as for I2C. The Pmod board is generic and can work with both the VCK190 and VMK180 development kits. The pinouts are identical between the boards, and usage should be straightforward.

Pin Mapping Pmod to FMC

The pin mapping is straightforward. The ACAP pins are connected to the input to the level translators, which map to the output pins on the Pmod connector at 3.3V. See Figure 29 for details.

Figure 30: **Pmod FMC Pin Mapping**

PMOD Conn	PMOD Conn pin#	Net Name	FMC Conn Pin	FMC Net Name	Board Net Name	Board Pin#	IO Standard	Bank #	Vcco	pkg-pin Name
J4	4	PMOD1_SCK	G6	LA00_CC	FMCP1_LA00_CC_P	BD23	SSTL15	706	VADJ_FMC	IO_L6P_GC_XCC_N2P0_M2P12_706
J7	1	PMOD2_CS	D8	LA01_CC	FMCP1_LA01_CC_P	BC23	SSTL15	706	VADJ_FMC	IO_L9P_GC_XCC_N3P0_M2P18_706
J4	1	PMOD1_CS	H7	LA02	FMCP1_LA02_P	AW24	SSTL15	706	VADJ_FMC	IO_L17P_N5P4_M2P34_706
J4	2	PMOD1_MOSI	G9	LA03	FMCP1_LA03_P	AV22	SSTL15	706	VADJ_FMC	IO_L14P_N4P4_M2P28_706
J4	3	PMOD1_MISO	H10	LA04	FMCP1_LA04_P	AU21	SSTL15	706	VADJ_FMC	IO_L16P_N5P2_M2P32_706
J4	7	PMOD1_IO5	D11	LA05	FMCP1_LA05_P	BF24	SSTL15	706	VADJ_FMC	IO_L5P_N1P4_M2P10_706
J4	8	PMOD1_IO6	C10	LA06	FMCP1_LA06_P	BC20	SSTL15	706	VADJ_FMC	IO_L10P_N3P2_M2P20_706
J4	9	PMOD1_IO7	H13	LA07	FMCP1_LA07_P	BC25	SSTL15	706	VADJ_FMC	IO_L11P_N3P4_M2P22_706
J4	10	PMOD1_IO8	G12	LA08	FMCP1_LA08_P	BC22	SSTL15	706	VADJ_FMC	IO_L8P_N2P4_M2P16_706
J7	2	PMOD2_MOSI	D14	LA09	FMCP1_LA09_P	BE25	SSTL15	706	VADJ_FMC	IO_L7P_N2P2_M2P14_706
J7	3	PMOD2_MISO	C14	LA10	FMCP1_LA10_P	BG25	SSTL15	706	VADJ_FMC	IO_L1P_N0P2_M2P2_706
J7	4	PMOD2_SCK	H16	LA11	FMCP1_LA11_P	BF23	SSTL15	706	VADJ_FMC	IO_L0P_XCC_N0P0_M2P0_706
J7	7	PMOD2_IO5	G15	LA12	FMCP1_LA12_P	BG21	SSTL15	706	VADJ_FMC	IO_L3P_XCC_N1P0_M2P6_706
J7	8	PMOD2_IO6	D17	LA13	FMCP1_LA13_P	BE21	SSTL15	706	VADJ_FMC	IO_L4P_N1P2_M2P8_706
J7	9	PMOD2_IO7	C18	LA14	FMCP1_LA14_P	AU24	SSTL15	706	VADJ_FMC	IO_L13P_N4P2_M2P26_706
J7	10	PMOD2_IO8	H19	LA15	FMCP1_LA15_P	AY22	SSTL15	706	VADJ_FMC	IO_L15P_XCC_N5P0_M2P30_706
J9	1	PMOD3_CS	G18	LA16	FMCP1_LA16_P	BF21	SSTL15	706	VADJ_FMC	IO_L2P_N0P4_M2P4_706
J9	4	PMOD3_SCK	D20	LA17_CC	FMCP1_LA17_CC_P	BB16	SSTL15	707	VADJ_FMC	IO_L6P_GC_XCC_N2P0_M2P66_707
J9	2	PMOD3_MOSI	C22	LA18	FMCP1_LA18_CC_P	BE17	SSTL15	707	VADJ_FMC	IO_L9P_GC_XCC_N3P0_M2P72_707
J9	3	PMOD3_MISO	H22	LA19	FMCP1_LA19_P	BA17	SSTL15	707	VADJ_FMC	IO_L7P_N2P2_M2P68_707
J9	7	PMOD3_IO5	G21	LA20	FMCP1_LA20_P	BE16	SSTL15	707	VADJ_FMC	IO_L8P_N2P4_M2P70_707
J9	8	PMOD3_IO6	H25	LA21	FMCP1_LA21_P	BE19	SSTL15	707	VADJ_FMC	IO_L0P_XCC_N0P0_M2P54_707
J9	9	PMOD3_IO7	G24	LA22	FMCP1_LA22_P	BF18	SSTL15	707	VADJ_FMC	IO_L4P_N1P2_M2P62_707
J9	10	PMOD3_IO8	D23	LA23	FMCP1_LA23_P	BB20	SSTL15	707	VADJ_FMC	IO_L1P_N0P2_M2P56_707

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This pin mapping can translate between the VCK190 and VMK180 boards. There is no difference in pin mapping. The signal voltage is controlled by the VADJ, which is set by the system controller. The default is 1.5V for VADJ and this should never be changed. This must match the I/O standard voltage, otherwise it is possible to cause damage to the I/O. The I/O standard used is typically SSTL15 (see Figure 29), but any 1.5V standard can be used for Pmod compliance. The TXS0108E level translator has a minimum signal voltage of 1.4V, which means only 1.5V I/O standards can be used with this PMOD FMC board.

Appendix D

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

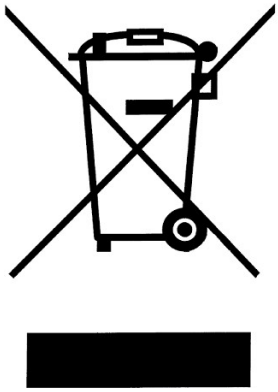
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

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Appendix E

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the VMK180 board and its documentation is available on these websites:

VMK180 Evaluation Kit

VMK180 Evaluation Kit — Master Answer Record 72740

These documents provide supplemental material useful with this guide:

1. *Versal Architecture and Product Data Sheet: Overview* (DS950)
2. *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956)
3. *Versal ACAP Technical Reference Manual* (AM011)
4. *Versal ACAP SelectIO Resources Architecture Manual* (AM010)
5. *Versal ACAP PCB Design User Guide* (UG863)
6. *Versal ACAP Memory Resources Architecture Manual* (AM007)
7. *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002)
8. *Tera Term Terminal Emulator Installation Guide* (UG1036)
9. *Vivado Design Suite User Guide: Using Constraints* (UG903)
10. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
11. *Versal ACAP Integrated Block for PCI Express LogiCORE IP Product Guide* (PG343)
12. *Versal ACAP System Monitor Architecture Manual* (AM006)
13. *Versal ACAP Clocking Resources Architecture Manual* (AM003)
14. *HDMI 1.4/2.0 Transmitter Subsystem Product Guide* (PG235)
15. HDMI Transmitter and Receiver Subsystem Answer Record 70514
16. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
17. VMK180 Software Install and Board Setup Tutorial (XTP629)
18. VMK180 System Controller Tutorial (XTP628)

These websites provide supplemental material useful with this guide:

19. Micron Technology (MTA9ADF1G72AZ-3GE1, MT53D512M32D2DS)
20. Standard Microsystems Corporation (SMSC) (USB3320)
21. SanDisk Corporation
22. SD Association

23. Silicon Labs (SI570, SI5332, SI53340)
24. Texas Instruments (TCA9548A, TCA6416A, DP83867)
25. PCI Express standard
26. Samtec, Inc. (SEAF series connectors, LPAF connectors)
27. VITA FMC Marketing Alliance (FPGA Mezzanine Card (FMC) VITA 57.1, 57.4 specifications)
28. Maxim Integrated Circuits (MAX6643)
29. Infineon Integrated Circuits (IR35215, IRPS5401, IR38164, IR3897)
30. Future Technology Devices International Ltd. (FT4232HL)
31. Integrated Device Technology, Inc. (IDT) (85411AMLF, 8T49N241, 8A34001)
32. SNIA Technology Affiliates (SFF-8431)
33. Nexperia/NXP Semiconductors (SC18IS602)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
03/07/2022 Version 1.1	
Models of Boards	Added kit model EK-VMK180-G.
Versal ACAP Kit Numbering	Modified ED option.
Board Features and Block Diagram	Clarified 72-bit (64-bit, and 8-bit ECC) DDR4 feature and updated the block diagram accordingly.
01/07/2021 Version 1.0	
Initial release.	N/A

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