MP3424A

Configurable-Current, CC/CV, Synchronous Step-Up Converter with Output Disconnect and Minimized Inrush Current

DESCRIPTION

The MP3424A is a synchronous, high-efficiency, current-mode, step-up (boost) converter with output disconnect. The MP3424A targets various load capability boosts from a battery input with an accurate load current limit.

The MP3424A starts up from an input voltage (V_{IN}) as low as 2V while providing inrush current limiting, output short-circuit protection (SCP), and a configurable load current limit. The integrated P-channel synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode. The P-channel MOSFET disconnects the output from the input during shutdown.

The 580kHz switching frequency allows for small external components, while internal compensation and soft start minimize the external component count. The MP3424A provides flexible current limit programming for up to 5V/3.1A load from a supply voltage down to 2.8V.

The MP3424A is available in a QFN-14 (2mmx2mm) package.

FEATURES

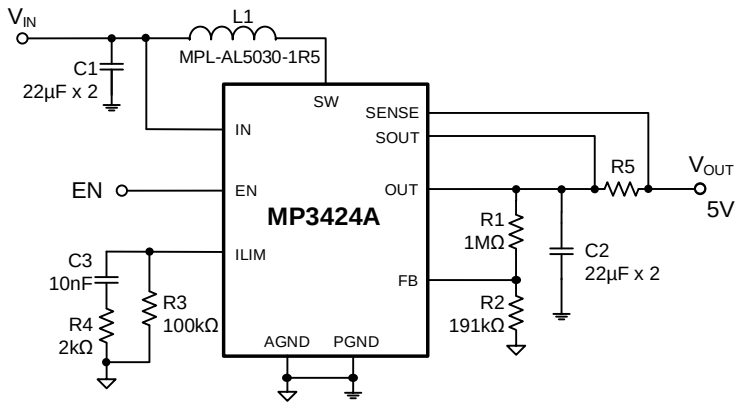
- 2V to 5.5V Operating Input Voltage Range
- 3V to 5.5V Output Range
- Supports 5V/3.1A Output from a 2.8V Input
- 270mA Linear Charge Inrush Current
- Switching Current Limit Configurable Up to 9.5A
- Configurable Average Load Current Limit
- 580kHz Fixed Switching Frequency
- Up to 97% Efficiency
- Internal Soft Start and Compensation
- True Output Load Disconnect from Input
- Over-Current Protection (OCP), Short-Circuit Protection (SCP), and Over-Temperature Protection (OTP)
- Available in a QFN-14 (2mmx2mm) Package

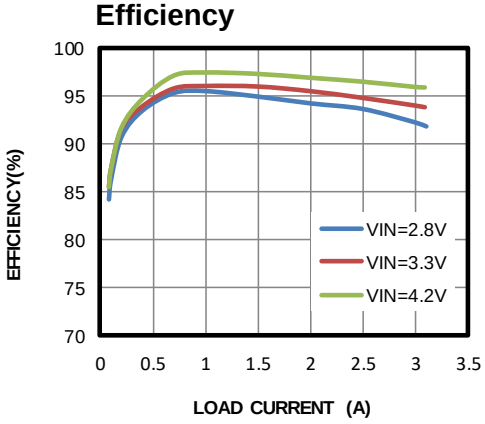
MPL Optimized Performance with MPS Inductor MPL-AL5030 Series

APPLICATIONS

- Battery-Powered Products
- Power Banks, Juice Packs, Battery Backup Units
- Optical Modules
- USB Power Supplies
- Consumer Electronic Accessories

TYPICAL APPLICATION





ORDERING INFORMATION

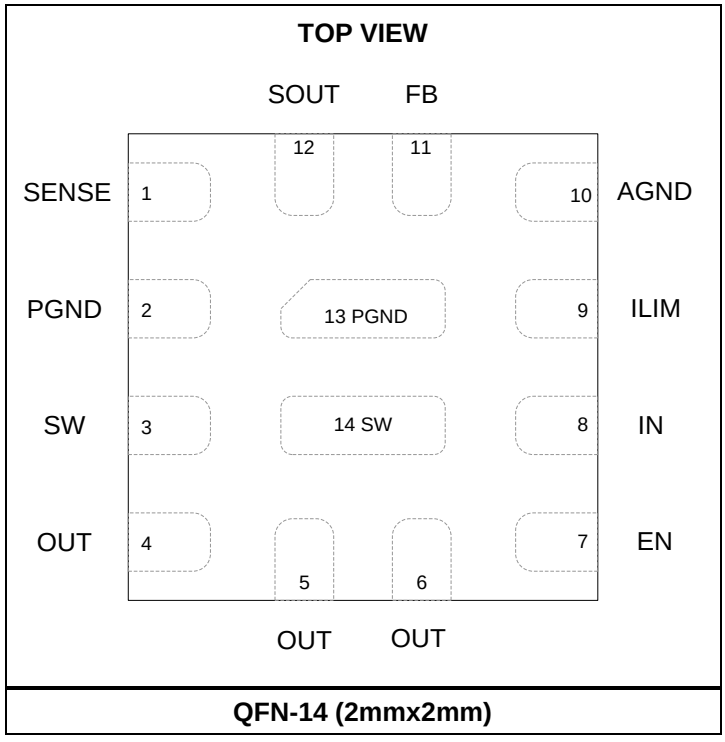
Part Number*	Package	Top Marking	MSL Rating
MP3424AGG	QFN-14 (2mmx2mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP3424AGG-Z).

TOP MARKING

LU: Product code of MP3424AGG
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1	SENSE	**Load current sense.** Connect a load-sense resistor signal between SENSE and SOUT to determine the maximum load current. If average load current limiting is not required, connect SENSE and SOUT directly to OUT.
2, 13	PGND	**Power ground.**
3, 14	SW	**Power switch output.** SW is the connection node of the internal N-channel MOSFET and synchronous P-channel MOSFET. Connect the power inductor between SW and the input power. Keep the PCB trace lengths as short and wide as possible to reduce EMI and voltage spikes.
4, 5, 6	OUT	**Output.** OUT is the drain of the internal synchronous rectifier MOSFET. The bias is derived from OUT when V_{OUT} exceeds V_{IN}. Keep the PCB trace length from OUT to the output filter capacitor as short and wide as possible. OUT is completely disconnected from IN when EN is low due to the output disconnect feature.
7	EN	**Chip enable control input.**
8	IN	**Power supply input.** The start-up bias is derived from IN. IN must be bypassed locally. Once OUT exceeds IN, the bias is derived from OUT. Once started, operation is completely independent from IN.
9	ILIM	**Switching current limit set.** A resistor from ILIM to AGND programs the low-side MOSFET (LS-FET) cycle-by-cycle peak current limit when the output constant load current limit is not triggered. When the output current (I_{OUT}) signal between SOUT and SENSE exceeds the current limit threshold, ILIM is pulled low to regulate the average load current. RC compensation is required in this condition. If average load current limiting is not required, RC compensation can be removed, and only a resistor from ILIM to AGND is required.
10	AGND	**Analog signal ground.**
11	FB	**Feedback input to the error amplifier (EA).** Connect a resistor divider tap to FB. The output voltage (V_{OUT}) can be adjusted from 3V to 5.5V.
12	SOUT	**Load current sense.** Connect a load-sense resistor signal between SOUT and SENSE to determine the maximum load current. If average load current limiting is not required, connect SENSE and SOUT directly to OUT.

ABSOLUTE MAXIMUM RATINGS (1)

SW pin.....-0.3V to +6.5V (10V for <5ns)
All other pins.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
.....2.55W (4)
Junction temperature.....150°C
Lead temperature.....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM).....2000V
Charged device model (CDM).....1500V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2V to 5.5V
V_{OUT} ..... 3V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (2mmx2mm)			
EVL3424A-G-00A (4)	49	14	°C/W
JESD51-7 (5)	80	16	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVL3424A-G-00A, 2-layer, 64mmx64mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J = -40°C to 125°C [6], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Voltage Range						
Quiescent current	I_Q	V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, V_{FB} = 0.85V, no switching, measured on OUT		320		µA
		V_{EN} = V_{IN} = 3.3V, V_{OUT} = 5V, V_{FB} = 0.85V, no switching, measured on IN		13.5		µA
Shutdown current	I_{SD}	V_{EN} = V_{OUT} = 0V, measured on IN, T_J = 25°C		0.1	1	µA
IN UVLO rising threshold	$V_{UVLO\_IN\_R}$	V_{IN} rising, V_{OUT} = 0V, T_J = 25°C		1.2	1.45	V
IN UVLO falling threshold	$V_{UVLO\_IN\_F}$	V_{IN} falling, V_{OUT} = 5V		0.61		V
V_{OUT} start switching rising threshold	$V_{UVLO\_OUT\_R}$			1.7	1.95	V
Step-Up Converter						
Operation frequency	f_{SW}	T_J = 25°C	500	580	660	kHz
		-40°C ≤ T_J ≤ +125°C	460	580	700	
Feedback voltage reference	V_{FB}	T_J = 25°C	794	805	816	mV
		-40°C ≤ T_J ≤ +125°C	790	805	820	mV
Feedback input current	I_{FB}	V_{FB} = 850mV		1	50	nA
N-channel MOSFET on resistance	$R_{NDS(ON)}$			11		mΩ
N-channel MOSFET leakage current	I_{N_LK}	V_{SW} = 5V		0.1		µA
P-channel MOSFET on resistance	$R_{PDS(ON)}$			17		mΩ
P-channel MOSFET leakage current	I_{P_LK}	V_{SW} = 5V, V_{OUT} = 0V		0.1		µA
Maximum duty cycle	D_{MAX}		90	95		%
Linear charge current limit	I_{CH_LIMIT}	V_{IN} = 3.3V, V_{OUT} = 1.2V		0.27	0.42	A
N-channel MOSFET current limit [7]	I_{SW_LIMIT}	R_{ILIM} = 100kΩ, V_{IN} = 3V, V_{OUT} = 5V		9.5		A
OUT average current limit threshold	V_{OCL}		26.5	30	33.5	mV
Logic Interface						
EN high-level voltage	V_{EN_H}	Rising	1.2			V
EN low-level voltage	V_{EN_L}	Falling			0.4	V
EN input current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal shutdown [7]				150		°C
Thermal shutdown hysteresis [7]				20		°C

Notes:

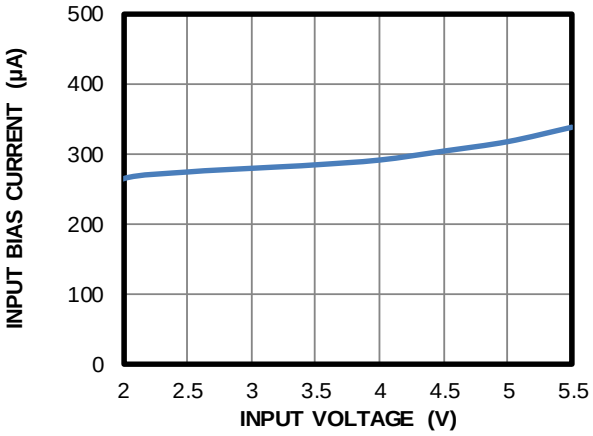
6) Guaranteed by over-temperature correlation. Not tested in production.
7) Guaranteed by sample characterization. Not tested in production.

TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

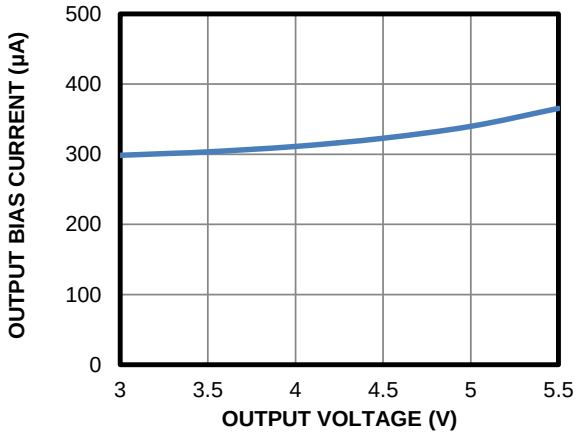
Input Bias Current vs. Input Voltage

$V_{IN} > V_{OUT}$



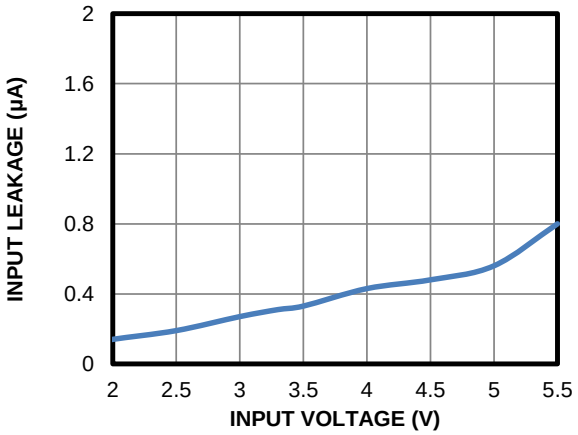
Output Bias Current vs. Output Voltage

$V_{OUT} > V_{IN}$

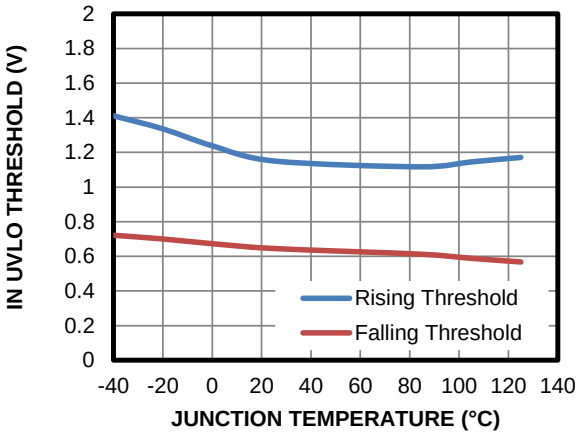


Input Leakage Current vs. Input Voltage

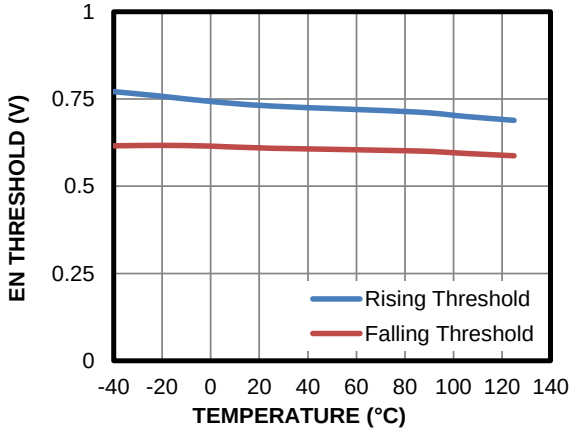
EN = low



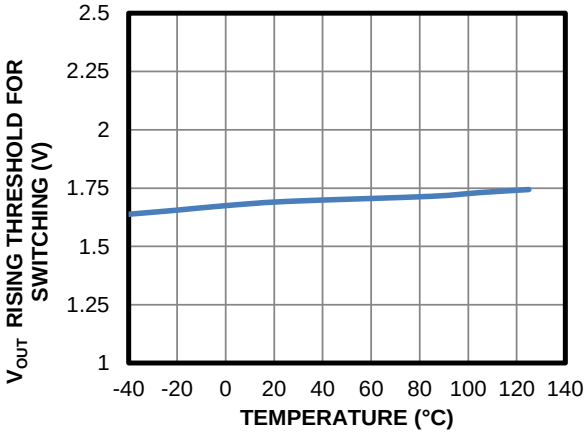
IN UVLO Threshold vs. Temperature



EN Threshold vs. Temperature



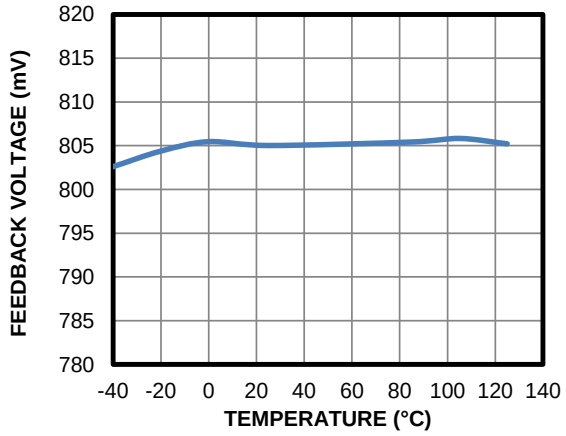
V_{OUT} Rising Threshold for Switching vs. Temperature



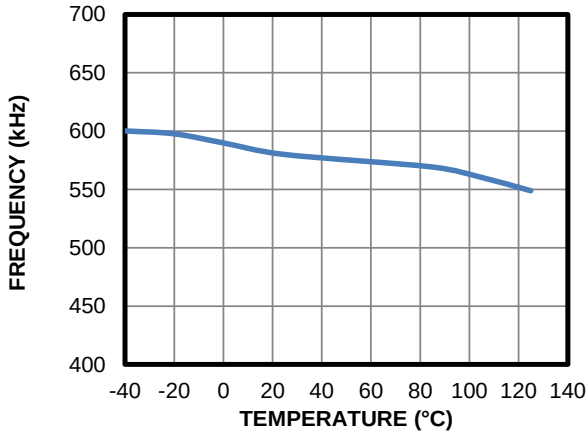
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

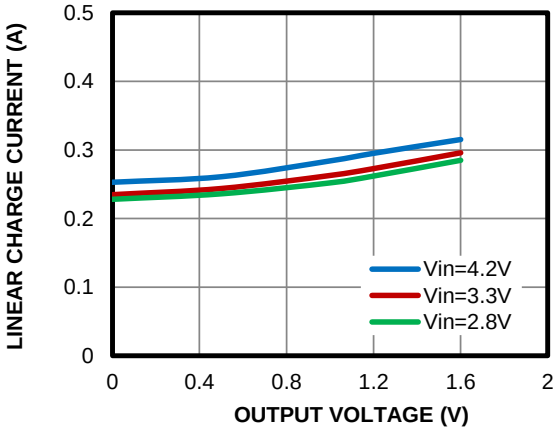
Feedback Voltage vs. Temperature



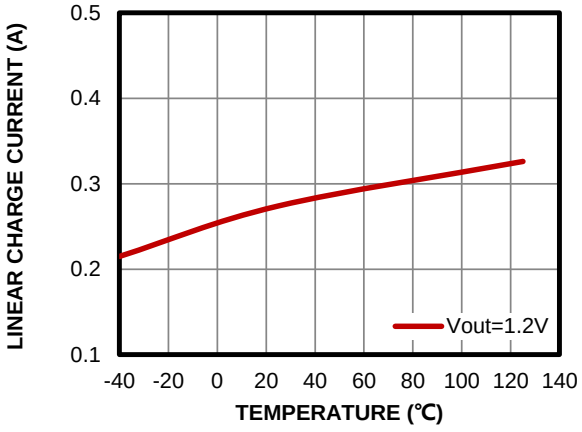
Frequency vs. Temperature



Linear Charge Current vs. Output Voltage

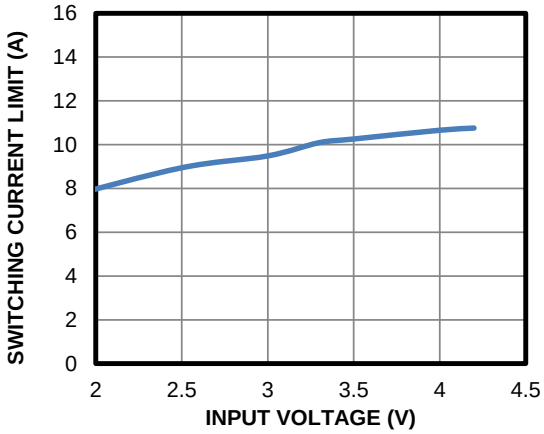


Linear Charge Current vs. Temperature

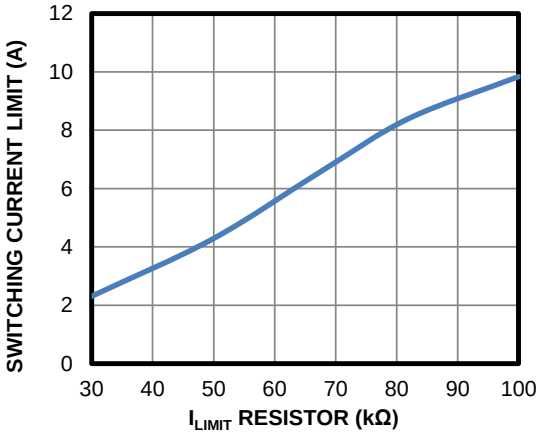


Switching Current Limit vs. Input Voltage

R_{LIMIT} = 100kΩ



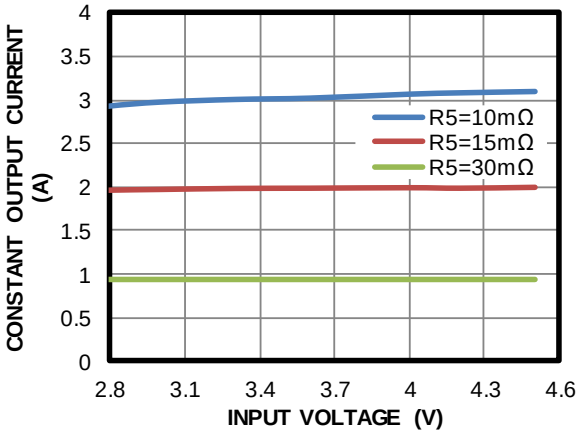
Switching Current Limit vs. I_{LIMIT} Resistor



TYPICAL CHARACTERISTICS *(continued)*

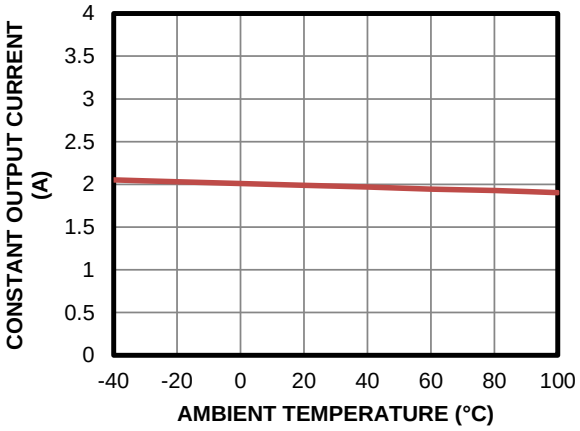
V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Constant Output Current vs. Input Voltage



Constant Output Current vs. Ambient Temperature

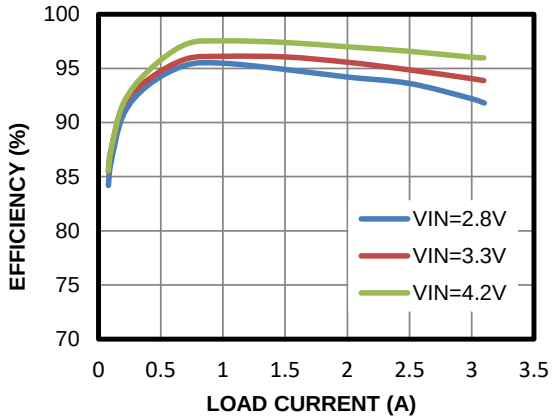
R5 = 15mΩ



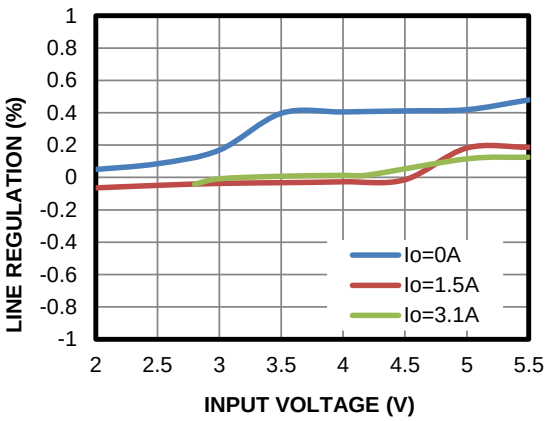
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

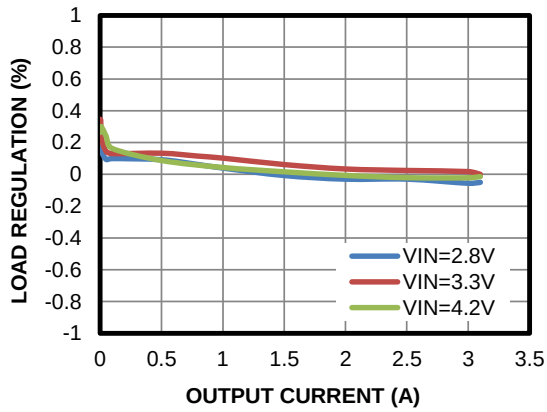
Efficiency vs. Load Current



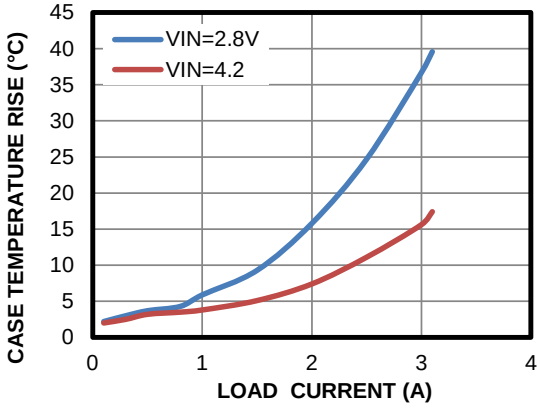
Line Regulation vs. Input Voltage



Load Regulation vs. Output Current



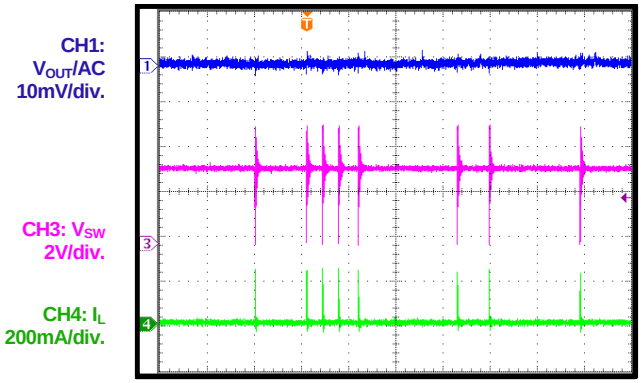
Case Temperature Rise vs. Load Current



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

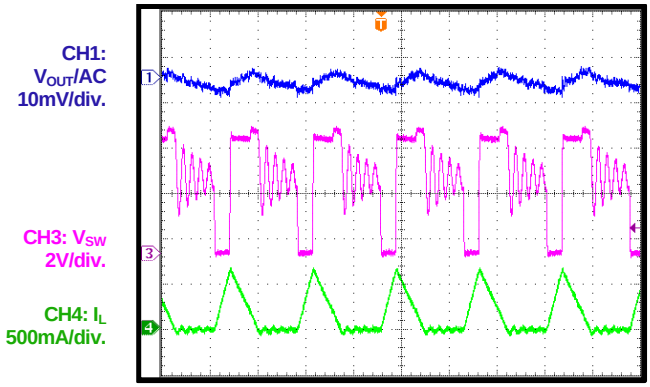
V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Output Voltage Ripple
Load = 0A



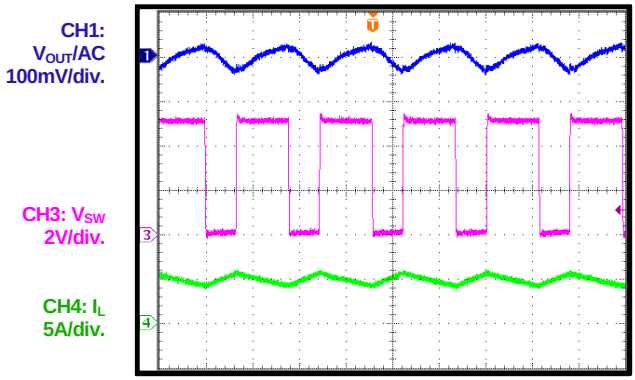
20µs/div.

Output Voltage Ripple
Load = 0.1A



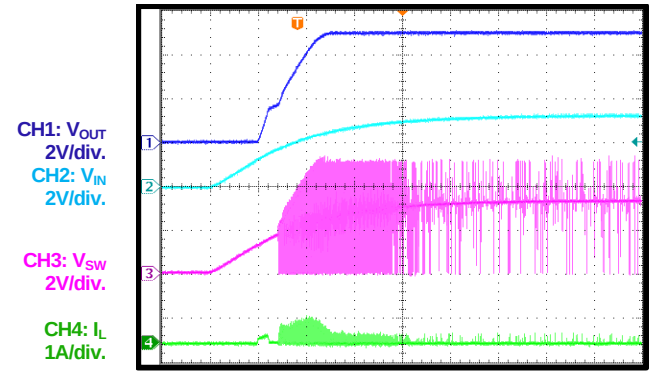
1µs/div.

Output Voltage Ripple
Load = 3.1A



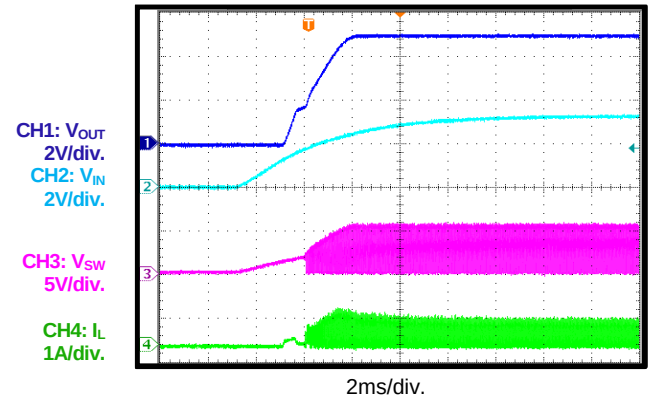
1µs/div.

Start-Up through VIN
Load = 0A



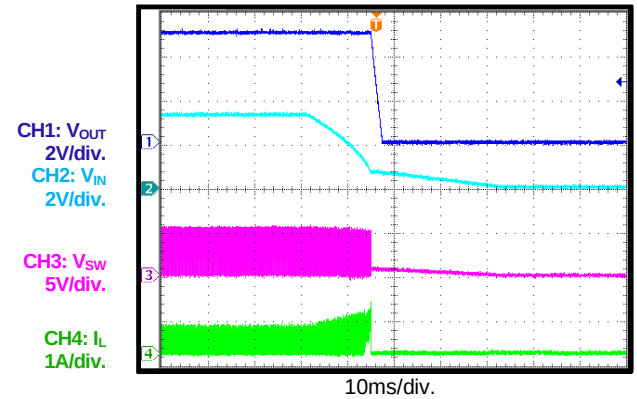
2ms/div.

Start-Up through VIN
Load = 0.1A



2ms/div.

Shutdown through VIN
Load = 0.1A



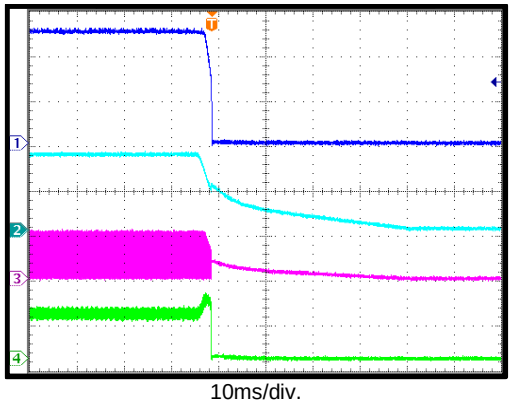
10ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

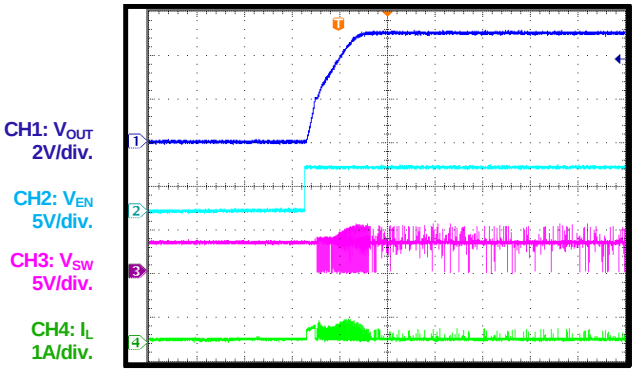
Load = 3.1A



10ms/div.

Start-Up through EN

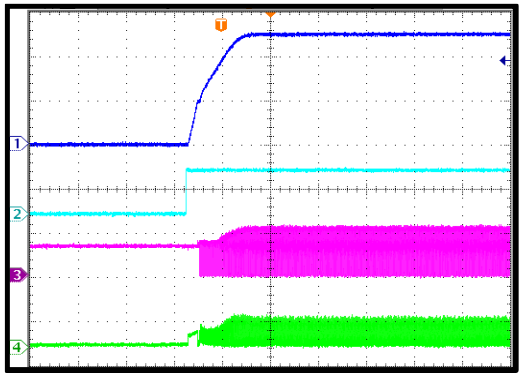
Load = 0A



2ms/div.

Start-Up through EN

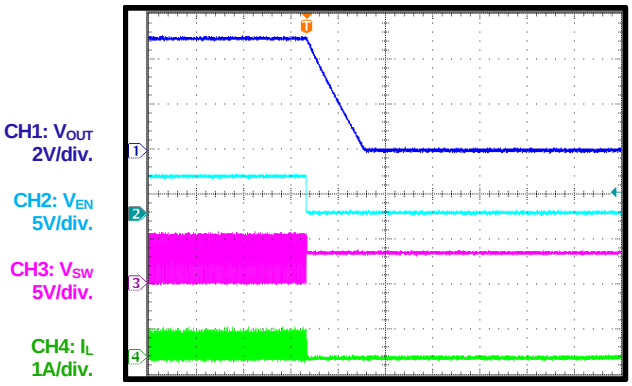
Load = 0.1A



2ms/div.

Shutdown through EN

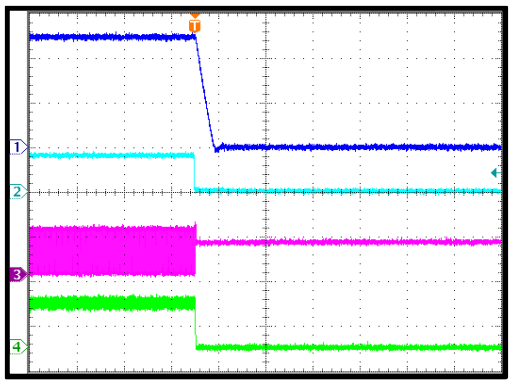
Load = 0.1A



2ms/div.

Shutdown through EN

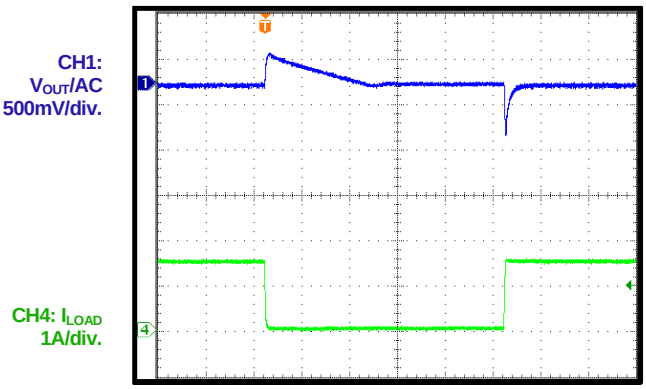
Load = 3.1A



200µs/div.

Load Transient

I_{LOAD} = 0A to 1.5A at 150mA/µs



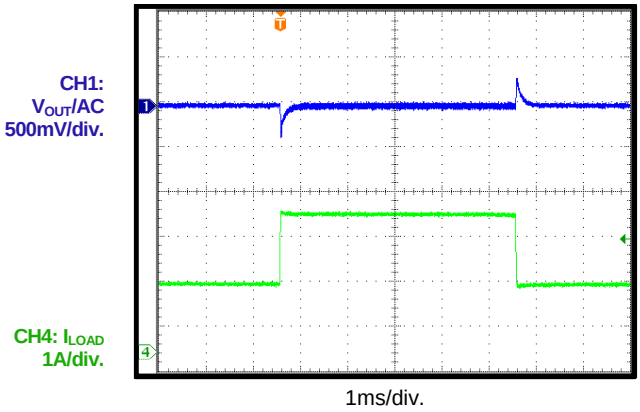
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

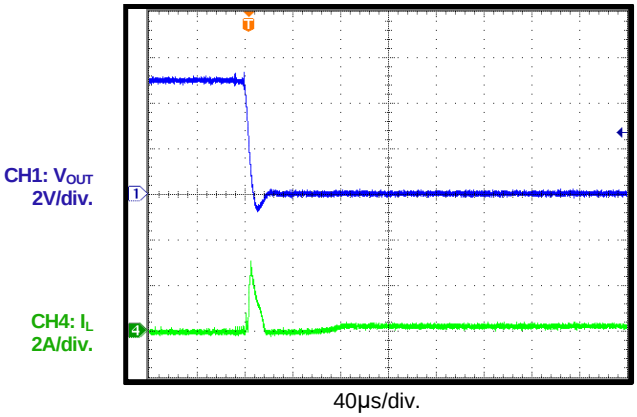
Load Transient

I_{LOAD} = 1.5A to 3.1A at 150mA/µs



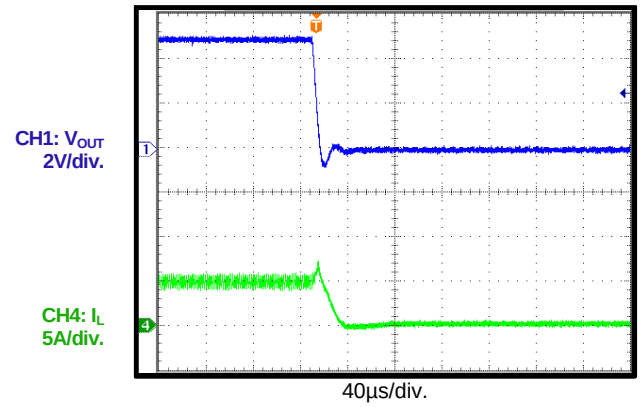
Short-Circuit Entry

0A load to short



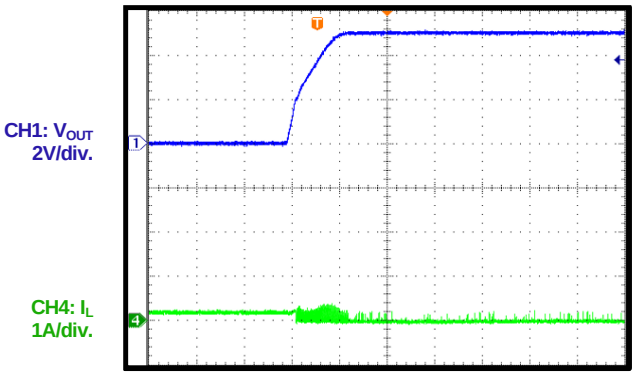
Short-Circuit Entry

3.1A load to short



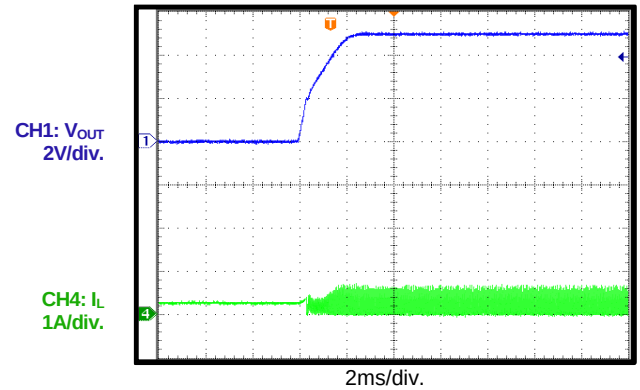
Short-Circuit Recovery

Recover to 0A load



Short-Circuit Recovery

Recover to 0.1A load



FUNCTIONAL BLOCK DIAGRAM

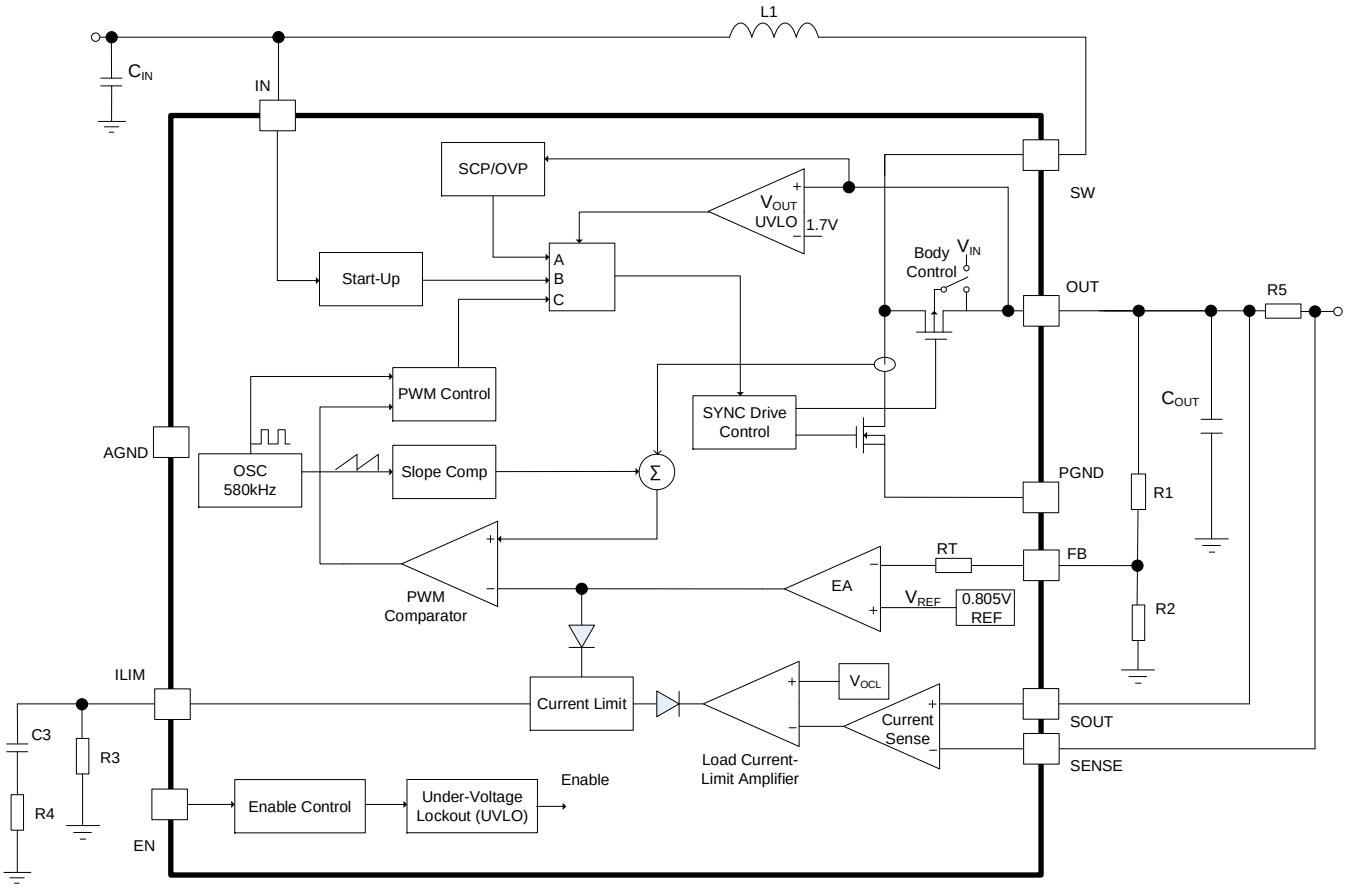


Figure 1: Functional Block Diagram

OPERATION

The MP3424A is a 580kHz, synchronous, step-up (boost) converter with true output disconnect in a QFN-14 (2mmx2mm) package. The device features fixed-frequency current mode pulse-width modulation (PWM) control for excellent line and load regulation. The special voltage loop and current loop provide flexibility for voltage regulation and overload protection. The special voltage loop offers linear charging and step-down mode to control the output start-up. The current loop includes a configurable current limit and a cycle-by-cycle current limit, which help protect the IC. Internal soft start and loop compensation simplify the design process and minimize the external component count. Internal low $R_{DS(ON)}$ MOSFETs enable the device to maintain high efficiency across a wide load current range.

Start-Up

When the IC is enabled and the IN voltage (V_{IN}) exceeds $V_{UVLO\_IN\_R}$, the MP3424A starts up in linear charge mode. During this linear charge period, the rectifier P-channel MOSFET (P-FET) turns on until the output capacitor is charged to 1.7V. The P-FET current is limited to 0.27A to avoid inrush current. This circuit also helps limit the output current (I_{OUT}) under short-circuit conditions.

Once the output is charged to 1.7V, the linear charge period ends, and the MP3424A begins switching in normal closed-loop operation. In normal operation, if the output voltage (V_{OUT}) is below the input voltage (V_{IN}) + 0.3V, then the MP3424A operates in step-down mode. If V_{OUT} is above V_{IN} + 0.3V, the MP3424A operates in boost mode. The switching current limit in both step-down mode and boost mode are programmed by R_{ILIM}, which is located between ILIM and GND. R_{ILIM} must always be below 100kΩ. Figure 2 and Table 1 show the operation mode and current limit during the start-up process.

Table 1: Operation Mode during Start-Up

V_{OUT} < 1.7V	Linear charge mode
V_{OUT} ≥ 1.7V, V_{OUT} < V_{IN} + 0.3V	Step-down mode
V_{OUT} ≥ 1.7V, V_{OUT} ≥ V_{IN} + 0.3V	Boost mode

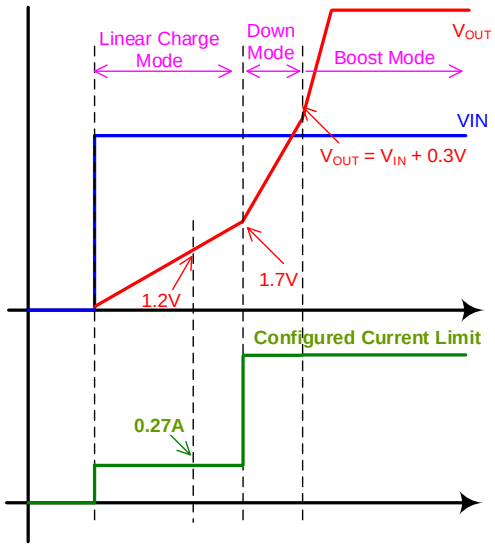


Figure 2: Current Limit and Operation Mode during Start-Up

In step-down mode, the gate of the high-side MOSFET (HS-FET) is pulled to V_{IN} and operates with a high impedance when the HS-FET is on. During step-down mode, the power loss is high. Step-down mode is designed to work during start-up and short-circuit protection (SCP). It is not recommended to operate the MP3424A in step-down mode for normal operation, unless the system performance will not be affected by the rise in temperature.

When V_{OUT} exceeds V_{IN}, the MP3424A powers the internal circuits from V_{OUT} instead of V_{IN}.

Soft Start (SS)

The MP3424A provides soft start (SS) by charging an internal capacitor with a current source. This soft-start voltage (V_{SS}) rises in proportion with the FB voltage (V_{FB}) during a linear charge period. Once the linear charge period elapses, the voltage on this capacitor is charged by a fixed internal current, and the reference voltage (V_{REF}) ramps up slowly. The reference soft-start time (t_{SS}) is typically 3ms (0V to 0.805V).

In the event of a commanded shutdown, thermal shutdown, or a short circuit at the output, the soft-start capacitor (C_{SS}) is discharged completely.

Device Enable (EN)

Pull the EN pin high to enable the MP3424A; pull it low to shut down the MP3424A. When the device is shut down, the regulator stops switching, all internal control circuitry turns off, and the load is isolated from the input.

Error Amplifier (EA)

The error amplifier (EA) is an internally compensated amplifier. The EA compares the internal 0.805V reference voltage (V_{REF}) against V_{FB} to generate an error signal. V_{OUT} can be adjusted by an external resistor divider.

Output Disconnect

The MP3424A offers true output disconnect by eliminating body diode conduction of the internal P-FET rectifier. This allows V_{OUT} to drop to 0V during shutdown, or for V_{IN} to be isolated when maintaining an external bias on V_{OUT}. This limits the inrush current limit at start-up, minimizing surge current seen by the input supply. To maintain the advantages of output disconnect, there must not be an external Schottky diode connected between SW and V_{OUT}.

Overload and Short-Circuit Protection (SCP)

When overload occurs, the inductor current (I_L) is limited cycle by cycle, and V_{OUT} drops. If V_{OUT} drops below V_{IN} + 0.3V, then the MP3424A runs back into step-down mode. When V_{OUT} drops below 1.7V, the MP3424A operates in linear charge mode.

At the same time, if V_{OUT} drops below 50% of the nominal output voltage, the MP3424A treats this as a short-circuit condition and shuts down immediately. After 40µs, the MP3424A exits short-circuit protection (SCP) and restarts with a new start-up cycle. If V_{OUT} exceeds 50% of the setting voltage under overload conditions, the MP3424A does not treat this as a short-circuit condition. The current is only controlled by cycle-by-cycle switching current limiting or an output current-sense resistor. See the Constant Output Current Limit section below for details on accurate current limit setting.

Constant Output Current Limit

The MP3424A integrates programmable current limit functions, including cycle-by-cycle current limiting and output load current limiting.

By connecting ILIM to AGND through a resistor, the MP3424A limits the low-side MOSFET (LS-FET) current cycle by cycle. The switching peak current can be configured by changing R_{ILIM}. The load current capability is affected by V_{IN}, V_{OUT}, and the inductance (L).

By inserting a sense resistor between the output capacitor and load terminal, the MP3424A can sense and limit the load current flowing through the current-sense resistor. The limited load current is 30mV / R_{SENSE} (R5 in Figure 1 on page 12). When the load current limit is triggered, the ILIM voltage (V_{ILIM}) is pulled low internally, which controls I_L, regulating the average load current. When using an output-sense resistor, RC compensation is required on ILIM.

Different load current limits can be achieved by changing R_{ILIM} or the output-sense resistor value. To set the average current limit, connect a 100kΩ resistor from ILIM to AGND and change the average current-sense resistor on the output port.

If load current limiting is not required, connect the SENSE and SOUT pins directly to OUT, and remove the RC compensation on ILIM.

The switching current signal is blanked for 70ns internally to enhance noise rejection. The average load current limit does not respond to the load change quickly due to the low-pass filter.

Over-Voltage Protection (OVP)

If V_{OUT} exceeds 6.5V, boost switching stops. This prevents an over-voltage (OV) condition from damaging the internal power MOSFET. When V_{OUT} drops below 6.5V, the device resumes switching automatically.

Thermal Shutdown

The MP3424A contains an internal temperature monitor. The switches turn off if the die temperature exceeds 150°C. Once the die temperature drops below 130°C, the device resumes normal operation.

APPLICATION INFORMATION

Setting the Output Voltage

V_{OUT} is fed back to the EA through a resistor divider. The feedback reference voltage (V_{REF}) is typically 0.805V. Calculate V_{OUT} with Equation (1):

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (1)$$

Where R1 is the top feedback resistor, R2 is the bottom feedback resistor, and V_{REF} is the reference voltage (typically 0.805V).

Set the values of R1 and R2 as high as necessary to achieve a low quiescent current. Note that setting the resistance too high can lead to noise and a low loop bandwidth. R1 should be between 600kΩ and 1MΩ for good leakage, stability, and transient balance.

Selecting the Current Limit Resistor

Peak Switching Current Limit

The MP3424A limits the LS-FET cycle-by-cycle current with a current-limit resistor (R_{ILIM}). The switching peak current can be configured by changing R_{ILIM}.

Load Average Current Limit

The MP3424A senses and limits the load current flowing through the current-sense resistor. R_{SENSE} is connected from the output capacitor to the load terminal and sets the load current limit (I_{OCL}). Estimate R_{SENSE} with Equation (2):

$$I_{OCL} = V_{OCL} / R_{SENSE} \quad (2)$$

Where V_{OCL} is typically 30mV, I_{OCL} is the load current limit (in A), and R_{SENSE} is the sense resistor (in Ω) (R5 in Figure 1 on page 12).

Use an RC compensation net on ILIM to regulate the stable load current limit loop. It is recommended to use a 2kΩ resistor and 10nF capacitor.

Input Capacitor Selection

Low-ESR input capacitors reduce input switching noise and the peak current drawn from the battery. Ceramic capacitors are recommended for input decoupling, and should be placed as close to the device as possible. Use a ceramic capacitor above 22µF to restrain the input voltage ripple.

Selecting the Output Capacitor

The output capacitor requires a minimum 22µF capacitance of at the configured V_{OUT} to ensure stability across the entire operating range. A higher capacitance may be required to lower the output ripple and transient ripple. Use low-ESR capacitors such as X5R or X7R ceramic capacitors. Assuming the ESR is 0, the minimum output capacitance (C_{OUT}) to support the ripple in PWM mode can be calculated using Equation (3):

$$C_{OUT} \geq \frac{I_{OUT} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_{SW} \times V_{OUT(MAX)} \times \Delta V} \quad (3)$$

Where $V_{OUT(MAX)}$ is the maximum output voltage, $V_{IN(MIN)}$ is the minimum input voltage, I_{OUT} is the output current, f_{SW} is the switching frequency, and ΔV_{OUT} is the acceptable output voltage ripple.

It is recommended to place a 1µF ceramic capacitor between OUT and PGND to reduce spikes on the SW node and improve EMI performance.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL5030 Series**

The MP3424A can utilize small surface-mount chip inductors due to its 580kHz f_{SW}. Inductor values between 1µH and 2.2µH are suitable for most applications. Larger inductances allow for slightly greater I_{OUT} capability; however, reducing the inductor ripple current also increases component size. Calculate the minimum inductance (L) with Equation (4):

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \times \Delta_L \times f_{SW}} \quad (4)$$

Where ΔI_L is the acceptable inductor current ripple.

The inductor current ripple is typically set to be between 30% and 40% of the average I_L. The inductor should have a low DCR to reduce resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL	1µH to 2.2µH	MPS
MPL-AL5030-1R5	1.5µH	MPS
MPL-AL5030-1R0	1µH	MPS
MPL-AL5030-2R2	2.2µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Design Example

Table 3 shows a design example following the application guidelines for the described specifications.

Table 3: Design Example

V_{IN}	2.8V to 4.2V
V_{OUT}	5V
I_{OUT}	3.1A

Figure 4 on page 18 shows the detailed application schematic. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the output capacitor as close to OUT and PGND as possible.
2. Place a small decoupling capacitor in parallel with the bulk output capacitor, and as close to OUT as possible. This is very important to reduce the spikes on SW and improve EMI performance.
3. Place the input capacitor and inductor as close to IN and SW as possible.
4. Keep the trace between the inductor and SW as wide and short as possible.
5. Keep the feedback (FB) loop far away from all noise sources, such as SW.
6. Place the feedback resistor dividers as close to FB and AGND as possible.
7. Connect the current-sense traces (SOUT and SENSE) from the sense resistor pad, and route them in close parallel with a small closed area, far away from noise sources such as the SW trace.
8. Place the ILIM set and compensation net close to ILIM and AGND.
9. Tie the ground return of the input and output capacitors as close to PGND as possible with a large copper GND area.
10. Place vias around GND to lower the die temperature.

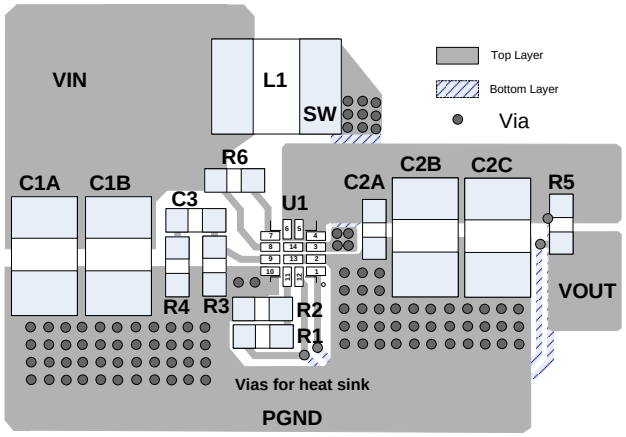


Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

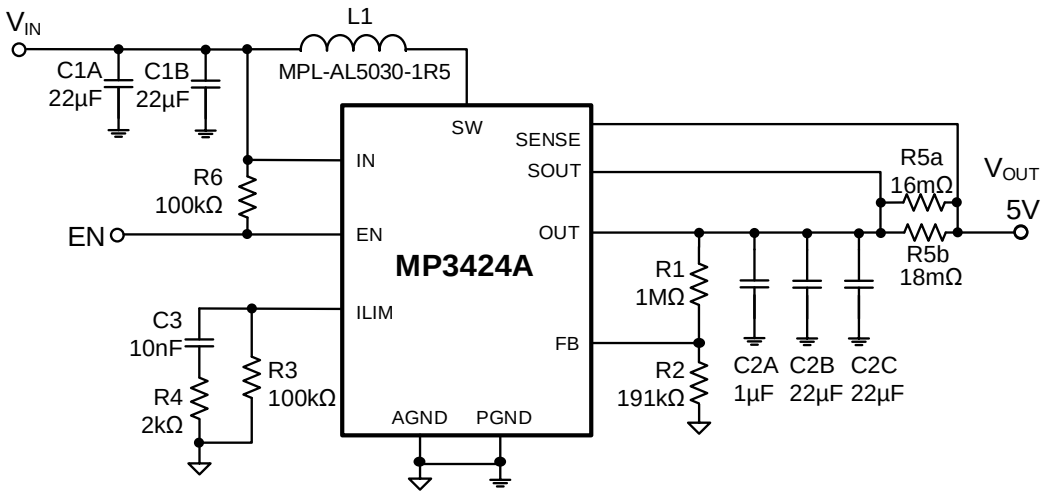


Figure 4: Typical Boost Circuit with Average Load Current Limit (V_{IN} = 2V to 4.2V, V_{OUT} = 5V)

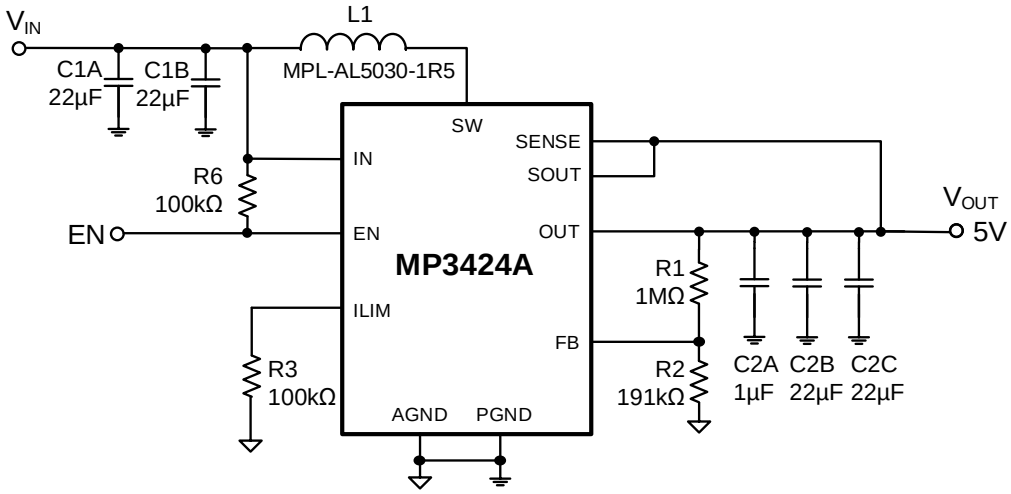
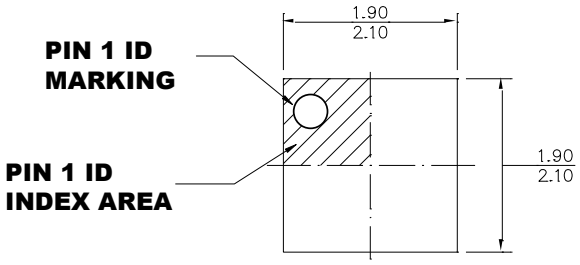


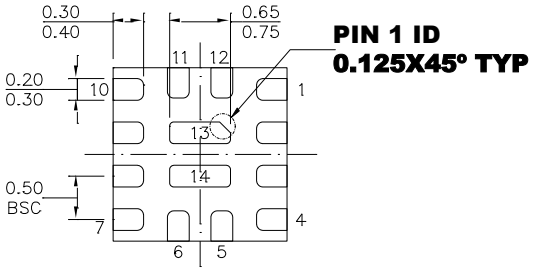
Figure 5: Typical Boost Circuit without Average Load Current Limit (V_{IN} = 2V to 4.2V, V_{OUT} = 5V)

PACKAGE INFORMATION

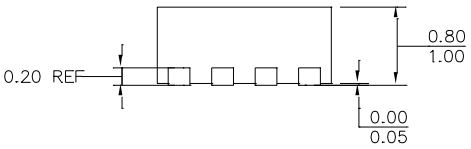
QFN-14 (2mmx2mm)



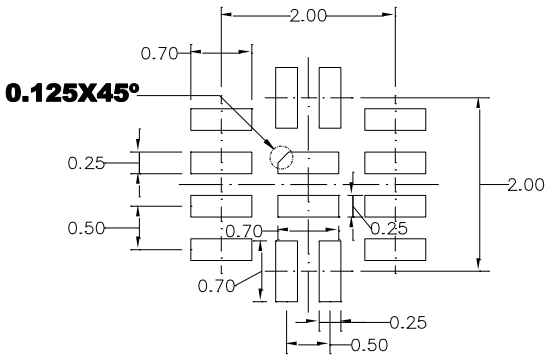
TOP VIEW



BOTTOM VIEW



SIDE VIEW

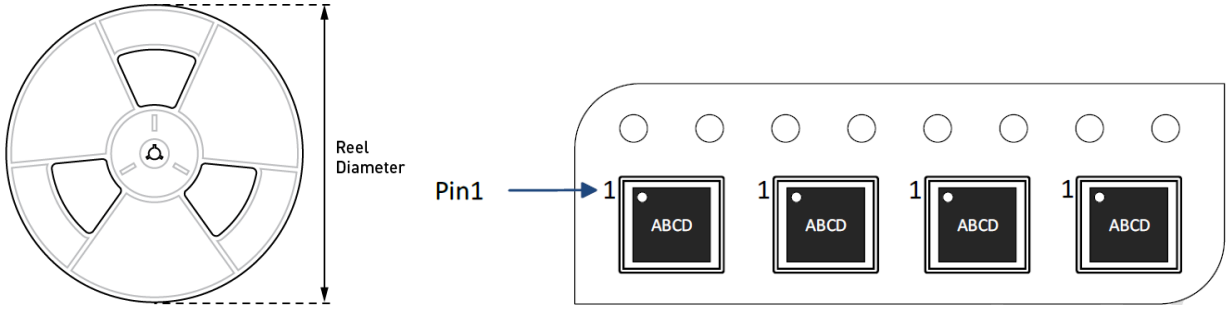


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3424AGG-Z	QFN-14 (2mmx2mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	06/22/2021	Initial Release	-