Lead-free Green

PI7C9X2G304SV

PCI EXPRESS GEN 2 PACKET SWITCH

3-Port, 4-Lane, ExtremeLo PCIe2.0 Packet Switch

DATASHEET

REVISION 9

August 2022

A Product Line of
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REVISION HISTORY

Date	Revision Number	Description
02/08/2017	0.1	Preliminary Datasheet
07/11/2018	1	Reg40h[15:8] next item point to 4ch for both up/downport port MSI register are for both up&downport, not downport only anymore Multiple Message Capable modify form 3b'001 to 3'b010 Update 74h[7], 8Ch[7][12]. Update 340h[4][5] Add cfg offset 300h to 314h Update 8Ch[12] Add cfg offset 318h and 31Ch Update 98h[15:0] Update REG[9c]: trigger[6:3], clear[2], port[1:0], and REG[a0] Update Ini for REG[98][15:0] = 0126 Add cfg offset B0h to FFh Delete Misc Control 5 (offset 314h) Updated section 14 Ordering Information Updated 7.2.54 OPERATION MODE –OFFSET 98h Added Fig 13-3 Part Marking Update Feature Add Chap 6.2 and 6.3 Add Chap 13 Update Table 9-3 Update Table 12-1
10/23/2018	2	Updated Section 1 Features Updated Section 12.4 Power Consumption
12/26/2018	3	Updated 3.2 PORT CONFIGURATION SIGNALS Updated Section 7.2.125 MISC CONTROL 0 REGISTER – OFFSET 300h Updated Section 7.2.126 MISC CONTROL 1 REGISTER – OFFSET 304h Updated Section 10 POWER MANAGEMENT Updated Section 12.1 Absolute Maximum Ratings
02/20/2019	4	New revision number due to document control process
09/11/2019	5	Updated Section 12.4 Power Consumption Updated Section 15 Ordering Information
10/24/2019	6	Updated Section 1 Features Updated Section 3.1 PCI Express Interface Signals Updated Table 5-2 Receiver Signal Detect Threshold Updated Figure 14-2 Part Marking
07/21/2020	7	Updated Section 8 Clock Scheme Updated Section 5-1 Physical Layer Circuit Updated Table 6-1, 6-3, 6-5 and 6-6 Updated Figure 6-6 and 6-9 Updated Section 6.1.4 and 7.2.2 Updated Notes for Table 12-2 DC Electrical Characteristics
12/15/2020	8	For Datasheet Status Change
08/10/2022	9	Updated Section 1 FEATURES Updated Section 3.1 PCI EXPRESS INTERFACE SIGNALS Updated Table 5-3 Updated Section 7.2.47 PHY PARAMETER 2 – OFFSET 7Ch Updated Section 7.2.50 XPIP_CSR5 – OFFSET 88h Updated Section 7.2.68 LINK CONTROL REGISTER – OFFSET D0h Updated Section 8 Clock Scheme Updated Figure 14-1 Package Outline Drawing Updated Figure 14-2 Part Marking Updated 6.1.3 EEPROM Space Address Map Updated 6.1.4 Mapping EEPROM Contents to Configuration Updated Table 6-1, 6-3 and 6-5 Removed MEMORY ECC ERROR MASK AND STATUS Register Updated Section 15 Ordering Information

Date	Revision Number	Description
		Updated Section 7.2.51 TL_CSR0 – OFFSET 8Ch Added Section 7.2.138 DEBUGOUT CONTROL – OFFSET 348h Added Section 7.2.139 DEBUGOUT DATA – OFFSET 34Ch

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1 FEATURES

- 4-lane PCI Express® Gen 2 Switch with 3 PCI Express ports
- Supports "Cut-through"(Default) as well as "Store and Forward" mode for packet switching
- Peer-to-peer switching between any two downstream ports
- 150 ns typical latency for packet routed through Switch without blocking
- Integrated reference clock for downstream ports
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Compliant with System Management (SM) Bus, Version 1.0
- Compliant with *PCI Express Base Specification Revision 2.1*
- Compliant with *PCI Express CEM Specification Revision 2.0*
- Compliant with *PCI-to-PCI Bridge Architecture Specification Revision 1.2*
- Compliant with *Advanced Configuration Power Interface (ACPI) Specification*
- Reliability, Availability and Serviceability
    - Supports Data Poisoning and End-to-End CRC
    - Advanced Error Reporting and Logging
    - IEEE 1149.1 JTAG interface support
- Advanced Power Saving
    - Empty downstream ports are set to idle state to minimize power consumption
- Link Power Management
    - Supports L0, L0s, L1, L2, L2/$L3_{Ready}$ and L3 link power states
    - Supports PCI-PM L1.1 and ASPM L1.1 of L1 PM Sub-state
    - Active state power management for L0s and L1 states
- Device State Power Management
    - Supports D0, $D3_{Hot}$ and $D3_{Cold}$ device power states
    - 3.3V Aux Power support in $D3_{Cold}$ power state
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability
    - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
    - Disabled VCs' buffer is assigned to enabled VCs for resource sharing
    - Independent TC/VC mapping for each port
    - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
    - Isochronous traffic class mapped to VC1 only
    - Strict time based credit policing
- Supports up to 512-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Support Access Control Service (ACS) for peer-to-peer traffic
- Support Address Translation (AT) packet for SR-IOV application
- Support OBFF and LTR
- Support Surprise Hot-Plug (DPC)
- Low Power Dissipation: 300 mW typical in L0 normal mode
- Industrial Temperature Range -40º to 85ºC
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- 128-pin LQFP 14mm x 14mm package

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
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2 GENERAL DESCRIPTION

Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 4-Lane PCIe Switch is in 3-Port type configuration. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs.

In the PCI Express Architecture, the PCIE Switch forwards posted and non-posted requests, and completion packets in either downstream or upstream direction concurrently as if a virtual PCI Bridge is in operation on each port. By visualizing the port as a virtual Bridge, the Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges. Similar to a PCI Bridge during enumeration, each port is given a unique bus number, device number, and function number by the initiating software. The bus number, device number, and function number are combined to form a destination ID for each specific port. In addition to that, the memory-map and IO address ranges are exclusively allocated to each port as well. After the software enumeration is finished, the packets are routed to the dedicated port based on the embedded address or destination ID. To ensure the packet integrity during forwarding, the Switch is not allowed to split the packets to multiple small packets or merge the received packets into a large transmit packet. Also, the IDs of the requesters and completers are kept unchanged along the path between ingress and egress port.

The Switch employs the architecture of Combined Input and Output Queue (CIOQ) in implementation. The main reason for choosing CIOQ is that the required memory bandwidth of input queue equals to the bandwidth of ingress port rather than increasing proportionally with port numbers as an output queue Switch does. The CIOQ at each ingress port contains separate dedicated queues to store packets. The packets are arbitrated to the egress port based on the PCIe transaction-ordering rule. For the packets without ordering information, they are permitted to pass over each other in case that the addressed egress port is available to accept them. As to the packets required to follow the ordering rule, the Head-Of-Line (HOL) issue becomes unavoidable for packets destined to different egress ports since the operation of producer-consumer model has to be retained; otherwise the system might occur hang-up problem. On the other hand, the Switch places replay buffer at each egress port to defer the packets before sending it out. This can assure the maximum throughput being achieved and therefore the Switch works efficiently. Another advantage of implementing CIOQ in PCIe Switch is that the credit announcement to the counterpart is simplified and streamlined because of the credit-based flow control protocol. The protocol requires that each ingress port maintains the credits independently without checking other ports' credit availability, which is otherwise required by pure output queue architecture.

The Switch supports two virtual channels (VC0, VC1) and eight traffic classes (TC0 ~ TC7) at each port. The ingress port independently assigns packets into the preferred virtual channel while the egress port outputs the packet based on the predefined port and VC arbitration algorithm. For instance, the isochronous packet is given a special traffic class number other than TC0 and mapped into VC1 accordingly. By employing the strict time based credit policy for port arbitration and assigning higher priority to VC1 than VC0, the Switch can therefore guarantee the time-sensitive packet is not blocked by regular traffic to assure the quality of service. In addition, some data-centric applications only carry TC0/VC0 traffic. As a result, there are no packets that would consume VC1 bandwidth. In order to improve the efficiency of buffer usage, the unused VC1 queues can be reassigned to VC0 and enable each of the ingress ports to handle more data traffic bursts. This virtual channel resource relocation feature enhances the performance of the PCIe Switch further.

The Switch provides the advanced feature of Access Control Service (ACS). This feature regulates which components are allowed to communicate with each other within the PCIe multiple-point fabric, and allows the system to have more control over packet routing in the Switch. As a result, peer-to-peer traffic can be facilitated more accurately and efficiently. When the system also implements Address Translation Service (ATS), the peer-to-peer requests with translated address can be routed directly by enabling the corresponding option in ACS to avoid possible performance bottleneck associated with re-direction, which introduces extra latency and may increase link and RC congestion.

The built-in Integrated Reference Clock Buffer of the PCI Express Switch supports four reference clock outputs. The clock buffer is from a single 100MHz clock input, and distributes the clock source to three outputs, which can be used by the downstream PCI Express end devices. The clock buffer feature can be enabled and disabled by strapping pin setting.

The DIODES™ PI7C9X2G304SV supports various types of power management ranged from device state, link state to platform-wise power saving mechanism. For device state, the D0, D1, D2, D3-hot, and D3-cold power states represent different amount of power dissipation in PI7C9X2G304SV. As to link state, each link of the PI7C9X2G304SV supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L2/L3 power states. In addition, PCI-PM L1.1 of L1 PM Sub-state and device-specific L2/L3 are implemented to reduce power consumption further.

3 PIN DESCRIPTION

3.1 PCI EXPRESS INTERFACE SIGNALS

NAME	PIN	TYPE	DESCRIPTION
REFCLKP REFCLKN	110, 111	I	**Reference Clock Input Pair:** Connect to 100MHz differential clock when integrated reference clock buffer is disabled (CLKBUF_PD=1), or connect to one of the Integrated Reference Clock Output Pairs (REFCLKO_P and REFCLKO_N) of this Switch when integrated reference clock buffer is enabled (CLKBUF_PD=0). The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.
PERP [3:0]	122, 102, 97, 128	I	**PCI Express Data Serial Input Pairs:** Differential data receive signals in four ports. Port 0 (Upstream Port) Lane 0 is PERP[0] and PERN[0] Port 0 (Upstream Port) Lane 1 is PERP[3] and PERN[3] Port 1 (Downstream Port) is PERP[1] and PERN[1] Port 2 (Downstream Port) is PERP[2] and PERN[2]
PERN [3:0]	121, 103, 98, 127	I	
PETP [3:0]	118, 106, 100, 124	O	**PCI Express Data Serial Output Pairs:** Differential data transmit signals in four ports. Port 0 (Upstream Port) Lane 0 is PETP[0] and PETN[0] Port 0 (Upstream Port) Lane 1 is PETP[3] and PETN[3] Port 1 (Downstream Port) is PETP[1] and PETN[1] Port 2 (Downstream Port) is PETP[2] and PETN[2]
PETN [3:0]	117, 107, 101, 123	O	
PERST_L	10	I	**System Reset (Active LOW):** When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized. Please refer to Table 12-2 for PERST_L spec.
DWNRST_L[2:1]	6, 5	O	**Downstream Device Reset (Active LOW):** DWNRST_L provides a reset signal to the devices connected to the downstream ports of the switch. The signal is active when either PERST_L is asserted or the device is just plugged into the switch. DWNRST_L [x] corresponds to Portx, where x= 1,2.
REXT	116	I	**External Reference Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry.
REXT_GND	115	I	**External Reference Resistor Ground:** Connect to an external resistor to REXT.
REFCLKI_P, REFCLKI_N	74, 73	I	**Integrated Reference Clock Input Pair:** Connect to external 100MHz differential clock for the integrated reference clock buffer.
REFCLKO_P[2:0]	78, 81, 85	O	**Integrated Reference Clock Output Pairs:** 100MHz external differential HCSL clock outputs for the integrated reference clock buffer.
REFCLKO_N[2:0]	77, 80, 83	O	
CLKBUF_PD	60	I	**Reference Clock Output Pairs Power Down:** When CLKBUF_PD is asserted high, the integrated reference clock buffer and Reference Clock Outputs are disabled. When it is asserted low, the integrated reference clock buffer and Reference Clock Outputs are enabled. This pin has internal pull-down. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.

3.2 PORT CONFIGURATION SIGNALS

NAME	PIN	TYPE	DESCRIPTION
VC1_EN	18	I	**Virtual Channel 1 Resource Sharing Enable:** The chip provides the capability to support virtual channel 1 (VC1), in addition to the standard virtual channel 0. When this pin is asserted high, Virtual Channel 1 is enabled, and virtual channel resource sharing is not available. When it is asserted low, the chip would allocate the additional VC1 resource to VC0, and VC1 capability is disabled. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.
RXPOLINV_DIS	24	I	**Rx Polarity Inversion Disable:** When RXPOLINV_DIS is asserted high, it indicates to disable Rx Polarity Inversion detection function. Otherwise, it indicates to enable Rx Polarity Inversion detection function. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.
PL_512B	53	I	**Max. Payload Size 512B:** When PL_512B is asserted high, it indicates the max. payload size capability is 512B. Otherwise, it indicates the max. Payload size is 256B. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.
PRSNT[2:1]	20, 19	I	**Present:** When PRSNT is asserted low, it indicates that the device is present in the slot of downstream port. Otherwise, it indicates the absence of the device. PRSNT[x] is correspondent to Port x, where x=1,2. These pins have internal pull-down resistors. If no board trace is connected to these pins, the internal pull-down resistors of these pins are enough. However, if pins are connected to a board trace and not driven, it is recommended that external 330-ohm pull-down resistors be used.
SLOTCLK	33	I	**Slot Clock Configuration:** It determines if the downstream component uses the same physical reference clock that the platform provides on the connector. When SLOTCLK is high, the platform reference clock is employed. This pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.
SLOT_IMP[2:1]	46, 45	I	**Slot Implemented:** These signals are asserted to indicate that the downstream ports are connected to slots. SLOT_IMP[x] corresponds to Portx, where x=1,2. When SLOT_IMP[x] is asserted, the Portx is connected to slot. Otherwise, it is chip-to-chip connection directly. These pins have internal pull-down resistors. If no board trace is connected to these pins, the internal pull-down resistors of these pins are enough. However, if pins are connected to a board trace and not driven, it is recommended that external 330-ohm pull-down resistors be used.
CLKREQ_L[2:0] / PORTSTATUS[2:0]	69, 68, 67	I/O / O	**Clock Request (Active Low):** When PORTSTATUS_L1.1_SEL is set LOW, the chip provides the capability to support PM L1 Substate, which requires a side-band clock request signal to control reference clock and PLL. When de-asserted, both of reference clock and PLL are turned off for entering PM L1 Substate to save power. When asserted, the reference clock becomes valid to enable PLL and power state exits L1 Substate. Please refer to Section 8 Clock Scheme. **Port Status:** When PORTSTTUS_L1.1_SEL is set HIGH, these signals indicate the status of each port. Please connect to pin header for debug used. PORTSTATUS[x] is correspondent to Port x, where x=0,1,2.

3.3 MISCELLANEOUS SIGNALS

NAME	PIN	TYPE	DESCRIPTION
EECLK	70	O	**EEPROM Clock:** Clock signal to the EEPROM interface.
EEPD	*71	I/O	**EEPROM Data:** Bi-directional serial data interface to and from the EEPROM. EEPROM Bypass(EEPROM_BYPASS): During system initialization, EEPD acts as the EEPROM_BYPASS pin. When tied low, eeprom function is disabled. When tied high, eeprom function is enabled. The pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.
SMBCLK	26	I	**SM Bus Clock:** System management Bus Clock. This pin requires an external 5.1K-ohm pull-up resistor.
SMBDATA	27	I/O	**SM Bus Data:** Bi-Directional System Management Bus Data. This pin requires an external 5.1K-ohm pull-up resistor.
SCAN_EN	72	I/O	**Full-Scan Enable Control:** For normal operation, SCAN_EN is an output with a value of “0”. SCAN_EN becomes an input during manufacturing testing.
GPIO[7:0]	44, 43, 42, 39, 38, 37, 35, 36	I/O	**General Purpose Input and Output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register. When SMBus is implemented, GPIO[7:5] act as the SMBus address pins, which set Bit 2 to 0 of the SMBus address. **Debug Mode Selection:** In debug mode, GPIO[4:0] are used for Debug Mode Selection.
PWR_SAV	28	I	**Power Saving Mode:** When PWR_SAV is asserted high, power saving mode is enabled. Otherwise, it power saving mode is disabled. This pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.
PORTSTATUS_ L1.1_SEL	22	I	**PortStatus_L1.1_SEL:** When tied low, L1.1 function is enabled. When tied high, PortStatus output mode is enabled. The pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.
SMBUS_EN	54	I	**System Manage Bus Enable:** Select either SMBUS or I2C protocol. When tied low, I2C protocol is selected. When tied high, SMBUS protocol is chosen. The pin has internal pull-down resistor. If no board trace is connected to this pin, the internal pull-down resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 330-ohm pull-down resistor be used.
TEST3 TEST5 TEST6	17 25 51	I	**Test3/5/6:** These pins are for internal test purpose. Test3, Test5 and Test6 should be tied to ground through a 330-ohm pull-down resistor.
TEST1	9	I	**Test1:** The pin is for internal test purpose. It should be tied to 3.3V through a 5.1K-ohm pull-up resistor for normal operation. **Debug Mode Enable**: In debug mode, it need be tired to low through a 330-ohm pull-down resistor.
TEST2	16	I	**Test2:** The pin is for internal test purpose. Test2 should be tied to 3.3V through a 5.1K-ohm pull-up resistor.
NC	7, 21, 47, 48, 52, 57, 58, 59, 75, 76, 86, 114		**Not Connected:** These pins can be just left open.

3.4 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN	TYPE	DESCRIPTION
TCK	89	I	**Test Clock:** Used to clock state information and data into and out of the chip during boundary scan. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TMS	92	I	**Test Mode Select:** Used to control the state of the Test Access Port controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor.
TDO	88	O	**Test Data Output:** Used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDI	93	I	**Test Data Input:** Used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TRST_L	94	I	**Test Reset (Active LOW):** Active LOW signal to reset the TAP controller into an initialized state. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor.

3.5 POWER PINS

NAME	PIN	TYPE	DESCRIPTION
VDDC	3, 23, 29, 31, 40, 55, 62, 65, 91	P	**VDDC Supply (1.0V):** Used as digital core power pins.
VDDR	1, 8, 49, 64, 96	P	**VDDR Supply (3.3V):** Used as digital I/O power pins.
CVDDR	79, 82, 84	P	**VDDR Supply (3.3V):** Used as reference clock power pins.
VDDCAUX	13, 14	P	**VDDCAUX Supply (1.0V):** Used as auxiliary core power pins.
VAUX	15	P	**VAUX Supply (3.3V):** Used as auxiliary I/O power pins.
AVDD	99, 105, 108, 119, 125	P	**AVDD Supply (1.0V):** Used as PCI Express analog power pins.
AVDDH	113	P	**AVDDH Supply (3.3V):** Used as PCI Express analog high voltage power pins.
CGND	109, 112	P	**Ground:** Used as reference clock ground pins.
VSS	2, 4, 11, 12, 30, 32, 34, 41, 50, 56, 61, 63, 66, 87, 90, 95, 104, 120, 126,129	P	**VSS Ground:** Used as ground pins.

4 PIN ASSIGNMENTS

4.1 PIN LIST of 128-PIN LQFP

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VDDR	33	SLOTCLK	65	VDDC	97	PERP[1]
2	VSS	34	VSS	66	VSS	98	PERN[1]
3	VDDC	35	GPIO[1]	67	CLKREQ_L[0]	99	AVDD
4	VSS	36	GPIO[0]	68	CLKREQ_L[1]	100	PETP[1]
5	DWNRST_L[1]	37	GPIO[2]	69	CLKREQ_L[2]	101	PETN[1]
6	DWNRST_L[2]	38	GPIO[3]	70	EECLK	102	PERP[2]
7	NC	39	GPIO[4]	71	EEPD	103	PERN[2]
8	VDDR	40	VDDC	72	SCAN_EN	104	VSS
9	TEST1	41	VSS	73	REFCLKI_N	105	AVDD
10	PERST_L	42	GPIO[5]	74	REFCLKI_P	106	PETP[2]
11	VSS	43	GPIO[6]	75	NC	107	PETN[2]
12	VSS	44	GPIO[7]	76	NC	108	AVDD
13	VDDCAUX	45	SLOT_IMP[1]	77	REFCLKO_N[2]	109	CGND
14	VDDCAUX	46	SLOT_IMP[2]	78	REFCLKO_P[2]	110	REFCLKP
15	VAUX	47	NC	79	CVDDR	111	REFCLKN
16	TEST2	48	NC	80	REFCLKO_N[1]	112	CGND
17	TEST3	49	VDDR	81	REFCLKO_P[1]	113	AVDDH
18	VC1_EN	50	VSS	82	CVDDR	114	NC
19	PRSNT[1]	51	TEST6	83	REFCLKO_N[0]	115	REXT_GND
20	PRSNT[2]	52	NC	84	CVDDR	116	REXT
21	NC	53	PL_512B	85	REFCLKO_P[0]	117	PETN[3]
22	PORTSTATUS_L1.1_SEL	54	SMBUS_EN	86	NC	118	PETP[3]
23	VDDC	55	VDDC	87	VSS	119	AVDD
24	RXPOLINV_DIS	56	VSS	88	TDO	120	VSS
25	TEST5	57	NC	89	TCK	121	PERN[3]
26	SMBCLK	58	NC	90	VSS	122	PERP[3]
27	SMBDATA	59	NC	91	VDDC	123	PETN[0]
28	PWR_SAV	60	CLKBUF_PD	92	TMS	124	PETP[0]
29	VDDC	61	VSS	93	TDI	125	AVDD
30	VSS	62	VDDC	94	TRST_L	126	VSS
31	VDDC	63	VSS	95	VSS	127	PERN[0]
32	VSS	64	VDDR	96	VDDR	128	PERP[0]
129	E_PAD						

5 FUNCTIONAL DESCRIPTION

Multiple virtual PCI-to-PCI Bridges (VPPB), connected by a virtual PCI bus, reside in the Switch. Each VPPB contains the complete PCIe architecture layers that consist of the physical, data link, and transaction layer. The packets entering the Switch via one of VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer. The following sections describe these function elements for processing PCIe packets within the Switch.

5.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the PHY Interface for PCI Express Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the Switch, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

5.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the PHY Parameter 2 Register (offset 7Ch, bit[6:4]) as listed in Table 5-1, which can be configured by EEPROM or SMBUS settings.

Table 5-1 Receiver Detection Threshold Settings

Receiver Detection Threshold	Threshold
000	1.0 us
001	2.0 us
010	4.0 us (Recommended)
011	5.0 us
100	10 us
101	20 us
110	40 us
111	50 us

5.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the PHY Parameter 2 Register (Offset 7Ch, bit[21:20]) as listed in Table 5-2, which can be configured on a per-port basis via EEPROM or SMBUS settings.

[1] Multiple lanes could share the PLL.

Table 5-2 Receiver Signal Detect Threshold

Receiver Signal Detect	Min (mV ppd)	Max (mV ppd)
00	50	150
01 (Recommended)	65	175
10	75	200
11	120	240

5.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the PHY Parameter 2 Register (Offset 7Ch, bit[25:22]) as listed in Table 5-3, which can be configured on a per-port basis via EEPROM or SMBUS settings.

Table 5-3 Receiver Equalization Settings

Receiver Equalization	Equalization
0000 (Recommended)	Off
0010	Low
0110	Medium
1110	High

5.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the PHY Parameter 2 Register (offset 7Ch, Bit[30]) is used for the selection of full swing signaling or half swing signaling, which can be configured on a per-port basis via EEPROM or SMBUS settings.

Table 5-4 Transmitter Swing Settings

Transmitter Swing	Mode	De-emphasis
0	Full Voltage Swing	Implemented
1	Half Voltage Swing	Not implemented

5.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the Switch Operation Mode Register (offset 74h) and one of the Drive De-Emphasis Base Level fields in the PHY Parameter 1 Register (offset 7Ah) are active for configuration of the amplitude and de-emphasis.

The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.
The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 5-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

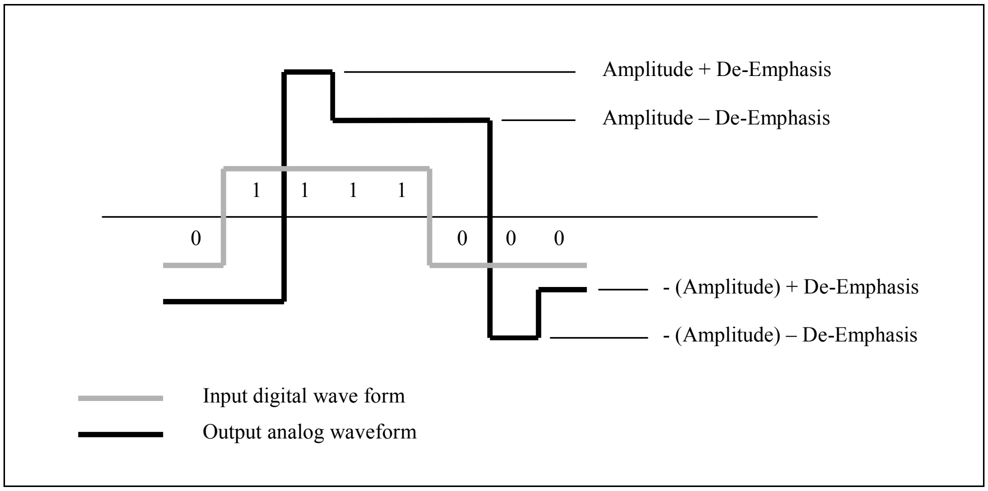


Figure 5-1 Driver Output Waveform

5.1.6 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the Switch Operation Mode Register (offset 74h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 5-5 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in Table 5-6, which can be configured by EEPROM or SMBUS settings.

Table 5-5 Drive Amplitude Base Level Registers

Active Register	De-Emphasis Condition	Swing Condition
C_DRV_LVL_3P5_NOM	-3.5 db	Full
C_DRV_LVL_6P0_NOM	-6.0 db	Full
C_DRV_LVL_HALF_NOM	N/A	Half

Table 5-6 Drive Amplitude Base Level Settings

Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)
00000	0	00111	175	01110	350
00001	25	01000	200	01111	375
00010	50	01001	225	10000	400
00011	75	01010	250	10001	425
00100	100	01011	275	10010	450
00101	125	01100	300	10011	475
00110	150	01101	325	Others	Reserved

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

5.1.7 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the PHY Parameter 1 Register (Offset 78h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 5-7 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 5-8, which can be configured globally via EEPROM or SMBUS settings.

Table 5-7 Drive De-Emphasis Base Level Register

Register	De-Emphasis Condition
C_EMP_POST_GEN1_3P5_NOM	-3.5 db
C_EMP_POST_GEN2_3P5_NOM	-3.5 db
C_EMP_POST_GEN2_6P0_NOM	-6.0 db

Table 5-8 Drive De-Emphasis Base Level Settings

Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)
00000	0.0	01011	69.0	10110	137.5
00001	6.0	01100	75.0	10111	144.0
00010	12.5	01101	81.0	11000	150.0
00011	19.0	01110	87.0	11001	156.0
00100	25.0	01111	94.0	11010	162.5
00101	31.0	10000	100.0	11011	169.0
00110	37.5	10001	106.0	11100	175.0
00111	44.0	10010	112.5	11101	181.0
01000	50.0	10011	119.0	11110	187.5
01001	56.0	10100	125.0	11111	194.0
01010	62.5	10101	131.0	-	-

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

5.1.8 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the PHY Parameter 2 Register (Offset 7Ch, bit[3:0]), which can be configured by EEPROM or SMBUS settings.

5.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.
In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes de-skew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

5.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping (see section 5.5), and it validates the correctness of the transaction type and format. If the TLP is found to contain an illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

5.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

If the incoming packet cannot be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

5.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that TC0 traffic is mapped into VC0 channel by default. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the appropriate VC0 and VC1 queues.

5.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD. Except NPHD, each virtual channel (VC0 or VC1) has its own corresponding packet header and data queue. When only VC0 is needed in some applications, VC1 can be disabled and its resources assigned to VC0 by asserting VC1_EN (Virtual Channel 1 Enable) to low.

5.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers. There are two PH queues for VC0 and VC1 respectively.

5.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue. There are two PD queues for VC0 and VC1 respectively.

5.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data. There is only one NPHD queue for VC0, since non-posted request cannot be mapped into VC1.

5.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there are no 4-DW completion headers. There are two CPLH queues for VC0 and VC1 respectively.

5.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue. There are two CPLD queues for VC0 and VC1 respectively.

5.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 5-9 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels. Since the transactions with the same TC label are not allowed to map into different virtual channels, it implies no ordering relationship between the traffic in VC0 and VC1.

Table 5-9 Summary of PCI Express Ordering Rules

Row Pass Column	**Posted Request**	**Read Request**	**Non-posted Write Request**	**Read Completion**	**Non-posted Write Completion**
Posted Request	Yes/No[1]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Read Request	No[2]	Yes	Yes	Yes	Yes
Non-posted Write Request	No[2]	Yes	Yes	Yes	Yes
Read Completion	Yes/No[3]	Yes	Yes	Yes	Yes
Non-Posted Write Completion	Yes[4]	Yes	Yes	Yes	Yes

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can

be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ‘‘pull’’ ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older bridges, which do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue

5.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which incoming packets to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC channel. It means that each port has two port arbitration circuitries for VC0 and VC1 respectively. At the upstream ports, in addition to the inter-port packets, the intra-port packet such as configurations completion would also join the arbitration loop to get the service from Virtual Channel 0.

5.9 VC ARBITRATION

After port arbitration, VC arbitration is executed among different VC channels within the same source. Three arbitration algorithms are provided to choose the appropriate VC: Strict Priority, Round Robin or Weighted Round Robin.

5.10 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this Switch, each port has its own separate queues for different traffic types and the credits are sent to data link layer on the fly. The data link layer compares the current available credits with the monitored ones and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent the link from entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. The output port broadcasts them to all the other ingress ports to get packet transmission.

5.11 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packets when the local resource (i.e. configuration register) is accessed, and regenerate the message that terminates at receiver to RC if acting as an upstream port.

5.12 ACCESS CONTROLS SERVICE

Traditionally, the packet routing between the peer-to-peer downstream ports is determined by either the address or ID field embedded in the packet header. ACS provides a mechanism for customer to selectively control access between PCI Express Endpoints attached to the downstream ports of packet switch. If ACS is enabled in the ingress port, the peer-to-peer packet forwarding will follow the rule sets of ACS rather than the destination ID or address. ACS is implemented as a set of capabilities and control registers in the associated hardware component. It brings the following benefits such as preventing the silent data corruption presented in Requests from being incorrectly routed to a peer Endpoint, validating every Request transaction between two downstream components and enabling direct routing of peer-to-peer Memory Requests whose addresses have been Translated when ATS system is being used.

6 EEPROM INTERFACE AND SYSTEM MANAGEMENT BUS

The EEPROM interface consists of two pins: EECLK (EEPROM clock output) and EEPD (EEPROM bi-directional serial data). The Switch may control an ISSI IS24C04 or compatible parts using into 512x8 bits. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PERST_L is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies a 7-bit EEPROM word address. The Switch does not control the EEPROM address input. It can only access the EEPROM with address input set to 0.

The System Management Bus interface consists of two pins: SMBCLK (System Management Bus Clock input) and SMBDATA (System Management Bus Data input/ output).

6.1 EEPROM INTERFACE

6.1.1 AUTO MODE EERPOM ACCESS

The Switch may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

6.1.2 EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [3] offset DCh (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '0' which indicates that the autoload initialization sequence is complete.

6.1.3 EEPROM SPACE ADDRESS MAP

15 – 8	7 – 0	BYTE OFFSET
EEPROM Signature (1516h)		00h
Vendor ID		02h
Device ID		04h
Extended VC Count / Link Capability / Switch Mode Operation / Interrupt pin for Port 1 ~ 2		06h
Subsystem Vender ID		08h
Subsystem ID		0Ah
Max_Payload_Size Support / ASPM Support / Role_Base Error Reporting / RefClk ppm Difference		0Ch
Global PHY TX Margin Parameter for Port 0~2		0Eh
Global PHY Parameter 0 for Port 0~2		10h
Global XPIP_CSR6[0] / Global PHY Parameter 1 for Port 0~2		12h
Global XPIP_CSR6[4:1] / Global PHY Parameter 2/3 for Port 0~2		14h
Global XPIP_CSR4[15:0] for Port 0~2		16h
Global XPIP_CSR4[31:16] for Port 0~2		18h
Global XPIP_CSR5[15:0] for Port 0~2		1Ah
Buffer_ctrl[4:0] / Globe XPIP_CSR6[7:5] for Port 0~2	Global XPIP_CSR5[23:16] for Port 0~2	1Ch
MAC_CTR / Global PHY Parameter 3 for Port 0~2		1Eh
NFTS / Deskew Mode Select / Scramble / XPIP_CSR2 for Port 0		20h
NFTS / Deskew Mode Select / Scramble / XPIP_CSR2 for Port 1		22h

15 – 8	7 – 0	BYTE OFFSET
NFTS / Deskew Mode Select / Scramble / XPIP_XSR2 for Port 2		24h
Reserved		26h
LTSSM CSR / PML1 Option for Port 0		28h
LTSSM CSR / PML1 Option for Port 1		2Ah
LTSSM CSR / PML1 Option for Port 2		2Ch
Reserved		2Eh
PHY Parameter2_0 for Port 0		30h
PHY Parameter2_0 for Port 1		32h
PHY Parameter2_0 for Port 2		34h
Reserved		36h
XPIP_CSR3[15:0] for Port 0		38h
XPIP_CSR3[15:0] for Port 1		3Ah
XPIP_CSR3[15:0] for Port 2		3Ch
Reserved		3Eh
Do_change_rate_cnt/ XPIP_CSR_2 for Port 0	PHY Parameter 3 / PHY Parameter2_1 for Port 0	40h
Sel_deemp/ Do_change_rate_cnt/ XPIP_CSR_2 for Port 1	PHY Parameter 3 / PHY Parameter2_1 for Port 1	42h
Sel_deemp/ Do_change_rate_cnt/ XPIP_CSR_2 for Port 2	PHY Parameter 3 / PHY Parameter2_1 for Port 2	44h
Reserved		46h
XPIP_CSR3[16:31] for Port 0		48h
XPIP_CSR3[16:31] for Port 1		4Ah
XPIP_CSR3[16:31] for Port 2		4Ch
Reserved		4Eh
PM Data for Port 0	PM Capability for Port 0	50h
PM Data for Port 1	PM Capability for Port 1	52h
PM Data for Port 2	PM Capability for Port 2	54h
Reserved		56h
MAC CSR for Port 0		58h
MAC CSR for Port 1		5Ah
MAC CSR for Port 2		5Ch
Reserved		5Eh
TC/VC Map for Port 0 (VC0)	Slot Clock / LPVC Count / Port Num for Port 0	60h
TC/VC Map for Port 1 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num for Port 1	62h
TC/VC Map for Port 2 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num for Port 2	64h
Reserved		66h
TL_CSR0/Clock PM Cap/L1PM Substrates Cap/TL_CSR1 for Port 0		68h
TL_CSR0/Clock PM Cap/L1PM Substrates Cap/TL_CSR1 for Port 1		6Ah
TL_CSR0/Clock PM Cap/L1PM Substrates Cap/TL_CSR1 for Port 2		6Ch
Reserved		6Eh
Power Budgeting Capability Register for Port 0		70h
Power Budgeting Capability Register for Port 1		72h
Power Budgeting Capability Register for Port 2		74h
Reserved		76h
REV_TS_CTR/Replay Time-out Counter for Port 0		78h
REV_TS_CTR /Replay Time-out Counter for Port 1		7Ah
REV_TS_CTR /Replay Time-out Counter for Port 2		7Ch
Reserved		7Eh
XPIP_CSR5[30:24] for Port 0	PM Control Para/Rx Polarity for Port 0	80h
XPIP_CSR5[30:24] for Port 1	PM Control Para/Rx Polarity for Port 1	82h
XPIP_CSR5[30:24] for Port 2	PM Control Para/Rx Polarity for Port 2	84h
Reserved		86h
Acknowledge Latency Timer for Port 0		88h
Acknowledge Latency Timer for Port 1		8Ah
Acknowledge Latency Timer for Port 2		8Ch
Reserved		8Eh
Reserved		90h
Slot Capability 0 for Port 1		92h
Slot Capability 0 for Port 2		94h
Reserved		96h
Reserved		98h
Slot Capability 1 for Port 1		9Ah

15 – 8	7 – 0	BYTE OFFSET
Slot Capability 1 for Port 2		9Ch
Reserved		9Eh
VC1 MAX Time Slot / TC/VC Map for Port 0		A0h
VC1 MAX Time Slot / TC/VC Map for Port 1		A2h
VC1 MAX Time Slot / TC/VC Map for Port 2		A4h
Reserved		A6h
Reserved		A8h - FEh

6.1.4 MAPPING EEPROM CONTENTS TO CONFIGURATION REGISTERS

ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
00h		**EEPROM signature**	1516h
02h	**00h ~ 01h**	**Vendor ID**	12D8h
04h	**02h ~ 03h**	**Device ID**	B304h
06h	**144h (Port 0~2)** 144h: Bit [0] **CCh (Port 0~2)** CCh: Bit [14:12] CCh: Bit [17:15] **74h (Port 0~2)** 74h: Bit [7] 74h: Bit [5] 74h: Bit [6] 74h: Bit [0] 74h: Bit [2:1] 74h: Bit [3] 74h: Bit [4] **3Ch (Port 1~2)** 3Ch: Bit [8]	**Extended VC Count for Port 0~2** ▪ Bit [0]: It represents the supported VC count other than the default VC **Link Capability for Port 0~2** ▪ Bit [3:1]: It represents L0s Exit Latency for all ports ▪ Bit [6:4]: It represents L1 Exit Latency for all ports **Switch Mode Operation for Port 0** ▪ Bit [7]: Non-Post TLP Sotre-Forward ▪ Bit [8]: no ordering on packets for different egress port mode ▪ Bit [9]: no ordering on different tag of completion mode ▪ Bit [10]: Store and Forward ▪ Bit [12:11]: Cut-through Threshold ▪ Bit [13] : Port arbitrator Mode ▪ Bit [14]: Credit Update Mode **Interrupt pin for Port 1~2** ▪ Bit [15]: Set when INTA is requested for interrupt resource	0806h bit[0]: HWInit
08h	**B4h ~ B5h**	**Subsystem Vender ID**	0000h
0Ah	**B6h ~ B7h**	**Subsystem ID**	0000h
0Ch	**C4h (Port 0~2)** C4h: Bit [1:0] **CCh (Port 0~2)** CCh: Bit [11:10] **C4h (Port 0~2)** C4h: Bit [15] **70h (Port 0~2)** 70h: Bit [14] **74h (Port 0~2)** 74h: Bit [15] **70h (Port 0~2)** 70h: Bit [13] **8Ch (Port 0~2)** 8Ch: Bit [5] **CCh (Port 1~3)** CCh: Bit [21]	**Max_Payload_Size Support for Port 0~2** ▪ Bit [1:0]: Indicated the maximum payload size that the device can support for the TLP **ASPM Support for Port 0~2** ▪ Bit [3:2] : Indicate the level of ASPM supported on the PCIe link **Role_Base Error Reporting for Port 0~2** ▪ Bit [4] : Indicate implement the role-base error reporting **MSI Capability Disable for Port 0~2** ▪ Bit [5] : Disable MSI capability **Compliance Pattern Parity Control Disable for Port 0~2** ▪ Bit [6] : Disable compliance pattern parity **Power Management Capability Disable for Port 0~2** ▪ Bit [7] : Disable Power Management Capability **ORDER RULE5 Enable for Port 0~2** ▪ Bit [8]: Capability for Post packet Pass Non-Post packet **Link Bandwidth Notification Capability for port 1~ 3** ▪ Bit [9]: Link Bandwidth Notification	001Dh bit[1:0]: HWInit

ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
		Capability **Ordering Frozen for Port 0~2** ▪ Bit [10]: Freeze the ordering feature **TX SOF Latency Mode for Port 0~2** ▪ Bit [11]: Set to zero to shorten latency **Surprise Down Capability Enable for Port 0~2** ▪ Bit [12]: Enable Surprise Down Capability **Power Management's Data Select Register R/W Capability for Port 0~2** ▪ Bit [13]: Enable Data Select Register R/W **LTR Capability Enable for Port 0~2** ▪ Bit [14]: LTR capability enable **4KB Boundary Check Enable for Port 0~2** ▪ Bit [15]: Enable 4KB Boundary Check	
	8Ch (Port 0~2) 8Ch: Bit [6] **8Ch (Port 0~2)** 8Ch: Bit [0] **CCh (Port 0~2)** CCh: Bit [19] **8Ch (Port 0~2)** 8Ch: Bit [1] **E4h (Port 0~2)** E4h: Bit [12] **8Ch (Port 0~2)** 8Ch: Bit [3]		
0Eh	**94h (Port 0~2)** 94h: Bit [4:0] 94h: Bit [9:5] 94h: Bit [14:10] **E4h (Port 0~2)** E4h: Bit [18]	**PHY TX Margin Parameter for Port 0~2** ▪ Bit [4:0]: C_DRV_LVL_3P5_MGN2 ▪ Bit [9:5]: C_DRV_LVL_6P0_MGN2 ▪ Bit [14:10]: C_DRV_LVL_HALF_MGN2 **OBFF Capability Enable for Port 0~2** ▪ Bit [15] : enable OBFF capability	916Bh
10h	**74h (Port 0~2)** 74h: Bit [20:16] 74h: Bit [25:21] 74h: Bit [30:26] **8Ch (Port 0~2)** 8Ch: Bit [31]	**PHY Parameter 0 for Port 0~2** ▪ Bit [4:0]: C_DRV_LVL_3P5_NOM ▪ Bit [9:5]: C_DRV_LVL_6P0_NOM ▪ Bit [14:10]: C_DRV_LVL_HALF_NOM **TL_CSR0[31] for Port 0~2** ▪ Bit [15] : P35_GEN2_MODE	0A73h
12h	**78h (Port 0~2)** 78h: Bit [20:16] 78h: Bit [25:21] 78h: Bit [30:26] **8Ch (Port 0~2)** 8Ch: Bit [16]	**PHY Parameter 1 for Port 0~2** ▪ Bit [4:0]: C_EMP_POST_GEN1_3P5_NOM ▪ Bit [9:5]: C_EMP_POST_GEN2_3P5_NOM ▪ Bit [14:10]: C_EMP_POST_GEN2_6P0_NOM **XPIP_CSR6[0] for Port 0~2** ▪ Bit [15]: XPIP_CSR6[0]	F6B5h
14h	**7Ch (Port 0~2)** 7Ch: Bit [3:0] 7Ch: Bit [6:4] **90h (Port 0~2)** 90h: Bit [19:15] **8Ch (Port (0~3)** 8Ch: Bit [20:17]	**PHY Parameter 2 for Port 0~2** ▪ Bit [3:0]: C_TX_PHY_LATENCY ▪ Bit [6:4]: C_REC_DETECT_USEC **PHY Parameter 3 for Port 0~2** ▪ Bit [11:7]: C_EMP_POST_HALF_DELTA **XPIP_CSR6[4:1] for Port 0~2** ▪ Bit [15:12]: XPIP_CSR6[4:1]	C0A7h
16h	**84h (Port 0~2)** 84h: Bit [15:0]	**XPIP_CSR4[15:0] for Port 0~2** ▪ Bit [15:0]: XPIP_CSR4[15:0]	0000h
18h	**84h (Port 0~2)** 84h: Bit [31:16]	**XPIP_CSR4[31:16] for Port 0~2** ▪ Bit [15:0]: XPIP_CSR4[31:16]	0000h
1A	**88h (Port 0~2)** 88h: Bit [15:0]	**XPIP_CSR5[15:0] for Port 0~2** Bit [15:0]: XPIP_CSR5[15:0]	3333h
1C	**88h (Port 0~2)** 88h: Bit [23:16] **8Ch (Port 0~2)** 8Ch: Bit [23:21] **98h (Port 0~2)** 98h: Bit [20:16]	**XPIP_CSR5[28:16] for Port 0~2** ▪ Bit [7:0]: XPIP_CSR5[23:16] **XPIP_CSR6[7:5] for Port 0~2** ▪ Bit [10:8]: XPIP_CSR6[7:5] **BUFFER_CTRL[4:0] for Port 0~2** ▪ Bit [15:11]: Reference clock Buffer control	7B08h
1E	**90h (Port 0~2)** 90h: Bit [21:20] 90h: Bit [23:22] 90h: Bit [25:24]	**PHY parameter 3 for Port 0~2** ▪ Bit [1:0]: C_DRV_LVL_3P5_DELTA ▪ Bit [3:2]: C_DRV_LVL_6P0_DELTA ▪ Bit [5:4]: C_DRV_LVL_HALF_DELTA	0000h

ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
	90h: Bit [27:26] 90h: Bit [29:28] 90h: Bit [31:30] **8Ch (Port 0~2)** 8Ch: Bit [29:26]	▪ Bit [7:6]: C_EMP_POST_GEN1_3P5_DELTA ▪ Bit [9:8]: C_EMP_POST_GEN2_3P5_DELTA ▪ Bit [11:10]: C_EMP_POST_GEN2_6P0_DELTA **MAC control parameter for Port 0~2** ▪ Bit [15:12]: MAC_CTR	
20h	**78h (Port 0)** 78h: Bit [7 :0] **68h (Port 0)** 68h: Bit [14:13] **78h (Port 0)** 78h: Bit [9:8] 78h: Bit [10] **78h (Port 0)** 78h: Bit [13:12] **78h (Port 0)** 78h: Bit [14]	**FTS Number for Port 0** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 0** ▪ Bit [9:8]: deskew mode select **Scrambler Control for Port 0** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s **Change_Speed_Sel for Port 0** ▪ Bit [14:13]: Change Speed select **Change_Speed_En for Port 0** ▪ Bit [15]: Change Speed enable	0080h
22h	**78h (Port 1)** 78h: Bit [7 :0] **68h (Port 1)** 68h: Bit [14:13] **78h (Port 1)** 78h: Bit [9:8] 78h: Bit [10] **78h (Port 1)** 78h: Bit [13:12] **78h (Port 1)** 78h: Bit [14]	**FTS Number for Port 1** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 1** ▪ Bit [9:8]: deskew mode select **Scrambler Control for Port 1** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s **Change_Speed_Sel for Port 1** ▪ Bit[14:13]: Change Speed select **Change_Speed_En for Port 1** ▪ Bit [15]: Change Speed enable	0080h
24h	**78h (Port 2)** 78h: Bit [7 :0] **68h (Port 2)** 68h: Bit [14:13] **78h (Port 2)** 78h: Bit [9:8] 78h: Bit [10] **78h (Port 2)** 78h: Bit [13:12] **78h (Port 2)** 78h: Bit [14]	**FTS Number for Port 2** ▪ Bit [7:0]: FTS number at receiver side **Deskew Mode Select for Port 2** ▪ Bit [9:8]: deskew mode select **Scrambler Control for Port 2** ▪ Bit [11:10]: scrambler control ▪ Bit [12]: L0s **Change_Speed_Sel for Port 2** ▪ Bit [14:13]: Change Speed select **Change_Speed_En for Port 2** ▪ Bit [15]: Change Speed enable	0080h
28h	**33Ch (Port 0)** 33Ch: Bit [7 :0] **98h (Port 0)** 98h: Bit [24] 98h: Bit [25] 98h: Bit [27:26]	**LTSSM CSR for Port 0** ▪ Bit [7:0]: LTSSM CSR **PML1 Option for Port 0** ▪ Bit [12]: pml1 option all ▪ Bit [13]: pml1 disable ▪ Bit [15:14]: clock request control	0004h
2Ah	**33Ch (Port 1)** 33Ch: Bit [7 :0] **98h (Port 1)** 98h: Bit [24] 98h: Bit [25] 98h: Bit [27:26]	**LTSSM CSR for Port 1** ▪ Bit [7:0]: LTSSM CSR **PML1 Option for Port 1** ▪ Bit [12]: pml1 option all ▪ Bit [13]: pml1 disable ▪ Bit [15:14]: clock request control	0004h
2Ch	**33Ch (Port 2)** 33Ch: Bit [7 :0]	**LTSSM CSR for Port 2** ▪ Bit [7:0]: LTSSM CSR	0004h

ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
	98h (Port 2) 98h: Bit [24] 98h: Bit [25] 98h: Bit [27:26]	**PML1 Option for Port 2** ▪ Bit [12]: pml1 option all ▪ Bit [13]: pml1 disable ▪ Bit [15:14]: clock request control	
30h	**7Ch (Port 0)** 7Ch: Bit [30 :16]	**PHY Parameter2_1 for Port 0** ▪ Bit [14:0]: PHY parameter 2	0010h
32h	**7Ch (Port 1)** 7Ch: Bit [30 :16]	**PHY Parameter2_1 for Port 1** ▪ Bit [14:0]: PHY parameter 2	0010h
34h	**7Ch (Port 2)** 7Ch: Bit [30 :16]	**PHY Parameter2_1 for Port 2** ▪ Bit [14:0]: PHY parameter 2	0010h
38h	**80h (Port 0)** 80h: Bit [15 :0]	**XPIP_CSR3_0 for Port 0** ▪ Bit [15:0]: XPIP_CSR3[15:0]	0000h
3Ah	**80h (Port 1)** 80h: Bit [15 :0]	**XPIP_CSR3_0 for Port 1** ▪ Bit [15:0]: XPIP_CSR3[15:0]	0000h
3Ch	**80h (Port 2)** 80h: Bit [15 :0]	**XPIP_CSR3_0 for Port 2** ▪ Bit [15:0]: XPIP_CSR3[15:0]	0000h
40h	**7Ch (Port 0)** 7Ch: Bit [12 :8] **90h (Port 0)** 90h: Bit [6 :0] **F0h (Port 0)** F0h: Bit [6] **78h (Port 0)** 78h: Bit [11] **8Ch (Port 0)** 8Ch: Bit [9:8]	**PHY Parameter 2_0 for Port 0** ▪ Bit [4:0]: PHY parameter 2 **PHY Parameter 3 for Port 0** ▪ Bit [11:5]: PHY parameter 3 **Selectable De-emphasis for Port 0** ▪ Bit [12]: Selectable De-emphasis **Compliance to Detect for Port 0** ▪ Bit [13]: compliance to detect **DO_CHG_DATA_CNT_SEL for Port 0** ▪ Bit [15:14]: DO_CHG_DATA_CNT_SEL	001Dh
42h	**7Ch (Port 1)** 7Ch: Bit [12 :8] **90h (Port 1)** 90h: Bit [6 :0] **F0h (Port 1)** F0h: Bit [6] **78h (Port 1)** 78h: Bit [11] **8Ch (Port 1)** 8Ch: Bit [9:8]	**PHY Parameter 2_0 for Port 1** ▪ Bit [4:0]: PHY parameter 2 **PHY Parameter 3 for Port 1** ▪ Bit [11:5]: PHY parameter 3 **Selectable De-emphasis for Port 1** ▪ Bit [12]: Selectable De-emphasis **Compliance to Detect for Port 1** ▪ Bit [13]: compliance to detect **DO_CHG_DATA_CNT_SEL for Port 1** ▪ Bit [15:14]: DO_CHG_DATA_CNT_SEL	101Dh
44h	**7Ch (Port 2)** 7Ch: Bit [12 :8] **90h (Port 2)** 90h: Bit [6 :0] **F0h (Port 2)** F0h: Bit [6] **78h (Port 2)** 78h: Bit [11] **8Ch (Port 2)** 8Ch: Bit [9:8]	**PHY Parameter 2_0 for Port 2** ▪ Bit [4:0]: PHY parameter 2 **PHY Parameter 3 for Port 2** ▪ Bit [11:5]: PHY parameter 3 **Selectable De-emphasis for Port 2** ▪ Bit [12]: Selectable De-emphasis **Compliance to Detect for Port 2** ▪ Bit [13]: compliance to detect **DO_CHG_DATA_CNT_SEL for Port 2** ▪ Bit [15:14]: DO_CHG_DATA_CNT_SEL	101Dh
48h	**80h (Port 0)** 80h: Bit [31 :16]	**XPIP_CSR3_1 for Port 0** ▪ Bit [15:0]: XPIP_CSR3[31:16]	000Fh
4Ah	**80h (Port 1)** 80h: Bit [31 :16]	**XPIP_CSR3_1 for Port 1** ▪ Bit [15:0]: XPIP_CSR3[31:16]	000Fh
4Ch	**80h (Port 2)** 80h: Bit [31 :16]	**XPIP_CSR3_1 for Port 2** ▪ Bit [15:0]: XPIP_CSR3[31:16]	000Fh
50h	**44h (Port 0)** 44h: Bit [3]	**No_Soft_Reset for Port 0** ▪ Bit [0]: No_Soft_Reset.	FFh

ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
	40h (Port 0) 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**Power Management Capability for Port 0** ▪ Bit [3:1]: AUX Current. ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states	
	44h (Port 0) 44h: Bit [31:24]	**Power Management Data for Port 0** ▪ Bit [15:8]: read only as Data register	00h
52h	**44h (Port 1)** 44h: Bit [3] **40h (Port 1)** 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**No_Soft_Reset for Port 1** ▪ Bit [0]: No_Soft_Reset. **Power Management Capability for Port 1** ▪ Bit [3:1]: AUX Current. ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states	FFh
	44h (Port 1) 44h: Bit [31:24]	**Power Management Data for Port 1** ▪ Bit [15:8]: read only as Data register	00h
54h	**44h (Port 2)** 44h: Bit [3] **40h (Port 2)** 40h: Bit [24:22] 40h: Bit [25] 40h: Bit [26] 40h: Bit [29:28]	**No_Soft_Reset for Port 2** ▪ Bit [0]: No_Soft_Reset **Power Management Capability for Port 2** ▪ Bit [3:1]: AUX Current ▪ Bit [4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit [5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit [7:6]: PME Support for D2 and D1 states	FFh
	44h (Port 2) 44h: Bit [31:24]	**Power Management Data for Port 2** ▪ Bit [15:8]: read only as Data register	00h
58h	**340h (Port 0)** 340h: Bit [15 :0]	**MAC_CSR for Port 0** ▪ Bit [15:0]: MAC CSR	0004h
5Ah	**340h (Port 1)** 340h: Bit [15 :0]	**MAC_CSR for Port 1** ▪ Bit [15:0]: MAC CSR	0004h
5Ch	**340h (Port 2)** 340h: Bit [15 :0]	**MAC_CSR for Port 2** ▪ Bit [15:0]: MAC CSR	0004h
60h	**D0h (Port 0)** D0h: Bit [28] **40h (Port 0)** 40h: Bit[21] **144h (Port 0)** 144h: Bit [4] **CCh (Port 0)** CCh: Bit [26:24]	**Slot Clock Configuration for Port 0** ▪ Bit [1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 0** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 0** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 0 **Port Number for Port 0** ▪ Bit [6:4]: It represents the logic port numbering for physical port 0	02h bit[1]: HWInit
	154h (Port 0) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 0** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0	FEh

ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
62h	**C0h (Port 1)** C0h: Bit [24] **D0h (Port 1)** D0h: Bit [28] **40h (Port 1)** 40h: Bit [21] **144h (Port 1)** 144h: Bit [4] **CCh (Port 1)** CCh: Bit [26:24]	**PCIe Capability Slot Implemented for Port 1** ▪ Bit [0]: When set, the slot is implemented for Port 1 **Slot Clock Configuration for Port 1** ▪ Bit [1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 1** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 1** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 1 **Port Number for Port 1** ▪ Bit [6:4]: It represents the logic port numbering for physical port 1	12h bit[0]: HWInit bit[1]: HWInit
	154h (Port 1) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 1** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0	FEh
64h	**C0h (Port 2)** C0h: Bit [24] **D0h (Port 2)** D0h: Bit [28] **40h (Port 2)** 40h: Bit [21] **144h (Port 2)** 144h: Bit [4] **CCh (Port 2)** CCh: Bit [26:24]	**PCIe Capability Slot Implemented for Port 2** ▪ Bit [0]: When set, the slot is implemented for Port 2 **Slot Clock Configuration for Port 2** ▪ Bit [1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 2** ▪ Bit [2]: When set, the DSI is required **LPVC Count for Port 2** ▪ Bit [3]: When set, the VC1 is allocated to LPVC of Egress Port 2 **Port Number for Port 2** ▪ Bit [6:4]: It represents the logic port numbering for physical port 2	22h bit[0]: HWInit bit[1]: HWInit
	154h (Port 2) 154h: Bit [7:1]	**VC0 TC/VC Map for Port 2** ▪ Bit [15:9]: When set, it indicates the corresponding TC is mapped into VC0	FEh
68h	**8Ch (Port 0)** 8Ch: Bit[10] 8Ch: Bit[11] **CCh (Port 0)** CCh: Bit [18] **244h (Port 0)** 244h: Bit [1] 244h: Bit[3] 244h: Bit[4] **344h (Port 0)** 344h: Bit [0] 344h: Bit [1]	**TL_CSR0 Register for Port 0** ▪ Bit [0]: Port Disable ▪ Bit [1]: Reset_p_sel **Clock PM Cap for Port 0** ▪ Bit [2]: clock pm cap. **L1PM Substrates Capability Register for Port 0** ▪ Bit [4]: pci_pm_l11_sup ▪ Bit [5]: aspm_pm_l11_sup ▪ Bit[6]: l1pm_subs_sup **TL_CSR1 Register for Port 0** ▪ Bit [8]: ARB_VC_MODE ▪ Bit [9]: GNT_FAIL_MODE	0376h
6Ah	**8Ch (Port 1)** 8Ch: Bit[10] 8Ch: Bit[11] **CCh (Port 1)** CCh: Bit [18] **244h (Port 1)** 244h: Bit [1] 244h: Bit[3] 244h: Bit[4] **344h (Port 1)**	**TL_CSR0 Register for Port 1** ▪ Bit [0]: Port Disable ▪ Bit [1]: Reset_p_sel **Clock PM Cap for Port 1** ▪ Bit [2]: clock pm cap. **L1PM Substrates Capability Register for Port 1** ▪ Bit [4]: pci_pm_l11_sup ▪ Bit [5]: aspm_pm_l11_sup ▪ Bit[6]: l1pm_subs_sup **TL_CSR1 Register for Port 1**	0370h

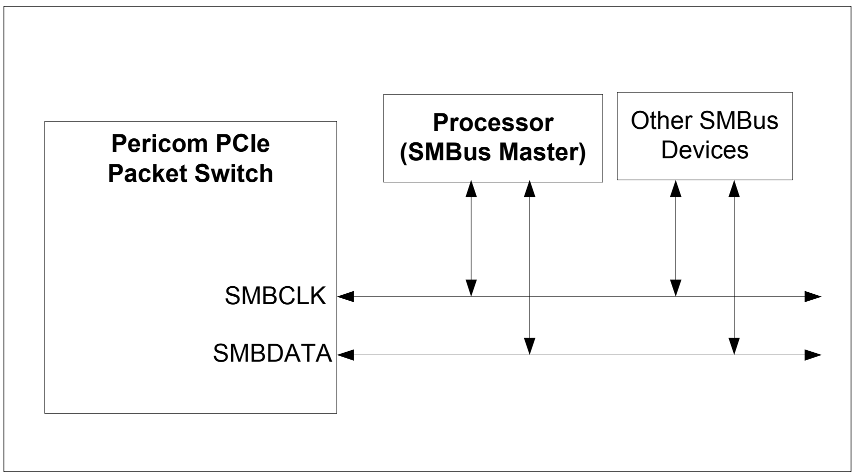
ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
	344h: Bit [0] 344h: Bit [1]	▪ Bit [8]: ARB_VC_MODE ▪ Bit [9]: GNT_FAIL_MODE	
6Ch	**8Ch (Port 2)** 8Ch: Bit[10] 8Ch: Bit[11] **CCh (Port 2)** CCh: Bit [18] **244h (Port 2)** 244h: Bit [1] 244h: Bit[3] 244h: Bit[4] **344h (Port 2)** 344h: Bit [0] 344h: Bit [1]	**TL_CSR0 Register for Port 2** ▪ Bit [0]: Port Disable ▪ Bit [1]: Reset_p_sel **Clock PM Cap for Port 2** ▪ Bit [2]: clock pm cap. **L1PM Substrates Capability Register for Port 2** ▪ Bit [4]: pci_pm_l11_sup ▪ Bit [5]: aspm_pm_l11_sup ▪ Bit[6]: l1pm_subs_sup **TL_CSR1 Register for Port 2** ▪ Bit [8]: ARB_VC_MODE ▪ Bit [9]: GNT_FAIL_MODE	0370h
70h	**214h (Port 0)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 0** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated	0004h
72h	**214h (Port 1)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 1** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated	0004h
74h	**214h (Port 2)** 214h: Bit [7:0] 214h: Bit [9:8] 214h: Bit [14:13] 218h: Bit [0]	**Power Budget Register for Port 2** ▪ Bit [7:0]: Base Power ▪ Bit [9:8]: Data Scale ▪ Bit [11:10]: PM State ▪ Bit [15]: System Allocated	0004h
78h	**70h (Port 0)** 70h: Bit [12:0] **8Ch (Port 0)** 8Ch: Bit [25:24]	**Replay Time-out Counter for Port 0** ▪ Bit [12:0]: Relay Time-out Counter **REV_TS_CTR for Port 0** ▪ Bit [14:13]: REV_TS_CTR	0000h
7Ah	**70h (Port 1)** 70h: Bit [12:0] **8Ch (Port 1)** 8Ch: Bit [25:24]	**Replay Time-out Counter for Port 1** ▪ Bit [12:0]: Relay Time-out Counter **REV_TS_CTR for Port 1** ▪ Bit [14:13]: REV_TS_CTR	0000h
7Ch	**70h (Port 2)** 70h: Bit [12:0] **8Ch (Port 2)** 8Ch: Bit [25:24]	**Replay Time-out Counter for Port 2** ▪ Bit [12:0]: Relay Time-out Counter **REV_TS_CTR for Port 2** ▪ Bit [14:13]: REV_TS_CTR	0000h
80h	**74h (Port 0)** 74h: Bit [13:8] 74h: Bit [14] **70h (Port 0)** 70h: Bit [31] **88h (Port 0)** 88h: Bit [31:24]	**PM Control Parameter for Port 0** ▪ Bit [1:0] : D3 enters L1 ▪ Bit [3:2] : L1 delay count select ▪ Bit [5:4] : L0s enable ▪ Bit [6] : Disable Rx polarity capability **VGA Decode Enable for Port 0** ▪ Bit [7]: Enable VGA decode **XPIP_CSR5[31:24] for Port 0** Bit[15:8]: XPIP_CSR5[31:24]	73A1h

ADDRESS	PCI CFG OFFSET	DESCRIPTION	Default Value
82h	**74h (Port 1)** 74h: Bit [13:8] 74h: Bit [14] **70h (Port 1)** 70h: Bit [31] **88h (Port 1)** 88h: Bit [31:24]	**PM Control Parameter for Port 1** ▪ Bit [1:0] : D3 enters L1 ▪ Bit [3:2] : L1 delay count select ▪ Bit [5:4] : L0s enable ▪ Bit [6] : Disable Rx polarity capability **VGA Decode Enable for Port 1** ▪ Bit [7]: Enable VGA decode **XPIP_CSR5[31:24] for Port 1** ▪ Bit [15:8]: XPIP_CSR5[31:24]	33A1h
84h	**74h (Port 2)** 74h: Bit [13:8] 74h: Bit [14] **70h (Port 2)** 70h: Bit [31] **88h (Port 2)** 88h: Bit [31:24]	**PM Control Parameter for Port 2** ▪ Bit [1:0] : D3 enters L1 ▪ Bit [3:2] : L1 delay count select ▪ Bit [5:4] : L0s enable ▪ Bit [6] : Disable Rx polarity capability **VGA Decode Enable for Port 2** ▪ Bit [7]: Enable VGA decode **XPIP_CSR5[31:24] for Port 2** ▪ Bit [15:8]: XPIP_CSR5[31:24]	33A1h
88h	**70h (Port 0)** 70h: Bit [30:16]	**Acknowledge Latency Timer for Port 0** ▪ Bit [14:0]: Acknowledge Latency Timer	0000h
8Ah	**70h (Port 1)** 70h: Bit [30:16]	**Acknowledge Latency Timer for Port 1** ▪ Bit [14:0]: Acknowledge Latency Timer	0000h
8Ch	**70h (Port 2)** 70h: Bit [30:16]	**Acknowledge Latency Timer for Port 2** ▪ Bit [14:0]: Acknowledge Latency Timer	0000h
92h	**D4h (Port 1)** D4h: Bit [15:0]	**Slot Capability 0 of Port 1** ▪ Bit [15:0]: Mapping to the low word of slot capability register	0000h
94h	**D4h (Port 2)** D4h: Bit [15:0]	**Slot Capability 0 of Port 2** ▪ Bit [15:0]: Mapping to the low word of slot capability register	0000h
9Ah	**D4h (Port 1)** D4h: Bit [31:16]	**Slot Capability 1 of Port 1** ▪ Bit [15:0]: Mapping to the high word of slot capability register	0008h
9Ch	**D4h (Port 2)** D4h: Bit [31:16]	**Slot Capability 1 of Port 2** ▪ Bit [15:0]: Mapping to the high word of slot capability register	0010h
A0h	**15Ch (Port 0)** 15Ch: Bit [22:16] **160h (Port 0)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 0** ▪ Bit [6:0]: The maximum time slot supported by VC1 **TC/VC Map for Port 0** ▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1	0000h
A2h	**15Ch (Port 1)** 15Ch: Bit [22:16] **160h (Port 1)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 1** ▪ Bit [6:0]: The maximum time slot supported by VC1 **TC/VC Map for Port 1** ▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1	0000h
A4h	**15Ch (Port 2)** 15Ch: Bit [22:16] **160h (Port 2)** 160h: Bit [7:0]	**VC1 MAX Time Slot for Port 2** ▪ Bit [6:0]: The maximum time slot supported by VC1 **TC/VC Map for Port 2** ▪ Bit [15:8]: When set, it indicates the corresponding TC is mapped into VC1	0000h

6.2 SMBus INTERFACE

The PI7C9X2G304SV provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the PI7C9X2G304SV is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

Figure 6-1 SMBus Architecture Implementation on PI7C9X2G304SV



The SMBus interface on the PI7C9X2G304SV consists of one SMBus clock pin (SMBCLK), a SMBus data pin (SMBDATA), and 3 SMBus address pins (GPIO[5:7]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the PI7C9X2G304SV responds to. The SMBus address pins generate addresses according to the following table:

Table 6-1 SMBus Address Pin Configuration

BIT	SMBus Address
0	GPIO[5]
1	GPIO[6]
2	GPIO[7]
3	1
4	1
5	0
6	1

6.2.1 SMBUS WRITE

The Write command is used to write the PI7C9X2G304SV registers. General SMBus Writes are illustrated in Figure 6-2. Table 6-2 explains the elements used in Figure 6-2.

Figure 6-2 SMBus Write Command Format, to Write to a PI7C9X2G304SV Register (PEC disable)

S	Slave Addr	Wr	A	Cmd Code = 08h	A	Offset	A	Port	A	P
S	Slave Addr	Wr	A	Cmd Code = 08h	A	Data Byte 1	A	Data Byte 2	A	P

: Master to Slave
: Slave to Master

Table 6-2 Bytes for SMBus Write

Field (Byte) On Bus	Bit(s)	Value/ Description
S	1	**START** condition
P	1	**STOP** condition
A	1	**Acknowledge** (this bit position may be 0 for an ACK or 1 for a NACK)
Cmd Code	7:0	**08h**
Offset	7:0	**PI7C9X2G304SV Register Address [7:0]**
Port	7:0	**Port Number** 0~2: Port 0 to Port 2 Others: Reserved
Data Byte 1	7:0	**Data Byte for register bits[7:0]**
Data Byte 2	7:0	**Data Byte for register bits [15:8]**

Table 6-3 is a sample to write SSVID register (offset B4h) in Port 1. The register value is 1234h, and the default SMBus Address is 1011000b.

Table 6-3 Sample SMBus Write Byte Sequence

Byte Number	Byte Type	Value	Description
1	Address	D0h	Bits [7:1] for the PI7C9X2G304SV default Slave address of 68h, with bit 0 Cleared to indicate a Write.
2	Cmd Code	08h	Command Code
3	Offset	B4h	Register address bits [7:0]
4	Port	01h	For Port 1
5	Address	D0h	Bits [7:1] for the PI7C9X2G304SV default Slave address of 68h, with bit 0 Cleared to indicate a Write.
6	Cmd Code	08h	Command Code
7	Data Byte 1	34h	Data Byte for register bits [7:0]
8	Data Byte 2	12h	Data Byte for register bits [15:8]

6.2.2 SMBUS READ

The Read command is used to read the PI7C9X2G304SV registers. General SMBus Reads are illustrated in Figure 6-3. Table 6-4 explains the elements used in Figure 6-3**.**

Figure 6-3 SMBus Read Command Format, to Read that Returns CFG Register Value (PEC disabled)

S	Slave Addr	Wr	A	Cmd Code = 08h	A	Offset	A	Port	A	P					
S	Slave Addr	Wr	A	Cmd code = 08h	A	S	Slave Adress	Rd	A	Data Byte 1	A	Data Byte 2	A	P	

: Master to Slave
: Slave to Master

Table 6-4 Bytes for SMBus Read

Field (Byte) On Bus	Bit(s)	Value/ Description
S	1	**START** condition
P	1	**STOP** condition
A	1	**Acknowledge** (this bit position may be 0 for an ACK or 1 for a NACK)
Cmd Code	7:0	**08h**
Offset	7:0	**PI7C9X2G304SV Register Address [7:0]**
Port	7:0	**Port Number** 0~2: Port 0 to Port 2 Others: Reserved
Data Byte 1	7:0	**Return value for CFG register bits [7:0]**
Data Byte 2	7:0	**Return value for CFG register bits [15:8]**

Table 6-5 is a sample to Read SSVID register (offset B4h) in Port 1. The register value is 0000h and the default SMBus Address is 1011000b.

Table 6-5 SMBus Block Write Portion

Byte Number	Byte Type	Value	Description
1	Address	D0h	Bits [7:1] for the PI7C9X2G304SV default Slave address of 68h, with bit 0 Cleared to indicate a Write.
2	Cmd Code	08h	Command Code
3	Offset	B4h	Register address bits [7:0]
4	Port	01h	For Port 1
5	Address	D0h	Bits [7:1] for the PI7C9X2G304SV default Slave address of 68h, with bit 0 Cleared to indicate a Write.
6	Cmd Code	08h	Command Code
7	Address	D1h	Bits [7:1] for the PI7C9X2G304SV default Slave address of 68h, with bit 0 set 1 to indicate a Read.
8	Data Byte 1	00h	Data Byte for register bits [7:0]
9	Data Byte 2	00h	Data Byte for register bits [15:8]

6.3 I²C SLAVE INTERFACE

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at relatively low rates (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the *I²C Bus v2.1*.

The PI7C9X2G304SV is an I²C Slave. Slave operations allow the PI7C9X2G304SV Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

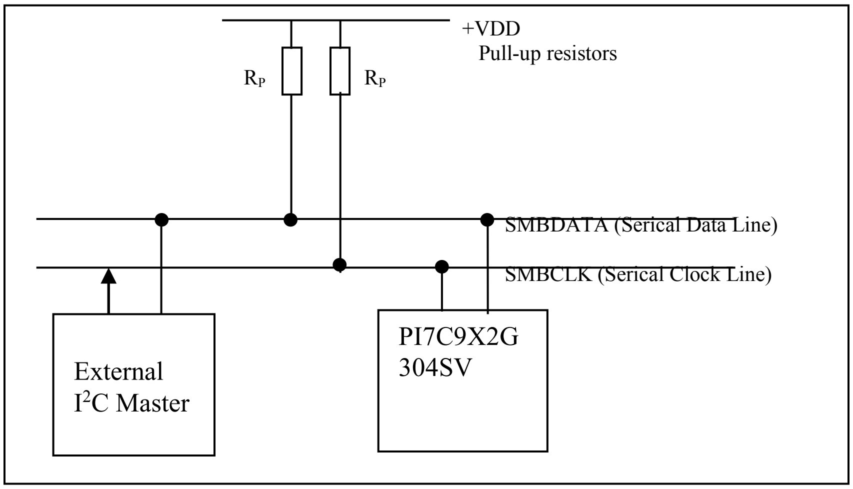


Figure 6-4 Standard Devices to I²C Bus Connection Block Diagram

The I²C interface on the Packet Switch consists of a I²C clock pin (SMBCLK), a I²C data pin (SMBDATA), and 3 I²C address pins (GPIO[7:5]). The I²C clock pin provides or receives the clock signal. The I²C data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The I²C address pins determine the address to which the Packet Switch responds to. The I²C address pins generate addresses according to the following table:

Table 6-6 I²C Address Pin Configuration

BIT	I2C Address
0	GPIO[5]
1	GPIO[6]
2	GPIO[7]
3	1
4	1
5	1
6	0

6.3.1 I²C REGISTER WRITE ACCESS

The PI7C9X2G304SV Configuration registers can be read from and written to, based upon I²C register Read and Write operations, respectively. An I²C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I²C Data bytes. Table 6-7 defines mapping of the I²C Data bytes to the Configuration register Data bytes.

The I²C packet starts with the S (START condition) bit. Data bytes are separated by the A (Acknowledge Control Packet (ACK)) or N (Negative Acknowledge (NAK)) bit. The packet ends with the P (STOP condition) bit.
If the Master generates an invalid command， the targeted PI7C9X2G304SV register is not modified.
The PI7C9X2G304SV considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I²C Master sends more than the four Data bytes (violating PI7C9X2G304SV protocol), further details regarding I²C protocol, the PI7C9X2G304SV returns a NAK for the extra Data byte(s).

Table 6-8 describes each I²C Command byte for Write access. In the packet described in Figure 6-5, Command Bytes 0 through 3 for Writes follow the format specified in Table 6-8.

Table 6-7 I^{2}C Register Write Access

I2C Data Byte Order	PCI Express Configuration Register Byte
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 6-8 I^{2}C Command Format for Write Access

Byte	Bit(s)	Description
1st (0)	7:3	**Reserved**
	2:0	**Command** 011b = Write register
2nd (1)	7:6	**Reserved**
	0	**Port Select[1]** 2nd Command byte, bits [0], and 3rd Command byte, bit 7, combine to form a 2-bit Port Select.
3rd (2)	7	**Port Select[0]** 2nd Command byte, bits [0], and 3rd Command byte, bit 7, combine to form a 2-bit Port Select. Port Select[1:0] is used to select Port to access. 0… Port 0 1… Port 1 2… Port 2
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G304SV register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G304SV register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G304SV register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G304SV register bits [31:24]) 0 = Corresponding PI7C9X2G304SV register byte will not be modified 1 = Corresponding PI7C9X2G304SV register byte will be modified
	1:0	**PI7C9X2G304SV Register Address [11:10]**
4th (3)	7:0	**PI7C9X2G304SV Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.

Figure 6-5 I^{2}C Write Packet

I^{2}C Write Packet Address Phase Byte

Address Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address [7:1]	Read/Write Bit 0 = Write	A

I2C Write Packet Command Phase Byte

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

I^{2}C Write Packet Data Phase Byte

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

The following tables illustrate a sample I2C packet for writing the PI7C9X2G304SV SSID/SSVID register (offset B4h) for Port 0, with data 1234_5678h and suppose GPIO[7:5] is set to 000b.

Figure 6-6 I²C Register Write Access Example

I²C Register Write Access Example – Address Cycle

Phase	Value	Description
Address	70h	Bits [7:1] for PI7C9X2G304SV I²C Slave Address (38h) with last bit (bit 0) for Write = 0

I²C Register Write Access Example – Command Cycle

Byte	Value	Description
0	03h	[7:3] Reserved [2:0] Command, 011b = Write register
1	00h for Port 0	[7:6] Reserved [0] Port Select[1]
2	3Ch for Port 0	[7] Port Select[0] [6] Reserved [5:2] Byte Enable, all active. [1:0] PI7C9X2G304SV Register Address, Bits [11:10]
3	2Dh	[7:0] PI7C9X2G304SV Register Address, Bits [9:2]

I²C Register Write Access Example – Data Cycle

Byte	Value	Description
0	12h	Data to Write for Byte 3
1	34h	Data to Write for Byte 2
2	56h	Data to Write for Byte 1
3	78h	Data to Write for Byte 0

Figure 6-7 I²C Write Command Packet Example

I²C Write Packet Address Phase Bytes

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address 1011_000b	Read/Write Bit 0 = Write	A

I²C Write Packet Command Phase Bytes

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0 0000_0011b	A	Command Byte 1 0000_0000b	A	Command Byte 2 0011_1100b	A	Command Byte 3 0010_1101b	A

I²C Write Packet Data Phase Bytes

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3 0001_0010b	A	Register Byte 2 0011_0100b	A	Register Byte 1 0101_0110b	A	Register Byte 0 0111_1000h	A	P

6.3.2 I²C REGISTER READ ACCESS

When the I²C Master attempts to read a PI7C9X2G304SV register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the I²C Bus, v2.1, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I²C Read access occurs, the internal buffer value is transferred on to the I²C Bus, starting from Byte 3 (bits [31: 24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I²C Master requests more than four bytes, the PI7C9X2G304SV re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I²C Read packets perform the following functions:

- 1st packet - Selects the register to read
- 2nd packet - Reads the register (sample 2nd packet provided is for a 7-bit PI7C9X2G304SV I²C Slave address)

Although two packets are shown for the I²C Read, the I²C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 6-9 describes each I²C Command byte for Read access. In the packet described in Figure 6-8, Command Bytes 0 through 3 for Reads follow the format specified in Table 6-9.

Table 6-9 I²C Command Format for Read Access

Byte	Bit(s)	Description
1st (0)	7:3	**Reserved**
	2:0	**Command** 100b = Read register
2nd (1)	7:6	**Reserved**
	0	**Port Select, Bits [1]** 2nd Command byte, bit [0], and 3rd Command byte, bit 7, combine to form a 2-bit Port Select.
3rd (2)	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 2-bit Port Select. Port Select[1:0] is used to select Port to access. 0… Port 0 1… Port 1 2… Port 2
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G304SV register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G304SV register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G304SV register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G304SV register bits [31:24]) 0 = Corresponding PI7C9X2G304SV register byte will not be modified 1 = Corresponding PI7C9X2G304SV register byte will be modified
	1:0	**PI7C9X2G304SV Register Address [11:10]**
4th (3)	7:0	**PI7C9X2G304SV Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.

Figure 6-8 I²C Read Command Packet

I²C Read Command Packet Address Phase Byte (1st Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

I²C Read Command Packet Command Phase Byte (1st Packet)

Write Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

I²C Read Data Packet Address Phase Byte (2nd Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address[7:1]	Read/Write Bit 1 = Read	A

I²C Read Data Packet Data Phase Byte (2nd Packet)

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

The following tables illustrate a sample I2C packet for reading the PI7C9X2G304SV SSID/SSVID register (offset B4h) for Port 0. The default value for SSID/SSVID register is 0000_0000h and suppose GPIO[7:5]=000b.

Figure 6-9 I²C Register Read Access Example

I²C Register Read Access Example – Address Cycle (1st Packet)

Phase	Value	Description
Address	70h	Bits [7:1] for PI7C9X2G304SV I²C Slave Address (38h) with last bit (bit 0) for Write = 0

I²C Register Read Access Example – Command Cycle (1st Packet)

Byte	Value	Description
0	04h	[7:3] Reserved [2:0] Command , 100b = Read register
1	00h for Port 0	[7:6] Reserved [0] Port Select[1]
2	3Ch for Port 0	[7] Port Select[0] [6] Reserved [5:2] Byte Enable, All active. [1:0] PI7C9X2G304SV Register Address, Bits [11:10]
3	2Dh	[7:0] PI7C9X2G304SV Register Address, Bits [9:2]

I²C Register Read Access Example – 2nd Packet

Phase	Value	Description
Address	71h	Bits [7:1] for PI7C9X2G304SV I2C Slave Address (38h) with last bit (bit 0) for Read = 1
Read	00h	Byte 3 of Register Read
	00h	Byte 2 of Register Read
	00h	Byte 1 of Register Read
	00h	Byte 0 of Register Read

Figure 6-10 I²C Read Command Packet

I²C Read Command Packet Address Phase Bytes (1st Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address 1011_000b	Read/Write Bit 0 = Write	A

I²C Read Command Packet Command Phase Bytes (1st Packet)

Command Cycle						
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**
Command Byte 0 0000_0100b	A	Command Byte 1 0000_0000b	A	Command Byte 2 0011_1100b	A	Command Byte 3 0010_1101b

I²C Read Data Packet Address Phase Bytes (2nd Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address [7:1] 0111_000b	Read/Write Bit 1 = Read	A

I^2C Read Data Packet Data Phase Bytes (2^{nd} Packet)

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**Stop**
Register Byte3 0000_0000b	A	Register Byte2 0000_0000b	A	Register Byte1 0000_0000b	A	Register Byte0 0000_00000b	P

7 REGISTER DESCRIPTION

7.1 REGISTER TYPES

REGISTER TYPE	DEFINITION
HwInt	Hardware Initialization
RO	Read Only
RW	Read / Write
RWC	Read / Write 1 to Clear
RWCS	Sticky – Read Only / Write 1 to Clear
RWS	Sticky – Read / Write
ROS	Sticky – Read Only

7.2 TRANSPARENT MODE CONFIGURATION REGISTERS

When the port of the Switch is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI Bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

31 –24	23 – 16	15 – 8	7 –0	BYTE OFFSET
Device ID		Vendor ID		00h
Primary Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h – 17h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32-bit				28h
Prefetchable Memory Limit Address Upper 32-bit				2Ch
I/O Limit Address Upper 16-bit		I/O Base Address Upper 16-bit		30h
Reserved			Capability Pointer to 40h	34h
Reserved				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch
Power Management Capabilities		Next Item Pointer= 4Ch	Capability ID=01h	40h
PM Data	PPB Support Extensions	Power Management Data		44h
Message Control		Next Item Pointer=: 64h	Capability ID=05h	4Ch
Message Address				50h
Message Upper Address				54h
Reserved		Message Data		58h
Reserved				5Ch – 60h
Length in Bytes (34h)		Next Item Pointer=B0h	Capability ID=09h	64h
XPIP_CSR0				68h
XPIP_CSR1				6Ch
ACK Latency Timer		Replay Time-out Counter		70h
PHY Parameter 0		Switch Modes		74h
PHY Parameter 1		XPIP_CSR2		78h
PHY Parameter 2				7Ch
XPIP_CSR3				80h
XPIP_CSR4				84h
XPIP_CSR5				88h
XPIP_CSR7	XPIP_CSR6	TL_CSR0		8Ch
PHY parameter 3				90h

31 –24	23 – 16	15 – 8	7 –0	BYTE OFFSET
Reserved	PHYL1 RXEQ	PHY TX Margin parameter		94h
Reserved	Buffer Ctrl	OP Mode		98h
Debug Control				9Ch
Debug Data Output				A0h
Reserved				A4h – ACh
Reserved		Next Item Pointer=C0h	SSID/SSVID Capability ID=0Dh	B0h
SSID		SSVID		B4h
GPIO Data and Control				B8h
EEPROM Data		EEPROM Address	EEPROM Control	BCh
PCI Express Capabilities Register		Next Item Pointer=00h	Capability ID=10h	C0h
Device Capabilities				C4h
Device Status		Device Control		C8h
Link Capabilities				CCh
Link Status		Link Control		D0h
Slot Capabilities				D4h
Slot Status		Slot Control		D8h
Reserved				DCh
Reserved				E0h
Device Capabilities 2				E4h
Device Status / Control 2				E8h
Link Capabilities 2				ECh
Link Status /Control 2				F0h
Slot Capabilities 2				F4h
Slot Status /Control 2				F8h
Reserved				FCh

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Next Capability Offset=140h	Cap. Version	PCI Express Extended Capability ID=0001h		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register				11Ch – 128h
Reserved				12Ch – 13Fh
Next Capability Offset=20Ch	Cap. Version	PCI Express Extended Capability ID=0002h		140h
Port VC Capability Register 1				144h
VC Arbitration Table Offset=3	Port VC Capability Register 2			148h
Port VC Status Register		Port VC Control Register		14Ch
Port Arbitration Table Offset=4	VC Resource Capability Register (0)			150h
VC Resource Control Register (0)				154h
VC Resource Status Register (0)		Reserved		158h
Port Arbitration Table Offset=6	VC Resource Capability Register (1)			15Ch
VC Resource Control Register (1)				160h
VC Resource Status Register (1)		Reserved		164h
Reserved				16Ch – 168h
VC Arbitration Table with 32 Phases				170h – 17Ch
Port Arbitration Table with 128 Phases for VC0				180h – 1BCh
Port Arbitration Table with 128 Phases for VC1				1C0h – 1FCh
Reserved				200h – 20Bh

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Next Capability Offset=220h/230h	Cap. Version	PCI Express Extended Capability ID=0004h		20Ch
Reserved			Data Select Register	210h
Data Register				214h
Reserved			Power Budget Capability Register	218h
Reserved				21Ch
Next Capability Offset=240h	Cap version	PCI Express Extended Capability ID=000Dh		220h
ACS Control		ACS Capability		224h
Reserved			Egress Control Vector	228h
Reserved				22Ch
Next Capability Offset=240h	Cap version	PCI Express Extended Capability ID=0018h		230h
Reserved / Max No-Snoop Latency Scale	Max No-Snoop Latency Value	Reserved / Max Snoop Latency Scale	Max Snoop Latency Value	234h
Reserved				238h – 23Ch
Next Capability Offset=260h/250h	Cap version	PCI Express Extended Capability ID=001Eh		240h
L1 PM Substates Capability				244h
L1 PM Substates Control 1				248h
L1 PM Substates Control 2				24Ch
Next Capability Offset=000h	Cap version	PCI Express Extended Capability ID=001Dh		250h
DPC Control		DPC Capability		254h
DPC Error Source ID		DPC Status		258h
Reserved				25Ch
Next Capability Offset=000h	Cap version	PCI Express Extended Capability ID=00FEh		260h
PTM Capability				264h
PTM Control				268h
Reserved				26Ch – 2FCh
Misc Control 0				300h
Misc Control 1				304h
Misc Control 2				308h
Misc Control 3				30Ch
Misc Control 4				310h
Reserved				314h
PHY/DLL/TL Error Counter				318h
Reserved				31Ch
Port Physical Layer Command and Status				320h
Port Disable / Quiet / Test Pattern Rate				324h
LED_CSR0				328h
LED_CSR1				32Ch
Reserved				338h – 330h
LTSSM_CSR				33Ch
MAC_CSR				340h
TL_CSR1				344h
Debugout Control				348h
Debugout Data				34Ch

7.2.1 VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO HWInt	Identifies Pericom as the vendor of this device. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 12D8h.

7.2.2 DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PI7C9X2G304SV. The default value may be changed by SMBus or auto-loading from EEPROM. Resets to B304h.

7.2.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface Resets to 0b.
1	Memory Space Enable	RW	0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface Reset to 0b.
2	Bus Master Enable	RW	0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction Reset to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI Express. Must be hardwired to 0.
8	SERR# enable	RW	0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex b1: Enables the Non-fatal and Fatal error reporting to Root Complex Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Switch, this bit does not affect the forwarding of INTx messages from the downstream ports. Reset to 0b.
15:11	Reserved	RsvdP	Not Support.

7.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RsvdP	Not Support.
19	Interrupt Status	RO	Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 0b.
20	Capabilities List	RO	Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure). Reset to 1b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.
26:25	DEVSEL# timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1 (by a completer) whenever completing a request on the primary side using the Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status on the primary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status on primary side. Reset to 0b.
30	Signaled System Error	RWC	Set to 1 when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the primary side of the port in a Switch receives a Poisoned TLP. Reset to 0b.

7.2.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of device. Hardwired to 00h.

7.2.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges.
23:16	Sub-Class Code	RO	Read as 04h to indicate device is a PCI-to-PCI Bridge.
31:24	Base Class Code	RO	Read as 06h to indicate device is a Bridge device.

7.2.7 CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. Reset to 00h.

7.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Primary Latency timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

7.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.

7.2.10 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Primary Bus Number	RW	Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration. Reset to 00h.

7.2.11 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Secondary Bus Number	RW	Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration. Reset to 00h.

7.2.12 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Subordinate Bus Number	RW	Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration. Reset to 00h.

7.2.13 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Secondary Latency Timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

7.2.14 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	32-bit Indicator	RO	Read as 1h to indicate 32-bit I/O addressing.
7:4	I/O Base Address [15:12]	RW	Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base address upper 16 bits address register. Reset to 0h.

7.2.15 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
11:8	32-bit Indicator	RO	Read as 1h to indicate 32-bit I/O addressing.
15:12	I/O Limit Address [15:12]	RW	Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits

BIT	FUNCTION	TYPE	DESCRIPTION
			[11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register. Reset to 0h.

7.2.16 SECONDARY STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Reserved	RsvdP	Not Support.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RsvdP	Not Support.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the secondary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.
26:25	DEVSEL_L timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1 (by a completer) whenever completing a request in the secondary side using Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status in the secondary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status in secondary side. Reset to 0b.
30	Received System Error	RWC	Set to 1 when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Bridge Control register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the secondary side of the port in a Switch receives a Poisoned TLP. Reset to 0b.

7.2.17 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Reserved	RsvdP	Not Support.
15:4	Memory Base Address [15:4]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are able to be written to. The lower 20 bits corresponding to address bits [19:0] are assumed to be 0. Reset to 000h.

7.2.18 MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Reserved	RsvdP	Not Support.
31:20	Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh. Reset to 000h.

7.2.19 PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	64-bit addressing	RO	Read as 1h to indicate 64-bit addressing.
15:4	Prefetchable Memory Base Address [31:20]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address. Reset to 000h.

7.2.20 PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	64-bit addressing	RO	Read as 1h to indicate 64-bit addressing.
31:20	Prefetchable Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be FFFFFh. The memory limit upper 32 bits register contains the upper half of the limit address. Reset to 000h.

7.2.21 PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Base Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 0000_0000h.

7.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Limit Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 0000_0000h.

7.2.23 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	I/O Base Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

7.2.24 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	I/O Limit Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

7.2.25 CAPABILITY POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability Pointer	RO	Pointer points to the PCI power management registers. Reset to 40h.

7.2.26 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Reset to 00h.

7.2.27 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	The Switch implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. The default value on the downstream ports may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.

7.2.28 BRIDGE CONTROL REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	Parity Error Response	RW	0b: Ignore Poisoned TLPs on the secondary interface 1b: Enable the Poisoned TLPs reporting and detection on the secondary interface Reset to 0b.
17	S_SERR# enable	RW	0b: Disables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface 1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface Reset to 0b.
18	ISA Enable	RW	0b: Forwards downstream all I/O addresses in the address range defined by the I/O Base, I/O Base, and Limit registers 1b: Forwards upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) Reset to 0b.
19	VGA Enable	RW	0: Ignores access to the VGA memory or IO address range 1: Forwards transactions targeted at the VGA memory or IO address range VGA memory range starts from 000A 0000h to 000B FFFFh VGA IO addresses are in the first 64KB of IO address space. AD [9:0] is in the ranges 3B0 to 3BBh and 3C0h to 3DFh. Reset to 0b.
20	VGA 16-bit decode	RW	0b: Executes 10-bit address decoding on VGA I/O accesses 1b: Executes 16-bit address decoding on VGA I/O accesses

BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 0b.
21	Master Abort Mode	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Secondary Bus Reset	RW	0b: Does not trigger a hot reset on the corresponding PCI Express Port 1b: Triggers a hot reset on the corresponding PCI Express Port At the downstream port, it asserts PORT_RST# to the attached downstream device. At the upstream port, it asserts the PORT_RST# at all the downstream ports. Reset to 0b.
23	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Primary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
25	Secondary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
26	Master Timeout Status	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Discard Timer SERR# enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
31:28	Reserved	RsvdP	Not Support.

7.2.29 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 01h to indicate that these are power management enhanced capability registers.
15:8	Next Item Pointer	RO	The pointer points to the Message capability register. Reset to 4Ch.
18:16	Power Management Revision	RO	Read as 011b to indicate the device is compliant to Revision 1.2 of *PCI Power Management Interface Specifications.*
19	PME# Clock	RO	Does not apply to PCI Express. Must be hardwired to 0b.
20	Reserved	RsvdP	Not Support.
21	Device Specific Initialization	RO	Read as 0b to indicate Switch does not have device specific initialization requirements. The default value may be changed by SMBus or auto-loading from EEPROM.
24:22	AUX Current	RO	Reset as 111b to indicate the Switch needs 375 mA in D3 state. The default value may be changed by SMBus or auto-loading from EEPROM.
25	D1 Power State Support	RO	Read as 1b to indicate Switch supports the D1 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.
26	D2 Power State Support	RO	Read as 1b to indicate Switch supports the D2 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.
31:27	PME# Support	RO	Read as 11111b to indicate Switch supports the forwarding of PME# message in all power states. The default value may be changed by SMBus or auto-loading from EEPROM.

7.2.30 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWNRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state Reset to 00b.
2	Reserved	RsvdP	Not Support.
3	No_Soft_Reset	RO	When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. This bit can be rewritten with EEPROM programming. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
7:4	Reserved	RsvdP	Not Support.
8	PME# Enable	RWS	When asserted, the Switch will generate the PME# message. Reset to 0b.
12:9	Data Select	RW	Select data registers. Reset to 0h.
14:13	Data Scale	RO	Reset to 00b.
15	PME status	ROS	Read as 0b as the PME# message is not implemented.

7.2.31 PPB SUPPORT EXTENSIONS – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RsvdP	Not Support.
22	B2_B3 Support for $D3_{HOT}$	RO	Does not apply to PCI Express. Must be hardwired to 0b.
23	Bus Power / Clock Control Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.

7.2.32 DATA REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Data Register	RO	Data Register. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.

7.2.33 MSI CAPABILITY REGISTER – OFFSET 4Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 05h to indicate that this is message signal interrupt capability register.
15:8	Next Item Pointer	RO	Pointer points to the Vendor specific capability register. Reset to 64h.

7.2.34 MESSAGE CONTROL REGISTER – OFFSET 4Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin Reset to 0b.
19:17	Multiple Message Capable	RO	Read as 010b.
22:20	Multiple Message Enable	RW	Reset to 000b.
23	64-bit address capable	RO	0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address Reset to 1b.
31:24	Reserved	RsvdP	Not Support.

7.2.35 MESSAGE ADDRESS REGISTER – OFFSET 50h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
31:2	Message Address	RW	If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. Reset to 0000_0000h.

7.2.36 MESSAGE UPPER ADDRESS REGISTER – OFFSET 54h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Message Upper Address	RW	This register is only effective if the device supports a 64-bit message address is set. Reset to 0000_0000h.

7.2.37 MESSAGE DATA REGISTER – OFFSET 58h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Message Data	RW	Reset to 0000h.
31:16	Reserved	RsvdP	Not Support.

7.2.38 VENDOR SPECIFIC CAPABILITY REGISTER – OFFSET 64h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 09h to indicate that these are vendor specific capability registers. Reset to 09h.
15:8	Next Item Pointer	RO	Pointer points to the SSID/SSVID capability register. Reset to B0h.
31:16	Length Information	RO	The length field provides the information for number of bytes in the capability structure (including the ID and Next pointer bytes). Reset to 0034h.

7.2.39 XPIP CSR0 – OFFSET 68h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR0	RW	Reset to 0400_1060h.

7.2.40 XPIP CSR1 – OFFSET 6Ch (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR1	RW	Reset to 0000_0800h.

7.2.41 REPLAY TIME-OUT COUNTER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	User Replay Timer	RW	A 12-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000h.
12	Enable User Replay Timer	RW	When asserted, the user-defined replay time-out value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
13	Power Management Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
14	MSI Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	Reserved	RsvdP	Not Support.

7.2.42 ACKNOWLEDGE LATENCY TIMER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION
29:16	User ACK Latency Timer	RW	A 14-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.
30	Enable User ACK Latency	RW	When asserted, the user-defined ACK latency value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
31	VGA Decode Enable	RO	Enable the VGA range decode. Reset to 1b.

7.2.43 SWITCH OPERATION MODE – OFFSET 74h (Upstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Store-Forward	RW	When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
2:1	Cut-through Threshold	RW	Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. The default value may be changed by SMBus or auto-loading from EEPROM. 00b: the threshold is set at the middle of forwarding packet 01b: the threshold is set ahead 1-cycle of middle point 10b: the threshold is set ahead 2-cycle of middle point. 11b: the threshold is set ahead 3-cycle of middle point. Reset to 01b.
3	Port Arbitration Mode	RW	When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending. When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
4	Credit Update Mode	RW	When set, the frequency of releasing new credit to the link partner will be all types per update. When clear, the frequency of releasing new credit to the link partner will be type oriented per update. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
5	Ordering on Different Egress Port Mode	RW	When set, there has ordering rule on packets for different egress port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
6	Ordering on Different Tag of Completion Mode	RW	When set, there has ordering rule between completion packet with different tag. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
7	Non-Post TLP Sotre-Forward	RW	When set, for Non-post TLP store-forward mode is used. Otherwise, Non-post TLP is working under cut-through mode. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
13:8	Power Management Control Parameter	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 10_0001b.
14	RX Polarity Inversion Disable	HwInt RO	The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM. Reset to the status of RXPOLINV_DIS strapped pin.
15	Compliance pattern Parity Control Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
20:16	C_DRV_LVL_3P5_NOM	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1_0011b
25:21	C_DRV_LVL_6P0_NOM	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 10_011b
30:26	C_DRV_LVL_HALF_NOM	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000_10b
31	Reserved	RsvdP	Not Support.

7.2.44 SWITCH OPERATION MODE – OFFSET 74h (Downstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Reserved	RsvdP	Not Support.
13:8	Power Management Control Parameter	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 10_0001b.
14	RX Polarity Inversion Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	Compliance Pattern Parity Control Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
20:31	Reserved	RsvdP	Not Support.

7.2.45 XPIP_CSR2 – OFFSET 78h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	XPIP_CSR2	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0080h.

7.2.46 PHY PARAMETER 1 – OFFSET 78h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	C_EMP_POST_GEN1_3P5_NOM	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1_0101b.
25:21	C_EMP_POST_GEN2_3P5_NOM	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 10_101b.
30:26	C_EMP_POST_GEN2_6P0_NOM	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 111_01b.
31	Reserved	RsvdP	Not Support.

7.2.47 PHY PARAMETER 2 – OFFSET 7Ch

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	C_TX_PHY_LATENCY	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 7h.
6:4	C_REC_DETEC_USEC	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 010b.
7	Reserved	RsvdP	Not Support.
8	P_CDR_FREQLOOP_EN	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.
10:9	P_CDR_THRESHOLD	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 10b.
12:11	P_CDR_FREQLOOP_GAIN	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 11b.
15:13	Reserved	RsvdP	Not Support.
16	P_DRV_LVL_MGN_DELATA_EN	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
17	P_DRV_LVL_NOM_DELATA_EN	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
18	P_EMP_POST_MGN_DELATA_EN	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
19	P_EMP_POST_NOM_DELATA_EN	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
21:20	P_RX_SIGDET_LVL	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 01b.
25:22	P_RX_EQ_1	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000b.
29:26	P_RX_EQ_2	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000b.
30	P_TXSWING	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
31	Reserved	RsvdP	Not Support.

7.2.48 XPIP_CSR3 – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR3	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000F_0000h.

7.2.49 XPIP_CSR4 – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	XPIP_CSR4	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000_0000h.

7.2.50 XPIP_CSR5 – OFFSET 88h

BIT	FUNCTION	TYPE	DESCRIPTION
29:0	XPIP_CSR5	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 7308_3333h for Upstream port. Reset to 3308_3333h for Downstream ports.
30	DO_CHG_DATA_RATE_CTRL	RO	The default value may be changed by SMBus, I2C or auto-loading from EEPROM. Reset to 1b (Upstream Port). Reset to 0b (Downstream Ports).
31	Gen1_Cap_Only	RO	The default value may be changed by SMBus, I2C or auto-loading from EEPROM. 0b: GEN2 capability 1b: GEN1 capability Reset to 0b.

7.2.51 TL_CSR0 – OFFSET 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	TX_SOF_FORM	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
1	PM Data Select Register R/W Capability	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
2	FC_UPDATE_MODE	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
3	4K Boundary Check Enable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
4	FIFOERR_FIX_SEL	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
5	MW Overpass Disable	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
6	Ordering Frozen Disable	RW	Disable the RO ordering rule. The default value may be changed by SMBus or auto-loading from EEPROM Reset to 0b.
7	Reserved	RsvdP	Not Support.
8:9	DO_CHG_DATA_CNT_SEL	RO	The trying number for doing change data rate. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00b.
10	Port Disable	RO	Disable this port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
11	Reset Select	RO	Reset select (upstream port only). The default value may be changed by SMBus or auto-loading from EEPROM. It is valid for up port only. Reset to 1b for up port. Reset to 0b for down port.
12	Power Saving Enable	HWInit	0b: power saving disable 1b: power saving enable.
15:13	Reserved	RsvdP	Not Support.
23:16	XPIP_CSR6	RO	XPIP_CSR6 Value. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 79h.

BIT	FUNCTION	TYPE	DESCRIPTION
25:24	REV_TS_CTR	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00b.
29:26	MAC Control Parameter	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0h.
30	Reserved	RsvdP	Not Support.
31	P35_GEN2_MODE	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

7.2.52 PHY PARAMETER 3 – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
6:0	PHY Parameter 3 (per lane)	RO	PHY's Lane mode. Reset to 000_0000b.
14:7	Reserved	RsvdP	Not Support.
31:15	PHY Parameter 3 (global)	RO	PHY's delta value setting. Reset to 0001h.

7.2.53 PHY PARAMETER 4 - OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PHY TX Margin	RO	Reset to 116Bh.
23:16	Multilane RXEQ	RO	Upstream Port only. Reset to 86h for Upstream Port. Reset to 00h for Downstream Ports.
31:24	Reserved	RsvdP	Not Support.

7.2.54 OPERATION MODE –OFFSET 98h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Operation mode	RO	{7'd0, VC0_NEGO_PENDING, SCAN_MODE, PKG_SEL[1:0], PHY_MODE, DEBUG_MODE, FAST_MODE, IDDQB, SROM_BYPASS}; Reset to 0102h.
20:16	Clock buffer control	HwInt RO	For Reference clock buffer control. The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM. Bit[20]: Reset to the status of CLKBUF_PD strapped pin. Bit[19:16]: Reset to 7h. Bit[20]: enable or disable reference clock outputs 0b: enable reference clock outputs 1b: disable reference clock outputs Bit[18:16]: enable or disable REFCLKO_P/N[2:0] 0b: disable 1b: enable Bit[19]: reserved
31:21	Reserved	RsvdP	Not Support.

7.2.55 LTSSM DEBUG CONTROL REGISTER – OFFSET 9Ch

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Debug Port Select	RW	Debug port select.

BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 00b.
5:2	Trigger Sel	RW	Select trigger point. 0001b: trigger from Detect state 0010b: trigger from Polling state 0011b: trigger from Configuration state 0100b: trigger from L0 state 0101b: trigger from L0s state 0110b: trigger from L1 state 0111b: trigger from L2 state 1000b: trigger from Disable state 1001b: trigger from Hot Reset state 1010b: trigger from Loopback state 1011b: trigger from Recovery state Others: Reserved Reset to 0h
6	Clear	RW	When set, it will clear the embedded debug data buffer. Reset to 0b
31:7	Reserved	RsvdP	Not Support.

7.2.56 LTSSM DEBUG DATA OUTPUT REGSITER – OFFSET ACh

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Debug Data Output	RO	It can be accessed by I2C/SMBUS only.

7.2.57 SSID/SSVID CAPABILITY REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SSID/SSVID Capabilities ID	RO	Read as 0Dh to indicate that these are SSID/SSVID capability registers.
15:8	Next Item Pointer	RO	Pointer points to the PCI Express capability register. Reset to C0h.
31:16	Reserved	RsvdP	Not Support.

7.2.58 SUBSYSTEM ID REGISTER – OFFSET B4h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	SSVID	RO	It indicates the sub-system vendor id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.
31:16	SSID	RO	It indicates the sub-system device id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.

7.2.59 GPIO CONTROL REGISTER – OFFSET B8h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	GPIO [0] Input	HwInt RO	State of GPIO [0] pin
1	GPIO [0] Output Enable	RW	0b: GPIO [0] is an input pin 1b: GPIO [0] is an output pin Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
2	GPIO [0] Output Register	RW	Value of this bit will be output to GPIO [0] pin if GPIO [0] is configured as an output pin. Reset to 0b.
3	Reserved	RsvdP	Not Support.
4	GPIO [1] Input	HwInt RO	State of GPIO [1] pin.
5	GPIO [1] Output Enable	RW	0b: GPIO [1] is an input pin 1b: GPIO [1] is an output pin Reset to 0b.
6	GPIO [1] Output Register	RW	Value of this bit will be output to GPIO [1] pin if GPIO [1] is configured as an output pin. Reset to 0b.
7	Reserved	RsvdP	Not Support.
8	GPIO [2] Input	HwInt RO	State of GPIO [2] pin
9	GPIO [2] Output Enable	RW	0b: GPIO [2] is an input pin 1b: GPIO [2] is an output pin Reset to 0b.
10	GPIO [2] Output Register	RW	Value of this bit will be output to GPIO [2] pin if GPIO [2] is configured as an output pin. Reset to 0b.
11	Reserved	RsvdP	Not Support.
12	GPIO [3] Input	HwInt RO	State of GPIO [3] pin.
13	GPIO [3] Output Enable	RW	0b: GPIO [3] is an input pin 1b: GPIO [3] is an output pin Reset to 0b.
14	GPIO [3] Output Register	RW	Value of this bit will be output to GPIO [3] pin if GPIO [3] is configured as an output pin. Reset to 0b.
15	Reserved	RsvdP	Not Support.
16	GPIO [4] Input	HwInt RO	State of GPIO [4] pin.
17	GPIO [4] Output Enable	RW	0b: GPIO [4] is an input pin 1b: GPIO [4] is an output pin Reset to 0b.
18	GPIO [4] Output Register	RW	Value of this bit will be output to GPIO [4] pin if GPIO [4] is configured as an output pin. Reset to 0b.
19	Reserved	RsvdP	Not Support.
20	GPIO [5] Input	HwInt RO	State of GPIO [5] pin.
21	GPIO [5] Output Enable	RW	0b: GPIO [5] is an input pin 1b: GPIO [5] is an output pin Reset to 0b.
22	GPIO [5] Output Register	RW	Value of this bit will be output to GPIO [5] pin if GPIO [5] is configured as an output pin. Reset to 0b.
23	Reserved	RsvdP	Not Support.
24	GPIO [6] Input	HwInt RO	State of GPIO [6] pin.
25	GPIO [6] Output Enable	RW	0b: GPIO [6] is an input pin 1b: GPIO [6] is an output pin Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
26	GPIO [6] Output Register	RW	Value of this bit will be output to GPIO [6] pin if GPIO [6] is configured as an output pin. Reset to 0b.
27	Reserved	RsvdP	Not Support.
28	GPIO [7] Input	HwInt RO	State of GPIO [7] pin.
29	GPIO [7] Output Enable	RW	0b: GPIO [7] is an input pin 1b: GPIO [7] is an output pin Reset to 0b.
30	GPIO [7] Output Register	RW	Value of this bit will be output to GPIO [7] pin if GPIO [7] is configured as an output pin. Reset to 0b.
31	Reserved	RsvdP	Not Support.

7.2.60 EEPROM CONTROL REGISTER – OFFSET BCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. Reset to 0b.
1	EEPROM Command	RW	Sends the command to the EEPROM. 0b: EEPROM read 1b: EEPROM write Reset to 0b.
2	EEPROM Error Status	RO	1b: EEPROM acknowledge was not received during the EEPROM cycle. Reset to 0b.
3	EEPROM Autoload Success	RO	0b: EEPROM autoload was unsuccessful or is disabled 1b: EEPROM autolad occurred successfully after RESET. Configuration registers were loaded with values in the EEPROM It will be cleared when read at this bit.
4	EEPROM Autoload Status	RO	0b: EEPROM autoload was unsuccessful or is disabled 1b: EEPROM autoload occurred successfully after PREST. Configuration registers were loaded with values stored in the EEPROM Reset to 0b.
5	EEPROM Autoload Disable	RW	0b: EEPROM autoload enabled 1b: EEPROM autoload disabled Reset to 1b.
7:6	EEPROM Clock Rate	RW	Determines the frequency of the EEPROM clock, which is derived from the primary clock. 00b: Reserved 01b: PEXCLK / 1024 (PEXCLK is 125MHz) 10b: Reserved 11b: Test Mode Reset to 01b.

7.2.61 EEPROM ADDRESS REGISTER – OFFSET BCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
8	Reserved	RsvdP	Not Support.
15:9	EEPROM Address	RW	Contains the EEPROM address. Reset to 00h.

7.2.62 EEPROM DATA REGISTER – OFFSET BCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	EEPROM Data	RW	Contains the data to be written to the EEPROM. After completion of a read cycle, this register will contain the data from the EEPROM. Reset to 0000h.

7.2.63 PCI EXPRESS CAPABILITY REGISTER – OFFSET C0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 10h to indicate that these are PCI express enhanced capability registers.
15:8	Next Item Pointer	RO	Read as 00h. No other ECP registers.
19:16	Capability Version	RO	Read as 0010b to indicate the device is compliant to Revision .2.0a of *PCI Express Base Specifications*.
23:20	Device/Port Type	RO	Indicates the type of PCI Express logical device. Reset to 0101b for Upstream port. Reset to 0110b for Downstream ports.
24	Slot Implemented	HwInt RO	When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream port of the Switch. The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM. Reset to the status of SLOT_IMP strapped pin.
29:25	Interrupt Message Number	RO	Read as 0b. No MSI messages are generated in the transparent mode.
31:30	Reserved	RsvdP	Not Support.

7.2.64 DEVICE CAPABILITIES REGISTER – OFFSET C4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Max_Payload_Size Supported	HwInt RO	Indicates the maximum payload size that the device can support for TLPs. Each port of the Switch supports 512 bytes max payload size. The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM. Reset to 001b when PL_512B strapped pin is set to 0. Reset to 010b when PL_512B strapped pin is set to 1.
4:3	Phantom Functions Supported	RO	Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester. Reset to 00b.
5	Extended Tag Field Supported	RO	Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester. Reset to 0b.
8:6	Endpoint L0s Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value. Reset to 000b.
11:9	Endpoint L1 Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value. Reset to 000b.
14:12	Reserved	RsvdP	Not Support.
15	Role_Based Error Reporting	RO	When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.
17:16	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
25:18	Captured Slot Power Limit Value	RO	It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to 00h. Reset to 00h.
27:26	Captured Slot Power Limit Scale	RO	It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to 00b. Reset to 00b.
31:28	Reserved	RsvdP	Not Support.

7.2.65 DEVICE CONTROL REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting Reset to 0b.
1	Non-Fatal Error Reporting Enable	RW	0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting Reset to 0b.
2	Fatal Error Reporting Enable	RW	0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting Reset to 0b.
3	Unsupported Request Reporting Enable	RW	0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting Reset to 0b.
4	Enable Relaxed Ordering	RO	When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns ‘0’ when read. Reset to 0b.
7:5	Max_Payload_Size	RW	This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. Reset to 000b.
8	Extended Tag Field Enable	RW	Does not apply to PCI Express Switch. Returns ‘0’ when read. Reset to 0b.
9	Phantom Function Enable	RW	Does not apply to PCI Express Switch. Returns ‘0’ when read. Reset to 0b.
10	Auxiliary (AUX) Power PM Enable	RWS	When set, indicates that a device is enabled to draw AUX power independent of PME AUX power. Reset to 0b.
11	Enable No Snoop	RO	When set, it permits to set the No Snoop bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns ‘0’ when read. Reset to 0b.
14:12	Max_Read_ Request_Size	RO	This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 000b. Reset to 000b.
15	Reserved	RsvdP	Not Support.

7.2.66 DEVICE STATUS REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RW1C	Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
17	Non-Fatal Error Detected	RW1C	Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
18	Fatal Error Detected	RW1C	Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
19	Unsupported Request Detected	RW1C	Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
20	AUX Power Detected	RO	Asserted when the AUX power is detected by the Switch Reset to 1b.
21	Transactions Pending	RO	Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0b. Reset to 0b.
31:22	Reserved	RsvdP	Not Support.

7.2.67 LINK CAPABILITIES REGISTER – OFFSET CCh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Indicates the maximum speed of the Express link. 0001b: 2.5Gb/s 0010b: 5.0Gb/s Otherwise: Reserved Reset to 0010b.
9:4	Maximum Link Width	RO	Indicates the maximum width of the given PCIe Link. Reset to 00_0001b (x1).
11:10	Active State Power Management (ASPM) Support	RO	Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 11b.
14:12	L0s Exit Latency	RO	Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 011b.
17:15	L1 Exit Latency	RO	Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000b.
18	Clock Power Management	RO	For upstream port, a value of 1b indicates that component tolerates the removal of any reference clock via CLKREQ#. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 1b for Upstream port. Reset to 0b for Downstream ports.

BIT	FUNCTION	TYPE	DESCRIPTION
19	Surprise Down Capability Enable	RO	Valid for downstream ports only. Reset to 0b for Upstream port. Reset to 1b for Downstream ports.
20	Data Link Layer Active Reporting Capable	RO	For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port, this bit must be set to 1b. For Upstream Port, this bit must be hardwired to 0b. Reset to 0b for upstream port. Reset to 0b for downstream ports.
21	Link bw notify cap	RO	Reset to 0b for Upstream port. Reset to 1b for Downstream ports.
23:21	Reserved	RsvdP	Not Support.
31:24	Port Number	RO	Indicates the PCIe Port Number for the given PCIe Link. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h for Port 0. Reset to 01h for Port 1. Reset to 02h for Port 2.

7.2.68 LINK CONTROL REGISTER – OFFSET D0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Active State Power Management (ASPM) Control	RW	00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled. Reset to 00b.
2	Reserved	RsvdP	Not Support.
3	Read Completion Boundary (RCB)	RO	Does not apply to PCI Express Switch. Returns ‘0’ when read. Reset to 0b.
4	Link Disable	RW	At upstream port, it is not allowed to disable the link, so this bit is hardwired to ‘0’. For downstream ports, it disables the link when this bit is set. Reset to 0b.
5	Retrain Link	RW	At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 0b. For downstream ports, it initiates Link Retraining when this bit is set. This bit always returns 0b when read.
6	Common Clock Configuration	RW	0b: The components at both ends of a link are operating with asynchronous reference clock 1b: The components at both ends of a link are operating with a distributed common reference clock Reset to 0b.
7	Extended Synch	RW	When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. Reset to 0b.
8	Reserved	RsvdP	Not Support.
9	HW Autonomous Width Disable	RW	Reset to 0b.
10	Reserved	RO / RW	For upstream Port is RO and reset to 0b. For downstream Port is RW and Reset to 0b.
11	Reserved	RO / RW	For upstream Port is RO and reset to 0b. For downstream Port is RW and Reset to 0b.
15:12	Reserved	RsvdP	Not Support.

7.2.69 LINK STATUS REGISTER – OFFSET D0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	Indicate the negotiated speed of the Express link: 0001b: 2.5 Gb/s. 0010b: 5.0 Gb/s. Reset to 0010b.
25:20	Negotiated Link Width	RO	Indicates the negotiated width of the given PCIe link. 0001b: x1 link Reset to 0001b.
26	Training Error	RO	When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. Reset to 0b.
27	Link Training	RO	When set, indicates the link training is in progress. Hardware clears this bit once link training is complete. Reset to 0b.
28	Slot Clock Configuration	HwInt RO	0b: the Switch uses an independent clock irrespective of the presence of a reference on the connector 1b: the Switch uses the same reference clock that the platform provides on the connector The default value may be changed by the status of strapped pin, SMBus or auto-loading from EEPROM. Reset to the status of SLOTCLK strapped pin.
29	Data Link Layer Link Active	RO	Indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. Reset to 0b.
31:30	Reserved	RsvdP	Not Support.

7.2.70 SLOT CAPABILITIES REGISTER – OFFSET D4h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Present	RO	When set, it indicates that an Attention Button is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
1	Power Controller Present	RO	When set, it indicates that a Power Controller is implemented for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
2	Reserved	RsvdP	Not Support.
3	Attention Indicator Present	RO	When set, it indicates that an Attention Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
4	Power Indicator Present	RO	When set, it indicates that a Power Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
5	Hot-Plug Surprise	RO	When set, it indicates that a device present in this slot might be removed from the system without any prior notification. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
6	Hot-Plug Capable	RO	When set, it indicates that this slot is capable of supporting Hot-Plug operation. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
14:7	Slot Power Limit Value	RW	It applies to Downstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.
16:15	Slot Power Limit Scale	RW	It applies to Downstream Port only. Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00b.
18:17	Reserved	RsvdP	Not Support.
31:19	Physical Slot Number	RO	It indicates the physical slot number attached to this Port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.

7.2.71 SLOT CONTROL REGISTER – OFFSET D8h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Pressed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event. Reset to 0b.
1	Power Fault Detected Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event. Reset to 0b.
2	Reserved	RsvdP	Not Support.
3	Presence Detect Changed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event. Reset to 0b.
4	Command Completed Interrupt Enable	RW	When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command. Reset to 0b.
5	Hot-Plug Interrupt Enable	RW	When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events. Reset to 0b.
7:6	Attention Indicator Control	RW	Controls the display of Attention Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the ATTENTION_INDICATOR_* Messages. Reset to 11b.
9:8	Power Indicator Control	RW	Controls the display of Power Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the POWER_INDICATOR_* Messages. Reset to 11b.
10	Power Controller Control	RW	0b: reset the power state of the slot (Power On) 1b: set the power state of the slot (Power Off) Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
11	Reserved	RsvdP	Not Support.
12	Data Link Layer State Changed Enable	RW	If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. Reset to 0b.
15:13	Reserved	RsvdP	Not Support.

7.2.72 SLOT STATUS REGISTER – OFFSET D8h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
16	Attention Button Pressed	RW1C	When set, it indicates the Attention Button is pressed. Reset to 0b.
17	Power Fault Detected	RW1C	When set, it indicates a Power Fault is detected. Reset to 0b.
18	MRL Sensor Changed	RO	When set, it indicates a MRL Sensor Changed is detected. Reset to 0b.
19	Presence Detect Changed	RW1C	When set, it indicates a Presence Detect Changed is detected. Reset to 0b.
20	Command Completed	RW1C	When set, it indicates the Hot-Plug Controller completes an issued command. Reset to 0b.
21	MRL Sensor State	RO	Reflects the status of MRL Sensor. 0b: MRL Closed 1b: MRL Opened Reset to 0b.
22	Presence Detect State	HwInt RO	Indicates the presence of a card in the slot. 0b: Slot Empty 1b: Card Present in slot This register is implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), this bit returns 1b. Reset to 0b when PRSNT strapped pin is set to 1. Reset to 1b when PRSNT strapped pin is set to 0.
23	Reserved	RsvdP	Not Support.
24	Data Link Layer State Changed	RW1C	This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed. Reset to 1b.
31:25	Reserved	RsvdP	Not Support.

7.2.73 DEVICE CAPABILITIES REGISTER 2 – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
10:0	Device Capabilities 2	RO	Reset to 000h.
11	LTR Mechanism Supported	RO	A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism. Reset to 1b.
17:12	Device Capabilities 2	RO	Reset to 00h.
19:18	OBFF Supported	RO	This field indicates if OBFF is supported. Reset to 01b.
31:20	Device Capabilities 2	RO	Reset to 000h.

7.2.74 DEVICE CONTROL REGISTER 2 – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
9:0	Device Control 2	RO	Reset to 000h.
10	LTR Mechanism Enable	RW	Enable LTR Mechanism Reset to 0b.
12:11	Device Control 2	RO	Reset to 00b.
14:13	OBFF Enable	RW	Enable OBFF Mechanism and select the signaling method. Reset to 00b.
15	Device Control 2	RO	Reset to 0b.

7.2.75 DEVIDE STATUS REGISTER 2 – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device Status 2	RO	Reset to 0000_0000h.

7.2.76 LINK CAPABILITIES REGISTER 2 – OFFSET ECh

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Link Capabilities 2	RO	Reset to 0000_0000h.

7.2.77 LINK CONTROL REGISTER 2 – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Target Link Speed	RWS	Reset to 0010b.
4	Enter Compliance	RWS	Reset to 0b.
5	HW_AutoSpeed_Dis	RW	Reset to 0b.
6	Select_Deemp	RO	Reset to 0b for Upstream port. Reset to 1b for Downstream ports.
9:7	Tran_Margin	RWS	Reset to 000b.
10	Enter Modify Compliance	RWS	Reset to 0b.
11	Compliance SOS	RWS	Reset to 0b.
12	Compliance_Deemp	RWS	Reset to 0b.
15:13	Reserved	RsvdP	Not Support.

7.2.78 LINK STATUS REGISTER 2 – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Current De-emphasis Level	RO	Reset to 0b.
31:17	Link Status 2	RO	Reset to 0000h.

7.2.79 SLOT CAPABILITIES REGISTER 2 – OFFSET F4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Slot Capabilities 2	RO	Reset to 0000_0000h.

7.2.80 SLOT CONTORL REGISTER 2 – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Slot Control 2	RO	Reset to 0000h.

7.2.81 SLOT STATUS REGISTER 2 – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Slot Status 2	RO	Reset to 0000h.

7.2.82 PCI EXPRESS ADVANCED ERROR REPORTING CAPABILITY REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting.
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number.
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Extended VC capability register. Reset to 140h.

7.2.83 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Status	RW1CS	When set, indicates that the Training Error event has occurred. Reset to 0b.
3:1	Reserved	RsvdP	Not Support.
4	Data Link Protocol Error Status	RW1CS	When set, indicates that the Data Link Protocol Error event has occurred. Reset to 0b.
5	Surprise Down Error Status	RW1CS	When set, indicates that the Surprise Down Error event has occurred. It is valid for downstream ports only. Reset to 0b.
11:6	Reserved	RsvdP	Not Support.
12	Poisoned TLP Status	RW1CS	When set, indicates that a Poisoned TLP has been received or generated. Reset to 0b.
13	Flow Control Protocol Error Status	RW1CS	When set, indicates that the Flow Control Protocol Error event has occurred. Reset to 0b.
14	Completion Timeout Status	RW1CS	When set, indicates that the Completion Timeout event has occurred. Reset to 0b.
15	Completer Abort Status	RW1CS	When set, indicates that the Completer Abort event has occurred. Reset to 0b.
16	Unexpected Completion Status	RW1CS	When set, indicates that the Unexpected Completion event has occurred. Reset to 0b.
17	Receiver Overflow Status	RW1CS	When set, indicates that the Receiver Overflow event has occurred. Reset to 0b.
18	Malformed TLP Status	RW1CS	When set, indicates that a Malformed TLP has been received. Reset to 0b.
19	ECRC Error Status	RW1CS	When set, indicates that an ECRC Error has been detected. Reset to 0b.
20	Unsupported Request Error Status	RW1CS	When set, indicates that an Unsupported Request event has occurred. Reset to 0b.
21	ACS Violation Status	RW1CS	When set, indicates that an ACS Violation event has occurred Reset to 0b.
31:21	Reserved	RsvdP	Not Support.

7.2.84 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Mask	RWS	When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
3:1	Reserved	RsvdP	Not Support.
4	Data Link Protocol Error Mask	RWS	When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
5	Surprise Down Error Mask	RWS	When set, the Surprise Down Error event is not logged in the Header Log register and not issued as an Error Message to RC either. It is valid for downstream ports only. Reset to 0b.
11:6	Reserved	RsvdP	Not Support.
12	Poisoned TLP Mask	RWS	When set, an event of Poisoned TLP has been received or generated is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Flow Control Protocol Error Mask	RWS	When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
14	Completion Timeout Mask	RWS	When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
15	Completer Abort Mask	RWS	When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
16	Unexpected Completion Mask	RWS	When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
17	Receiver Overflow Mask	RWS	When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
18	Malformed TLP Mask	RWS	When set, an event of Malformed TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
19	ECRC Error Mask	RWS	When set, an event of ECRC Error has been detected is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
20	Unsupported Request Error Mask	RWS	When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
21	ACS Violation Mask	RWS	Reset to 0b
31:22	Reserved	RsvdP	Not Support.

7.2.85 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
3:1	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
4	Data Link Protocol Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
5	Surprise Down Error Severity	RWS	0b: Non-Fata 1b: Fatal It is valid for downstreams port only. Reset to 1b.
11:6	Reserved	RsvdP	Not Support.
12	Poisoned TLP Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
13	Flow Control Protocol Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
14	Completion Timeout Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
15	Completer Abort Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
16	Unexpected Completion Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
17	Receiver Overflow Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
18	Malformed TLP Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
19	ECRC Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0.
20	Unsupported Request Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
21	ACS violation Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
31:21	Reserved	RsvdP	Not Support.

7.2.86 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Status	RW1CS	When set, the Receiver Error event is detected. Reset to 0b.
5:1	Reserved	RsvdP	Not Support.
6	Bad TLP Status	RW1CS	When set, the event of Bad TLP has been received is detected. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
7	Bad DLLP Status	RW1CS	When set, the event of Bad DLLP has been received is detected. Reset to 0b.
8	REPLAY_NUM Rollover Status	RW1CS	When set, the REPLAY_NUM Rollover event is detected. Reset to 0b.
11:9	Reserved	RsvdP	Not Support.
12	Replay Timer Timeout Status	RW1CS	When set, the Replay Timer Timeout event is detected. Reset to 0b.
13	Advisory Non-Fatal Error status	RW1CS	When set, the Advisory Non-Fatal Error event is detected. Reset to 0b.
31:14	Reserved	RsvdP	Not Support.

7.2.87 CORRECTABLE ERROR MASK REGISTER – OFFSET 114 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Mask	RWS	When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
5:1	Reserved	RsvdP	Not Support.
6	Bad TLP Mask	RWS	When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
7	Bad DLLP Mask	RWS	When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
8	REPLAY_NUM Rollover Mask	RWS	When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:9	Reserved	RsvdP	Not Support.
12	Replay Timer Timeout Mask	RWS	When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Advisory Non-Fatal Error Mask	RWS	When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either. Reset to 1b.
31:14	Reserved	RsvdP	Not Support.

7.2.88 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	First Error Pointer	ROS	It indicates the bit position of the first error reported in the Uncorrectable Error Status register. Reset to 00000b.
5	ECRC Generation Capable	RO	When set, it indicates the Switch has the capability to generate ECRC. Reset to 1b.
6	ECRC Generation Enable	RWS	When set, it enables the generation of ECRC when needed. Reset to 0b.
7	ECRC Check Capable	RO	When set, it indicates the Switch has the capability to check ECRC. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
8	ECRC Check Enable	RWS	When set, the function of checking ECRC is enabled. Reset to 0b.
31:9	Reserved	RsvdP	Not Support.

7.2.89 HEADER LOG REGISTER – OFFSET From 11Ch to 128h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	1st DWORD	ROS	Hold the 1st DWORD of TLP Header. The Head byte is in big endian.
63:32	2nd DWORD	ROS	Hold the 2nd DWORD of TLP Header. The Head byte is in big endian.
95:64	3rd DWORD	ROS	Hold the 3rd DWORD of TLP Header. The Head byte is in big endian.
127:96	4th DWORD	ROS	Hold the 4th DWORD of TLP Header. The Head byte is in big endian.

7.2.90 PCI EXPRESS VIRTUAL CHANNEL CAPABILITY REGISTER – OFFSET 140h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel.
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number.
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Power Budgeting capability register. Reset to 20Ch.

7.2.91 PORT VC CAPABILITY REGISTER 1 – OFFSET 144h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended VC Count	RO HwInt	It indicates the number of extended Virtual Channels in addition to the default VC supported by the Switch. The default value may be changed by the status of strapped pin, or auto-loading from EEPROM. Bit[2:1]: Reset to 00b. Bit[0]: Reset to the status of VC1_EN strapped pin.
3	Reserved	RsvdP	Not Support.
6:4	Low Priority Extended VC Count	RO	It indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. The default value may be changed by auto-loading from EEPROM. Reset to 000b.
7	Reserved	RsvdP	Not Support.
9:8	Reference Clock	RO	It indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock. Reset to 00b.
11:10	Port Arbitration Table Entry Size	RO	Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits. Reset to 10b.
31:12	Reserved	RsvdP	Not Support.

7.2.92 PORT VC CAPABILITY REGISTER 2 – OFFSET 148h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	VC Arbitration Capability	RO	It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC. Reset to 03h if offset 144h.bit[0]=1. Reset to 00h if offset 144h.bit[0]=0.
23:8	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	VC Arbitration Table Offset	RO	It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 03h if offset 144h.bit[0]=1. Reset to 00h if offset 144h.bit[0]=0.

7.2.93 PORT VC CONTROL REGISTER – OFFSET 14Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Load VC Arbitration Table	RW	When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
3:1	VC Arbitration Select	RW	This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Switch are 0b and 1b. Other value than these written into this register will be treated as default. Reset to 0b.
15:4	Reserved	RsvdP	Not Support.

7.2.94 PORT VC STATUS REGISTER – OFFSET 14Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	VC Arbitration Table Status	RO	When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of “Load VC Arbitration Table” is set. Reset to 0b.
31:17	Reserved	RsvdP	Not Support.

7.2.95 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. Reset to 09h.
13:8	Reserved	RsvdP	Not Support.
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch. Reset to 0b.
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by auto-loading from EEPROM. Reset to 7Fh.
23	Reserved	RsvdP	Not Support.
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 04h for Port Arbitration Table (0).

7.2.96 VC RESOURCE CONTROL REGISTER (0) – OFFSET 154h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TC/VC Map	RW	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. The default value may be changed by auto-loading from EEPROM. Reset to FFh.
15:8	Reserved	RsvdP	Not Support.
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b and 011b at VC0, other value than these written into this register will be treated as default. Reset to 000b.
23:20	Reserved	RsvdP	Not Support.
26:24	VC ID	RO	This field assigns a VC ID to the VC resource. Reset to 000b.
30:27	Reserved	RsvdP	Not Support.
31	VC Enable	RW	0b: disables this Virtual Channel 1b: enables this Virtual Channel Reset to 1b.

7.2.97 VC RESOURCE STATUS REGISTER (0) – OFFSET 158h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Reserved	RsvdP	Not Support.
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of “Load Port Arbitration Table” is set. Reset to 0b.
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. Reset to 0b.
31:18	Reserved	RsvdP	Not Support.

7.2.98 VC RESOURCE CAPABILITY REGISTER (1) – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. Reset to 19h if offset 144h.bit[0]=1. Reset to 00h if offset 144h.bit[0]=0.
13:8	Reserved	RsvdP	Not Support.
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by auto-loading from EEPROM. Reset to 7Fh if offset 144h.bit[0]=1. Reset to 00h if offset 144h.bit[0]=0.
23	Reserved	RsvdP	Not Support.
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 08h for Port Arbitration Table (1) if offset 144h.bit[0]=1. Reset to 00h if offset 144h.bit[0]=0.

7.2.99 VC RESOURCE CONTROL REGISTER (1) – OFFSET 160h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TC/VC Map	RW (Exception for bit0)	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this filed is read-only and must be set to "0" for the VC1. The default value may be changed by auto-loading from EEPROM. Reset to 00h.
15:8	Reserved	RsvdP	Not Support.
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b, 011b and 100b at VC1, other value than these written into this register will be treated as default. Reset to 000b.
23:20	Reserved	RsvdP	Not Support.
26:24	VC ID	RW	This field assigns a VC ID to the VC resource. Reset to 001b if offset 144h.bit[0]=1. Reset to 000b if offset 144h.bit[0]=0.
30:27	Reserved	RsvdP	Not Support.
31	VC Enable	RW	0b: disables this Virtual Channel 1b: enables this Virtual Channel Reset to 0b.

7.2.100 VC RESOURCE STATUS REGISTER (1) – OFFSET 164h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Reserved	RsvdP	Not Support.
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set. Reset to 0b.
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. Reset to 0b.
31:18	Reserved	RsvdP	Not Support.

7.2.101 VC ARBITRATION TABLE REGISTER – OFFSET 170h

The VC arbitration table is a read-write register array that contains a table for VC arbitration. Each table entry allocates four bits, of which three bits are used to represent VC ID and one bit is reserved. A total of 32 entries are used to construct the VC arbitration table. The layout for this register array is shown below.

Table 7-1 Register Array Layout for VC Arbitration

31 - 28	27 - 24	23 - 20	19 - 16	15 - 12	11 - 8	7 - 4	3 - 0	Byte Location
Phase [7]	Phase [6]	Phase [5]	Phase [4]	Phase [3]	Phase [2]	Phase [1]	Phase [0]	00h
Phase [15]	Phase [14]	Phase [13]	Phase [12]	Phase [11]	Phase [10]	Phase [9]	Phase [8]	04h
Phase [23]	Phase [22]	Phase [21]	Phase [20]	Phase [19]	Phase [18]	Phase [17]	Phase [16]	08h
Phase [31]	Phase [30]	Phase [29]	Phase [28]	Phase [27]	Phase [26]	Phase [25]	Phase [24]	0Ch

7.2.102 PORT ARBITRATION TABLE REGISTER (0) and (1) – OFFSET 180h and 1C0h

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 128 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

Table 7-2 Table Entry Size in 4 Bits

63 - 56	55 - 48	47 - 40	39 - 32	31 - 24	23 - 16	15 - 8	7 - 0	Byte Location
Phase [15:14]	Phase [13:12]	Phase [11:10]	Phase [9:8]	Phase [7:6]	Phase [5:4]	Phase [3:2]	Phase [1:0]	00h
Phase [31:30]	Phase [29:28]	Phase [27:26]	Phase [25:24]	Phase [23:22]	Phase [21:20]	Phase [19:18]	Phase [17:16]	08h
Phase [47:46]	Phase [45:44]	Phase [43:42]	Phase [41:40]	Phase [39:38]	Phase [37:36]	Phase [35:34]	Phase [33:32]	10h
Phase [63:62]	Phase [61:60]	Phase [59:58]	Phase [57:56]	Phase [55:54]	Phase [53:52]	Phase [51:50]	Phase [49:48]	18h
Phase [79:78]	Phase [77:76]	Phase [75:74]	Phase [73:72]	Phase [71:70]	Phase [69:68]	Phase [67:66]	Phase [65:64]	20h
Phase [95:94]	Phase [93:92]	Phase [91:90]	Phase [89:88]	Phase [87:86]	Phase [85:84]	Phase [83:82]	Phase [81:80]	28h
Phase [111:110]	Phase [109:108]	Phase [107:106]	Phase [105:104]	Phase [103:102]	Phase [101:100]	Phase [99:98]	Phase [97:96]	30h
Phase [127:126]	Phase [125:124]	Phase [123:122]	Phase [121:120]	Phase [119:118]	Phase [117:116]	Phase [115:114]	Phase [113:112]	38h

7.2.103 PCI EXPRESS POWER BUDGETING CAPABILITY REGISTER – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting.
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number.
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Extended ACS capability register/LTR capability register. Reset to 230h for Upstream port. Reset to 220h for Downstream ports.

7.2.104 DATA SELECT REGISTER – OFFSET 210h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Data Selection	RW	It indexes the power budgeting data reported through the data register. When 00h, it selects D0 Max power budget When 01h, it selects D0 Sustained power budget Other values would return zero power budgets, which means not supported Reset to 00h.
31:8	Reserved	RsvdP	Not Support.

7.2.105 POWER BUDGETING DATA REGISTER – OFFSET 214h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Base Power	RO	It specifies the base power value in watts. This value represents the required power budget in the given operation condition. The default value may be changed by auto-loading from EEPROM. Reset to 04h.
9:8	Data Scale	RO	It specifies the scale to apply to the base power value. Reset to 00b.
12:10	PM Sub State	RO	It specifies the power management sub state of the given operation condition. It is initialized to the default sub state. Reset to 000b.
14:13	PM State	RO	It specifies the power management state of the given operation condition. It defaults to the D0 power state. Reset to 00b.
17:15	Type	RO	It specifies the type of the given operation condition. It defaults to the Maximum power state. Reset to 111b.
20:18	Power Rail	RO	It specifies the power rail of the given operation condition. Reset to 010b.
31:21	Reserved	RsvdP	Not Support.

7.2.106 POWER BUDGET CAPABILITY REGISTER – OFFSET 218h

BIT	FUNCTION	TYPE	DESCRIPTION
0	System Allocated	RO	When set, it indicates that the power budget for the device is included within the system power budget. The default value may be changed by auto-loading from EEPROM. Reset to 0b.
31:1	Reserved	RsvdP	Not Support.

7.2.107 ACS EXTENDED CAPABILITY HEADER – OFFSET 220h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 000Dh to indicate PCI Express Extended Capability ID for ACS Extended Capability.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Pointer points to the PCI Express Extended L1PM Substates Extended capability register. Reset to 240h.

7.2.108 ACS CAPABILITY REGISTER – OFFSET 224h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	ACS Source Validation	RO	Indicated the implements of ACS Source Validation. Reset to 1b.
1	ACS Translation Blocking	RO	Indicated the implements of ACS Translation Blocking. Reset to 1b.
2	ACS P2P Request Redirect	RO	Indicated the implements of ACS P2P Request Redirect. Reset to 1b.
3	ACS P2P Completion Redirect	RO	Indicated the implements of ACS P2P Completion Redirect. Reset to 1b.
4	ACS Upstream Forwarding	RO	Indicated the implements of ACS Upstream Forwarding. Reset to 1b.
5	ACS P2P Egress control	RO	Indicated the implements of ACS P2P Egress control. Reset to 1b.
6	ACS Direct Translated P2P	RO	Indicated the implements of ACS Direct Translated P2P. Reset to 1b.
7	Reserved	RsvdP	Not Support.
15:8	Egress Control Vector Size	RO	Encodings 01h –FFh directly indicate the number of applicable bits in the Egress Control Vector. Reset to 08h.
16	ACS Source Validation Enable	RW	Enable the source validation. Reset to 0b.
17	ACS Translation Blocking Enable	RW	Enable ACS Translation Blocking. Reset to 0b.
18	ACS P2P Request Redirect	RW	Enable ACS P2P Request Redirect. Reset to 0b.
19	ACS P2P Completion Redirect Enable	RW	Enable ACS P2P Completion Redirect. Reset to 0b.
20	ACS Upstream Forwarding Enable	RW	Enable ACS Upstream Forwarding. Reset to 0b.
21	ACS P2P Egress control Enable	RW	Enable ACS P2P Egress control. Reset to 0b.
22	ACS Direct Translated P2P Enable	RW	Enable ACS Direct Translated P2P. Reset to 0b.
31:23	Reserved	RsvdP	Not Support.

7.2.109 EGRESS CONTROL VECTOR – OFFSET 228h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Egress Control Vector	RW	When a given bit is set, peer-to-peer requests targeting the associated Port are blocked or redirected. Reset to 00h.
31:8	Reserved	RsvdP	Not Support.

7.2.110 LTR EXTENDED CAPABILITY HEADER – OFFSET 230h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 0018h to indicate PCI Express Extended Capability ID for LTR Extended Capability.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Pointer points to the PCI Express Extended L1PM Substates Extended capability register. Reset to 240h.

7.2.111 MAX SNOOP LATENCY REGISTER – OFFSET 234h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
9:0	Max Snoop Latency Value	RW	.Specifies the maximum snoop latency that a device is permitted to request Reset to 000h.
12:10	Max Snoop Latency Scale	RW	This register provides a scale for the value contained within the Maximum Snoop Latency Value field Reset to 000b
15:13	Reserved	RsvdP	Not Support.

7.2.112 MAX NO-SNOOP LATENCY REGISTER – OFFSET 234h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
25:16	Max No-Snoop Latency Value	RW	.Specifies the maximum no-snoop latency that a device is permitted to request Reset to 000h.
28:26	Max No-Snoop Latency Scale	RW	This register provides a scale for the value contained within the Maximum No-Snoop Latency Value field Reset to 000b.
31:29	Reserved	RsvdP	Not Support.

7.2.113 LI PM SUBSTATES EXTENDED CAPABILITY HEADER – OFFSET 240h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 001Eh to indicate PCI Express Extended Capability ID for L1 PM Substates Extended Capability. Reset to 001Eh.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Pointer points to the PCI Express Extended PTM Extended capability register/DPC Extended capability register. Reset to 260h for Upstream port. Reset to 250h for Downstream ports.

7.2.114 L1 PM SUBSTATES CAPABILITY REGISTER – OFFSET 244h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Reserved	RsvdP	Not Support.
1	PCI-PM L1.1 Supported	RO	When set this bit indicates that PCI-PM L1.1 is supported and must be set by all ports implementing L1 OM Substates. The default value may be changed by auto-loading from EEPROM. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
2	Reserved	RsvdP	Not Support.
3	ASPM L1.1 Supported	RO	When set this bit indicates that ASPM L1.1 is supported. The default value may be changed by SMBus, I2C or auto-loading from EEPROM. Reset to 0b.
4	L1 PM Substates Supported	RO	When set this bit indicates that this port supports L1 PM Substates. The default value may be changed by auto-loading from EEPROM. Reset to 1b.
31:5	Reserved	RsvdP	Not Support.

7.2.115 L1 PM SUBSTATES CONTROL 1 REGISTER – OFFSET 248h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Reserved	RsvdP	Not Support.
1	PCI-PM L1.1 Enable	RW	When set this bit enables PCI-PM L1.1. Required for both upstream and downstream ports. Reset to 0b.
2	Reserved	RsvdP	Not Support.
3	ASPM L1.1 Enable	RW	When set this bit enables ASPM L1.1. Required for both upstream and downstream ports. Reset to 0b.
31:4	Reserved	RsvdP	Not Support.

7.2.116 L1 PM SUBSTATES CONTROL 2 REGISTER – OFFSET 24Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RO	Reset to 0000_0000h.

7.2.117 DPC EXTENDED CAPABILITY HEADER – OFFSET 250h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 001Dh to indicate PCI Express Extended Capability ID for DPC Extended Capability. Reset to 001Dh.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Read as 000h. No other ECP registers.

7.2.118 DPC CAPABILITY REGISTER – OFFSET 254h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	DPC Interrupt Message Number	RO	This field indicates which MSI vector is used for the interrupt message generated in association with the DPC Capability structure. Reset to 0_0001b.
15:5	Reserved	RsvdP	Not Support.

7.2.119 DPC CONTROL REGISTER – OFFSET 254h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
17:16	DPC Trigger Enable	RW	This field enables DPC and controls the conditions that cause DPC to be triggered. 00b… DPC is disabled 01b… DPC is enabled and is triggered when the Downstream port detects and unmasked uncorrectable error or when the Downstream port receives an ERR_FATAL message. 10b… DPC is enabled and is triggered when the Downstream port detects an unmasked uncorrectable error or when the Downstream port receives an ERR_NONFATAL or ERR_FATAL message 11b… Reserved Reset to 00b.
18	DPC Completion Control	RW	This bit controls the Completion Status for Completions formed during DPC. 0b: Completer Abort (CA) Completion Status 1b: Unsupported Request (UR) Completion Status Reset to 0b.
19	DPC Interrupt Enable	RW	When set, this bit enables the generation of an interrupt to indicate that DPC has been triggered. Reset to 0b.
20	DPC ERR_COR Enable	RW	When set, this bit enables the sending of an ERR_COR message to indicate that DPC has been triggered. Reset to 0b.
31:21	Reserved	RsvdP	Not Support.

7.2.120 DPC STATUS REGISTER – OFFSET 258h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	DPC Trigger Status	RW1C	When set, this bit indicates that DPC has been triggered. Reset to 0b.
2:1	DPC Trigger Reason	RW1C	This field indicates why DPC has been triggered. 00b… DPC was triggered due to an unmasked uncorrectable error 01b… DPC was triggered due to receiving an ERR_NONFATAL 10b… DPC was triggered due to receiving an ERR_FATAL 11b… Reserved Reset to 2’b00.
3	DPC Interrupt Status	RW1C	This bit is set if DPC is triggered while the DPC interrupt Enable bit is set. Reset to 0b.
15:4	Reserved	RsvdP	Not Support.

7.2.121 DPC ERROR SOURCE ID REGISTER – OFFSET 258h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	DPC Error Source ID	RO	When the DPC Trigger Reason field indicates that DPC was triggered due to the reception of an ERR_NONFATAL or ERR_FATAL, this register contains the Requester ID of the received message. Otherwise, the value of this register is undefined. Reset to 0000h.

7.2.122 PTM EXTENDED CAPABILITY HEADER REGISTER – OFFSET 260h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PCI Express Extended Capability ID	RO	Read as 001Fh to indicate PCI Express Extended Capability ID for PTM Extended Capability.
19:16	Capability Version	RO	Must be 1h for this version.
31:20	Next Capability ID	RO	Read as 000h. No other ECP registers.

7.2.123 PTM CAPABILITY REGISTER – OFFSET 264h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	PTM Requester Capable	RO	Read as 1b to indicate the switch implement the PTM Requester role.
1	PTM Responder Capable	RO	Read as 1b to indicate the switch implement the PTM Responder role.
2	PTM Root Capable	RO	Read as 1b to indicate the switch implement a PTM Time Source Role and are capable of serving as the PTM Root.
7:3	Reserved	RsvdP	Not Support.
15:8	Local Clock Granularity	RO	Indicates the period of this Time Source's local clock in ns. Reset to 00h.
31:16	Reserved	RsvdP	Not Support.

7.2.124 PTM CONTROL REGISTER – OFFSET 268h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	PTM Enable	RW	When set, this function is permitted to participate in the PTM mechanism according to its selected role. Reset to 0b.
1	Root Select	RW	When set, if the PTM Enable bit is also set, this Time Source is the PTM Root. Reset to 0b.
7:2	Reserved	RsvdP	Not Support.
15:8	Effective Granularity	RW	This field provides information relating to the expected accuracy of the PTM clock, but doesn not otherwise affect the PTM mechanism. Reset to 00h.
31:16	Reserved	RsvdP	Not Support.

7.2.125 MISC CONTROL 0 REGISTER – OFFSET 300h

BIT	FUNCTION	TYPE	DESCRIPTION
19:0	CLKREQ_L Wait Time	RW	Once entering L1.1 power state, the port will deassert CLKREQ_L immediately. However, CLKREQ_L signal is an open-drain wire-or signal with the link partner. If the link partner does not deassert CLKREQ_L for a certain period of time, which is defined by CLKREQ_L Wait Time, the port will assert CLKREQ_L again to resume back to L1 state. The CLKREQ_L wait time decides how long the switch will wait for CLKREQ_L being deasserted by the link partner. The unit is "10 ns". Reset to 0_0FFFh. It is about 40 us.
31:20	Reserved	RsvdP	Not Support.

7.2.126 MISC CONTROL 1 REGISTER – OFFSET 304h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PM_L1.1 Delay Time	RW	It is used to decide when the port will enter into PM L1.1 state from L1 state. If the value of PM L1.1 delay time is smaller, the power saving is much effective, but it takes longer time to recover from low power state. If the timer delay value is larger, the power saving is not much effective, but it recovers from low power state to normal power state quicker. The smallest value for PM L1.1 Delay is 0001h, which is equivalent to 4 ns. Reset to 01FFh.
31:16	ASPM_L1.1 Delay Time	RW	It is used to decide when the port will enter into ASPM L1.1 state from L1 state. If the value of ASPM L1.1 delay time is smaller, the power saving is much effective, but it takes longer time to recover from low power state. If the timer delay value is larger, the power saving is not much effective, but it recovers from low power state to normal power state quicker. The smallest value for ASPM L1.1 Delay is 0001h, which is equivalent to 4ns. Reset to 01FFh.

7.2.127 MISC CONTROL 2 REGISTER – OFFSET 308h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Misc Control 2	RW	Reset to 0.

7.2.128 MISC CONTROL 3 REGISTER – OFFSET 30Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Misc Control 3	RW	Reset to 0.

7.2.129 MISC CONTROL 4 REGISTER – OFFSET 310h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Misc Contro 4	RW	Reset to 000F_FFFFh.

7.2.130 PHY/DLL/TL ERROR COUNTER – OFFSET 318h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	PHY/DLL/TL Error Counter	RO	Indicates the error number. Reset to 00h.
16	CPL Available Credit Error	RW1CS	When set, the CPL available credit error is detected. Reset to 0b.
17	NP Available Credit Error	RW1CS	When set, the NP available credit error is detected. Reset to 0b.
18	Post Available Credit Error	RW1CS	When set, the Post available credit error is detected. Reset to 0b.
23:19	Reserved	RsvdP	Not Support.

BIT	FUNCTION	TYPE	DESCRIPTION
28:24	PHY/DLL/TL Error Source Select	RW	0_0000b: training error 0_0001b: uc_sts error 0_0011b: acs error 0_0100b: rx error 0_0101b: replay rollover error 0_0110b: replay timerout error 0_0111b: cpl available credit error 0_1000b: np available credit error 0_1001b: post available credit error 0_1010b: rx nack 0_1011b: rx nack 0_1100b: rx recovery 0_1101b: tx recovery Others: reserved Reset to 0_0000b.
29	Reserved	RsvdP	Not Support.
30	Error Counter Clear	RW	When set, PHY/DLL/TL Error counter is clear. When read, will return '1' always. Reset to 0b.
31	Enable Error Counter	RW	When set, it will enable PHY/DLL/TL Error counter. Reset to 0b.

7.2.131 PORT PHYSICAL LAYER COMMAND AND STATUS REGISTER – OFFSET 320h

BIT	FUNCTION	TYPE	DESCRIPTION
0	PORT0_Loopback_ CMD	RW	Test used only. Reset to 0b.
1	PORT0_Scramble_ Disable_CMD	RW	Test used only. Reset to 0b.
2	PORT0_Compliance_ Receive	RW	Test used only. Reset to 0b.
3	PORT0_ LOOPBACK_ST_I	RW	Test used only. Reset to 0b.
4	PORT0_Rate_Ctrl	RW	Test used only. Reset to 0b.
5	PORT0_Deemphasis_ Ctrl	RW	Test used only. Reset to 0b.
6	PORT0_Compliance_ Mode	RW	Test used only. Reset to 0b.
7	Reserved	RsvdP	Not Support.
8	PORT1_Loopback_ CMD	RW	Test used only. Reset to 0b.
9	PORT1_Scramble_ Disable_CMD	RW	Test used only. Reset to 0b.
10	PORT1_Compliance_ Receive	RW	Test used only. Reset to 0b.
11	PORT1_ LOOPBACK_ST_I	RW	Test used only. Reset to 0b.
12	PORT1_Rate_Ctrl	RW	Test used only. Reset to 0b.
13	PORT1_Deemphasis_ Ctrl	RW	Test used only. Reset to 0b.
14	PORT1_Compliance_ Mode	RW	Test used only. Reset to 0b.
15	Reserved	RsvdP	Not Support.
16	PORT2_Loopback_ CMD	RW	Test used only. Reset to 0b.
17	PORT2_Scramble_ Disable_CMD	RW	Test used only. Reset to 0b.
18	PORT2_Compliance_ Receive	RW	Test used only. Reset to 0b.
19	PORT2_ LOOPBACK_ST_I	RW	Test used only. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
20	PORT2_Rate_Ctrl	RW	Test used only. Reset to 0b.
21	PORT2_Deemphasis_Ctrl	RW	Test used only. Reset to 0b.
22	PORT2_Compliance_Mode	RW	Test used only. Reset to 0b.
31:23	Reserved	RsvdP	Not Support.

7.2.132 PORT DISABLE/QUIET/TEST PATTERN RATE REGISTER – OFFSET 324h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Port Disable	RW	0b: Enable Link Training operation 1b: LTSSM remains in the Detect.Quiet state. Bit[0]: for Port 0 Bit[1]: for Port 1 Bit[2]: for Port 2 Reset to 000b.
7:3	Reserved	RsvdP	Not Support.
10:8	Port Quiet/Test Pattern Rate	RW	0b: LTSSM is allowed to exit the Detect.Quiet state 1b: LTSSM remains in the Detect.Quiet state Bit[8]: for Port 0 Bit[9]: for Port 1 Bit[10]: for Port 2 Reset to 000b.
15:11	Reserved	RsvdP	Not Support.
18:16	Port Pattern Rate	RW	Test used only. Bit[16]: for Port 0 Bit[17]: for Port 1 Bit[18]: for Port 2 Reset to 000b.
31:19	Reserved	RsvdP	Not Support.

7.2.133 CSR_LED0 – OFFSET 328h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	LED_CSR00	RW	Reset to 00h.
8	LED_CSR01	RW	Reset to 0b.
31:9	Reserved	RsvdP	Not Support.

7.2.134 CSR_LED1 – OFFSET 32Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	LED_CSR10	RW	Reset to 00h.
15:8	LED_CSR11	RW	Reset to 00h.
23:16	LED_CSR12	RW	Reset to 00h.
31:24	LED_CSR13	RW	Reset to 00h.

7.2.135 LTSSM_CSR – OFFSET 33Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	LTSSM_CSR	RO	The default value may be changed by auto-loading from EEPROM. Reset to 00h.
31:8	Reserved	RsvdP	Not Support.

7.2.136 MAC_CSR – OFFSET 340h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	MAC_CSR	RO	The default value may be changed by auto-loading from EEPROM. Bit[4]: Adaptive ACK Policy Bit[5]: Fix_Disable_Detect Reset to 04h.
31:16	Reserved	RsvdP	Not Support.

7.2.137 TL_CSR1 – OFFSET 344h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TL_CSR1	RW	Reset to 03h.
31:8	Reserved	RsvdP	Not Support.

7.2.138 DEBUGOUT CONTROL – OFFSET 348h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	Debug Mode Select	RW	Debug mode select. Selects a signal group for probing the current internal status. For example, “0” represents LTSSM signal group. As to other values, please inquire internal team for further information,
7:5	Debug Port_Select	RW	Selects a port number for monitoring at a given signal group.
8	Debug Output Start	RW	Start to capture debug output data.
31:9	Reserved	RsvdP	Not Support.

7.2.139 DEBUGOUT DATA – OFFSET 34Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Debug Output Data	RO	Content of the debug output data.

8 CLOCK SCHEME

The built-in HCSL integrated reference clock buffer of the PI7C9X2G304SV supports three reference clock outputs. It can be enabled and disabled by strapping the CLKBUF_PD pin.

When CLKBUF_PD pin is asserted low, the integrated reference clock buffer is enabled. The integrated reference clock buffer distributes a single 100MHz reference clock input to three reference clock output pairs, REFCLKO_P[2:0] and REFCLKO_N[2:0]. One of the integrated reference clock buffer output pairs of the Switch can be connected to the Switch through REFCLKP/N pins, and the other two integrated reference clock buffer outputs can be used by downstream devices.

Specified reference clock output pairs can be disabled through the Clock Buffer Control bits in the Operation Mode Register (offset 98h.bit[23:16]) via either I2C, SMBUS or EEPROM.

The integrated reference clock buffer requires an external 100MHz differential clock input pair through REFCLKI_P and REFCLKI_N pins as shown in Table 5-1.

Table 8-1 AC Switching and DC Electrical Characteristics for REFCLKIP/N and REFCLKOP/N[2:0]

Symbol	Parameters	Min.	Typ.	Max.	Unit	Note
F_{IN}	Reference Clock Frequency		100		MHz	
T_{rise}/ T_{fall}	Rise and Fall Time in 20-80%	175		700	ps	2
ΔT_{rise}/ ΔT_{fall}	Rise and Fall Time Variation			125	ps	2
T_{pd}	Propagation Delay	2.5		6.5	ns	
V_{HIGH}	Voltage High including overshoot	660		1150	mV	2
V_{LOW}	Voltage Low including undershoot	-300		V_{HIGH}-0.5V	mV	2
V_{cross}	Absolute crossing point voltage	250		550	mV	2
V_{swing}	Voltage including overshoot	300		1800	mV	2, 4
T_{DC}	Duty Cycle	45		55	%	3

Note:
1. Test configuration is Rs=33.2Ω and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. If the reference clock input is HCSL type, it should use DC coupling; if not in HCSL protocol (ex: LVPECL, LVDS , etc), it should be AC coupling, and refer to application note to add application circuit to rebuild dc bias. If rebuild dc bias for the best 400mV, there is no limit on the V_{swing}. However, there have two exceptions can be accepted:
   a. If input is LVPECL, use ac-coupling and no rebuild dc bias, the min V_{swing} is 550mV (single ended).
   b. If input is LVDS with 100 ohm cross at the inputs and use dc-coupling, the min V_{swing} is 250mV (single ended).

When CLKBUF_PD pin is asserted high, the clock buffer is disabled. PI7C9X2G304SV requires an external 100MHz different clock input pair through REFCLKP/N Pins as shown in Table 8-2.

Table 8-2 AC Switching and DC Electrical Characteristics for REFCLKP/N

Symbol	Parameters	Min.	Typ.	Max.	Unit	Note
F_{IN}	Reference Clock Frequency		100		MHz	1, 2
A_j	Accuracy	-300		+300	ppm	3
$T_{REFCLK-HF-RMS}$	> 1.5 MHz to Nyquist RMS jitter after applying PCIe filter function			3.1	ps RMS	3
$T_{REFCLK-LF-RMS}$	10 kHz - 1.5 MHz RMS jitter			3.0	ps RMS	3
SSC_{freq}	Spread Spectrum Clock frequency	30		33	kHz	3
T_{rise}/ T_{fall}	Rise and Fall Time in 20-80%	175		700	ps	2
ΔT_{rise}/ ΔT_{fall}	Rise and Fall Time Variation			125	ps	2
T_{pd}	Propagation Delay	2.5		6.5	ns	
V_{HIGH}	Voltage High including	0.8			V	2

Symbol	Parameters	Min.	Typ.	Max.	Unit	Note
	overshoot					
V_{LOW}	Voltage Low including undershoot			800	mV	2
V_{swing}	Voltage including overshoot	300			mV	2
T_{DC}	Duty Cycle	45		55	%	3

Note:

1. Does not include ±300ppm. Only certain clock frequencies will produce valid PCI Express data.
2. Measurement taken from Single-end waveform.
3. Measurement taken from Differential waveform.
4. As PCIe PHY accept CML type reference clock source and will rebuild command mode voltage by itself, it needs add ac-coupling.

When implement L1.1 function, the connection of REFCLKO_P[2:0] and REFCLKO_N[2:0] to the REFCLKP/N pins of PI7C9X2G304SV and the reference clock input of downstream-port devices have to follow the table shown below.

Table 8-3 Connection Map for REFCLKO_P/N[2:0]

Reference Clock Source Pins	REFCLKOP [0] REFCLKON [0]	REFCLKO_P[1] REFCLKO_N[1]	REFCLKO_P[2] REFCLKO_N[2]
Reference Clock Destination Pins	REFCLKP REFCLKN	Downstream port-1 device	Downstream port-2 device

The REFCLKO_P/N[2:0] is not only enabled or disabled by a global control signal CLKBUF_PD, but also controlled by CLKREQ_L[2:0] pins and internal downstream-port device clock status individually based on L1 PM Substate rule. The output control signals for REFCLKO_P/N[2:0] are mapped as the following table.

Table 8-4 Output Control for REFCLKO_P/N[2:0]

Reference Clock Source Pins	REFCLKOP [0] REFCLKON [0]	REFCLKO_P[1] REFCLKO_N[1]	REFCLKO_P[2] REFCLKO_N[2]
Clock Request Control Pins	CLKREQ_L[0]	CLKREQ_L[1]	CLKREQ_L[2]

The CLKREQ_L[0] is an upstream control signal that should be connected from the switch output with external pull-up to the CLKREQ_L pin on the host chip (Root Complex). The switch combines the CLKREQ_L[2:1] and drives the resulting signal out on the CLKREQ_L[0]. When endpoints do not have any packets to transmit, the switch and endpoints will not drive CLKREQ_L[2:1], CLKREQ_L[2:1] will be high due to external pull-up resistor and the reference clock REFCLKOP/N[2:1] for down ports will stop. Then, the switch does not drive the CLKREQ_L[0] low on its upstream port. If the Root Complex does not have any packets requiring transmission, it does not drive the CLKREQ_L[0] either. In this case, the CLKREQ_L[0] will be high due to external pull-up resistor and the reference clock REFCLKO/P[0] for the upstream port will stop.

9 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X2G304SV for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

9.1 INSTRUCTION REGISTER

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up.
PI7C9X2G304SV implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in the following table. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction.

Table 9-1 Instruction Register Codes

Instruction	Operation Code (binary)	Register Selected	Operation
EXTEST	00000	Boundary Scan	Drives / receives off-chip test data
SAMPLE	00001	Boundary Scan	Samples inputs / pre-loads outputs
HIGHZ	00101	Bypass	Tri-states output and I/O pins except TDO pin
CLAMP	00100	Bypass	Drives pins from boundary-scan register and selects Bypass register for shifts
IDCODE	01100	Device ID	Accesses the Device ID register, to read manufacturer ID, part number, and version number
BYPASS	11111	Bypass	Selected Bypass Register
INT_SCAN	00010	Internal Scan	Scan test
PHY_TEST_SIG	01001	Private	Private
MEM_BIST	01010	Memory BIST	Memory BIST test

9.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X2G304SV.

9.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 9-2 JTAG Device ID Register

Bit	Type	Value	Description
31-28	RO	0001	Version number
27-12	RO	0000010100001000	Last 4 digits (hex) of the die part number
11-1	RO	01000111111	Pericom identifier assigned by JEDEC
0	RO	1	Fixed bit equal to 1'b1

9.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X2G304SV package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

9.5 JTAG BOUNDARY SCAN REGISTER ORDER

Table 9-3 JTAG Boundary Scan Register Definition

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
0	DWNRST_L[1]	5	Output2	
1	DWNRST_L[2]	6	Output2	
2			Internal	
3	TEST1	9	Input	
4	PERST_L	10	Input	
5	TEST2	16	Input	
6	TEST3	17	Birdir	12
7	VC1_EN	18	Birdir	12
8	PRSNT[1]	19	Birdir	12
9	PRSNT[2]	20	Birdir	12
10			Internal	
11	PORTSTSTUS_L1.1_SEL	22	Birdir	12
12			Control	
13	RXPOLINV_DIS	24	Birdir	12
14	TEST5	25	Birdir	12
15	SMBCLK	26	Birdir	12
16	SMBDATA	27	Birdir	12
17	PWR_SAV	28	Birdir	12
18	SLOTCLK	33	Birdir	12
19	GPIO[0]	36	Birdir	20
20			Control	
21	GPIO[1]	35	Birdir	22
22			Control	
23	GPIO[2]	37	Birdir	24
24			Control	
25	GPIO[3]	38	Birdir	26
26			Control	
27	GPIO[4]	39	Birdir	28
28			Control	
29	GPIO[5]	42	Birdir	30
30			Control	
31	GPIO[6]	43	Birdir	32
32			Control	
33	GPIO[7]	44	Birdir	34
34			Control	
35	SLOT_IMP[1]	45	Birdir	45
36	SLOT_IMP[2]	46	Birdir	45
37			Internal	
38			Internal	
39	TEST6	51	Birdir	45
40			Internal	
41	PL_512B	53	Birdir	45
42	SMBUS_EN	54	Birdir	45
43			Internal	

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
44			Internal	
45			Control	
46			Internal	
47	CLKBUF_PD	60	Birdir	45
48	CLKREQ_L[0] / PORTSTATUS[0]	67	Birdir	49
49			Control	
50	CLKREQ_L[1] / PORTSTATUS[1]	68	Birdir	51
51			Control	
52	CLKREQ_L[2] / PORTSTATUS[2]	69	Birdir	53
53			Control	
54	EECLK	70	Output2	
55	EEPD	71	Birdir	56
56			Control	

10 POWER MANAGEMENT

The PI7C9X2G304SV supports D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X2G304SV device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States. PI7C9X2G304SV also supports ASPM (Active State Power Management) to facilitate the link power saving. In addition, PCI-PM and ASPM L1.1 of L1 PM Substate is supported to reduce power consumption further.

In order to reduce further power consumption of high-speed circuit in L1 power state, the switch follows PCI-SIG ECN of L1 PM Substates with CLKREQ to implement L1.1 power sub-state for each port of packet switch. When the link is already put into L1 state, it can enter L1.1 sub-state by asserting CLKREQ sideband signal. In L1.1 sub-state, the PLL circuit and receiver buffer are turned off to lower idle power dramatically for that link of associated port. Once CLKREQ de-assertion is detected, the link is recovered from L1.1 sub-state to L1 state and the previously shut-down circuit is resumed.

The PI7C9X2G304SV requires that all lanes and ports enter L1.1 for power-saving to be effective. If any one of lanes or ports is not in L1.1 (such as an empty downstream port or the port connected to device not supporting L1.1), the PLL, which is shared by all lanes or ports, cannot be turned off. As a result, the core power would not be reduced because of internal clock kept running. In such a scenario, it suggests to put that port in L1 state instead of L1.1.

11 POWER SEQUENCE

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (3.3V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (100 ms) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

It is recommended to power up the I/O voltage (3.3V) first and then the core voltage (1.0V) or power up I/O voltage and core voltage simultaneously for both Aux and Main power rails.

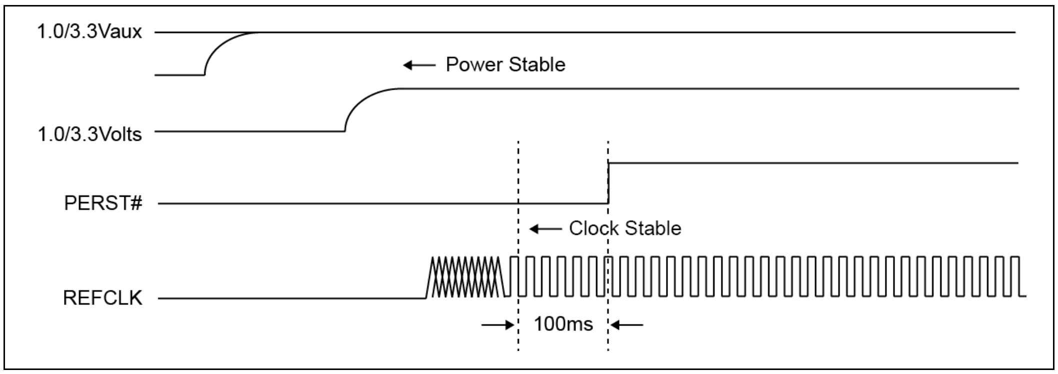


Figure 11-1 Initial Power-Up Sequence

Power-down sequence is the reverse of power-up sequence.

12 ELECTRICAL AND TIMING SPECIFICATIONS

12.1 ABSOLUTE MAXIMUM RATINGS

Table 12-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Absolute Max. Rating
Storage Temperature (T_{store})	-65ºC to 150ºC
Junction Temperature (T_j)	125 ºC
Digital core and analog supply voltage to ground potential (VDDC, AVDD and VDDCAUX)	-0.3v to 1.5v
Digital I/O and analog high supply voltage to ground potential (VDDR, CVDDR, AVDDH and VAUX)	-0.3v to 4.0v
DC input voltage for Digital I/O signals	-0.3v to 4.0v
ESD Rating Human Body Model (JEDEC Class 2) Charge Device Mode (JEDEC Class 2)	 2 kv 200v

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

12.2 DC SPECIFICATIONS

Table 12-2 DC Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
VDDC[1]	Digital Core Power	0.95	1.0	1.1	V
VDDR	Digital I/O Power	3.0	3.3	3.6	
CVDDR	Reference Clock Power	3.0	3.3	3.6	
VDDCAUX[1]	Auxiliary Core Power	0.95	1.0	1.1	
VAUX	Auxiliary I/O Power	3.0	3.3	3.6	
AVDD[1]	PCI Express Analog Power	0.95	1.0	1.1	
AVDDH	PCI Express Analog High Voltage Power	3.0	3.3	3.6	
V_{IH}	Input High Voltage	2.0		5.5	
V_{IL}	Input Low Voltage	-0.3		0.8	
V_{OH}	Output High Voltage	2.4			
V_{OL}	Output Low Voltage			0.4	
R_{PU}	Pull-up Resistor	63K	92K	142K	Ω
R_{PD}	Pull-down Resistor	57K	91K	159K	
RST#Slew[2]	PERST_L Slew Rate	50			mV/ns

Note:
1. VDDC/VDDCAUX/AVDD pins' voltage is 0.95v min. important to not operate below these levels. Taking typical PCB/power supply noise factors into consideration, we recommend that customers use 1.0v typical voltage in their board design to ensure solid margin.
2. The min. value for PERST_L Slew Rate is 50 mV/ns, which translates to the requirement that the time for PERST_L from 0V to 3.3V should be less than 66 ns.

12.3 AC SPECIFICATIONS

Table 12-3 PCI Express Interface - Differential Transmitter (TX) Output (5.0 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	199.94	200.0	200.06	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Low power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO-3.5dB}$	-3.0	-	-4.0	dB
TX de-emphasis level ratio	$V_{TX-DE-RATIO-6dB}$	-5.5		-6.5	dB
Transmitter Eye including all jitter sources	T_{TX-EYE}	0.75	-	-	UI
TX deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI
TX RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	-	3.0	Ps RMS
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.15	-	-	UI
TX rise/fall mismatch	$T_{RF-MISMATCH}$	-	-	0.1	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	16	MHz
Minimum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	8	-	-	MHz
TX PLL peaking with 8 MHz min BW	$PKG_{TX-PLL1}$	-	-	3.0	dB
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	-	120	Ω
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
TX DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	0	-	5	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 4 UI	ps

Table 12-4 PCI Express Interface - Differential Transmitter (TX) Output (2.5 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Low power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO}$	-3.0	-	-4.0	dB
Minimum TX eye width	T_{TX-EYE}	0.75	-	-	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125	-	-	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	22	MHz
Maximum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	1.5	-	-	MHz
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Transmitter DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps	ps

Parameter	Symbol	Min	Typ	Max	Unit
				+ 2 UI	

Table 12-5 PCI Express Interface - Differential Receiver (RX) Input (5.0 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	199.94	200.0	200.06	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	120	-	1200	mV
Total jitter tolerance	TJ_{RX}	0.68	-	-	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV

Table 12-6 PCI Express Interface - Differential Receiver (RX) Input (2.5 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	175	-	1200	mV
Receiver eye time opening	T_{RX-EYE}	0.4	-	-	UI
Maximum time delta between median and deviation from median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80	-	120	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
DC input CM input impedance during reset or power down	$Z_{RX-HIGH-IMP-DC}$	200	-	-	kΩ
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV
Lane to Lane skew	$L_{RX-SKEW}$	-	-	20	ns

12.4 POWER CONSUMPTION

Table 12-7 Power Consumption

Active Lane per Port	1.0VDDC		1.0VAUX		1.0AVDD		3.3AVDDH		3.3VDDR		3.3VAUX		Total		Unit
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
2/1/1	120.00	297.00	2.20	2.42	128.00	283.80	29.37	32.31	26.40	87.12	0.03	0.04	306.00	702.68	mW

Test Conditions:
- Typical power measured under the conditions of 1.0V/ 3.3V power rail without device usage on all downstream ports.
- Maximum power measured under the conditions of 1.1V/ 3.63V with PCIe2 devices usage on all downstream ports.
- Ambient Temperature at 25°C
- Power consumption in the table is a reference, be affected by various environments, bus traffic and power supply etc.

12.5 OPERATING AMBIENT TEMPERATURE

Table 12-8 Operating Ambient Temperature

(Above which the useful life may be impaired.)

Item	Min.	Max.	Unit
Ambient Temperature with power applied	-40	85	°C

Note:
Exposure to high temperature conditions for extended periods of time may affect reliability.

13 THERMAL DATA

The information described in this section is provided for reference only.

Table 13-1 Thermal Data

Power (Watt)	T_a (℃)	JEDEC Board	Airflow (m/s)	Θ_{JA} (℃/W)	T_j (℃)	Θ_{JC} (℃/W)
0.64	85	4-Layer	0	25.5	101.32	11.7
			1	21.3	98.632	
			2	19.9	97.736	

Note:

1. T_a: Ambient Temperature
2. T_J: Junction Temperature
3. Maximum allowable junction temperature = 125℃
4. Θ_{JA}: Thermal Resistance, Junction-to-Ambient
5. Θ_{JC}: Thermal Resistance, Junction-to-Case
6. Power measured under the conditions of 1.0V/ 3.3V with PCIe2 devices usage on all downstream ports
7. The shaded fields provide a recommendation that allows PI7C9X2G304SV to support Industrial Temperature Range.

14 PACKAGE INFORMATION

The package of PI7C9X2G304SV is a 14mm x 14mm LQFP (128 Pin) package. The following are the package information and mechanical dimension:

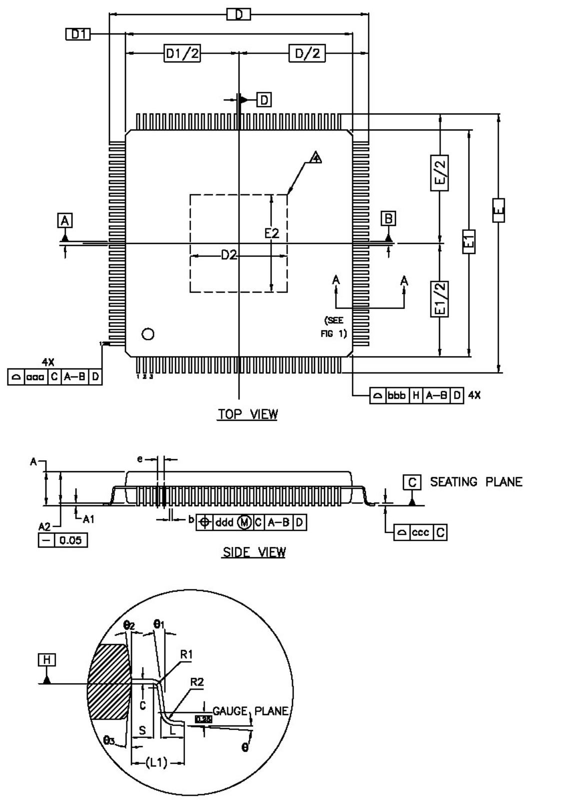


FIGURE 1 SECTION A–A

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	—	0.16	—	—	0.006	—
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		
D2	5.10	—	5.99	0.20	—	0.236
E2	5.10	—	5.99	0.20	—	0.236

NOTE :

1. ALL DIMENSION IN MM
2. REFER JEDEC MS–026
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR
4. THE OPTIONAL EXPOSED PAD IS COINCIDENT WITH THE BOTTOM SIDE OF THE PACKAGE AND NOT ALLOWED TO PROTRUDE BEYOND THAT SURFACE.

PERICOM Semiconductor Corporation

DATE: 12/11/14

DESCRIPTION: 128-pin Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FDE128

DOCUMENT CONTROL #: PD-2193

REVISION: --

15-0001

Figure 14-1 Package Outline Drawing

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code
Bar above assy code means ULA BOM
Bar above fab code means Cu wire

Figure 14-2 Part Marking

15 ORDERING INFORMATION

Part Number	Temperature Range	Package Description	Pb-Free & Green
PI7C9X2G304SVAFDEEX	-40^{o} to 85^{o}C (Industrial Temperature)	128-pin, Low Profile Quad Flat Package (LQFP)	Yes

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.