



A Product Line of
Diodes Incorporated



SPECIFICATION FOR APPROVAL

CUSTOMER _____

NOMINAL FREQUENCY 66.000000 MHz

PRODUCT TYPE TYPE FN 7.0x5.0 SEAM SEALED CRYSTAL CLOCK OSCILLATOR

SPEC. NO. (P/N) FN6600061

CUSTOMER P/N _____

ISSUE DATE May 30, 2018

VERSION C

APPROVED	PREPARED	QA

Diodes Incorporated

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- *Pb-free
- *RoHS Compliant
- *HF-Halogen Free
- *REACH Compliant

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VERSION HISTORY

Version No.	Version Date	Description	Notes
A	Dec.8,2011	Initial Release	
B	Aug.12,2011	1.Added Start up time spec: 10ms max2.Updated Suggested IR Reflow Profile & Format	
C	May.30,2018	Updated logo	



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ELECTRICAL SPECIFICATIONS

SRe Part Number : FN6600061

Item	Symbol	Specifications	Units	Notes
Nominal Frequency	Fo	66.000000	MHz	
Frequency Stability	FT	± 25	ppm	**See note
Operating Temperature Range	TR	-40 to +85	°C	
Supply Voltage	V _{DD}	+3.3 ± 10.0%	V	
Logic Type	LT	LVC MOS		
Supply Current, Output Enabled	I _{DD/OE}	40	mA	Max.
Supply Current, Output Disabled	I _{DD/OD}	10	µA	Max.
Duty Cycle (Symmetry)	DC/SY	45 / 55	%	Measured 50% of Waveform
Rise / Fall Time	T _R /T _F	5	ns	Max. measured 20/80% of Waveform
Output Voltage "0" Level	V _{OL}	10% V _{DD}	V	Max.
Output Voltage "1" Level	V _{OH}	90% V _{DD}	V	Min.
Output Load	CL	15	pF	Max
Jitter, Phase	RMS	1.5	ps	Max, 12KHz ~ 20MHz Frequency Band
Jitter, Accumulated	RMS(1-σ)	5	ps	Max, 20,000 Consecutive Periods
Jitter, Peak to Peak	Pk-Pk	50	ps	Max, 100,000 Random Periods
Start Up Time		10	ms	Max
Storage Temperature Range		-55 to +125	°C	

※ This product doesn't include harmful substance that stipulated by SONY SS-00259 Level 1 and S-AT2-001 Level 1 standard. RoHS Compliant (Pb - Free).

**Stability includes all combinations of Operating Temperature, Load changes, rated Input (Supply) Voltage changes, Initial Calibration Tolerance (25°C), Aging (1 year at 25°C Average Effective Ambient Temperature), Shock and Vibration.

Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (Pin1), Output Enable	0.7V _{DD}			V	Or Open
Input Voltage (Pin1), Output Disable (low power standby)			0.3V _{DD}	V	Output is Hi-Z
Internal Pullup Resistance	30			KΩ	
Output Disable Delay			200	ns	
Output Enable Delay			2	ms	



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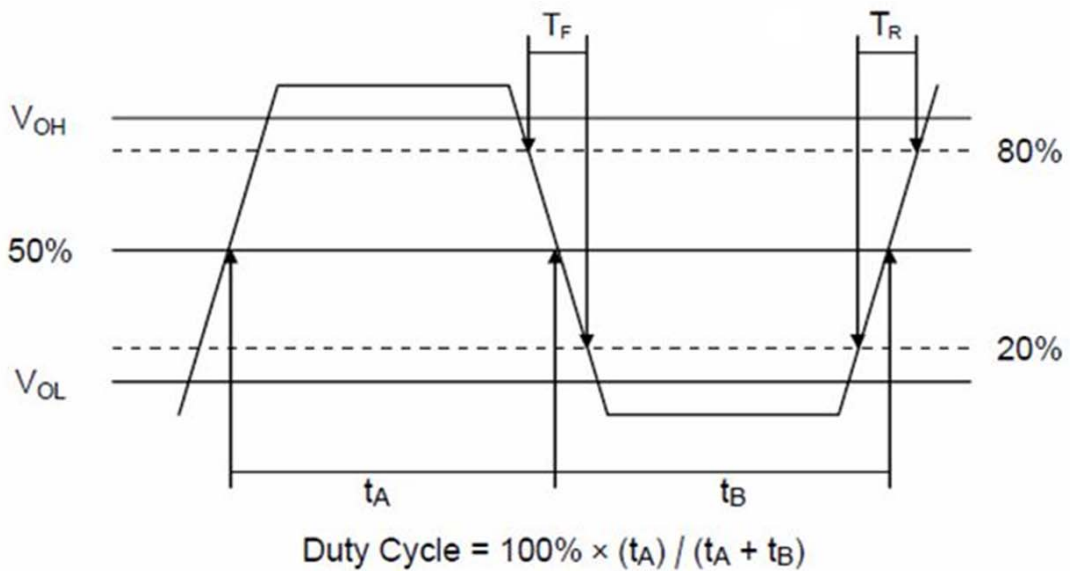
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TEST CIRCUIT



OUTPUT WAVEFORM



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RELIABILITY SPECIFICATIONS

ENVIRONMENTAL:

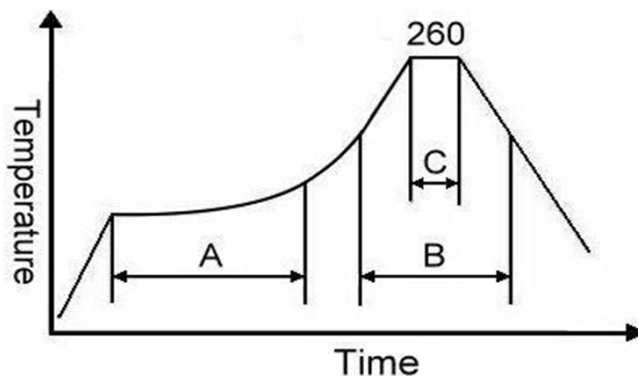
- a) THERMAL SHOCK: MIL-STD-883, Method 1011, Condition A
- b) MOISTURE RESISTANCE: MIL-STD-883, Method 1004
- c) VIBRATION: MIL-STD-883, Method 2007, Condition A
- d) RESISTANCE TO SOLDERING HEAT: J-STD-020D Table 5-2 Pb-free devices (except 2 cycles max)
- e) HAZARDOUS SUBSTANCE: Pb - free and RoHS Compliant.

MECHANICAL:

- a) SHOCK: MIL-STD-883, Method 2002, Condition B
- b) SOLDERABILITY: JESD22-B102-D Method 2 (Preconditioning E)
- c) TERMINAL STRENGTH: MIL-STD-883, Method 2004, Test Condition D
- d) GROSS LEAK: MIL-STD-883, Method 1014, Condition C
- e) FINE LEAK: MIL-STD-883, Method 1014, Condition A2, $R1=2 \times 10^{-8}$ atm cc/s
- f) SOLVENT RESISTANCE: MIL-STD-202, Method 215

SUGGESTED IR REFLOW PROFILE

*As per IPC-JEDEC J-STD-020D



Note:

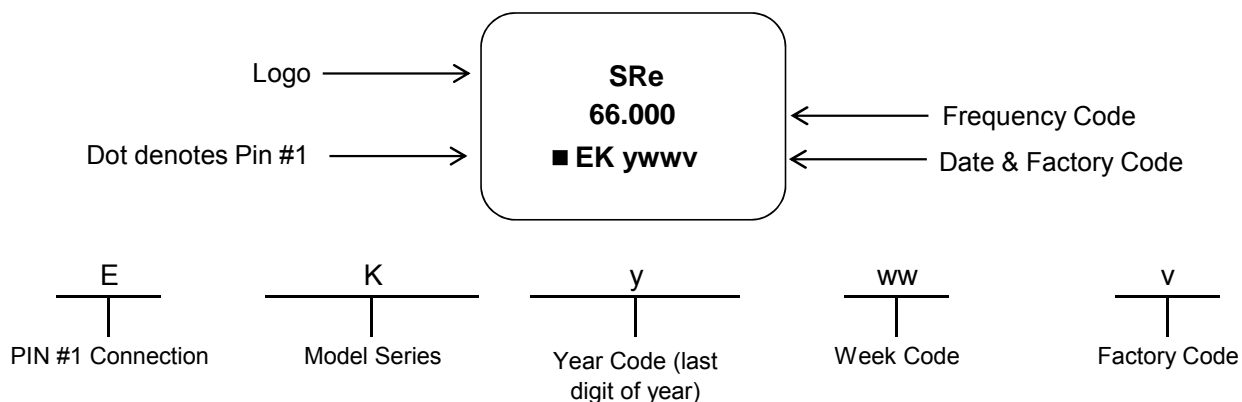
	Stage	Temperature	Time
A	Preheat	150~200°C	60~120 Sec
B	Primary Heat	217°C	60~150 Sec
C	Peak	260°C	10 Sec

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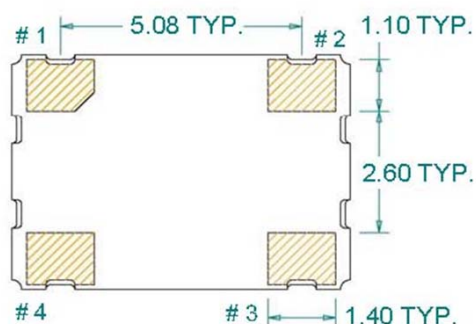
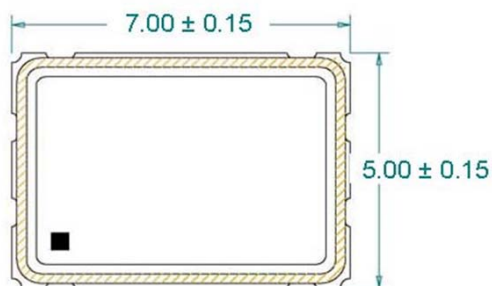
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MARKING

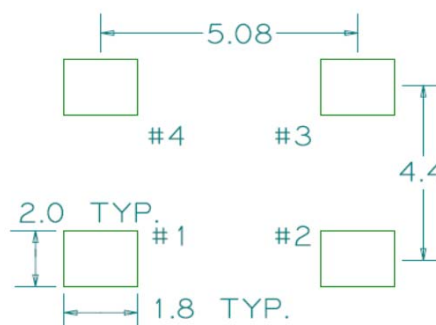


MECHANICAL DRAWINGS (Scale:None. Dimensions are in mm.)



(Bottom View)

Recommended Land Pattern*



*External high-frequency power decoupling is recommended. (see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

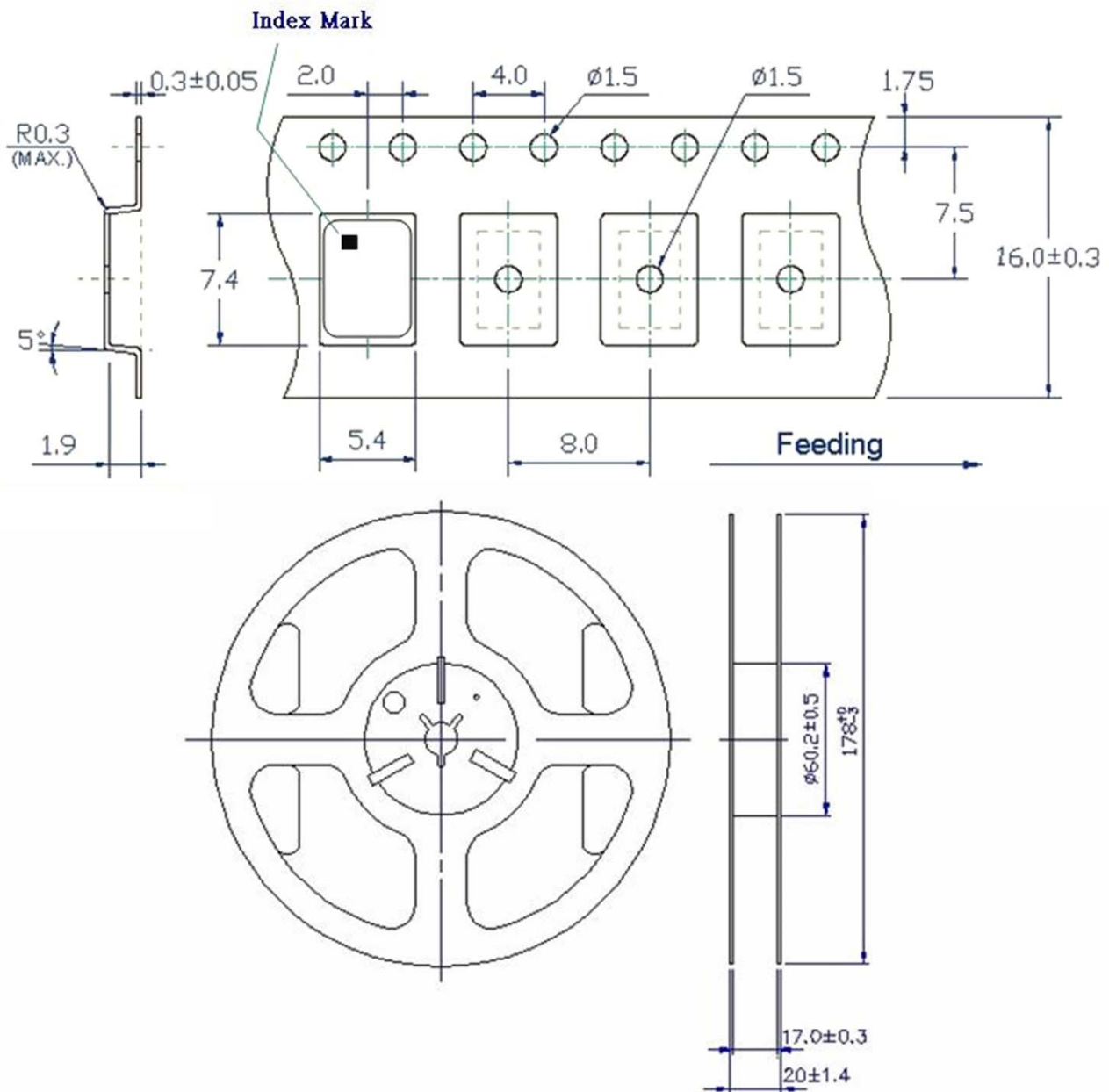
Pin	Function
1	OE
2	Ground
3	Clock Output
4	V _{DD}

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TAPE&REEL



1. 230mm minimum leader which consist of carrier and/or tape followed by a minimum of 160mm of empty carrier tape sealed with cover tape.
2. 160mm minimum trailer of empty carrier tape sealed with cover tape.

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PACKING

