KAF-0261

512 (H) x 512 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−0261 Image Sensor is a high performance, charge coupled device (CCD) designed for a wide range of image sensing applications.

The sensor incorporates true two−phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes a transparent gate electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Selectable on−chip output amplifiers allow operation to be optimized for different imaging needs: Low Noise (when using the high−sensitivity output) or Maximum Dynamic Range (when using the low−sensitivity output).

The low dark current of the KAF−0261 makes this device suitable for low light imaging applications without sacrificing charge capacity.

Figure 1. KAF−0261 CCD Image Sensor

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD
Number of Active Pixels	512 (H) x 512 (V)
Pixel Size	20 μm (H) x 20 μm (V)
Active Image Size	10.2 mm (H) x 10.2 mm (V)
Chip Size	11.3 mm (H) x 11.6 mm (V)
Optical Fill Factor	100%
Output Sensitivity High Sensitivity Output High Dynamic Range Output	 10 μV/electron 2.0 μV/electron
Saturation Signal High Sensitivity Output High Dynamic Range	 200,000 electrons 500,000 electrons
Readout Noise (1 MHz)	22 electrons rms
Dark Current (25°C, Accumulation Mode)	< 30 pA/cm^3
Dark Current Doubling Rate	6°C
Dynamic Range (Sat Sig/Dark Noise) High Sensitivity Output	83 dB
High Dynamic Range Output Range	87 dB
Quantum Efficiency (450, 550, 650 nm)	35%, 55%, 58%
Maximum Data Rate High Sensitivity Output High Dynamic Range Output	 5 MHz 2 MHz
Transfer Efficiency	> 0.99997
Package	CERDIP Package
Cover Glass	Clear or AR coated, 2 sides

Features

- True Two Phase Full Frame Architecture
- Transparent Gate Electrode for High Sensitivity
- 100% Fill Factor
- Low Dark Current
- User−selectable Outputs Allow either Low Noise or High Dynamic Range Operation
- Single Readout Register
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Scientific Imaging

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAF−0261−AAA−CD−BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	KAF−0261−AAA S/N
KAF−0261−AAA−CD−AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
KAF−0261−AAA−CP−BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade	
KAF−0261−AAA−CP−AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
KEK−4H0081−KAF−0261−12−5	Evaluation Board (Complete Kit)	N/A

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

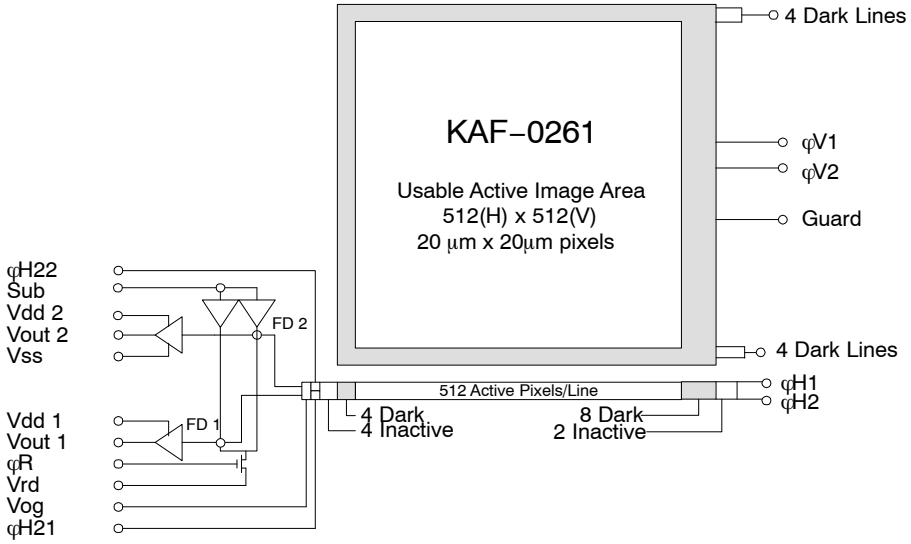

Figure 2. Block Diagram

Shaded areas represent 4 non−imaging pixels at the beginning and 8 non−imaging pixels at the end of each line. There are also 4 non−imaging lines at the top and bottom of each frame.

The KAF−0261 consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier (See Figure 1). Both registers incorporate two−phase buried channel CCD technology. The vertical register consists of 20 μm x 20 μm photocapacitor sensing elements (pixels) that also serves as the transport mechanism. The pixels are arranged in a 512 (H) x 512 (V) array; an additional 12 columns (4 at the left and 8 at the right) and 8 rows (4 each at top and bottom) of non−imaging pixels are added as dark reference. There is no storage array, so this device must be synchronized with strobe illumination or shuttered during readout.

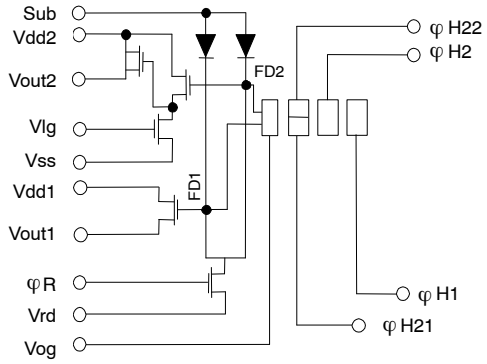

Figure 3. Output Structure

Output Structure

The final gate of the horizontal register is split into two sections, ϕH21 and ϕH22. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single−stage output (Vout1), ϕH22 is tied to a negative voltage to block charge transfer, and ϕH21 is tied to ϕH2 to transfer charge. To use the high sensitivity two−stage output (Vout2), ϕH21 is tied to a negative voltage and ϕH22 is tied to ϕH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression Vfd = Q/Cfd.

The translation from electrons to voltages is called the output sensitivity or charge−to−voltage conversion. After the output has been sensed off−chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron−hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (ϕV1, ϕV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non−linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will ‘bloom’ into vertically adjacent pixels.

Charge Transport

Integrated charge is transported to the output in a two−step process. Rows of charge are first shifted line by line into the horizontal CCD. ‘Lines’ of charge are then shifted to the output pixel by pixel. The timing diagram illustrated in Figure 7 illustrates how the integration of charge is performed with ϕV1 and ϕV2 held low. Transfer to the horizontal CCD begins when ϕV1 is brought high, causing charge from the ϕV1 and ϕV2 gates to combine under the ϕV1 gate. The ϕV1 and ϕV2 gates are now reversed in polarity, causing the charge packets to ‘spill’ forward under the ϕV2 gate of the next pixel. The falling edge of ϕV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the ϕV1 electrode of the next pixel. The sequence completes when ϕV1 is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using ϕH1 and ϕH2 pins) as shown. The falling edge of ϕH2 forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) which is buffered by the output amplifier. The cycle repeats until all lines are read.

DEVICE DESCRIPTION

Pin Description and Device Orientation

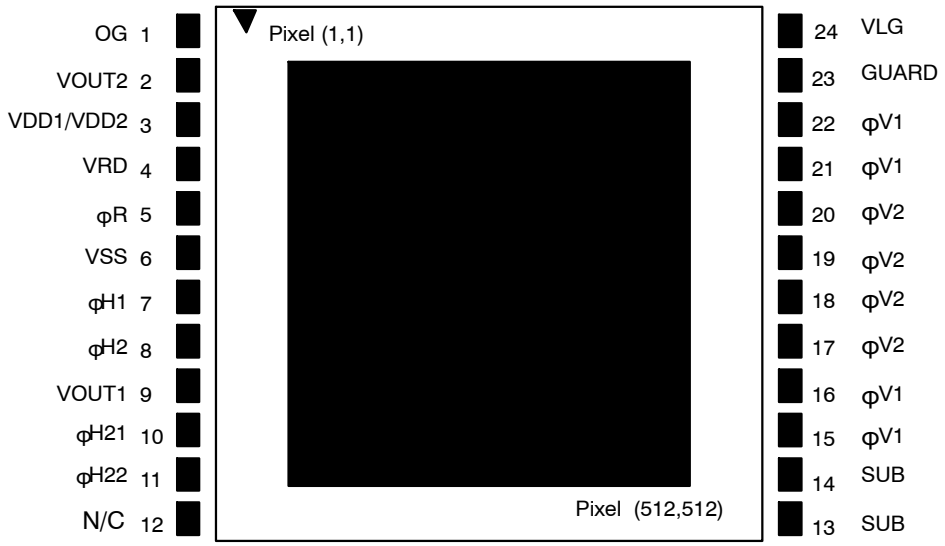

Figure 4. Pinout Diagram

Table 3. PIN DESCRIPTION

Pin	Name	Description
1	OG	Output Gate
2	VOUT2	Video Output from High Sensitivity Two−Stage
3	VDD1 / VDD2	Amplifier Supply for VOUT1 and VOUT2 Amplifiers
4	VRD	Reset Drain
5	ϕR	Reset Clock
6	VSS	Output Amplifier Return
7	ϕH1	Horizontal (Serial) CCD Clock − Phase 1
8	ϕH2	Horizontal (Serial) CCD Clock − Phase 2
9	VOUT1	Video Output from High Dynamic Range Single−Stage Amplifier
10	ϕH21	Last Horizontal (Serial) CCD Phase − Split Gate
11	ϕH22	Last Horizontal (Serial) CCD Phase − Split Gate
12	N/C	No Connection
13	VSUB	Substrate
14	VSUB	Substrate
15	ϕV1	Vertical (Parallel) CCD Clock − Phase 1
16	ϕV1	Vertical (Parallel) CCD Clock − Phase 1
17	ϕV2	Vertical (Parallel) CCD Clock − Phase 2
18	ϕV2	Vertical (Parallel) CCD Clock − Phase 2
19	ϕV2	Vertical (Parallel) CCD Clock − Phase 2
20	ϕV2	Vertical (Parallel) CCD Clock − Phase 2
21	ϕV1	Vertical (Parallel) CCD Clock − Phase 1
22	ϕV1	Vertical (Parallel) CCD Clock − Phase 1
23	GUARD	Guard Ring
24	VLG	First Stage Load Transistor Gate for Two−Stage

1. Pins 15, 16, 21, and 22 must be connected together − only one Phase 1−clock driver is required.
2. Pins 17, 18, 19, and 20 must be connected together − only one Phase 2−clock driver is required.

IMAGING PERFORMANCE

Typical Operational Conditions

All values apply to nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons − to convert to voltage, multiply by the amplifier sensitivity.

Specifications

Table 4. ELECTRO−OPTICAL

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Optical Fill Factor	FF		100		%		
Photoresponse Non−uniformity	PRNU			5	% rms	Full Array	die[10]
Quantum Efficiency (450, 550, 650 nm)	QE					See QE curve (Figure 7)	design[11]

Table 5. CCD PARAMETERS COMMON TO BOTH OUTPUTS

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Sat. Signal − Vccd register	N_{e^-sat}	450	500		ke^-	2	design[11]
Dark Current	Jd		15.3 400	30 750	pA/cm^2 e^-pixel/sec	25°C (mean of all pixels)	die[10]
Dark Current Doubling Temp	DCDR	5	6.3	7.5	°C		design[11]
Dark Signal Non−uniformity	DSNU			750	e^-/pix/sec	4	die[10]
Charge Transfer Efficiency	CTE		.99997			5	die[10]
Photoresponse Non−linearity	PRNL		1	2	%	9	
Blooming Suppression	Bs		none				

Table 6. CCD PARAMETERS SPECIFIC TO HIGH GAIN OUTPUT AMPLIFIER

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Output Sensitivity	Vout/Ne^-		10		μV/electron		design[11]
Sat. Signal	N_{e^-sat}	180	200	240	ke^-	1	design[11]
Total Sensor Noise	n_{e^-total}		13	20	e^-rms	7	design[11]
Horizontal CCD Frequency	f_H		2	5	MHz	6	design[11]
Dynamic Range	DR	79	83		dB	8	design[11]

Table 7. CCD PARAMETERS SPECIFIC TO LOW GAIN (HIGH DYNAMIC RANGE) OUTPUT AMPLIFIER

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Output Sensitivity	Vout/Ne^-		2		μV/electron		design[11]
Sat. Signal	N_{e^-sat}	550K	628K		ke^-	3	design[11]
Total Sensor Noise	n_{e^-total}		22	30	e^-rms	7	die[10]
Horizontal CCD Frequency	f_H		0.5	2	MHz	6	design[11]
Dynamic Range	DR	85	87		dB	8	design[11]

1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register.
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 16 sub arrays (128 x 128) exceed the maximum dark current specification.
5. For 2 MHz data rate and T = 30°C to −40°C.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
7. At $T_{integration}$ = 0; data rate = 1 MHz; temperature = −30°C.
8. Uses 20LOG (N_{e^-sat} / n_{e^-total}) where N_{e^-sat} refers to the appropriate saturation signal.
9. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
10. A parameter that is measured on every sensor during production testing.
11. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES (QE)

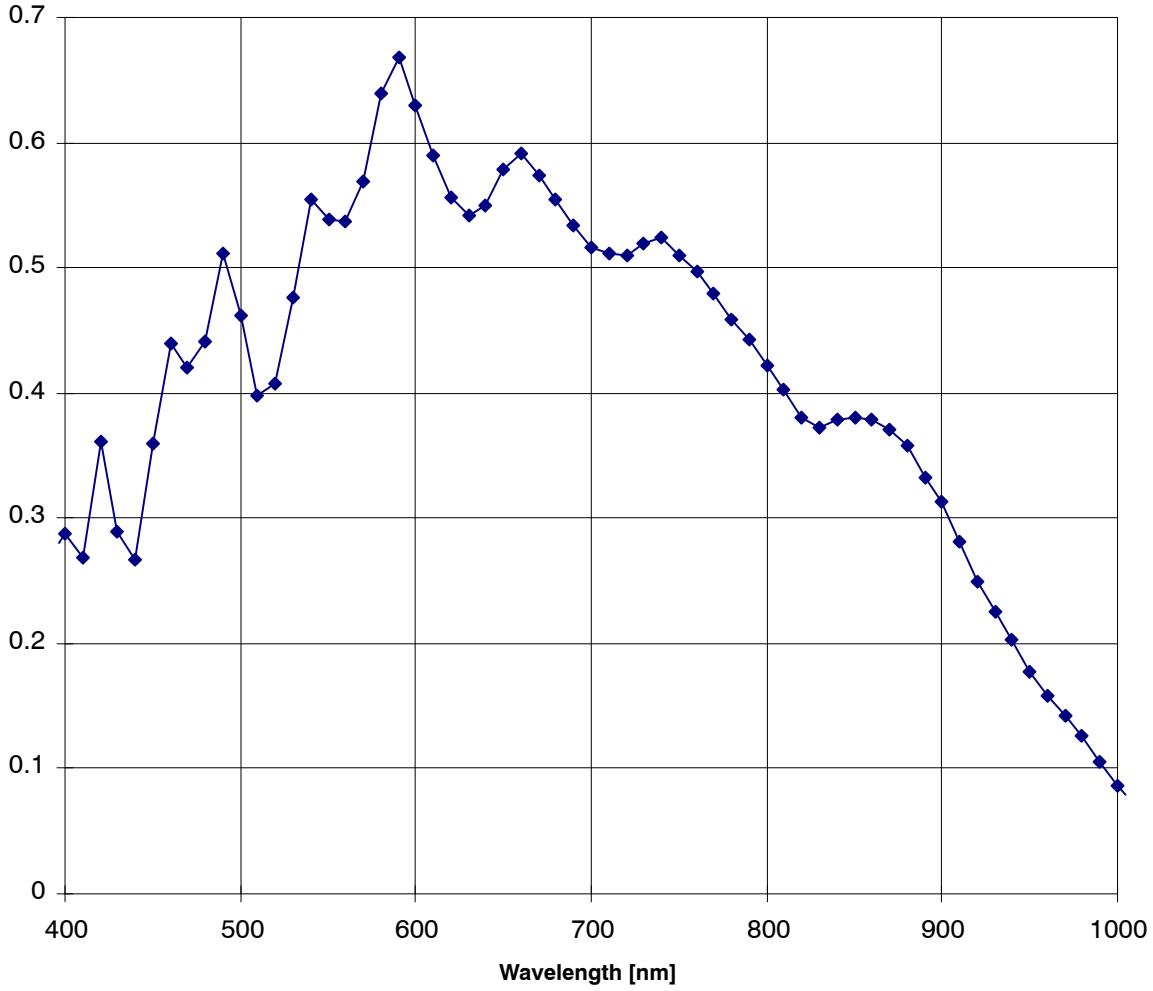

Figure 5. Typical Spectral Response

DEFECT SPECIFICATIONS

Table 8. MAXIMUM DEFECT COUNTS

Point Defect	Cluster Defect	Column Defect
10	4	0

Dark Defects

A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation

Bright Defect

A pixel whose dark current exceeds 4500 electrons/pixel/second at 25°C

Cluster Defect

A grouping of not more than 5 adjacent point defects

Column Defect

A grouping of point defects along a single column. (Dark Column)

A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25°C. (Bright Column)

A column that does not exhibit the minimum charge capacity specification. (Low charge capacity)

A column that loses > 500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)

Neighboring Pixels

The surrounding 128 x 128 pixels of ±64 columns/rows

Defects are separated by no less than 3 pixels in any one direction.

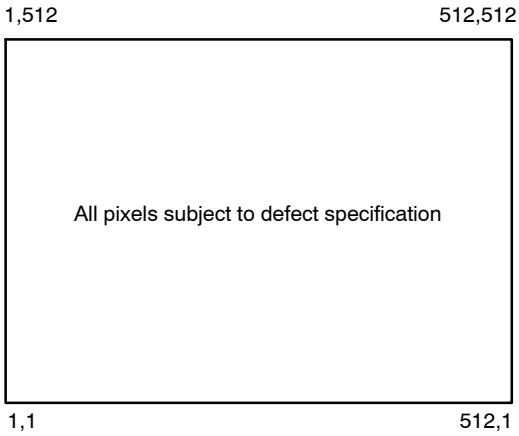

Figure 6. Active Pixel Region

OPERATION

Table 9. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Voltage	All Clocks	−16	+16	V	1
Voltage	OG	0	+8	V	2
Voltage	VRD, VSS, VDD, GUARD	0	+20	V	2
Current	Output Bias Current (IDD)		10	mA	
Capacitance			10	pF	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Voltage between any two clocks or between any clock and Vsub.
2. Voltage with respect to Vsub.

WARNING: For maximum performance, built−in gate protection has been added only to the OG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage. Devices are rated as Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test).

Table 10. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Pin Impedance
Substrate	VSUB	0.0	0.0	0.0	V	Common
Output Amplifier Supply	VDD	15.0	+17.0	17.5	V	5 pF, 2 KΩ (Note 1)
Output Amplifier Return	VSS	1.4	+2.0	2.1	V	5 pF, 2 KΩ
Reset Drain	VRD	11.5	+12	12.5	V	5 pF, 1 MΩ
Output Gate	OG	4.0	4.5	5.0	V	5 pF, 10 MΩ
Guard Ring	GUARD	9.0	+10.0	15.0	V	350 pF, 10 MΩ
Load Gate	VLG	VSS − 1.0	VSS	VSS + 1.0	V	

1. Vdd = 17 volts for applications where the expected output voltage > 2.0 Volts. For applications where the expected useable output voltage is < 2 Volts Vdd can be reduced to 15 Volts.

AC Operating Conditions

Table 11. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Pin Impedance
Vertical Clock − Phase 1	ϕV1	Low	−10.2	−10.0	−9.0	V	13 nF, 10 MΩ
Vertical Clock − Phase 1	ϕV1	High	0.0	0	2.0	V	
Vertical Clock − Phase 2	ϕV2	Low	−10.2	−10.0	−9.0	V	16 nF, 10 MΩ
Vertical Clock − Phase 2	ϕV2	High	0.0	0	2.0	V	
Horizontal Clock − Phase 1	ϕH1	Low	−2.2	−2.0	−1.8	V	160 pF, 10 MΩ
Horizontal Clock − Phase 1	ϕH1	High	7.8	+8.0	8.2	V	
Horizontal Clock − Phase 2	ϕH2	Low	−2.2	−2.0	−1.8	V	110 pF, 10 MΩ
Horizontal Clock − Phase 2	ϕH2	High	7.8	+8.0	8.2	V	
Reset Clock	ϕR	Low	2.0	3.0	3.5	V	10 pF, 10 MΩ
Reset Clock	ϕR	High		10.0		V	

Table 12. AMPLIFIER SELECTION

Description	Symbol	Level	Using the High Gain Output (Vout2)			Using the High Dynamic Range Output (Vout1)			Units	Pin Impedance
			Min	Nom	Max	Min	Nom	Max		
Horizontal Clock − Phase 1	ϕH21	Low	−4	ϕH2 low	ϕH2 low		ϕH2		V	10 pF, 10 MΩ
Horizontal Clock − Phase 1	ϕH21	High	−4	ϕH2 low	ϕH2 low		ϕH2		V	
Horizontal Clock − Phase 2	ϕH22	Low		ϕH2		−4	ϕH2 low	ϕH2 low	V	10 pF, 10 MΩ
Horizontal Clock − Phase 2	ϕH22	High		ϕH2		−4	ϕH2 low	ϕH2 low	V	

1. When using Vout1 ϕH21 is clocked identically with ϕH2 while ϕH22 is held at a static level. When using Vout2 ϕH21 and ϕH22 are exchanged so that ϕH22 is identical to ϕH2 and ϕH21 is held at a static level. The static level should be the same voltage as ϕH2 low.
2. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MΩ are expected resistances. These pins are only verified to 1 MΩ.
3. ϕV1, 2 capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.
4. This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult ON Semiconductor in those situations in which operating conditions meet or exceed minimum or maximum levels.

Timing

Table 13. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		5	8	MHz	1, 2, 3
V1, V2 Clock Frequency	f_V		100	125	kHz	1, 2, 3
Pixel Period (1 Count)	t_{pix}	125	200		ns	
ϕH1, ϕH2 Set−up Time	$t_{\phi HS}$	500	1000		ns	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	4	5		μs	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	40	64		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	78	122		μs	7

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5−10% of clock period. Crossover of register clocks should be between 40−60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (520 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 530 * t_{pix} + t_{pix}$

Normal Readout Timing

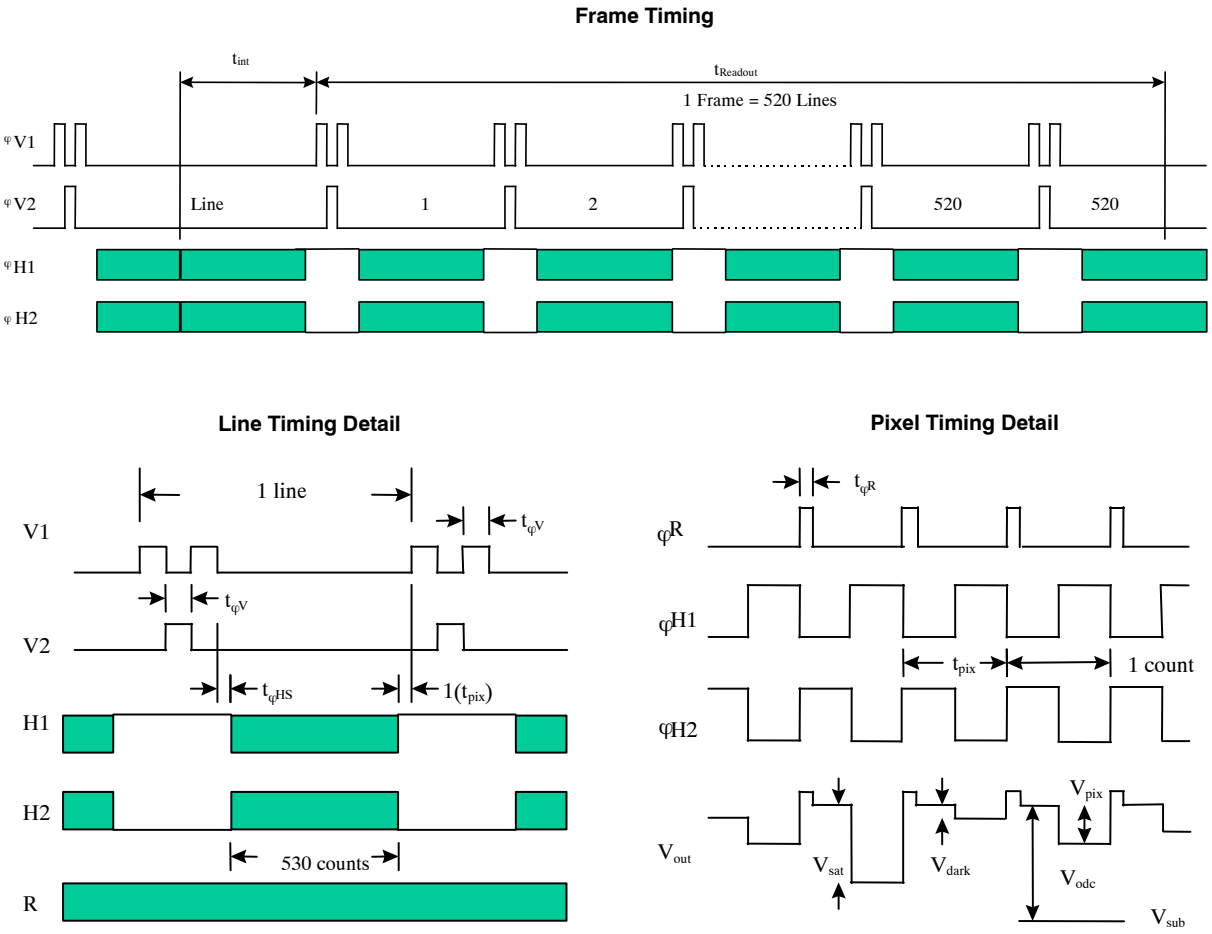

Figure 7. Timing Diagrams

NOTE: This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult ON Semiconductor in those situations, which require special consideration.

STORAGE AND HANDLING

Table 14. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	−100	+80	°C	At Device
Operating Temperature	T_{OP}	−70	+50	°C	At Device

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

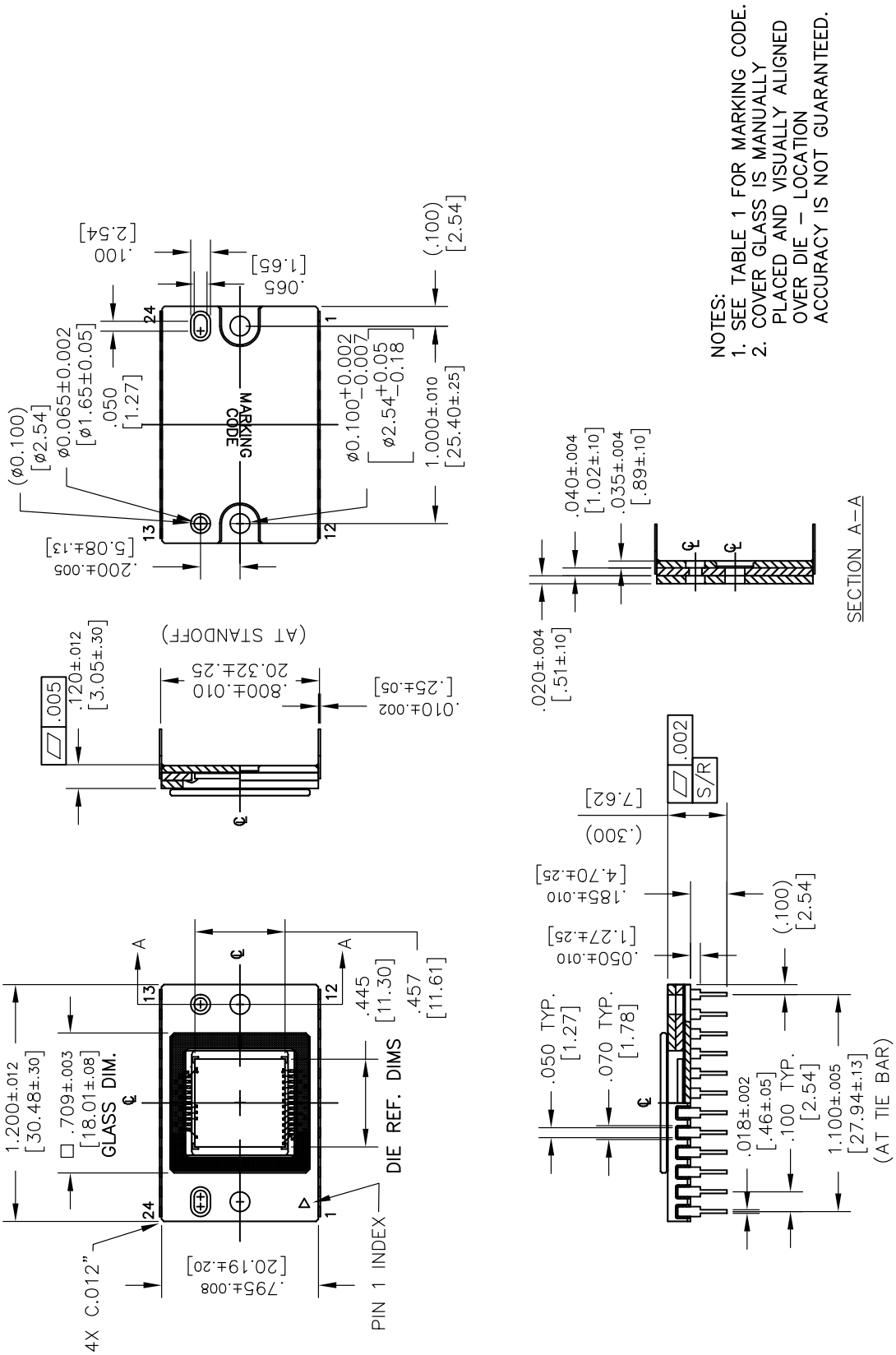

Figure 8. Completed Assembly (1 of 2)

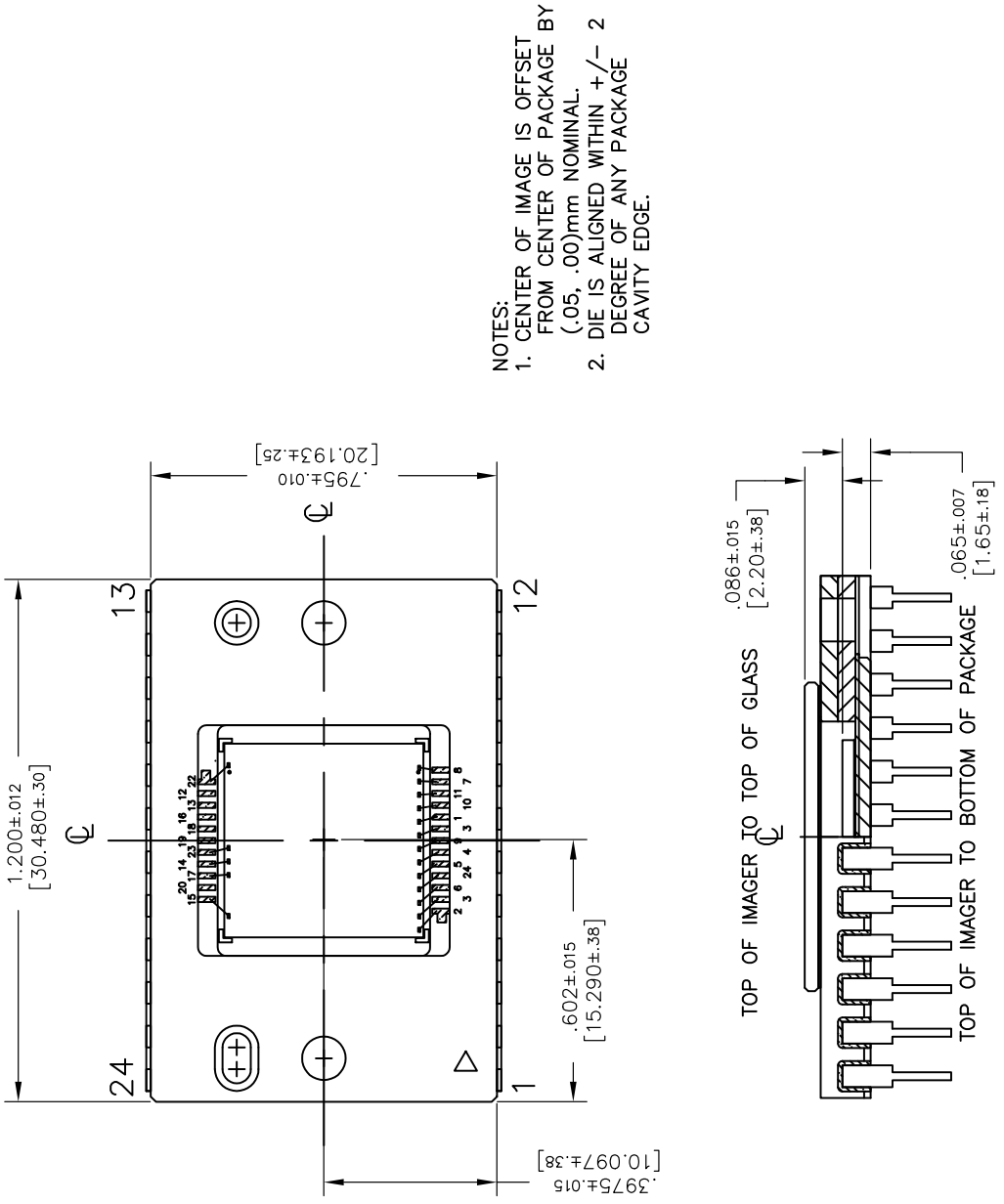

Figure 9. Completed Assembly (2 of 2)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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