40 W adapter evaluation board

Using the new 950 V CoolMOS™ P7 and ICE2QS03G QR flyback controller in a snubberless flyback for improved efficiency

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Order code: EVAL_40W_FLY_P7_950V

Scope and purpose

The evaluation board described in this application note provides a test platform for the new 950 V CoolMOS™ P7 series of superjunction HV MOSFETs. The adapter uses the ICE2QS03G, a second-generation current mode control QR flyback controller and an IPA95R450P7 950 V CoolMOS™ P7 series power MOSFET. This application note is intended for those who have experience with flyback converter designs and will not cover the overall design process in depth, but it will cover specific design aspects for this controller and the 950 V CoolMOS™ P7 in charger and adapter applications. This design is done using a snubberless flyback in order to improve the overall system efficiency while reducing the cost of the snubber network. This document will also show the overall benefits that the 950 V CoolMOS™ P7 presents for SMPS. For a detailed introduction to flyback converter design please read Design guide for QR flyback converter [1].

Intended audience

Power supply design engineers

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Description

1 Description

This 40 W adapter evaluation board (EVAL_40W_FLY_P7_950V) is intended to be a form, fit and function test platform for charger and adapter applications to show the operation of the 950 V CoolMOS™ P7 as well as the overall controller design. The evaluation board is designed around a QR flyback topology for improved switching losses that allows higher power density designs and lower radiated and conducted emissions. This board also employs a snubberless flyback design in order to reduce the overall system costs while increasing system efficiency. This new efficiency can be used to give extra design flexibility to either further reduce system costs or increase power density. A 40 W universal input isolated flyback evaluation board with a 19 V output based on the ICE2QS03G controller and the 950 V CoolMOS™ P7 MOSFET is described in this application note, and test results are presented.

Figure 1 40 W flyback evaluation board (3D model)

2 QR flyback overview

The QR flyback offers improved efficiency and EMI performance over the traditional fixed-frequency flyback converter by reducing switching losses. This is accomplished by controlling the turn-on time of the primary MOSFET (Q_{pri} in Figure 3). In a flyback operating in Discontinuous Conduction Mode (DCM), the energy is first stored in the primary side when the primary MOSFET (Q_{pri}) is turned on, allowing the primary current to ramp up. The primary MOSFET (Q_{pri}) turns off, and the energy stored in the transformer transfers into the secondary-side capacitor. The energy that is left in the primary inductance (L_{pri}) after transferring the energy to the secondary then resonates with the combined output capacitance of the MOSFET ($C_{DS\_parasitic}$) consisting of the MOSFET output capacitance (C_{OSS}), stray drain source capacitance from the transformer and layout, and any additional external drain source capacitance on this node. In a fixed-frequency flyback the switch turn-on happens regardless of the MOSFET drain source voltage (V_{DS}). If switching occurs at a higher V_{DS} (Figure 2), this leads to more switching losses (E_{OSS} losses). The QR flyback waits to turn on Q_{pri} until the V_{DS} voltage reaches the minimum possible voltage shown in Figure 2, and then turns on the MOSFET.

$$P_{sw\_on} = 0.5 f_{sw} C_{OSS} V_{DS}^2$$

Since the turn-on switching losses are a function of V^2 (as shown above), this reduces the overall system switching losses. This has the added benefit of lowering the amount of switched energy, which helps reduce switching noise from the converter, resulting in lower radiated and conducted emissions.

The 950 V CoolMOS™ P7 technology generates improvements in the operation of QR flyback converters through having lower output capacitance (C_{OSS}) that helps to reduce the losses of the device during turn-on. The improvements that the 950 V CoolMOS™ P7 offers will be further addressed in Section 4.

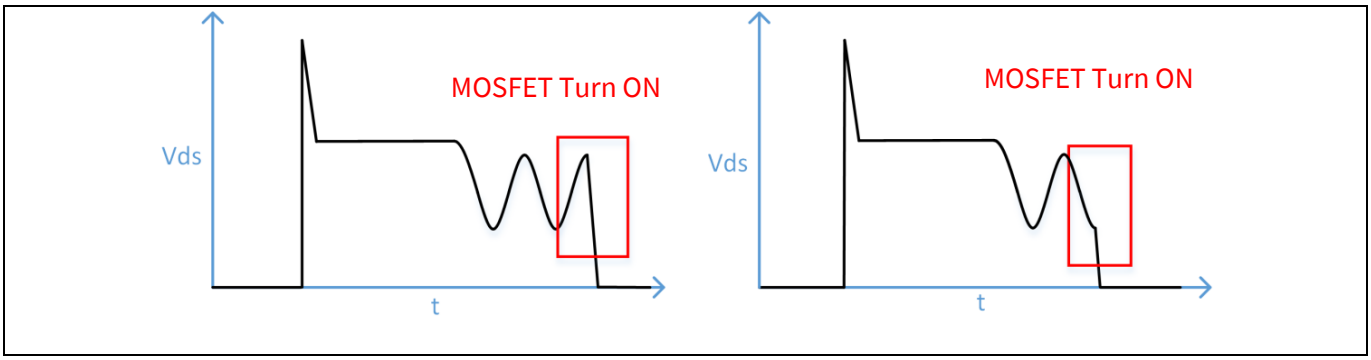

Figure 2 Fixed-frequency flyback primary MOSFET drain source waveform (left) vs a QR flyback primary MOSFET drain source waveform (right)

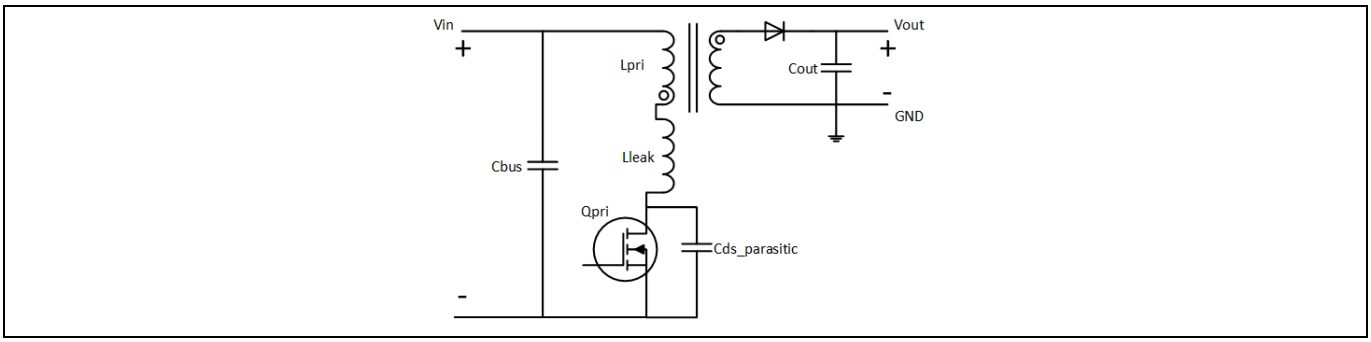

Figure 3 Simplified flyback schematic

3 ICE2QS03G functional overview

The ICE2QS03G PWM controller is a second-generation QR flyback controller IC developed by Infineon Technologies. Typical applications include TV sets, DVD players, set-top boxes, netbook adapters, home audio and printer applications. This controller implements switching at the lowest ringing voltage and also includes pulse skipping at light loads for maximum efficiency across a wide load range.

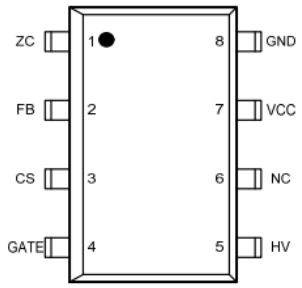

Figure 4 ICE2QS03G pin-out

Table 1 ICE2QS03G pin description

Pin	Name	Description
1	Zero Crossing (ZC)	Detects the minimum trough (valley) voltage for turn-on for the primary switch turn-on time
2	Feedback (FB)	Voltage feedback for output regulation
3	Current Sense (CS)	Primary-side current sense for short-circuit protection and current mode control
4	Gate drive output (GATE)	MOSFET gate driver pin
5	High Voltage (HV)	Connects to the bus voltage for the initial start-up through the high voltage start-up cell
6	No Connect (NC)	No connection
7	Power supply (V_{CC})	Positive IC for the power supply
8	Ground (GND)	Controller ground

4 950 V CoolMOS™ P7 benefits for adapters

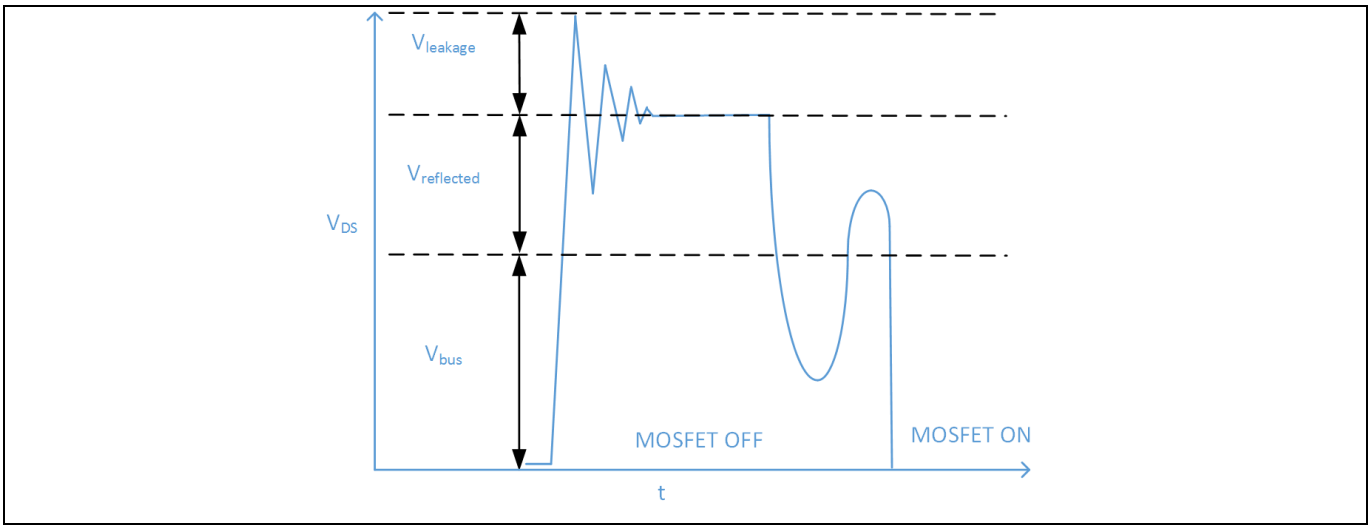

Figure 5 The MOSFET drain source voltage in a flyback converter is the sum of the bus voltage (V_{bus}), reflected voltage ($V_{reflected}$) and leakage ringing voltage ($V_{leakage}$)

The 950 V CoolMOS™ P7 superjunction MOSFET provides several benefits for charger and adapter applications when compared to the 600 V and 650 V MOSFETs traditionally used. The additional breakdown voltage can be used to increase the efficiency of designs, increase the allowable AC input voltage, or increase the surge capabilities of designs. The P7 family of devices also has better performance when comparing switching losses to previous generations of MOSFETs.

A 950 V breakdown voltage allows for a higher combination of bus voltage, reflected voltage and leakage ringing voltage than can be achieved with 600 V or 650 V devices. This allows for getting rid of the snubber component cost while still maintaining enough breakdown voltage margin for operation. This snubberless operation will be covered in more detail in Section 5. It is also possible to use this extra voltage margin to allow for bus voltages extending beyond the typical 265 V AC high-line, which is typically needed in countries with less grid stability for chargers and adapters.

The P7 family of devices also has an improved switching performance that is better than existing Infineon and competitor devices. One switching loss mechanism is the E_{OSS} of the MOSFET. The E_{OSS} is the main loss contributor for the turn-on of the MOSFET in a QR flyback. The energy that is stored in the output capacitance of the MOSFET needs to be discharged every cycle before the MOSFET is turned on. As shown in Figure 6, the output capacitance energy storage of the 950 V CoolMOS™ P7 is better when compared to equivalent competitor devices or previous generations of CoolMOS™ technologies. This improvement is most significant at higher AC input voltages where the switching losses begin to play a larger role in the loss breakdown.

950 V CoolMOS™ P7 benefits for adapters

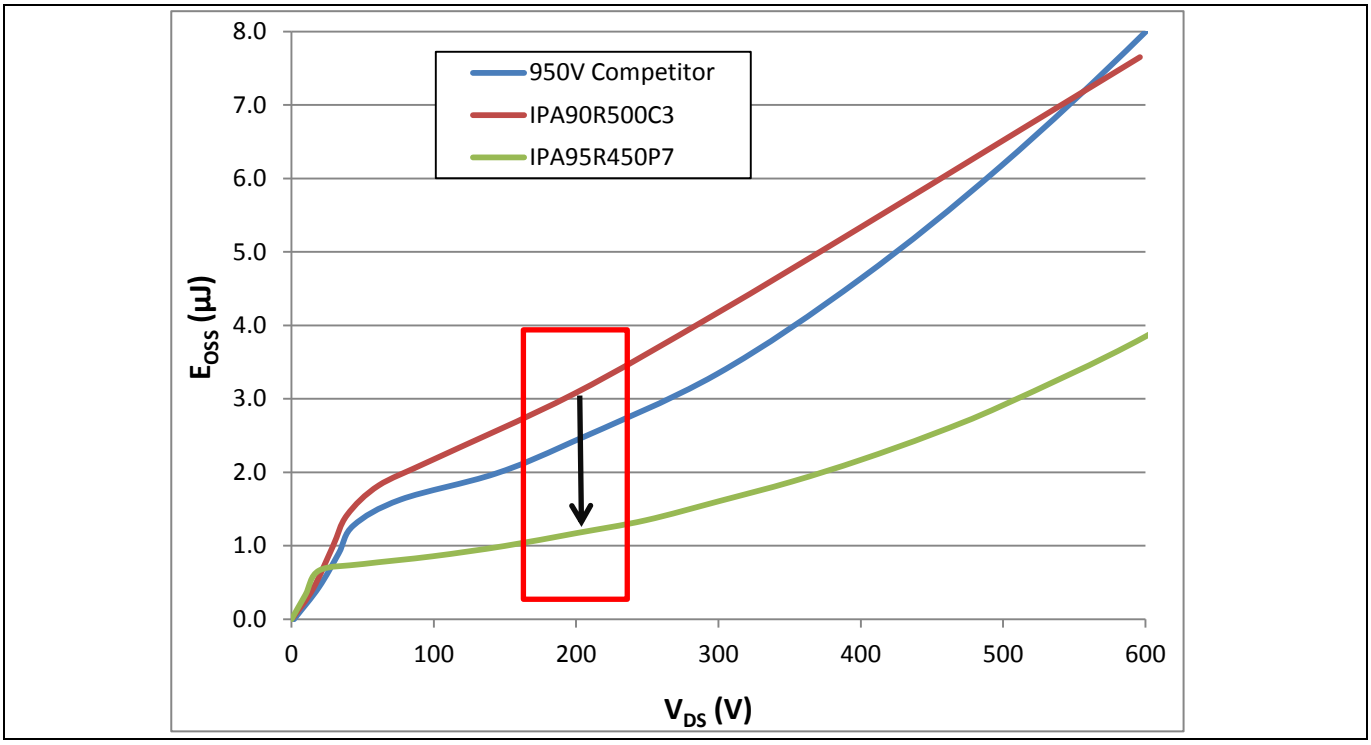

Figure 6 E_{oss} comparison of a 900 V 500 mΩ C3 MOSFET, a 950 V 450 mΩ P7 MOSFET and a competitor's 950 V 450 mΩ device

Figure 6 shows that the amount of energy stored in the output capacitance during a typical QR high-line turn-on of 200 V is reduced by 1.9 µJ every switching cycle, which in a 100 kHz design corresponds to 190 mW.

This improved E_{oss} performance of the P7 family of devices can be seen below in the 230 V AC measurements where a plug-and-play replacement of the C3 and competitor devices was done with the P7 MOSFET. It can be clearly seen that at the high-line operation the P7 gives an improvement of 0.35 percent in efficiency and 8.0°C on the MOSFET at full load.

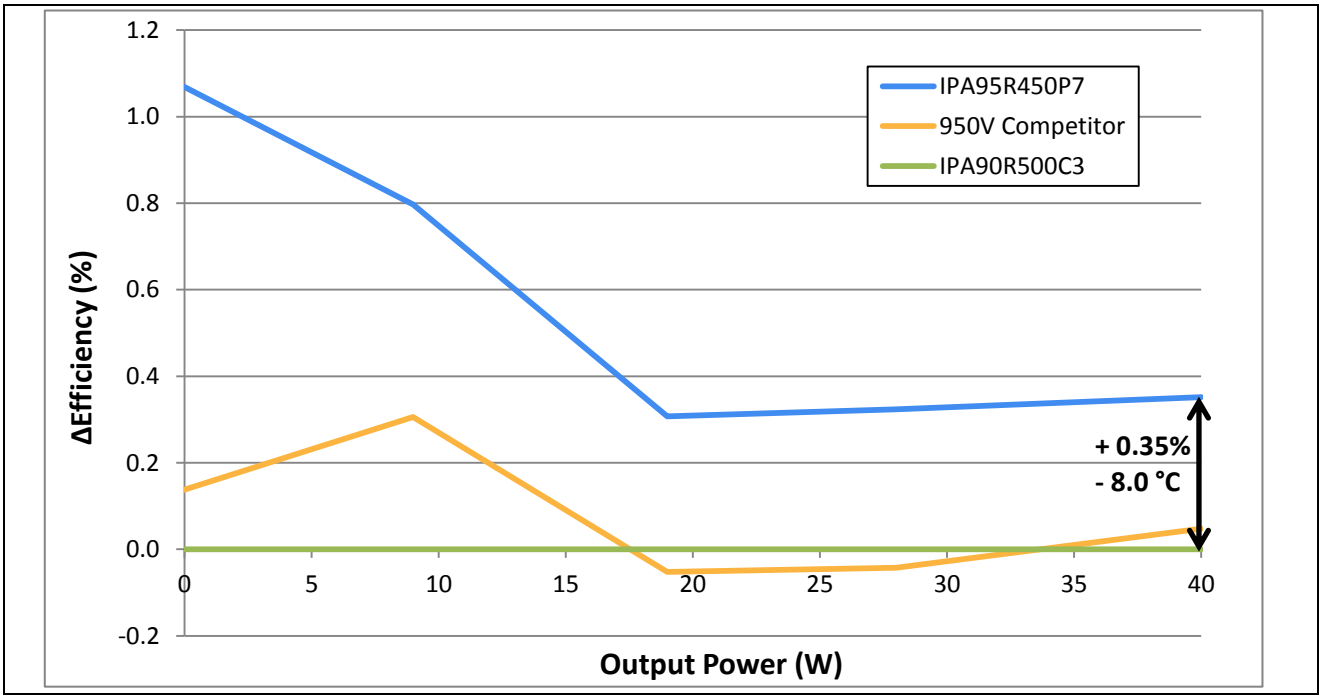

Figure 7 Efficiency of the 40 W adapter at 230 V AC showing the C3 and competitor's devices referenced to the P7 MOSFET

950 V CoolMOS™ P7 benefits for adapters

SPICE models of the 950 V CoolMOS™ P7 MOSFETs are provided on the Infineon website. These models have been created with MOSFET characterization data covering different MOSFET parameters, and provide a high level of accuracy. Below, Figure 8 shows the difference between an adapter's measured waveforms and the simulated waveforms when using the 700 V CoolMOS™ P7 SPICE models. These models can be used to better understand the loss mechanisms that are responsible for power dissipation in the primary MOSFET of the flyback converter, and they help to optimize designs.

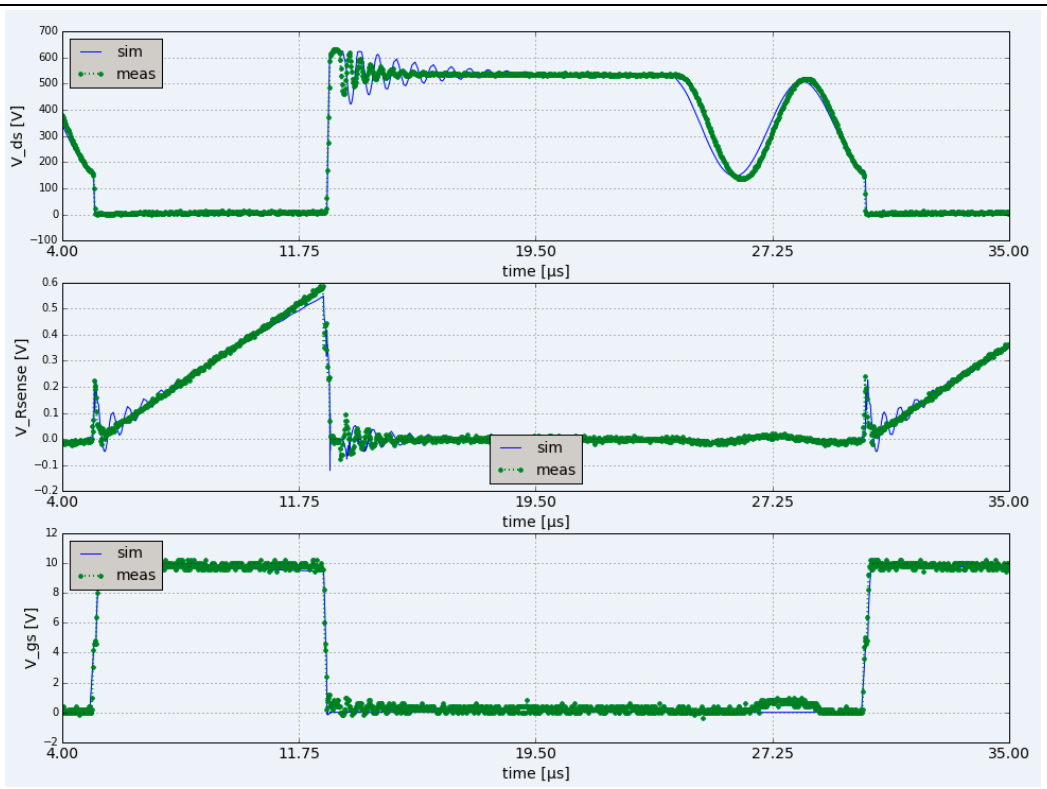

Figure 8 Simulated switching (blue) vs measured (green) switching at 230 V AC operation in an Infineon flyback evaluation board

5 Design considerations

5.1 950 V snubberless flyback design

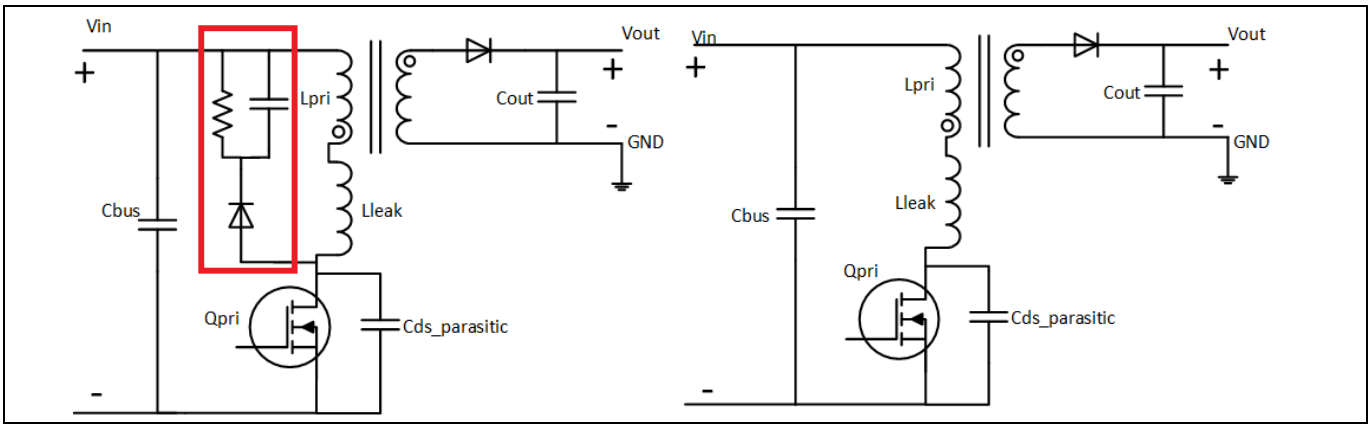

Figure 9 The typical RCD snubber configuration is shown on the left (red box). The snubberless configuration where this RCD network is removed is shown on the right.

Typically in a charger/adapter design a snubber network is used in order to clamp the leakage ringing, which occurs when the MOSFET switches off and the energy stored in the leakage energy rings with the total $C_{ds\_parasitic}$. By moving to a snubberless design PCB space can be saved by removing the snubber network, the snubber network hotspot can be eliminated, and the cost of the RCD snubber network can be eliminated. Depending on how the design has been configured, eliminating the snubber network can also help to improve system efficiency.

The losses of the system are reduced in a snubberless design due to the removal of two key loss mechanisms. The first is that the RCD network charges up to the reflected voltage every switching cycle regardless of the system load. The leakage inductance energy also increases this voltage, leading to further losses across the snubber resistor. The second loss mechanism comes from the additional capacitance added to the switching node from the RCD network as well as needing to charge the capacitance across the RCD diode junction. These loss mechanisms are eliminated by removing the RCD snubber network.

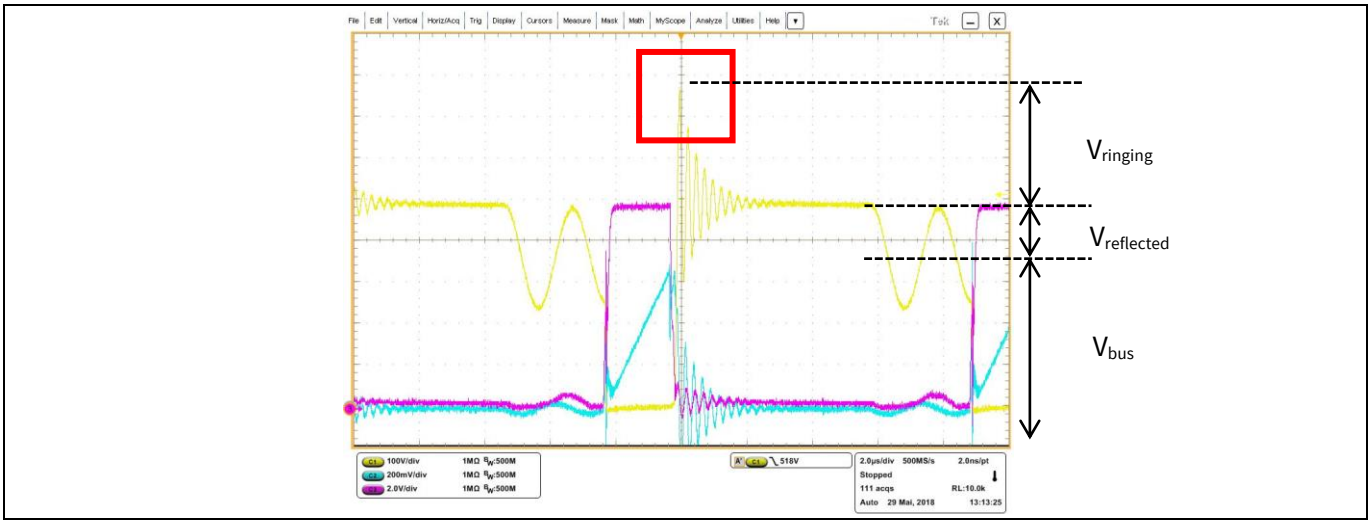

Figure 10 The MOSFET V_{DS} margin needs consideration for snubberless operation. The peak MOSFET voltage is determined by the V_{bus}, $V_{reflected}$ and $V_{ringing}$.

Design considerations

To keep the MOSFET drain source voltage from getting too high, an additional drain source capacitance is added across the drain node of the MOSFET. This leads to a higher C_{DS} switching loss when compared to the design with a snubber network, as shown in Figure 10 in red. The energy that is stored in the transformer leakage inductance gets dissipated in the high frequency copper loss of the transformer rather than in the RCD network, and this is what leads to the dampening of the snubber ringing waveform.

In designing a snubberless flyback converter, it is critical to make sure the $V_{(BR)DSS}$ of the MOSFET is not exceeded. The V_{DS} of a MOSFET consists of three main sections, as shown in Figure 10. The V_{DS} is the total of the bus voltage (V_{bus}), the reflected voltage ($V_{reflected}$) and the ringing voltage ($V_{ringing}$). The ringing voltage of the MOSFET is the only portion that is affected in the transition from an RCD snubber to a snubberless design. To understand how to remove the snubber, the mechanism behind the drain source ringing needs to be understood.

When the MOSFET is turned on in a flyback converter the current through the primary side of the transformer begins to ramp. When the MOSFET turns off this energy then transfers to the secondary of the flyback converter. Not all this energy transfers to the secondary, and the leakage inductance is the energy that cannot couple to the secondary. This energy then transfers to the total output capacitance of the MOSFET, which consists of the MOSFET C_{DS}, transformer parasitic capacitance, trace capacitance and any other capacitance on the drain node. An LC ringing occurs with the period set by the C_{DS} total and the $L_{leakage}$. To control the peak voltage of the drain source ringing an external capacitance can be added in parallel to the drain source of the MOSFET. In this adapter, an additional 100 pF capacitor on the drain source of the MOSFET was required to provide energy storage for the leakage energy at full load. A MOSFET with a 950 V breakdown voltage was used, which helps for the snubberless operation with a HV DC input. The peak drain source voltage at the maximum input voltage and maximum load was 782 V, which gives 17.6 percent margin. A minimum of 10 percent margin should be kept from the drain source breakdown voltage with worst-case component tolerances, so with this design there is still quite a bit of margin.

Some equations to get a first estimate of the peak V_{DS} voltage are shown below. The voltage derived from these equations is then shown to give the first estimate of the $V_{DS\ peak}$ compared to the measured value.

The peak bus voltage can be calculated by using the peak of the AC input voltage, as shown below.

$$V_{bus} = V_{ACinput\_max}\sqrt{2} = 265\text{ V AC} * 1.414 = 374\text{ V}$$

The reflected voltage is the transformer turns ratio multiplied by the output voltage.

$$V_{reflected} = (V_{out} + V_{rectifier})\frac{N_{pri}}{N_{sec}} = 128\text{ V}$$

The peak voltage caused by the ringing of the C_{DS} and leakage inductance can be approximated, with all the leakage energy transferring into the C_{DS} total capacitance.

$$V_{ringing} = I_{pk}\sqrt{\frac{L_{leakage}}{C_{DS\,total}}} = 307\text{ V}$$

Adding these three voltage portions of the drain source waveform yields the peak drain source voltage.

$$V_{DS\,peak} = V_{bus} + V_{reflected} + V_{ringing} = 809\text{ V}$$

This value of 809 V is conservative compared to the measured 782 V_{DS} peak. These equations tend to yield a conservative estimate of the breakdown voltage, since not all of the leakage energy transfers ideally to the total C_{DS} capacitance. This is good because it ends up ensuring that the device breakdown is not exceeded, although it can sacrifice some efficiency by being overly conservative.

Design considerations

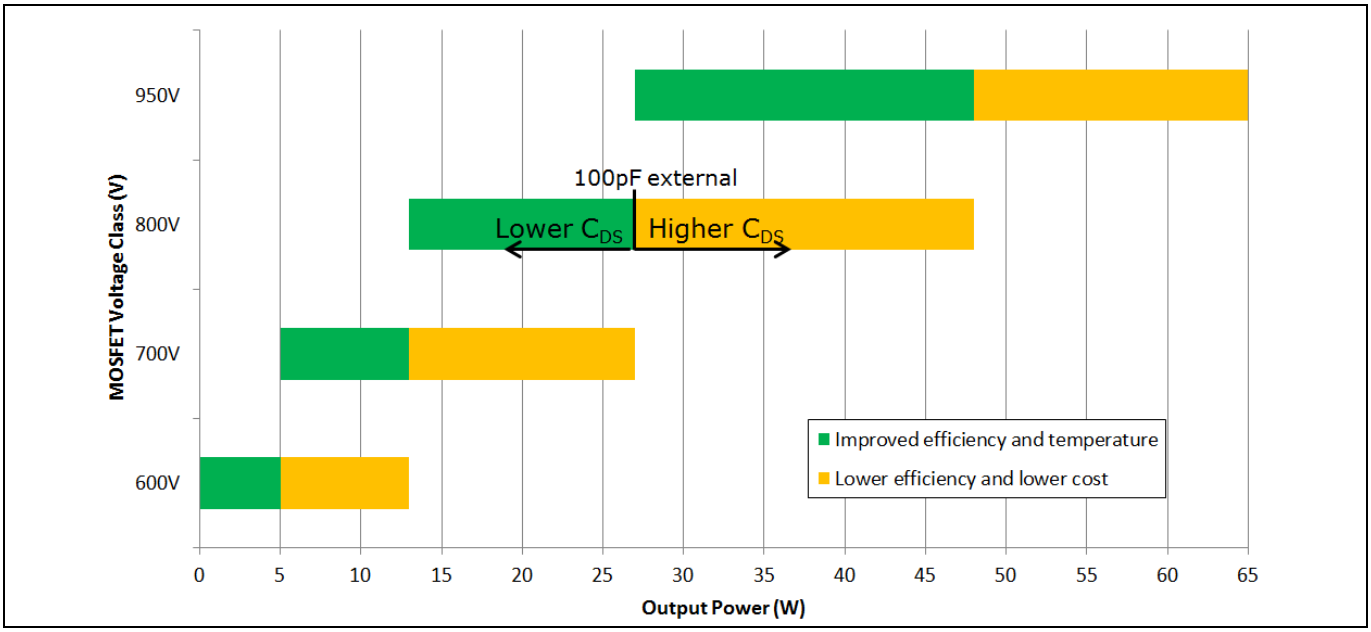

Figure 11 Snubberless flyback output power vs MOSFET voltage class for standard universal input 90 V AC to 265 V AC off-line power supplies

Looking at the benefits of the snubberless flyback operation, the question arises of where the snubberless concept is applicable. In a flyback converter the peak current on the input of the transformer increases as the system output power increases. Below is the equation for the peak current in a DCM flyback converter:

$$I_{pk} = \frac{2P_{in}}{V_{DCmin}D_{max}}$$

Looking at this peak current equation, it is clear that as the peak current increases with everything else held constant, the ringing and the V_{DS} peak will also increase.

$$V_{ringing} = I_{pk}\sqrt{\frac{L_{leakage}}{C_{DS\,total}}}$$

This leads to the chart shown in Figure 11, which takes common charger adapter DCM flyback requirements and looks at the $V_{(DS)BRR}$ voltage required for different output powers. This shows that as the output power of the system increases, a larger MOSFET breakdown voltage is required. This becomes a limiting factor in where a snubberless design can be used.

The other aspect shown in this chart is that a snubberless flyback converter can be designed with a larger and larger C_{DS} to absorb the transformer leakage energy. There is a point where the required additional C_{DS} capacitance losses will match the R_{CD} snubber losses, and then the only benefit to the snubberless operation is reduced PCB area and system cost. This boundary is shown in Figure 11 by the transition from green to yellow.

From the graph above, it can be seen that for an efficiency benefit in snubberless operation devices with a 600 V breakdown they should be used below 5 W, the 700 V devices should be used to 13 W, 800 V devices can be used to 27 W, and 950 V devices can be used to 48 W. Going beyond these boundaries would lower the system efficiency. The graph in Figure 11 makes several assumptions about the system design operating point, so these should be taken as guidelines rather than a hard boundary.

5.2 Snubberless thermal performance improvement

The worst-case nominal thermal conditions for the system under steady-state operation occur at 90 V AC and full output power (40 W). Table 2 shows the thermal improvement of the 950 V CoolMOS™ P7 when used in the 40 W adapter at 90 V AC and 40 W of output power due to the improvement in efficiency shown in the previous section. As shown below, the mold compound temperature of the 950 V CoolMOS™ P7 device is 5.1°C lower. Table 3 shows the maximum temperature under the worst-case operating conditions for these components when using the IPA95R450P7. These component temperatures are the limiting factor for the overall power density of the converter, and this can help to increase power density or improve thermal margins in designs.

Table 2 Flyback MOSFET thermal rise with 90 V AC, 40 W output at ambient temperature (25°C)

Device	Temperature rise	Temperature Δ referenced to P7
Competition	66.8°C	+8.0°C
IPA90R500C3	66.8°C	+8.0°C
IPA95R450P7	58.8°C	0.0°C

Table 3 Maximum component thermal rise at 90 V AC, 40 W output

Ref. des.	Component description	Maximum temperature rise
Q1	Flyback MOSFET	30.6°C
D3	Bridge rectifier	54.9°C
L1	Common mode choke	59.3°C
T1	Flyback transformer	67.8°C
D2	Flyback output diode	53.6°C
R22, R23, R28	Flyback snubber resistors	79.2°C

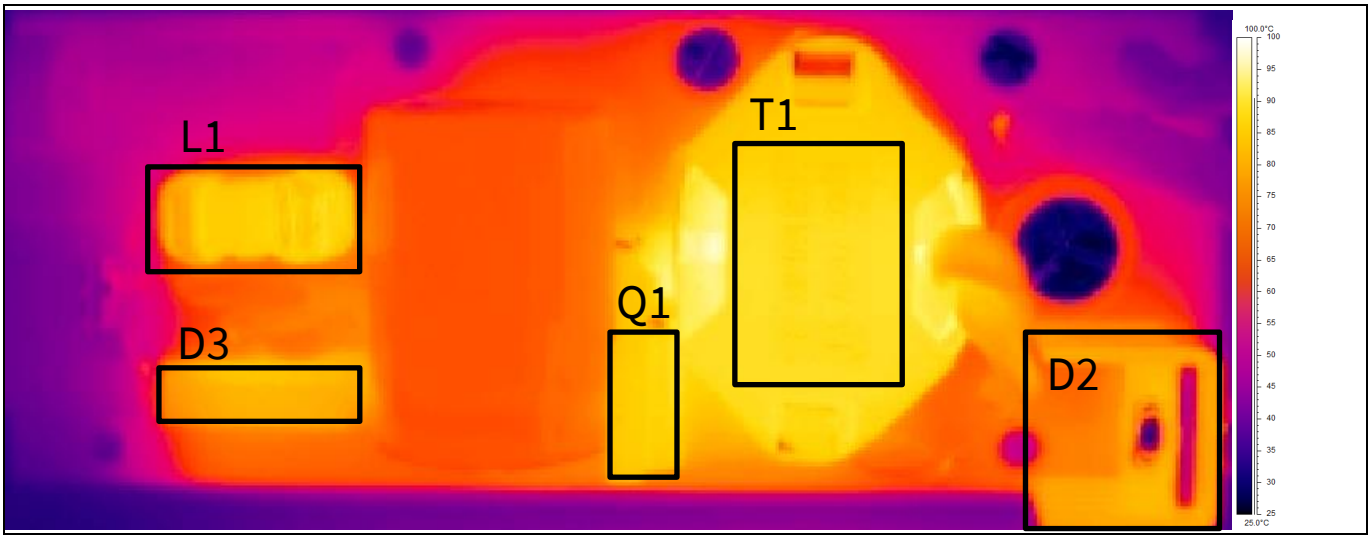

Figure 12 90 V AC input, full load, top side. The line filter (L1) and bridge rectifier (D1) are hottest at this point due to higher AC input currents.

In the table below it can be seen that by taking a version of the board using a 700 V CoolMOS™ P7 MOSFET and then transitioning to a snubberless design the hotspot on the PCB can be reduced by 40.6°C. This enables further shrinking of the design to increase the power density and reduce stress on the PCB.

Design considerations

Table 4 Snubber vs snubberless operation at 90 V AC, 40 W output

Board version	Ref. des.	Component description	Maximum temperature rise
700 V CoolMOS™ P7 40 W design with snubber	R22, R23, R28	Flyback snubber resistors	79.2°C
950 V CoolMOS™ P7 40 W design without snubber	R22, R23, R28	Unpopulated flyback snubber network	38.6°C

Below it can be seen in thermal images of the two versions of the boards how the hotspot is significantly reduced by eliminating the snubber network. This opens up more PCB space and allows for reducing the system cost by eliminating the snubber network.

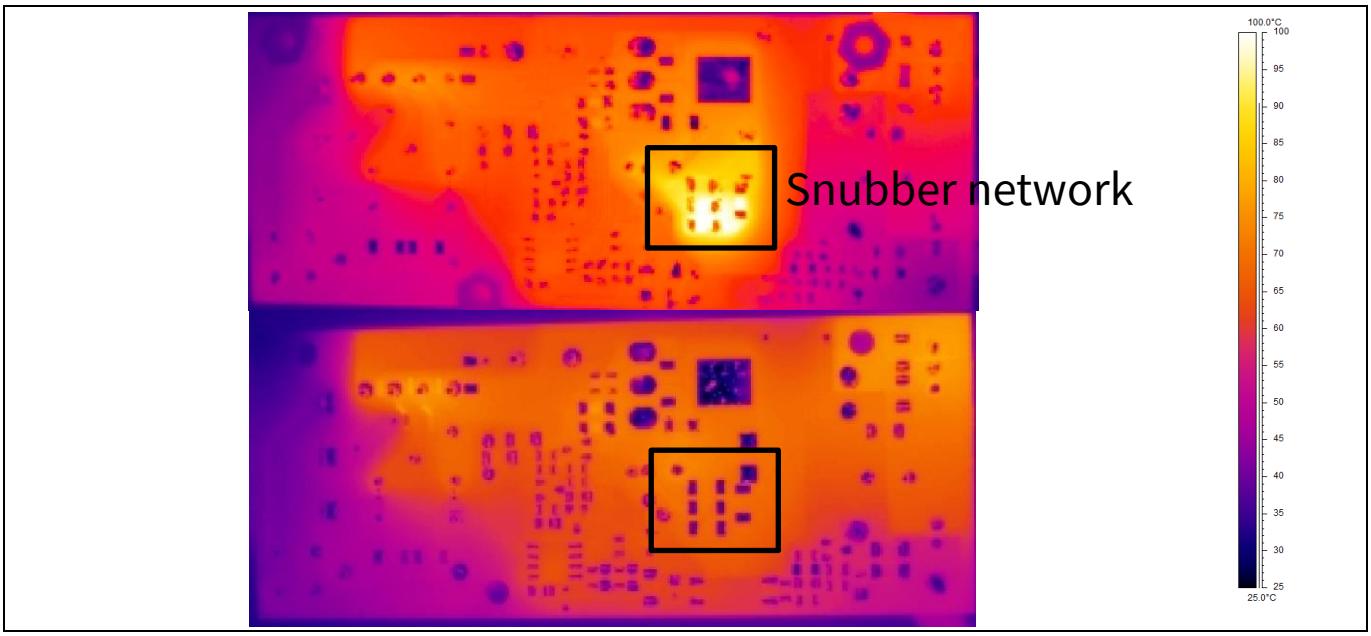

Figure 13 90 V AC input, full load, bottom side.

In Figure 13 on the top the 700 V CoolMOS™ P7 40 W version of the demo board using a snubber network is shown. On the bottom picture the 950 V CoolMOS™ P7 40 W version of the demo board is placed. The snubber resistors are the hottest components on the PCB creating additional thermal losses.

5.3 UVLO circuit

The Under Voltage Lock Out (UVLO) circuit provides a mechanism to shut down the power supply when the AC-line input voltage is lower than the specified voltage range. The UVLO event is detected by sensing the voltage level at U2's (TL431) REF pin (V_{REF_typ} = 2.5 V) through the voltage divider resistors (R12, R13, R14 and R17 inFigure 18) from the bulk capacitor C1. Q2 acts as a switch to enter or leave UVLO mode by controlling the FB pin voltage. Q3, together with R17, acts as voltage hysteresis for the UVLO circuit, and U2 (TL431) acts as a comparator. The system enters UVLO mode by controlling the FB pin voltage of U1 to 0 V (when the voltage input level goes back to input voltage range), V_{REF} increases to 2.5 V (then switches Q2 and Q3 off) and when V_{cc} hits 18 V, UVLO mode is released. The calculation for the UVLO circuit is shown below:

V_{REF} = 2.5 V

R12 = 4.99 MΩ R13 = 4.99 MΩ R14 = 330 kΩ R17 = 681 kΩ

$$V_{bulk\_enterUVLO} = \frac{(R12 + R13 + R14)Vref}{R14}$$

Design considerations

$$V_{bulk\_leaveUVLO} = \frac{\left[\left(\frac{R14R17}{R14+R17}\right) + R12 + R13\right] Vref}{\left(\frac{R14R17}{R14+R17}\right)}$$

$V_{bulk\_enterUVLO} = 77.8\ V_{DC}$

$V_{bulk\_leaveUVLO} = 114.3\ V_{DC}$

The “enter UVLO” threshold is set at 77.8 V_{DC} to allow for the bus capacitance voltage to drop under 90 V AC at full-load operation with some margin to avoid false triggering.

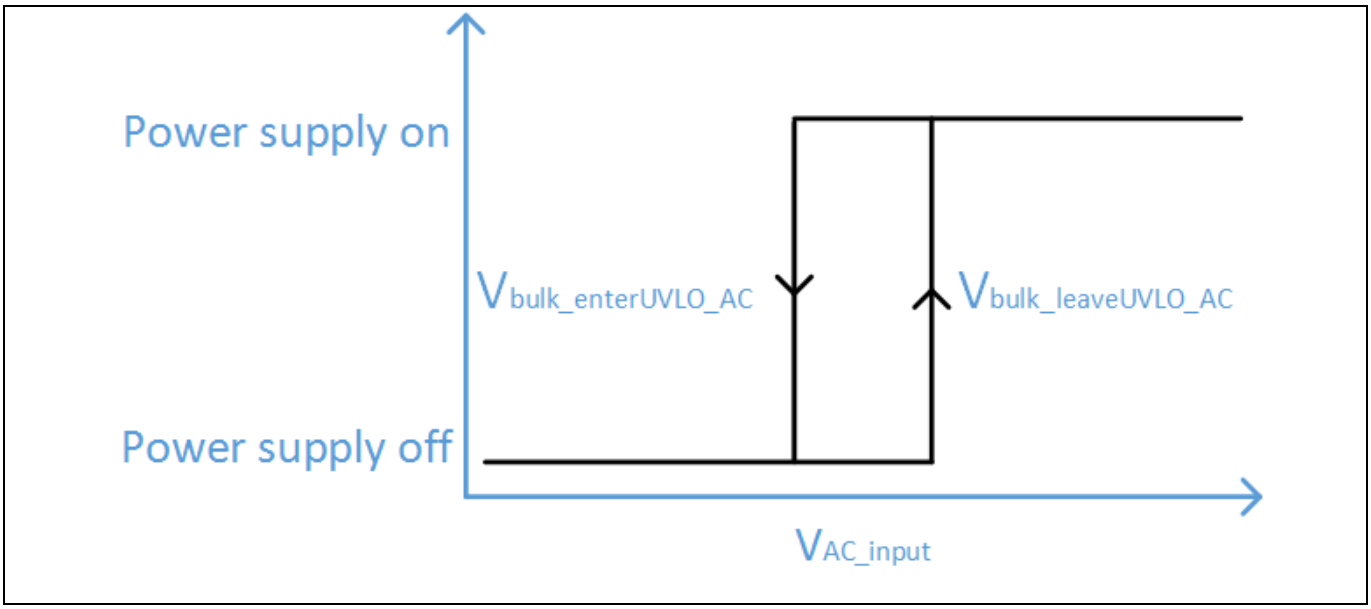

Figure 14 Power supply status vs AC input voltage showing the hysteretic behavior of the UVLO circuit

6 Evaluation board overview

6.1 Evaluation board pictures

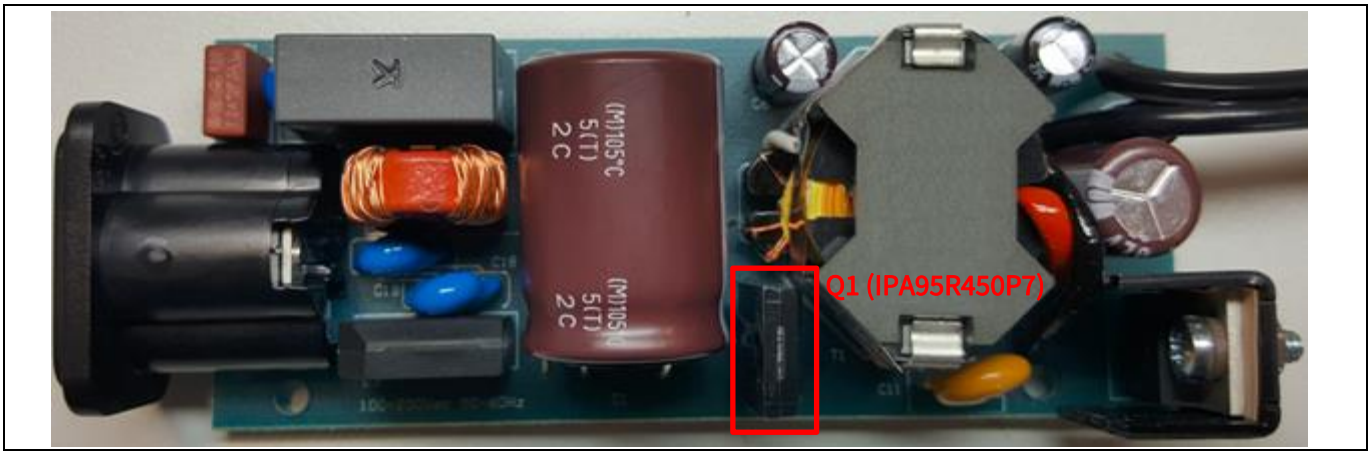

Figure 15 Top side of the 40 W Infineon adapter with a TO-220 FullPAK

As can be seen in the picture above, the Infineon demo board comes equipped with a MOSFET in a TO-220 FP package (IPA95R450P7).

To evaluate other packages and power levels, on the back side of the board, an additional DPAK (or SOT223) footprint was designed. The MOSFET can be easily removed from the top side, and soldered into another package variant on the back side (as shown in the red box in Figure 16).

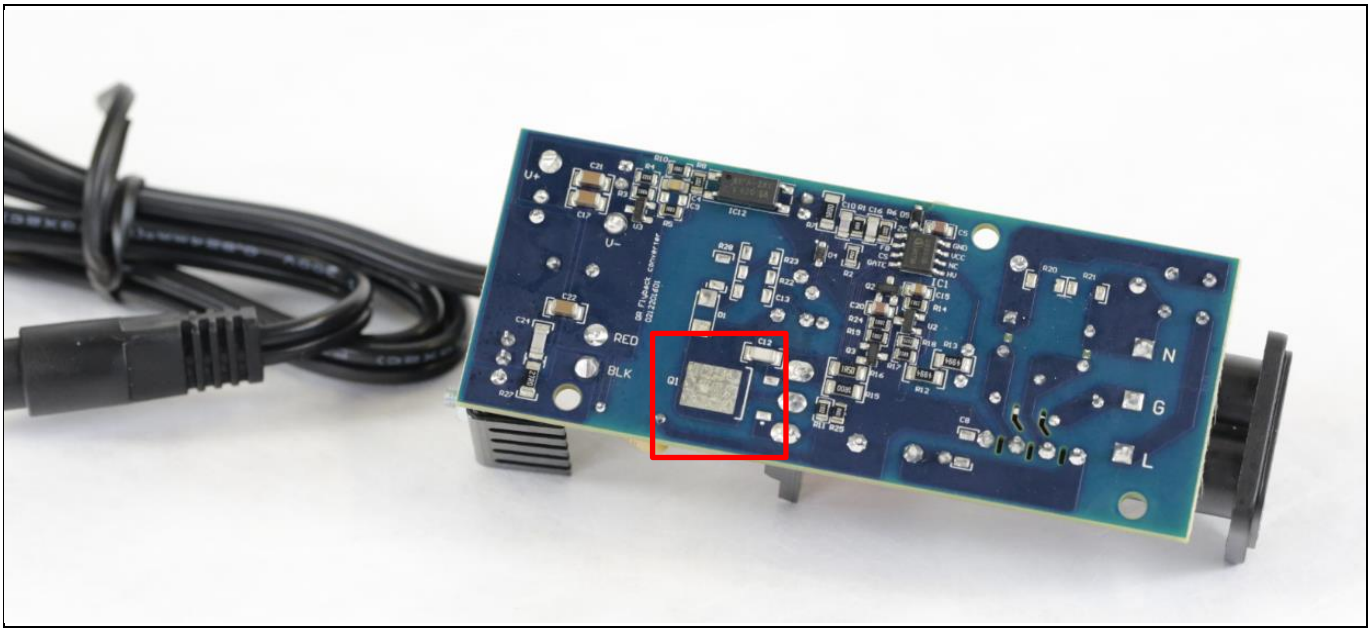

Figure 16 Back side of the 40 W adapter (DPAK/SOT223 package option)

Evaluation board overview

Figure 17 40 W Infineon adapter demo board (order code: EVAL_40W_FLY_P7_950V)

6.2 Evaluation board specifications

Table 5

Section	Parameter	Specification
Input ratings	Input voltage	90 V AC to 265 V AC
	Input frequency	47 Hz to 63 Hz
	Input current at 100 V AC, 40 W	0.85 A maximum
	Power factor	0.53 at 100 V AC 0.36 at 265 V AC
	Peak efficiency at 230 V AC, 40 W Peak efficiency at 90 V AC, 40 W	90.5 percent 88.6 percent
	Surge	2 kV IEC61000-4-5
Output ratings	Nominal output voltage	19.0 V
	Tolerance	2 percent
	Output current	2.10 A
	Output power	40 W
	Line regulation	0.5 percent
	Load regulation	0.5 percent
	Output ripple	Less than 200 mV_{PP}
	Quiescent power draw	55 mW at 100 V AC 111 mW at 265 V AC
	Switching frequency	25 kHz to 60 kHz
Mechanical	Dimensions	Length: 10.0 cm (3.94 in.) Width: 3.7 cm (1.46 in.) Height: 2.6 cm (1.02 in.)
Environmental	Ambient operating temperature	-25°C to 50°C

6.3 Evaluation board features

- **Fold-back point protection:** For a QR flyback converter, the maximum possible output power is increased when a constant current limit value is used across the entire mains input voltage range. This is usually not desirable, as this will increase the cost of the transformer and output diode in the case of output over-power conditions. The internal fold-back protection is implemented to adjust the V_{CS} voltage limit according to the bus voltage. Here, the input-line voltage is sensed using the current flowing out of the ZC pin, during the MOSFET on-time. As the result, the maximum current limit adjusts with the AC-line voltage.
- **V_{cc} Over Voltage and Under Voltage Protection (OVP/UVP):** During normal operation, the V_{cc} voltage is continuously monitored. When the V_{cc} voltage increases to V_{VCC} OVP or V_{cc} voltage falls below the UVLO level V_{VCC} off, the IC will enter auto-restart mode.
- **Over-load/open-loop protection:** In the case of an open control loop, the feedback voltage is pulled up with an internal block. After a fixed blanking time, the IC enters auto-restart mode. In case of a secondary short-circuit or over-load, the regulation voltage V_{FB} will also be pulled up, the same protection is applied and the IC will auto-restart.
- **Adjustable output OVP:** During the off-time of the power switch, the voltage at the zero-crossing pin, ZC, is monitored for output over-voltage detection. If the voltage is higher than the preset threshold 3.7 V for a preset period of 100 µs, the IC is latched off.

Evaluation board overview

- **Auto-restart for over-temperature protection:** The IC has a built-in over-temperature protection function. When the controller's temperature reaches 140°C, the IC will shut down the switch and enters auto-restart. This can protect the power MOSFET from overheating.
- **Short winding protection:** The source current of the MOSFET is sensed via external resistors R15 and R16. If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} of 1.68 V during the on-time of the power switch, the IC is latched off. This constitutes a short winding protection. To avoid an accidental latch-off, a spike blanking time of 190 ns is integrated into the output of the internal comparator.

6.4 Schematic

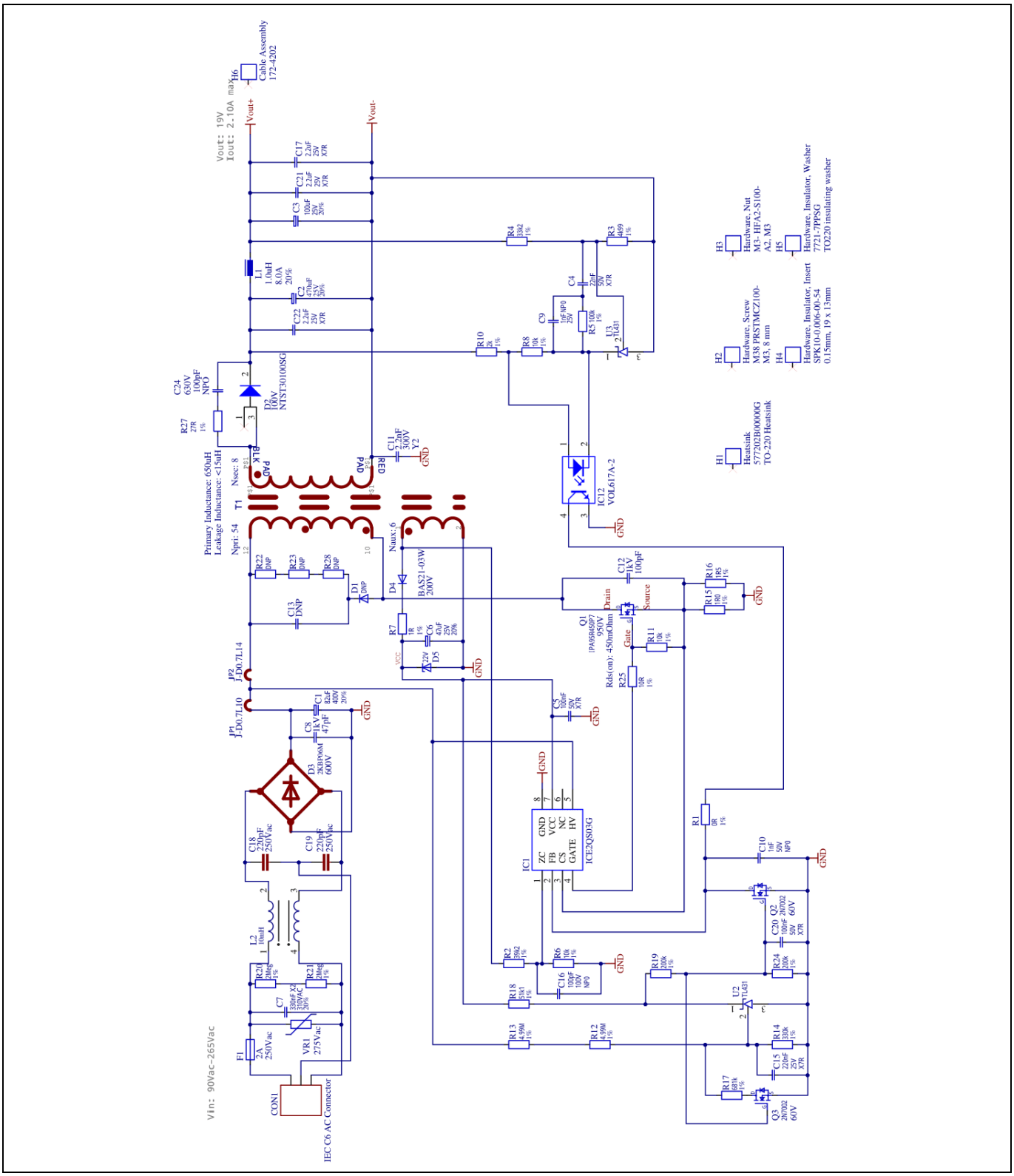

Figure 18 40 W adapter schematic (snubberless version)

6.5 BOM with Infineon components in bold

Table 6

Reference	Description	Part number	Manufacturer
C1	Electrolytic capacitor, 82 µF, 20 percent, 400 V	EKXG401ELL820MM25S	United Chemi-Con
C2	Electrolytic capacitor, 470 µF, 20 percent, 25 V	EKZE250ELL471MJ16S	United Chemi-Con
C3	Electrolytic capacitor, 100 µF, 20 percent, 25 V	EEU-FR1E101	Panasonic
C4	Ceramic capacitor, 22 nF, X7R, 50 V, CAP0805W	VJ0805Y223KNAAO	Vishay
C5, C20	Ceramic capacitor, 100 nF, X7R, 50 V, CAP0805W	C2012X7R2A104K125AA	TDK
C6	Electrolytic capacitor, 47 µF, 20 percent, 25 V, 5 mm	UPM1E470MED	Nichicon
C7	Foil capacitor, 330 nF, X2, 20 percent, 310 V AC, C_Foil 15 mm – V2	R463I33305002K	Kemet
C10	Ceramic capacitor, 1 nF, NP0, 50 V, CAP0805W	CGA4C2C0G1H102J060AA	TDK
C11	Capacitor Y2, 2.2 nF, Y2, 300 V, CAP-DISC 7.5 mm	AY2222M35Y5US63L7	Vishay
C12	Ceramic capacitor, 100 pF, X7R, 1000 V, CAP1206W	C1206C101KDRACTU	Kemet
C13	DNP		
C15	Ceramic capacitor, 220 nF, X7R, 25 V, CAP0805W	C2012X7R1H224K125AA	TDK
C16	Ceramic capacitor, 68 pF, NP0, 100 V, CAP0805W	MC0805N680J101CT	Multicomp
C17, C21, C22	Ceramic capacitor, 2.2 µF, X7R, 25 V, CAP1206W	C3216X7R1E225K160AA	TDK
C18, C19	220 pF/250 V AC, 220 pF, 250 V AC, C075-045X100	VY2221K29Y5SS63V0	Vishay
C24	Ceramic capacitor, 100 pF, NPO, 630 V, CAP1206W	CGA5C4C0G2J101J060AA	TDK
CON1	ST-04A, IEC C6 AC connector, ST-A04	6160.0003	Schurter
D1	DNP		
D2	Diode, NTST30100SG, 100 V, TO-220_standing	NTST30100SG	OnSemi
D3	2KBP06M, 2KBP06M, 600 V, KBPM	2KBP06M-E4/51	Vishay
D4	**Diode, BAS21-03W, 200 V, SOD323**	**BAS21-03W**	**Infineon**
D5	Diode, 22 V Zener, SOD323	BZX384-C22	NXP
F1	T2, 2 A, 250 V AC, small fuse	40012000440	Littelfuse
H1	Heatsink, TO-220 heatsink	577202B00000G	Aavid thermalloy
H2	Hardware, screw, M3, 8 mm	M38 PRSTMCZ100-	Duratool

Evaluation board overview

Reference	Description	Part number	Manufacturer
H3	Hardware, nut, A2, M3	M3- HFA2-S100-	Duratool
H4	Hardware, insulator, insert, 0.15 mm, 19 x 13 mm	SPK10-0.006-00-54	Bergquist
H5	Hardware, insulator, washer, TO-220 insulating washer	7721-7PPSG	Aavid Thermalloy
H6	Cable assembly	172-4202	Memory Protection Devices, Inc.
IC1	**QR PWM controller**	**ICE2QS03G**	**Infineon**
IC12	VOL617A-2, VOL617A-2, LSOP 4-pin	VOL617A-2X001T	Vishay
L1	Choke, 1.0 µH, 20 percent, inductor, 4 µ7, 4.2 A	7447462010	Wurth
L2	Inductance, 10 mH, inductor common mode small	744821110	Wurth
Q1	**NMOS, IPA95R450P7, 950 V, TO-220FP**	**IPA95R450P7**	**Infineon**
Q2, Q3	**NMOS, 2N7002, 60 V, SOT23**	**2N7002**	**Infineon**
R1	Resistor, 0R, 1 percent, RES0805R	CRCW08050000Z0EA	Vishay
R2	Resistor, 39k2, 1 percent, RES0805R	ERJ6ENF3922V	Panasonic
R3	Resistor, 4k99, 1 percent, RES0805R	CRCW08054K99FKEA	Vishay
R4	Resistor, 33k2, 1 percent, RES0805R	CRCW080533K2FKEA	Vishay
R5	Resistor, 100k, 1 percent, RES0805R	CRCW0805100KFKEA	Vishay
R6, R8, R11	Resistor, 10k, 1 percent, RES0805R	CRCW080510K0FKEA	Vishay
R7, R15	Resistor, 1R, 1 percent, RES1206W	CRCW12061R00FKEA	Vishay
R10	Resistor, 2k, 1 percent, RES0805R	CRCW08052K00FKEA	Vishay
R12, R13	Resistor, 4.99 M, 1 percent, RES1206W	CRCW12064M99FKEB	Vishay
R14	Resistor, 330k, 1 percent, RES0805R	CRCW0805330KFKEA	Vishay
R16	Resistor, 1R5, 1 percent, RES1206W	CRCW12061R50JNEAIF	Vishay
R17	Resistor, 681 k, 1 percent, RES0805R	CRCW0805681KFKEA	Vishay
R18	Resistor, 51k1, 1 percent, RES0805R	ERJ6ENF5112V	Panasonic
R19, R24	Resistor, 200 k, 1 percent, RES0805R	CRCW0805200KFKEA	Vishay
R22, R23, R28	DNP		
R25	Resistor, 10R, 1 percent, RES1206W	CRCW120610R0FKEA	Vishay
R27	Resistor, 27R, 1 percent, RES1206W	CRCW120627R0FKEA	Vishay
T1	Transformer, RM10	ICE 8045.0804.043	I.C.E. Transformers
U2, U3	Reference IC, TL431	TL431ACDBZT	TI
VR1	Varistor, 8.6 J, 275 V AC	B72205S0271K101	EPCOS

6.6 PCB layout

The PCB was designed using Altium Designer 16. Schematic and board files are available on request.

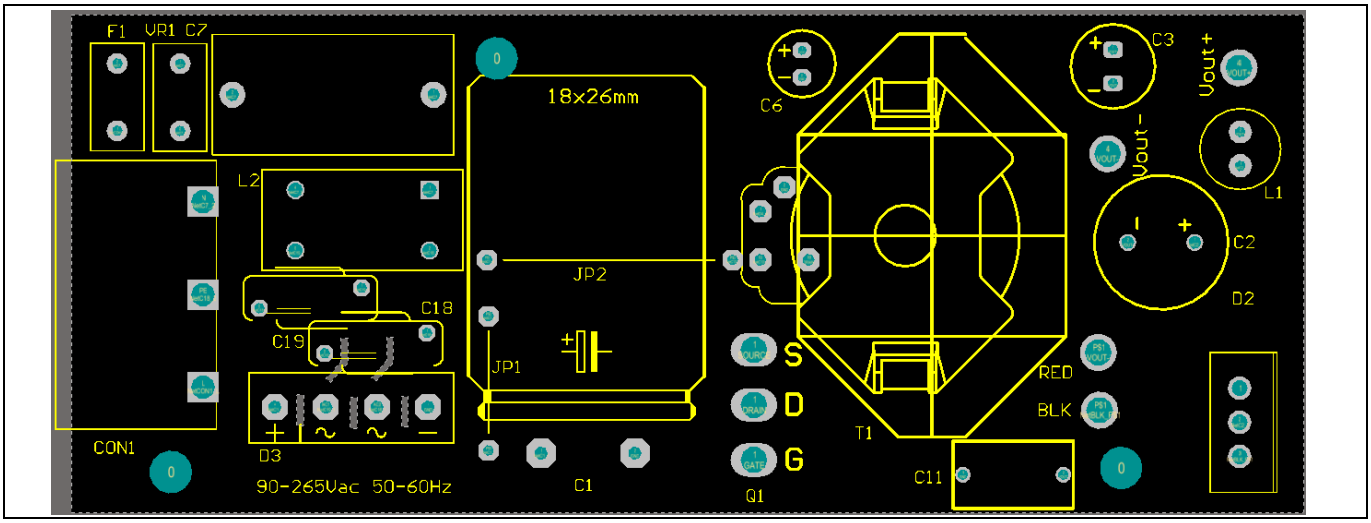

Figure 19 Board layout top

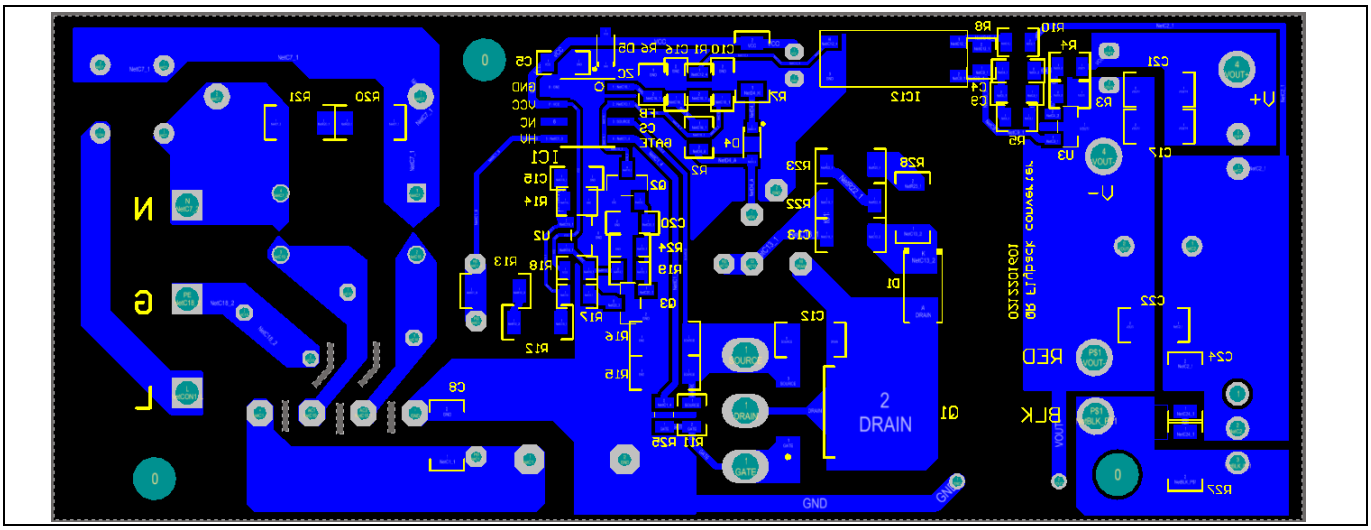

Figure 20 Board layout bottom

6.7 Transformer construction

The transformer for the 40 W adapter was built by I.C.E. Transformers: http://www.icetransformers.com/

Table 7 Transformer specification

Manufacturer	I.C.E. Transformers
Core size	RM10
Core material	3C95
Bobbin	8-pin RM10 vertical
Primary inductance	650 µH measured from pin 6 to pin 4 at 10 kHz
Leakage inductance	Less than 15 µH measured from pin 6 to pin 4 at 10 kHz pins S-, S+, 1 and 2 shorted

*100 percent of components are Hi-Pot tested to 4.2 kV primary to secondary for 1 minute.

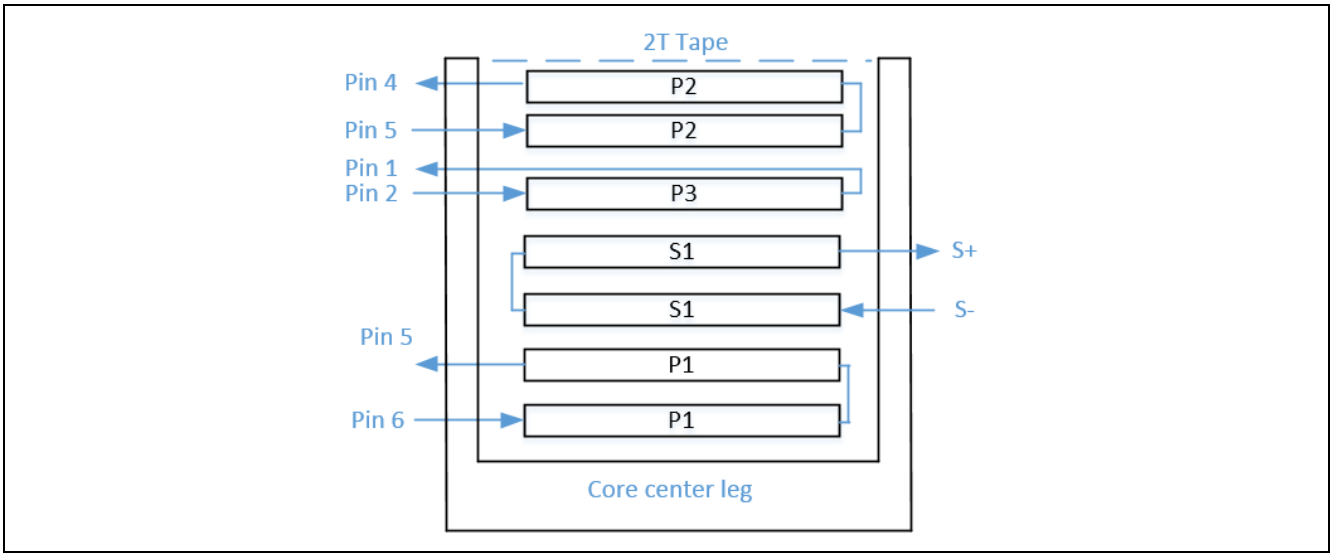

Figure 21 Transformer windings stack-up

1. S- in red tube, S+ in black tube
2. S- length 30 mm, solder length 5 mm
3. S+ length 30 mm, solder length 5 mm
4. Cut pin 3, pin 5, core clip PCB mount pins and secondary pins.
5. Add a flux band of 8 mm copper foil with two layers of tape and 3 mm of cuffing on each side. Add around the core with the tape side facing out. Use 0.35 mm solder to pin 2.
6. Vacuum varnish the entire assembly.
7. Cut the core clamp pins off of the transformer.

Table 8 Transformer windings stack-up

Name	Start	Stop	Turns	Wire gauge	Layer	Winding
P1	6	5	27	1 x 0.35 mm	Primary	Evenly spaced
S1	S-	S+	8	2 x 0.50 mm triple insulated	Secondary	Evenly spaced
P3	2	1	6	1 x 0.15 mm, with margin tape	Auxiliary	Evenly spaced
P2	5	4	27	1 x 0.35 mm	Primary	Evenly spaced
T1			2	Tape		

7 Measurements

7.1 Efficiency results

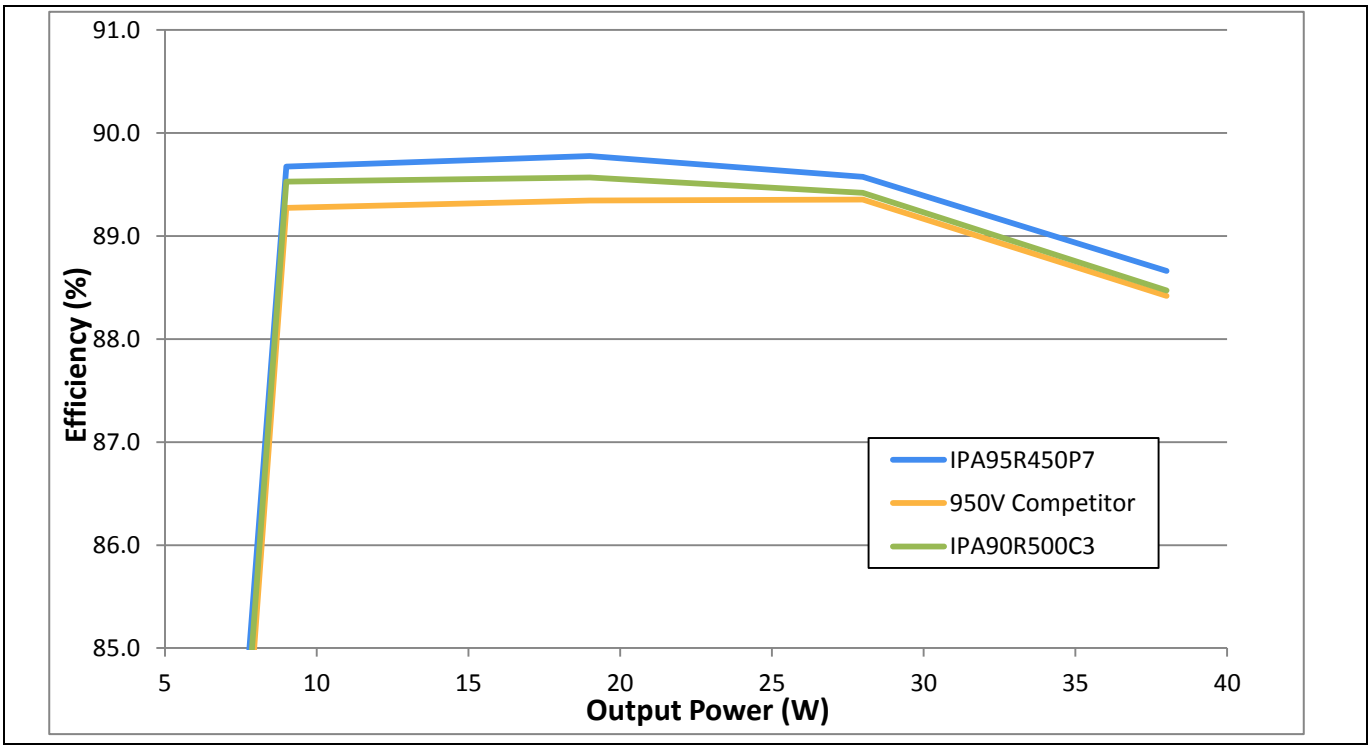

Figure 22 40 W adapter efficiency at 90 V AC with the IPA95R450P7 compared to the C3 technology and a 950 V competitor

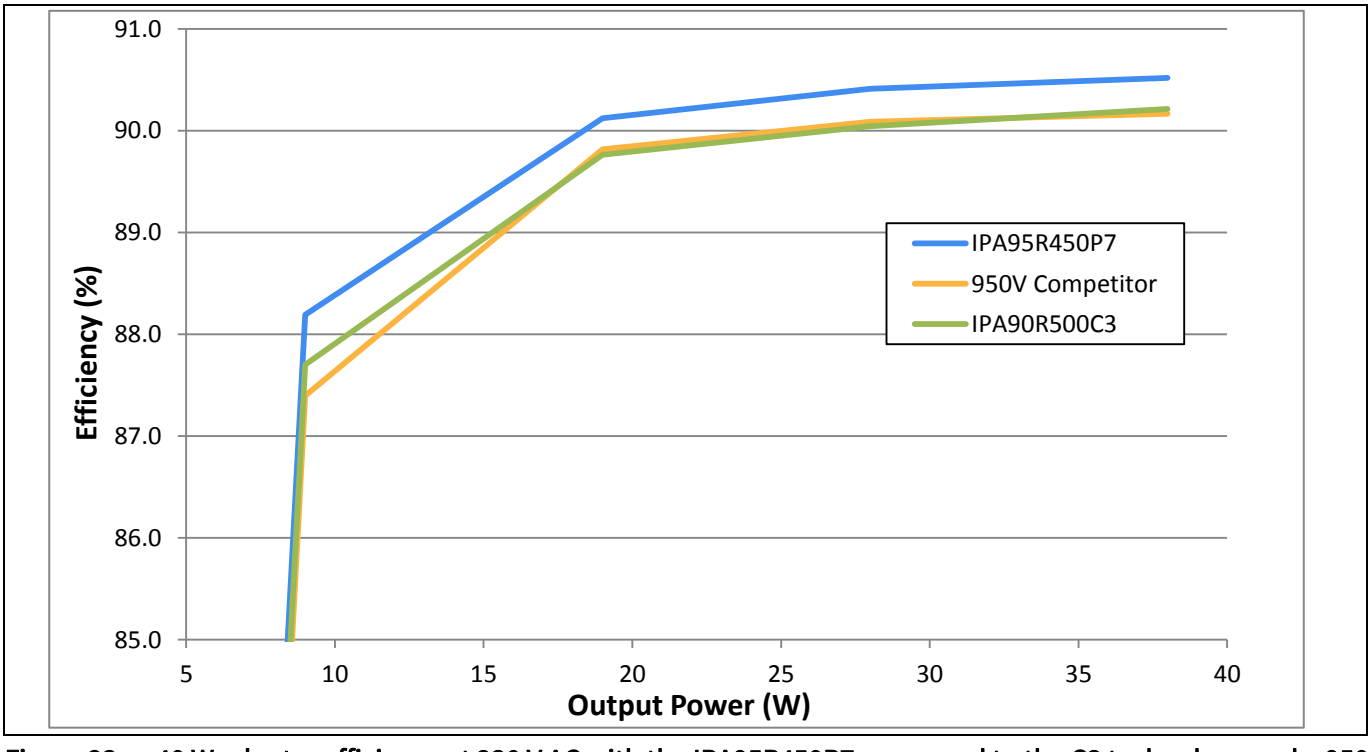

Figure 23 40 W adapter efficiency at 230 V AC with the IPA95R450P7 compared to the C3 technology and a 950 V competitor

Measurements

Figures 22 and Figure 23 show the benefits of changing to a P7 device from the previous C3 technology or a competitor's device. The efficiency graphs below are done as efficiency deltas relative to the C3 IPA90R500C3 in order to make the efficiency differences clearer.

The 90 V AC and full-load efficiency difference ends up reducing the mold compound temperature by 5.1°C.

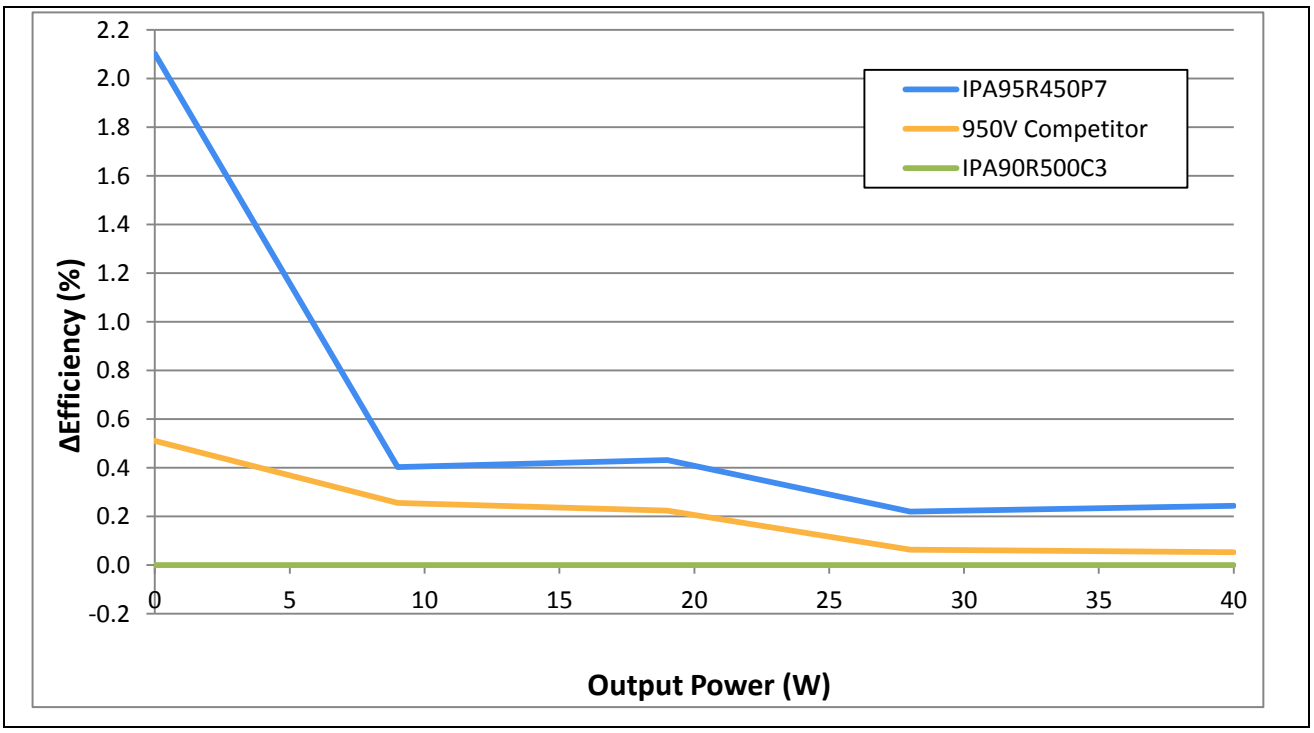

Figure 24 Efficiency of the 40 W adapter at 90 V AC showing the C3 and competitor's devices referenced to the P7 MOSFET

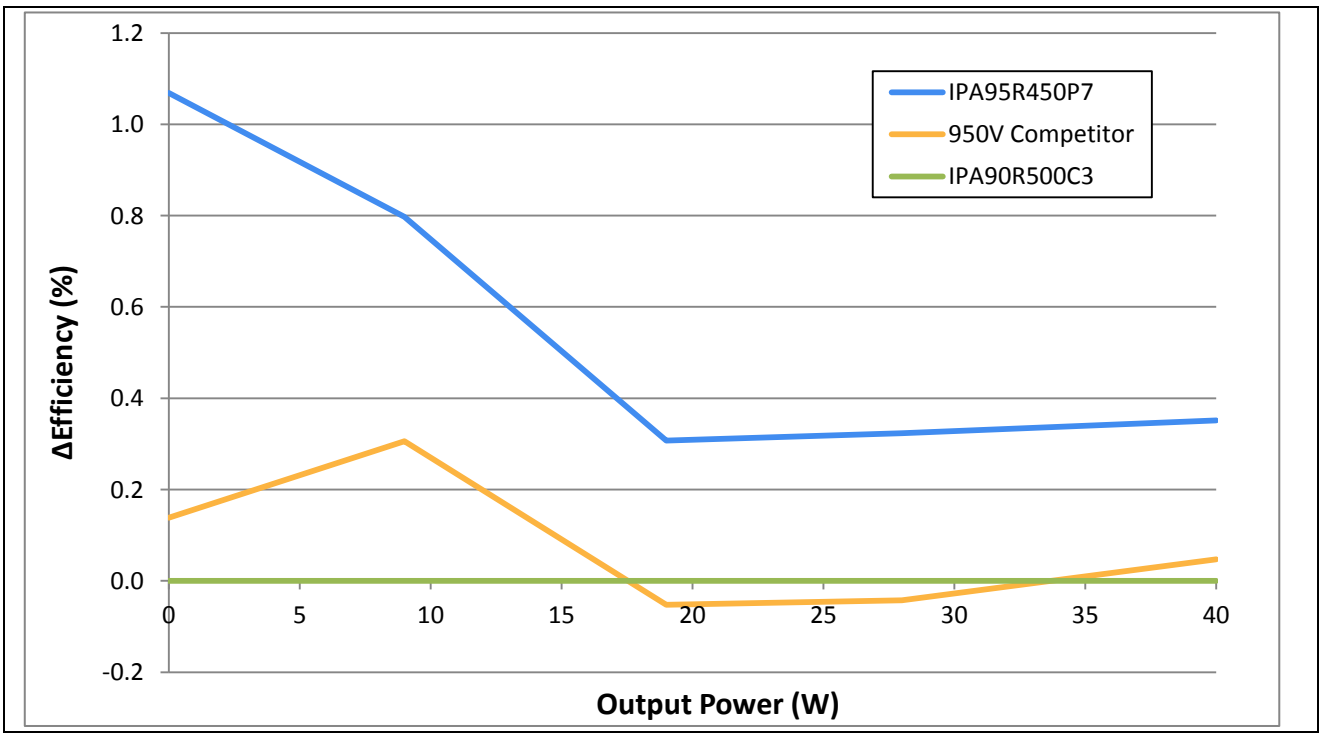

Figure 25 Efficiency of the 40 W adapter at 230 V AC showing the C3 and competitor's devices referenced to the P7 MOSFET

7.2 High-line and low-line operation

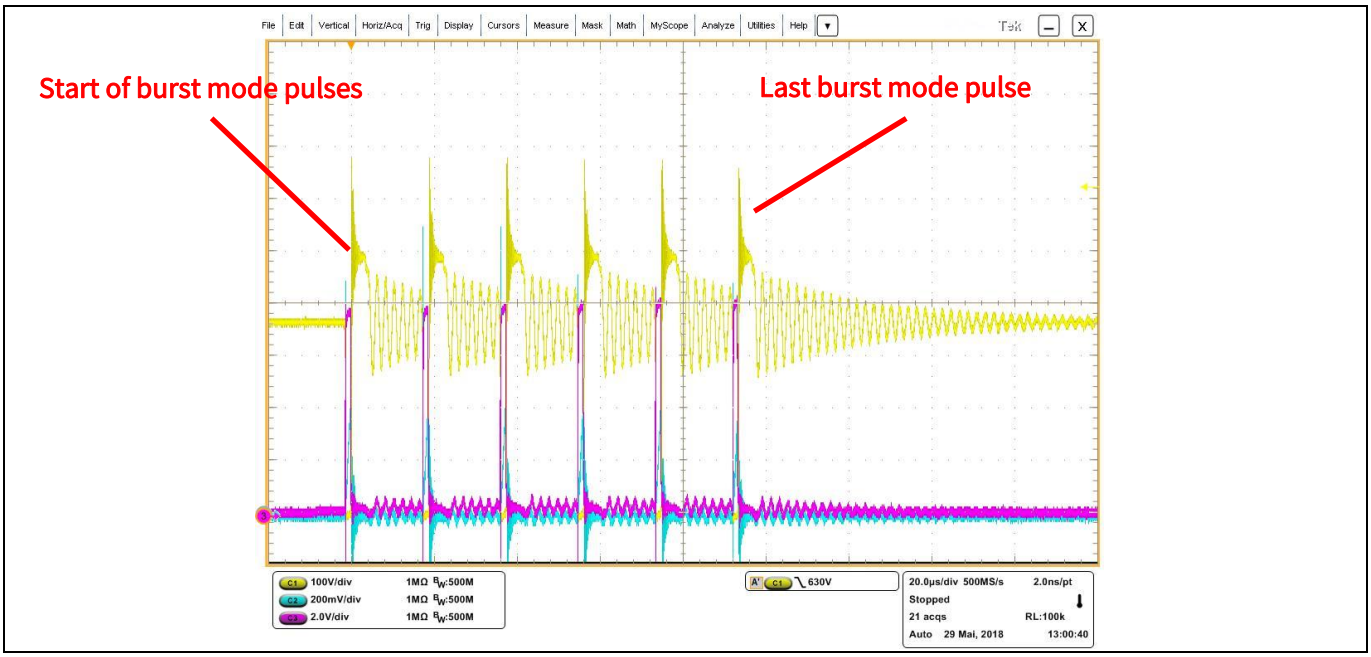

Figure 26 High-line (265 V AC), no load. The ICE2QS03G is operating in burst mode to minimize idle power consumption. The burst mode pulse train shown above occurs every 33.8 ms. QR valley switching does not occur during burst mode due to the ICE2QS03G changing operating modes at light load. V_{DS} maximum is 687 V in burst mode operation.

CH1 (yellow): Q1 V_{DS}

CH2 (cyan): Q1 I_{DS}

CH3 (magenta): Q1 V_{GS}

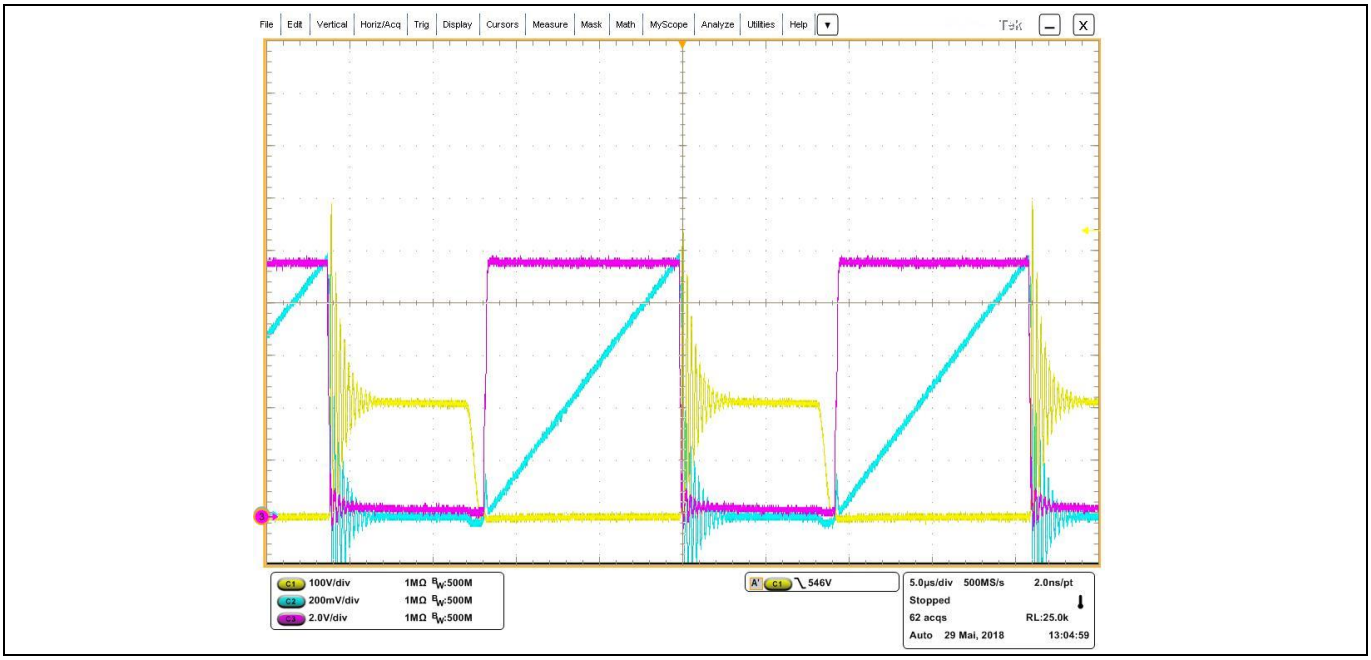

Figure 27 Low-line (90 V AC), full load (40 W). This is the peak current that the primary MOSFET Q1 will encounter during steady-state operation.

Measurements

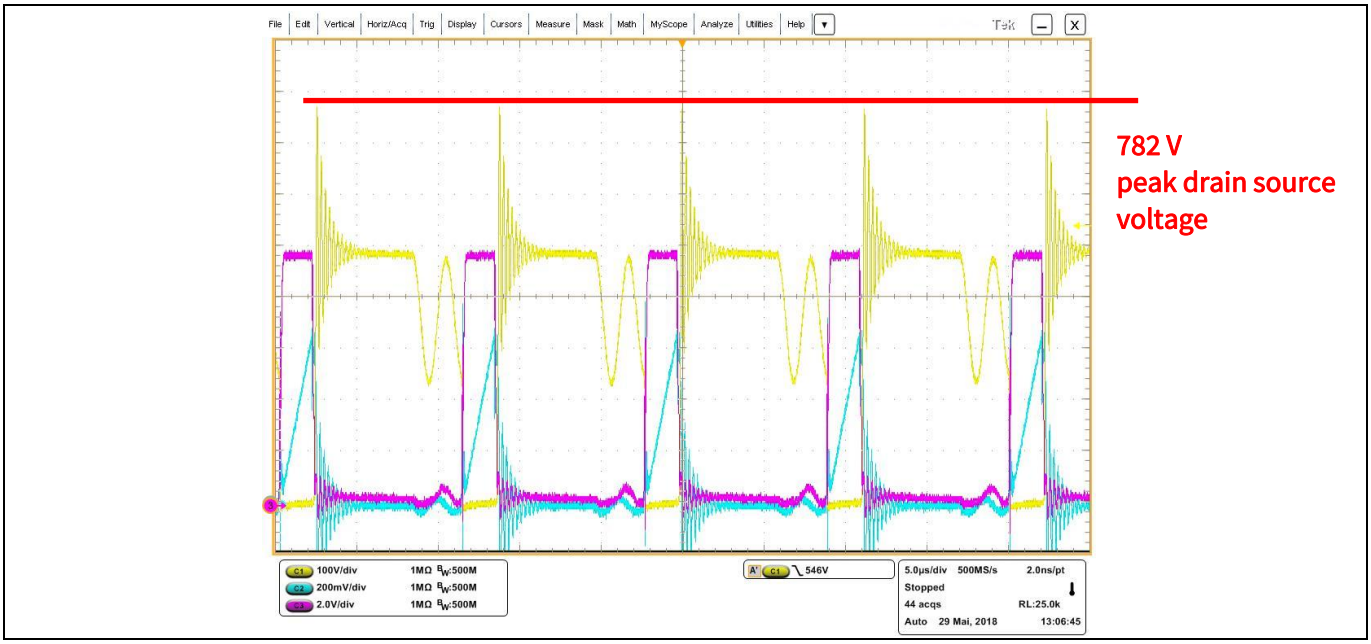

Figure 28 High-line (265 V AC), full load (40 W).

CH1 (yellow): Q1 V_{DS}
CH2 (cyan): Q1 I_{DS}
CH3 (magenta): Q1 V_{GS}

This shows the worst case drain source voltage of 782 V. This still gives 17.6 percent margin from the MOSFET breakdown voltage under worst-case conditions even with snubberless operation. This means the efficiency could be further improved by reducing the C_{DS} external on the MOSFET.

8 Conclusion

The P7 series of CoolMOS™ superjunction MOSFETs offer the best solution for flyback applications. The improvement in switching loss performance over the Infineon CoolMOS™ C3 and competitor devices in this particular design leads to an improvement in efficiency of 0.23 percent, which in turn leads to a reduction in MOSFET temperature of 5.1°C at the thermally critical point of 90 V AC input. The P7 also gives an increase in full-load efficiency of 0.35 percent at 230 V AC, which leads to an 8°C reduction in MOSFET temperature. This board also shows that it is possible to use the additional breakdown voltage of the 950 V CoolMOS™ P7 to eliminate the snubber network in order to save PCB space and cost, and still meet efficiency requirements. This new benchmark in 950 V MOSFETs enables higher efficiency, higher power density and additional breakdown voltage to give designers more flexibility.

9 References

[1] Design guide for QR flyback converter

[2] ICE2QS03G datasheet, Infineon Technologies AG

[3] 2N7002 datasheet, Infineon Technologies AG

[4] BAS21-03W datasheet, Infineon Technologies AG

[5] ICE2QS03G design guide [ANPS0027]

[6] Converter design using the quasi-resonant PWM controller ICE2QS03G, Infineon Technologies AG, 2006 [ANPS0003]

Revision history

Major changes since the last revision

Page or reference	Description of change

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Edition 2018-07-20

Published by

Infineon Technologies AG

81726 München, Germany

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Document reference

AN_1805_PL52_1806_130547

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