DS91D176

Multipoint-LVDS (M-LVDS) Transceiver

Evaluation Kit User Manual

April 2006
Rev 0.2

Overview

The purpose of this document is to familiarize you with the DS91D176 evaluation board, suggest the test setup procedures and instrumentation, and to guide you through some typical measurements that will demonstrate the performance of the device.

The primary function of the board is to assist a system designer in development and analysis of an M-LVDS clock distribution network in an ATCA backplane. The board also enables the user to examine performance and all functions of the DS91D176 as a standalone device. As a side feature, one can utilize the board to access switch fabric interface of an ATCA backplane.

The DS91D176 is a high-speed M-LVDS differential transceiver designed for multipoint applications with multiple drivers or receivers. The device conforms to TIA/EIA-899 standard. It utilizes M-LVDS technology for low power, high-speed and superior noise immunity.

Description

Figure 1 below represents the top layer drawing of the board with the silkscreen annotations. It is a 6 x 4 inch 10 layer printed circuit board (PCB) that features seven DS91D176 (U1-U7) devices.

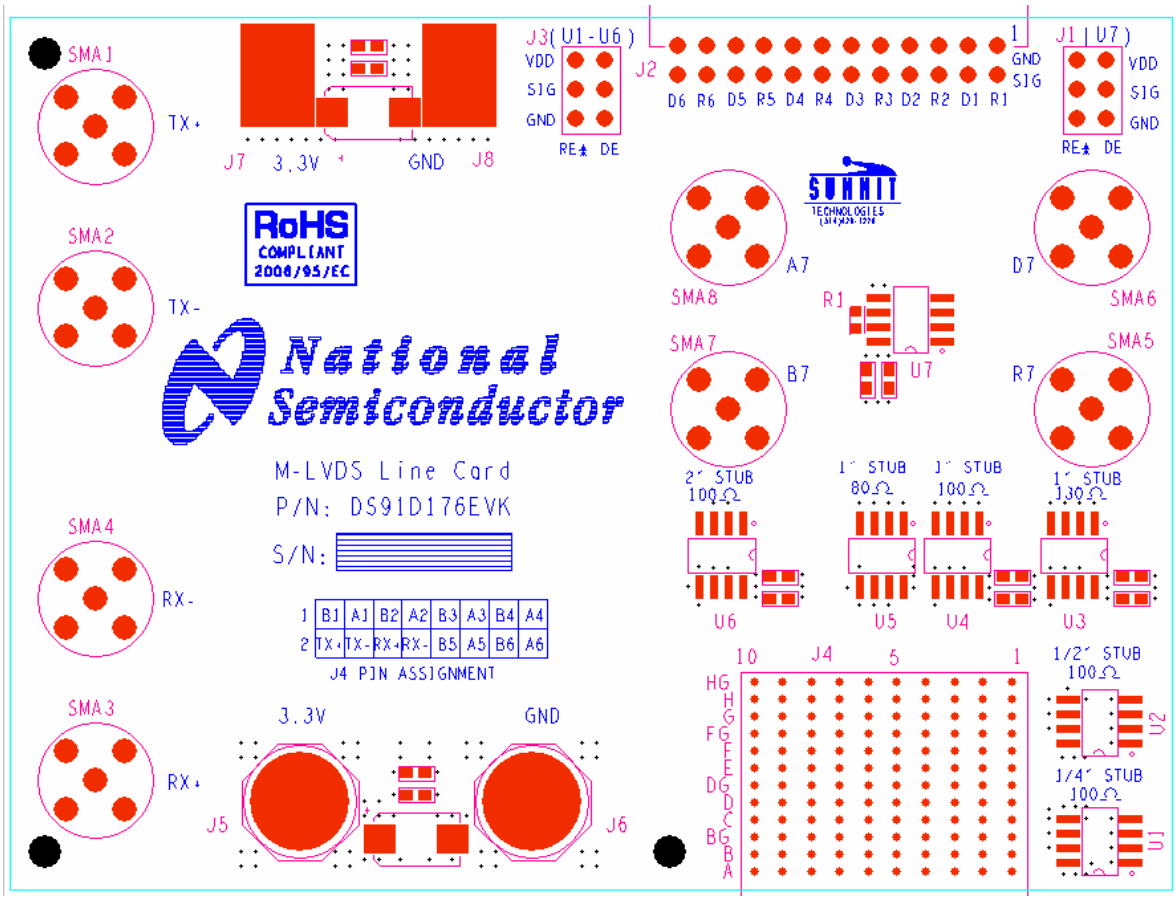


Figure 1: DS91D176 Evaluation Board - Top View

Devices U1 through U6 can serve as building blocks for M-LVDS clock distribution networks in ATCA backplanes. Their M-LVDS I/O pins directly connect to the first two row pins of J4, which is an ADF (Advanced Differential Fabric) connector. When J4 is inserted into any ATCA backplane slot (location J20/P20 for those of you familiar with ATCA backplanes), the M-LVDS I/O pins of each device electrically connect to one of the clock busses (there are six clock busses in an ATCA backplane – See Figure 3). The PCB traces that connect device M-LVDS pins with the J4 connector pins have different characteristics for each device. These traces are also

called stubs. Table 1 provides characteristic of each stub, M-LVDS pins to J4 pin mapping and LVCMOS pins to J2 pins mapping.

Device	M-LVDS Pins	J4 Pins	Stub Length	Z_{STUB}	LVCMOS Pins	J2 Pins
U1	A1 B1	B1 A1	0.25”	100 Ω	R1 D1	2 4
U2	A2 B2	D1 C1	0.50”	100 Ω	R1 D1	6 8
U3	A3 B3	F1 E1	1.00”	130 Ω	R1 D1	10 12
U4	A4 B4	H1 G1	1.00”	100 Ω	R1 D1	14 16
U5	A5 B5	D2 C2	1.00”	80 Ω	R1 D1	18 20
U6	A6 B6	B2 A2	2.00”	100 Ω	R1 D1	22 24

Table 1: U1-U6 Stub Characteristics and Pin Mapping

J1 configures U1 through U6 as either driver or receiver.

J7 and J8 are power and ground banana plug receptacles. J5 and J6 are redundant power and ground connections.

U7 is for a standalone evaluation. Its I/O pins (both, M-LVDS and LVCMOS) connect to SMA connectors (SMA5-SMA8) for easy interface with instrumentation. J3 configures U7 as either driver or receiver. There is a provision to terminate M-LVDS inputs of the U7 with a SM0603 sized resistor.

Connectors, SMA1, SMA2, SMA3 and SMA4 connect to J4 pins H2, G2, F2 and E2 respectively. If the board is plugged in an ATCA backplane, locations J21/P21, J22/P22, J23/P23 and J24/P24 in any slot, fabric interface is accessed with these connectors.

Figure 2 provides a simplified block diagram view of the signal paths between the connecters and IC’s.

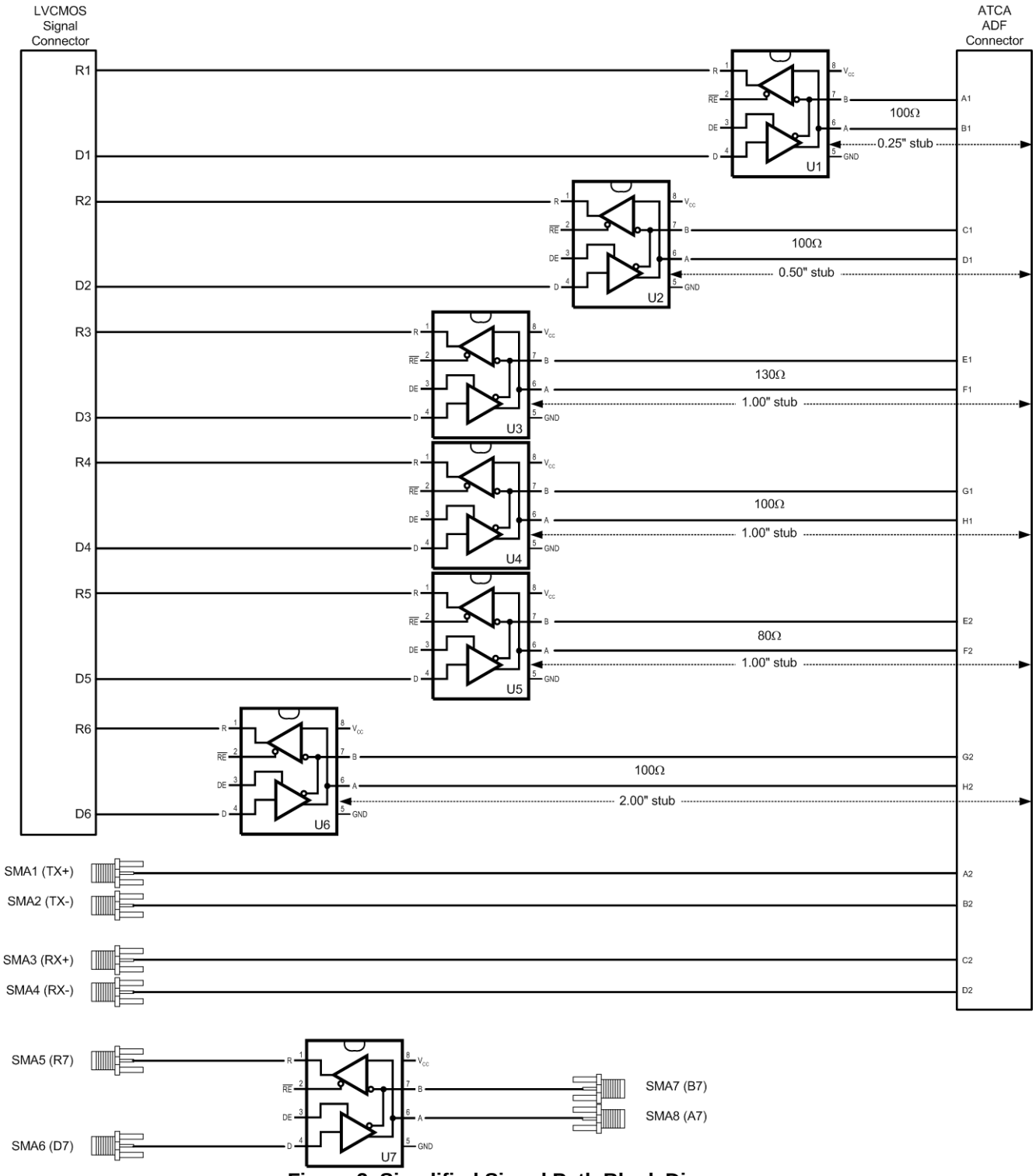


Figure 2. Simplified Signal Path Block Diagram

Building an Evaluation M-LVDS Clock Distribution Network in an ATCA Backplane

The following is a recommended procedure for building an evaluation M-LVDS clock distribution network with DS91D176 evaluation boards. The assumption is that the user already has an ATCA backplane. Figure 3 depicts configuration of a generic M-LVDS clock network in an ATCA backplane.

1. Use two or more DS91D176 evaluation boards and install them at backplane location J20/P20, in the desired slots.

2. Apply the power to the boards (3.3 V typical) between J7 and J8 banana plug receptacles, observe the value of $I_{CC,}$ and compare it with the expected value (refer to the datasheet) to ensure that the devices are functional.

3. Select the board you want to configure as a clock driver/distributor. This is accomplished by setting DE and RE* pins to VDD (J1). Connect a clock generator to one of the driver inputs (J2).

4. Configure the remaining boards as clock receivers. This is accomplished by setting DE and RE* pins to GND (J1).

5. Observe clock waveforms by either connecting receiver LVCMOS output pins (J1) directly to an oscilloscope or by probing receiver M-LVDS input pins with a differential probe.

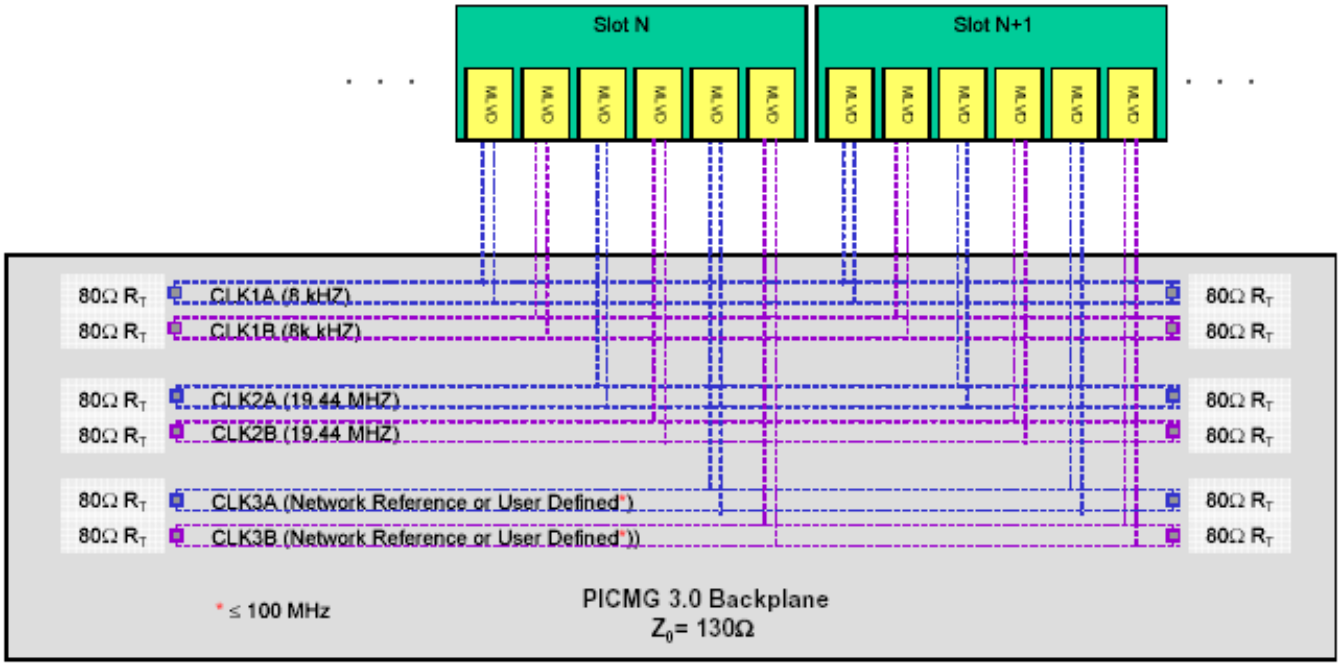


Figure 3. M-LVDS Clock Distribution Network in an ATCA Backplane

The above block diagram details the clock channels. They are all 130-ohm differential and doubly terminated with 80 ohms at either end of the backplane. The parallel combination of 80-ohm resistors means that the MLVDS devices will be driving a 40-ohm load termination. The maximum stub length from the backplane is defined in the ATCA standard as 1 inch or 2.5 cm.

Figure 4 shows a picture of a 14-slot ATCA backplane fully populated with DS91D176 evaluation boards.

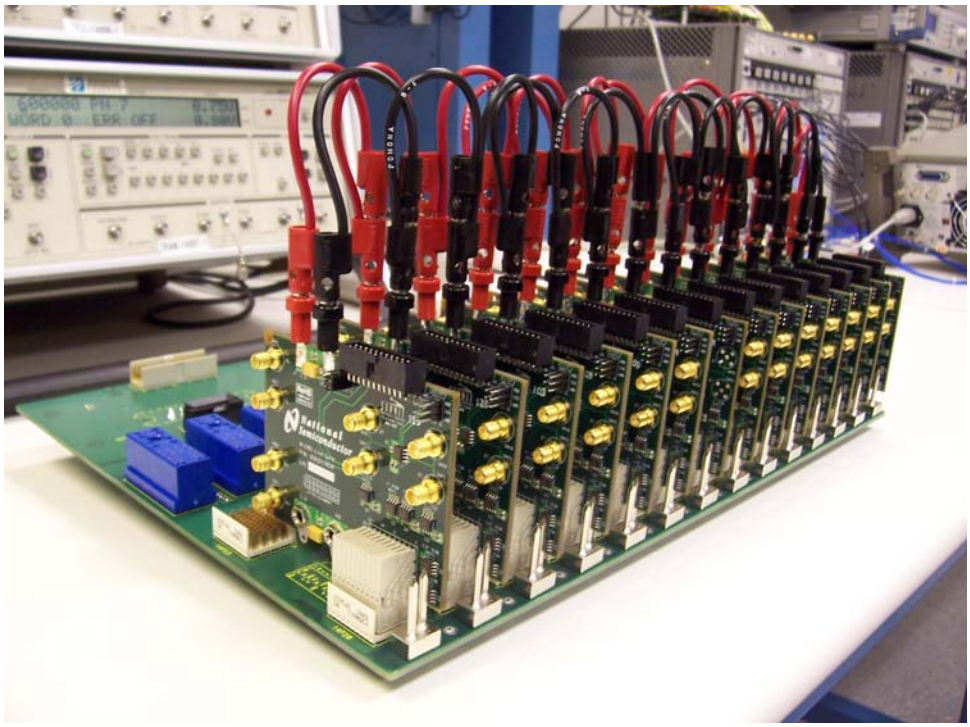


Figure 4. DS91D176 Evaluation Boards in an ATCA Backplane

Figure 5 shows 19.44 MHz clock waveforms obtained with a differential probe, Tektronix P6330, on the M-LVDS input pins of U1, U2, U4 and U6 devices of the receiver board in slot #8. The14-Slot backplane was fully populated. The clock driver/distributor board was in slot #7.

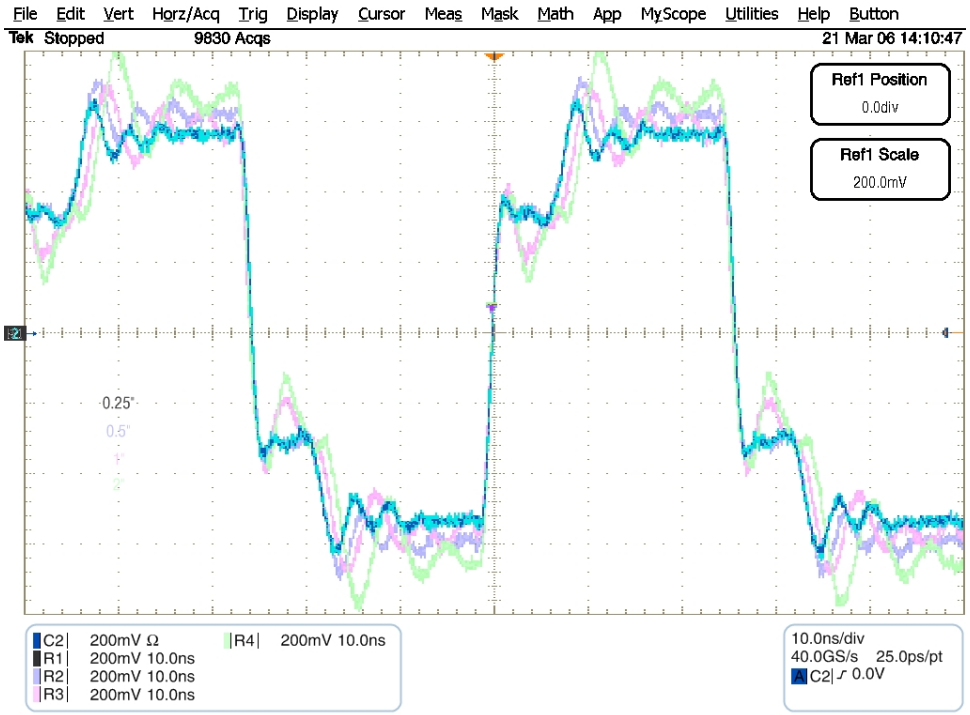


Figure 5. 19.44 MHz Clock Waveforms Show Stub Length Effects on Signal Integrity

Building an Evaluation Point-Point Link with DS91D176 Evaluation Boards

The following is a recommended procedure for building an evaluation M-LVDS point-point network with DS91D176 evaluation boards. Figure 6 depicts a typical setup and instrumentation used for evaluation of a point-to-point link.

1. Use two DS91D176 evaluation boards

2. Apply the power to the boards (3.3 V typical) between J7 and J8 banana plug receptacles, observe the value of $I_{CC,}$ and compare it with the expected value (refer to the datasheet) to ensure that the devices are functional.

3. Configure U7 on one board as a driver. This is accomplished by setting DE and RE* pins to VDD (J3). Connect a signal generator to the driver inputs (SMA6).

4. Configure U7 on the other board as a receiver. This is accomplished by setting DE and RE* pins to GND (J3).

5. Select a differential interconnect with balanced 100-ohm differential impedance (i.e. UTP cable) and connect the M-LVDS pins of both devices with it.

6. Terminate the interconnect with a matching resistor on the inputs of U7 on the receiver board (R1).

7. Observe waveforms by either connecting the receiver LVCMOS output pins (SMA5) directly to an oscilloscope or by probing receiver M-LVDS input pins with a differential probe.

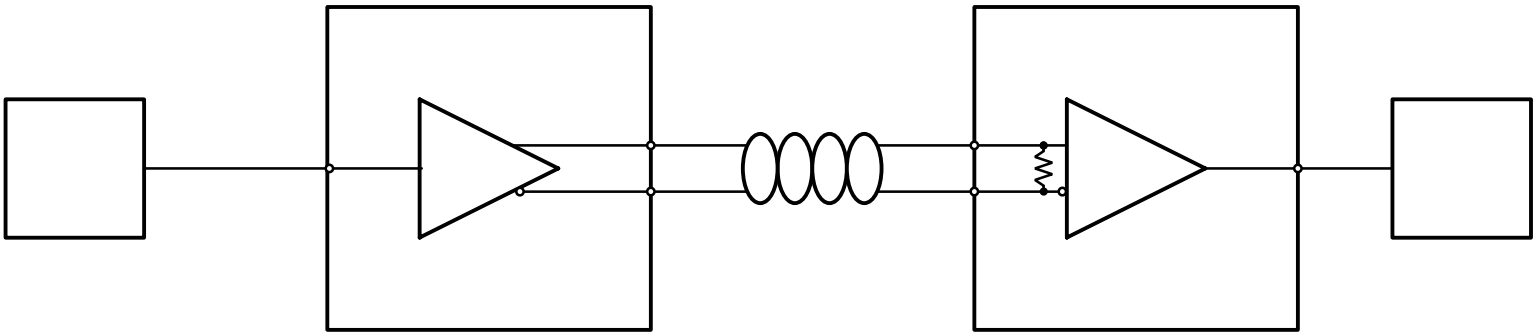


Figure 6. M-LVDS Point to Point Link with DS91D176 Boards and UTP Cable

Figure 7 shows eye diagrams acquired at the output of the DS91D176 driver loaded with a 100-ohm resistor and after 50 m Cat5e cable terminated with a 100-ohm resistor. The generator connected to the driver input simulated a 100 Mb/s PRBS-7 NRZ.

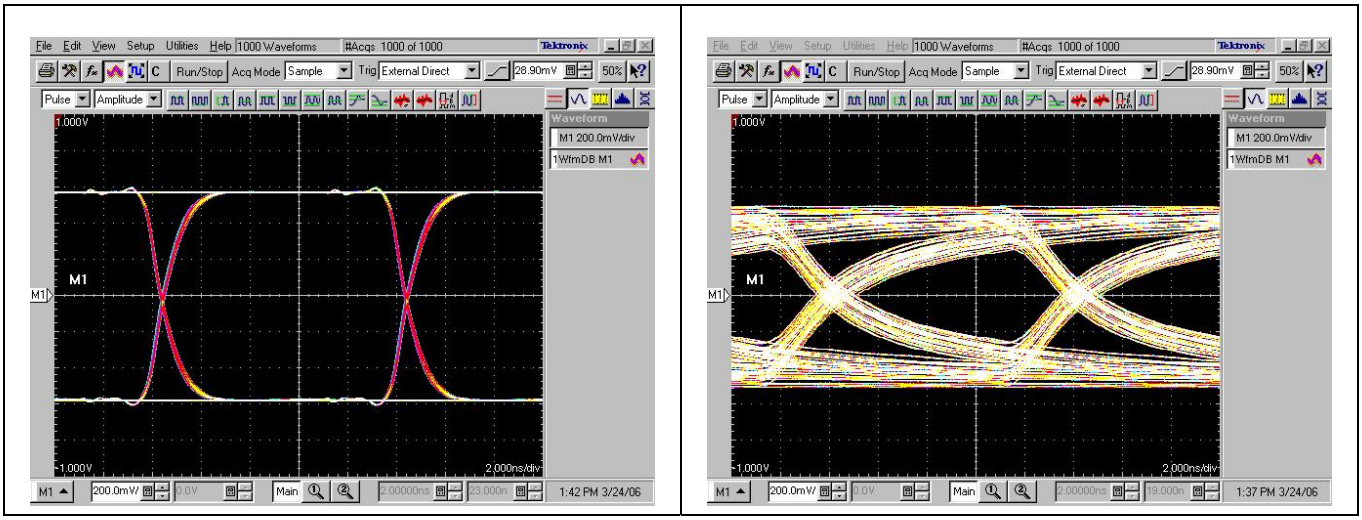


Figure 7: Eye Diagram Before and After 50 m of Cat5e

Microstrip and Stripline Geometries Used

Figures 8 to 12 show trace geometries used in the board design. Table 2 provides trace type to electrical net cross-reference.

Trace Type / Figure	DS91D176 Evaluation Board Nets
50-ohm Single-ended Microstrip / Figure 8	All LVCMOS nets
100-ohm Differential Microstrip / Figure 9	U7 M-LVDS nets, SMA1-SMA4 nets
100-ohm Differential Stripline / Figure 10	U1, U2, U4, U6 M-LVDS nets
130-ohm Differential Stripline / Figure 11	U3 M-LVDS nets
80-ohm Differential Stripline / Figure 12	U5 M-LVDS nets

Table 2: Trace Type to Electrical Net Cross-reference.

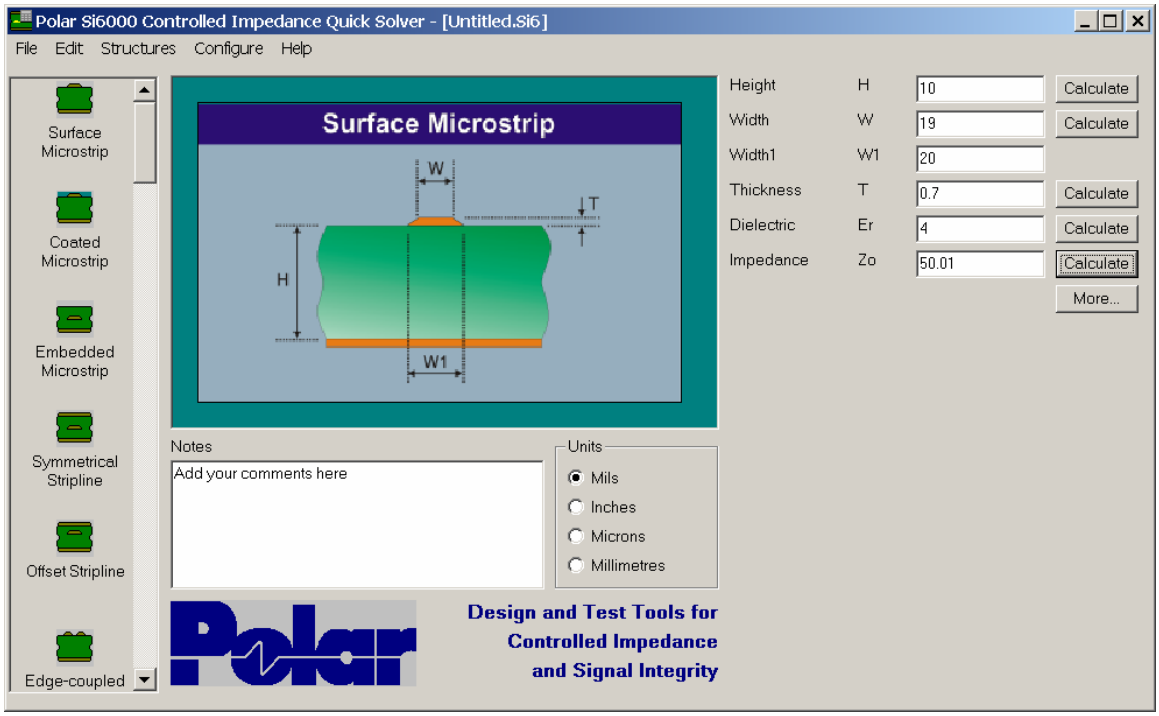


Figure 8. 50-ohm Single-ended Microstrip

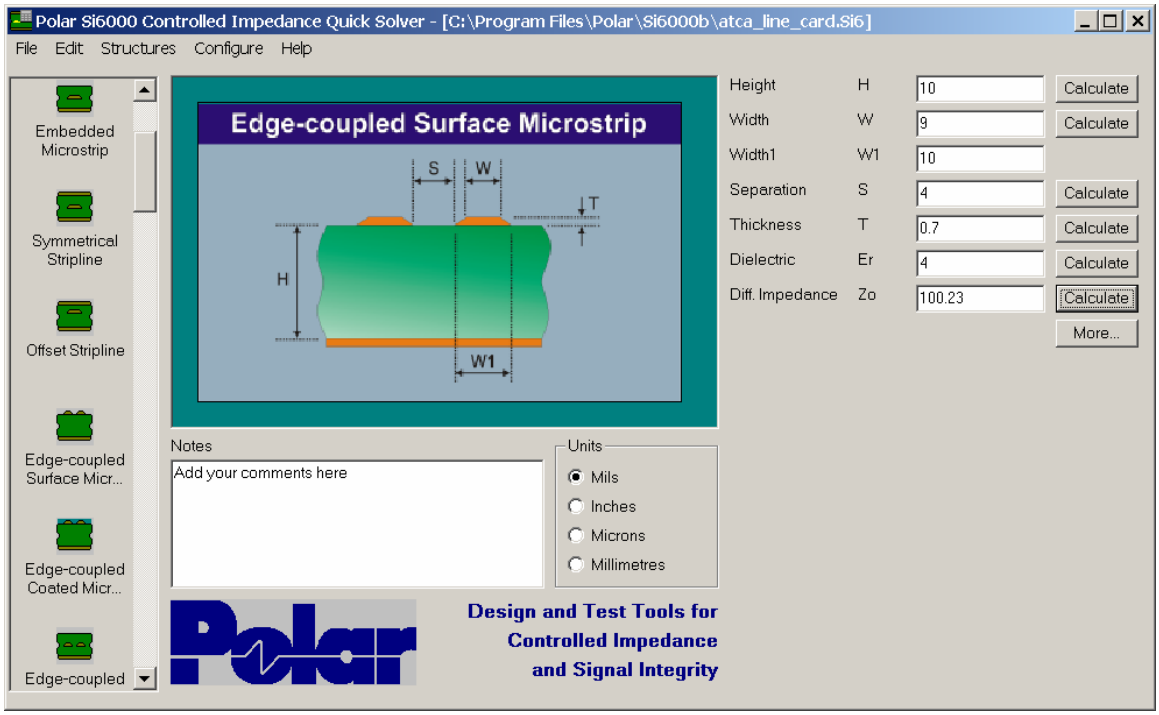


Figure 9. 100-ohm Differential Microstrip

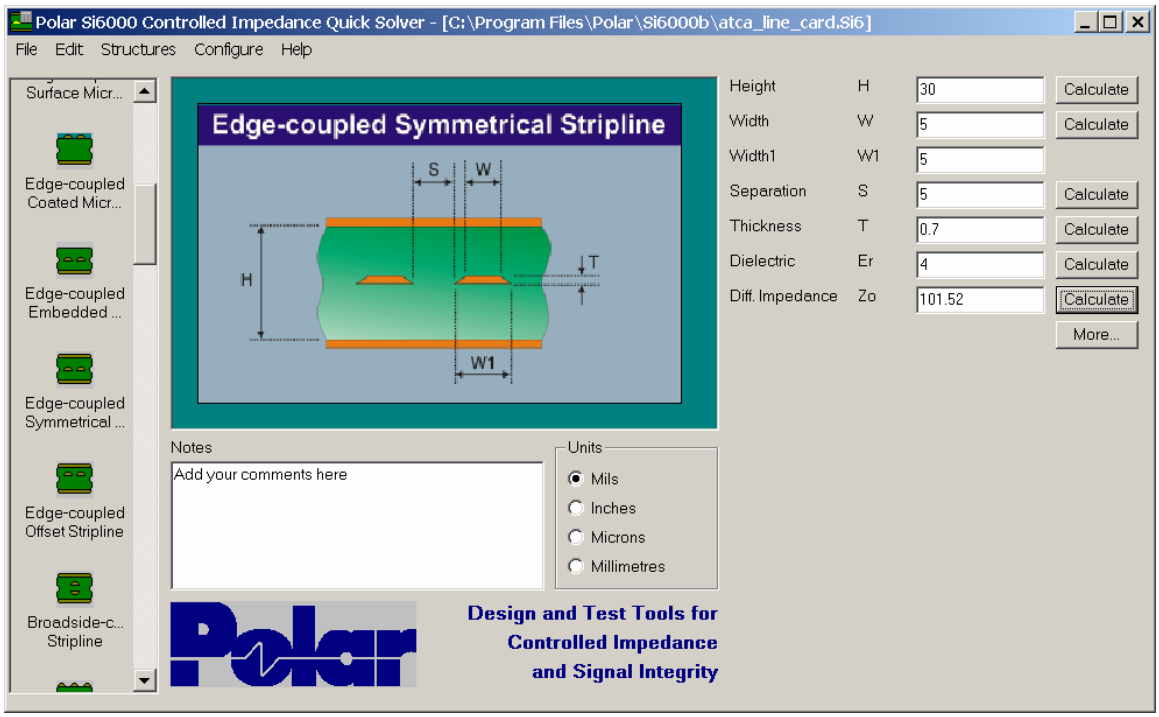


Figure 10. 100-ohm Differential Stripline

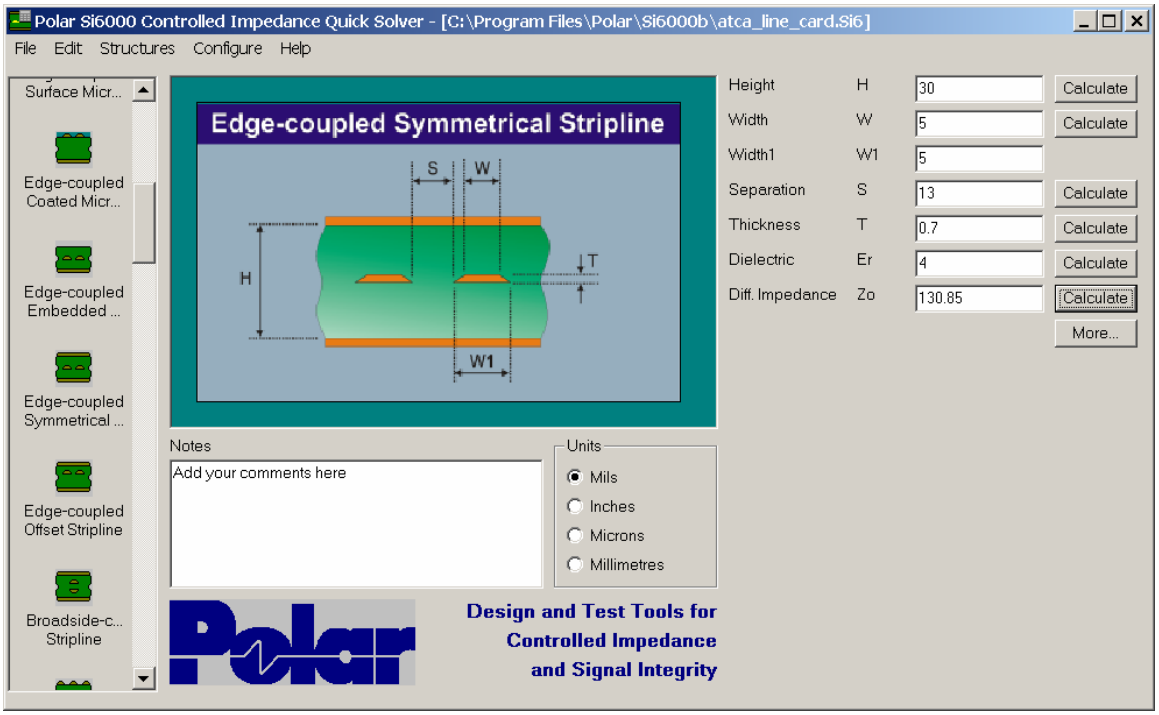


Figure 11. 130-ohm Differential Stripline

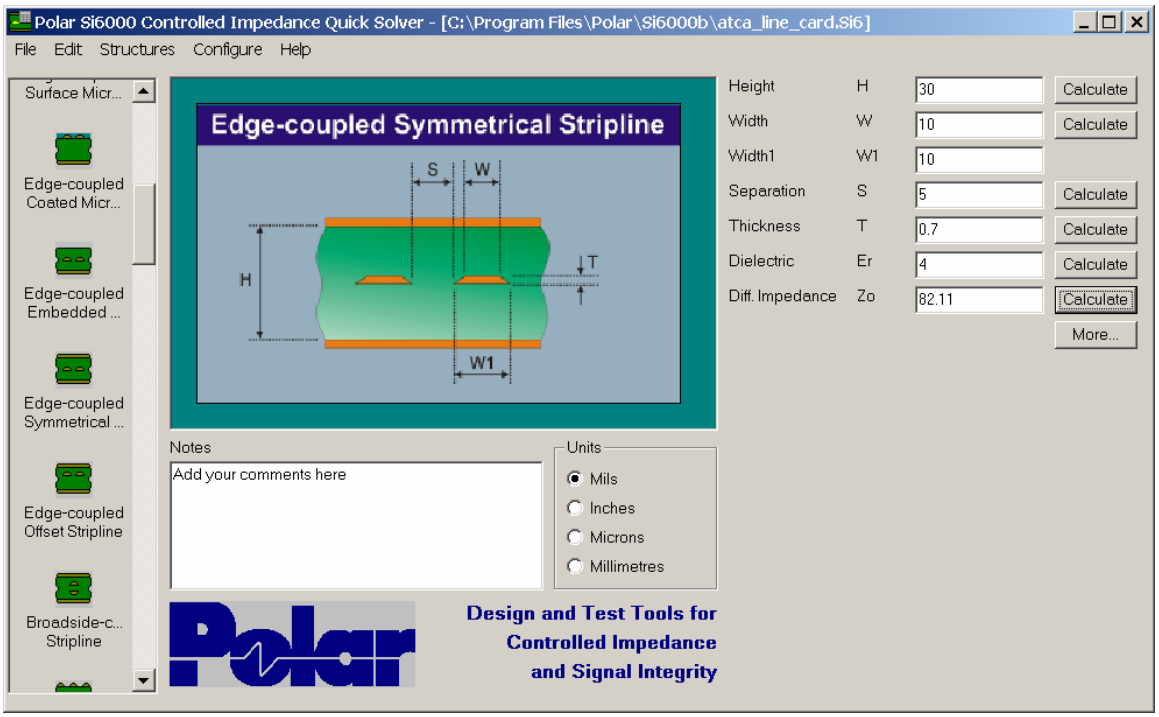


Figure 12. 80-ohm Differential Stripline

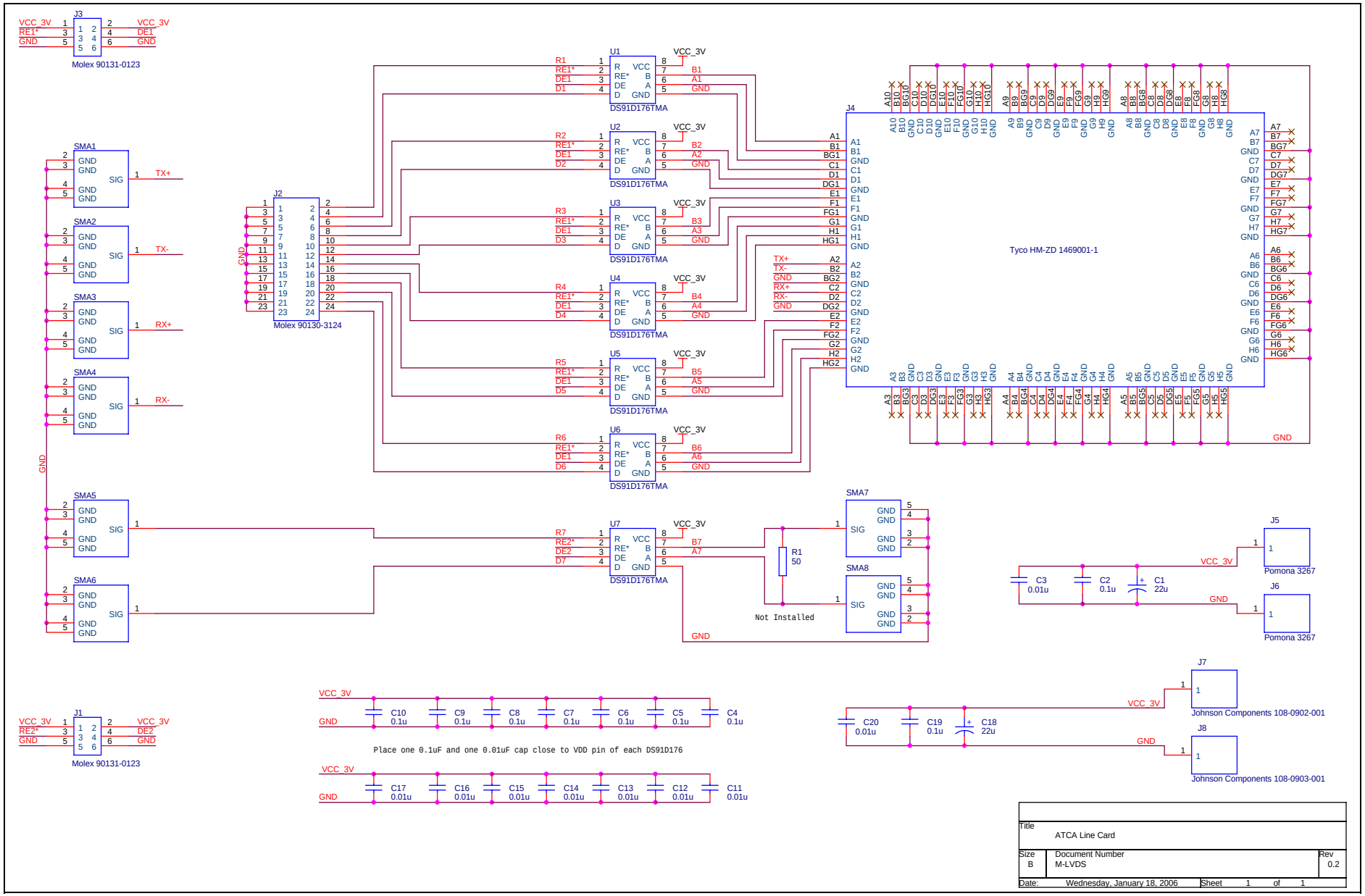
Layer Stack Up:

1/2 oz. ---------- SIG1
10 mills
1/2 oz. ----------GND
15 mills
1/2 oz. ---------- SIG2
15 mills
1/2 oz. ----------GND
3 mills
1/2 oz. ----------PWR
3 mills
1/2 oz. ---------- PWR
3 mills
1/2 oz. ----------GND
15 mills
1/2 oz. ---------- SIG3
15 mills
1/2 oz. ---------- GND
10 mills
1/2 oz. ---------- SIG4

Bill Of Materials

Item	Quantity	Reference	Part
1	2	C18, C1	22u; SM7343; C1 Not Installed;
2	9	C2, C4, C5, C6, C7, C8, C9, C10, C19	0.1u; SM0603; C2 Not Installed;
3	9	C3, C11, C12, C13, C14, C15, C16, C17, C20	0.01u; SM0603; C3 Not Installed;
4	2	J3, J1	Molex 90131-0123
5	1	J2	Molex 90130-3124
6	1	J4	Tyco HM-ZD 1469001-1
7	2	J5, J6	Pomona 3267; Not Installed;
8	1	J7	Johnson Components 108-0902-001
9	1	J8	Johnson Components 108-0903-001
10	4	SMA1, SMA2, SMA3, SMA4,	Not Installed;
11	4	SMA5, SMA6, SMA7, SMA8	Johnson Components 142-0701-231
11	7	U1, U2, U3, U4, U5, U6, U7	DS91D176TMA
12	1	R1	50; SM0603; Not Installed;

Schematic


J3
Molex 90131-0123
J2
Molex 90130-3124
J1
Molex 90131-0123
U1
U2
U3
U4
U5
U6
U7
DS91D176TMA
J4
Tyco HM-ZD 1469001-1
SMA1
SMA2
SMA3
SMA4
SMA5
SMA6
SMA7
SMA8
R1
50
Not Installed
J5
J6
J7
J8
Pomona 3267
Johnson Components 108-0902-001
Johnson Components 108-0903-001
Place one 0.1uF and one 0.01uF cap close to VDD pin of each DS91D176
ATCA Line Card
M-LVDS
Wednesday, January 18, 2006

Revision History

Revision 0.1: Initial draft – dglisic 12Apr2006
Revision 0.2: Minor edits, added simplified block diagram – bstearns 14 April2006

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