



IGLOO® and ProASIC®3 FPGAs
The Industry's Lowest Power FPGAs



Microchip's IGLOO® and ProASIC®3 Flash-based FPGAs offer the lowest power, highest-reliability and are live at power up, setting them apart from traditional SRAM based FPGAs.

Low-density IGLOO and ProASIC3 families also deliver more capabilities, making them an ideal solution for applications constrained by power, space and cost. These FPGAs are perfect for bridging, I/O expansion, level shifting, glue logic and memory interfacing in consumer and portable medical device markets, industrial controls, as well as military and commercial aircraft. Only Microchip FPGAs deliver the power, size and reliability benefits that reduce time-to-market and enable long-term profitability.

IGLOO® Family	IGLOO/e	IGLOO nano	IGLOO PLUS
Arm® - Enabled	M1 IGLOO/e		
Overview	The low-power programmable solution	The industry's lowest-power, smallest-size solution	The low-power FPGA with more I/O per LE compared to IGLOO
Equivalent LEs	330-35K	100-3K	330-1K
Max User I/Os	341	71	212
Power Consumption	5 µW	2 µW	5 µW

ProASIC®3 Series	ProASIC3/e	ProASIC3 nano	ProASIC3L
Arm® Enabled	M1 ProASIC3/E		M1 ProASIC3L
Overview	The low-power, low-cost FPGA solution	Lowest cost solution with enhanced I/O capabilities	The FPGA that balances low power, performance, and low cost
Equivalent LEs	330-35K	100-3K	3K-35K
Max User I/Os	620	71	620
Power Consumption	3 mW	0.9 mW	0.49 mW

Advantages of Flash FPGAs

Low Power Across the Board

The Flash*Freeze technology used in IGLOO and ProASIC3 FPGA family enables entering and exiting an ultra-low power mode while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

Unparalleled Security

Flash-based low-density FPGA families do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. The family incorporates FlashLock, which provides a unique combination of re-programmability and design security without external overhead. A built-in 128-bit AES decryption engine secures in-system programming.

Superior Reliability

An Single Event Upset (SEU) where alpha and neutron radiation causes loss of configuration data is also called a firm error. SEUs at ground level are now becoming a major concern for life critical and safety critical applications such as aviation, industrial automation, medical devices and automotive electronics.

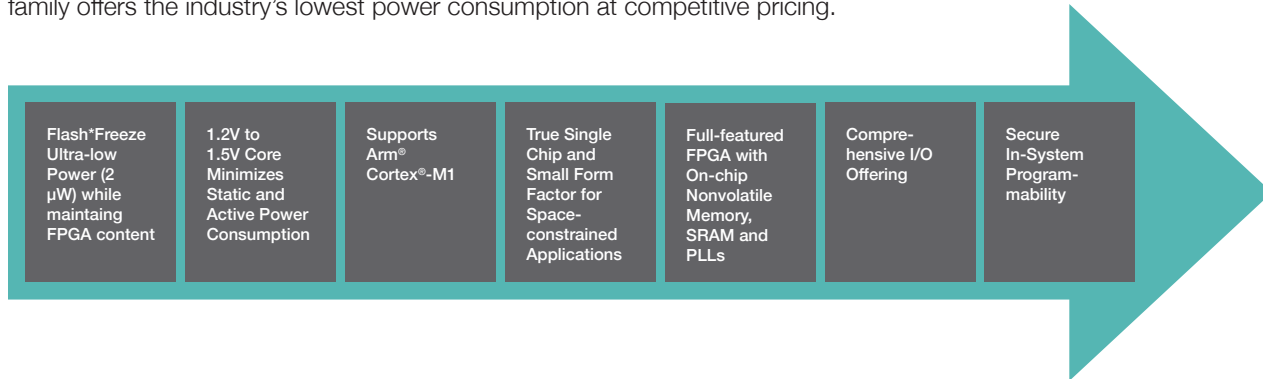
Flash-based IGLOO and ProASIC3 families are not susceptible to SEUs caused by high-energy ionizing particles. No mitigation techniques for configuration upsets are required. They maintain system integrity at even high altitudes and sea Level.

Instant-On

A system is composed of multiple components with inter-dependencies, and the designer's task is to make sure these components all work together. It is vital to choose instant-on devices in the system's critical path in order to achieve efficient system operation. Microchip's low density IGLOO and ProASIC 3 FPGA families are on in a few micro seconds.

IGLOO Flash FPGAs

The IGLOO families, which include IGLOO/e, IGLOO nano and IGLOO PLUS devices, are reprogrammable, full-featured Flash FPGAs designed to meet the demanding power and area requirements of today's portable and power-conscious electronics. The family offers the industry's lowest power consumption at competitive pricing.



IGLOO/e

The IGLOO/e family offers a broad portfolio with small footprint packages, re-programmability, and an abundance of advanced features.

- Available in logic densities from 330 LEs to 35K LEs
- 1 Kbit of on-chip, programmable, nonvolatile FlashROM storage
- 1.2V to 1.5V operation
- Clock conditioning circuitry based on up to 6 integrated Phase-Locked Loops (PLLs)

- Up to 504 Kbits of true dual-port SRAM
- Up to 341 user I/Os
- Best design security

M1 IGLOO/e devices support the high-performance, 32-bit Arm Cortex[®]-M1 processor developed by Arm for implementation in FPGAs. Cortex-M1 is available for free from Microchip for use in M1 IGLOO/e FPGAs.

IGLOO [®] Devices	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
Cortex [®] -M1 Devices				M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,00	3,000,000
Equivalent LEs	330	700	1.5 K	3K	5K	7K	11K	7K	35K
Quiescent Current (typical) in Flash*Freeze Mode (μ W)	5	10	16	24	32	36	53	49	137
RAM kbits (1,024 bits)		18	36	36	54	108	144	108	504
4,608-bit Blocks		4	8	8	12	24	32	24	112
FlashROM Bits	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1024	1024
Secure (AES) ISP1		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLLs in CCCs		1	1	1	1	1	1	6	6
I/O Banks	2	2	2	4	4	4	4	8	8
Maximum User I/Os	77	71	133	143	178	215	300	165	341
Speed Grades	Std.	Std.	Std.	Std.	Std.	Std.	Std.	Std.	Std.
Temperature Grades	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I	C, I

IGLOO [®] Devices	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
Cortex [®] -M1 Devices				M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
QN48	34								
UC81	66								
CS81	66								
CS121			96						
VQ100	77	71	71	68/13					
CS196			133	143/353	143/35				
FG144			97	97/24		97/25	97/25		
FG256					178/38	177/43	177/44	165/79	
CS281						215/53	215/53		
FG484							300/74		341/168

IGLOO PLUS

IGLOO PLUS devices are optimized to meet the needs of I/O-intensive, power-conscious applications that require exceptional features. Offering more I/Os per LEs than the IGLOO family and supporting independent Schmitt trigger inputs, hot-swapping and Flash*Freeze bus hold. Available in logic densities from 330 LEs to 1.5K LEs

- 1 Kbit of on-chip, programmable, nonvolatile FlashROM storage
- 1.2V to 1.5V operation
- Clock conditioning circuitry based on integrated Phase-Locked Loops (PLLs)
- Up to 36 Kbits of true dual-port SRAM
- Up to 212 user I/Os
- Best design security

IGLOO® PLUS Devices	AGLP030	AGLP060	AGLP125
System Gates	30,000	60,000	125,000
Equivalent LEs	330	700	1.5 K
Quiescent Current (typical) in Flash*Freeze Mode (µW)	5	10	16
RAM kbits (1,024 bits)		18	36
4,608-bit Blocks		4	8
FlashROM Bits	1,024	1,024	1,024
Secure (AES) ISP		Yes	Yes
Integrated PLLs in CCCs		1	1
I/O Banks	4	4	4
Maximum User I/Os	120	157	212
Speed Grades	Std.	Std.	Std.
Temperature Grades	C, I	C, I	C, I

IGLOO® PLUS Devices	AGLP030	AGLP060	AGLP125
CS201 (8 × 8 mm)	120	157	
CS281 (10 × 10 mm)			212
CS289 (14 × 14 mm)	120	157	212
VQ128 (14 × 14 mm)	101		
VQ176 (20 × 20 mm)		137	

IGLOO Nano

IGLOO nano low-power FPGAs offer groundbreaking possibilities in power, size and operating temperature. The 1.2V to 1.5V IGLOO nano devices have been designed for high-volume applications where power and size are key decision criteria. IGLOO nano low power FPGAs offer the largest selection of small footprint packages with the smallest 3x3 mm micro-chip scale package. Available in logic densities from 100 LEs to 3K LEs

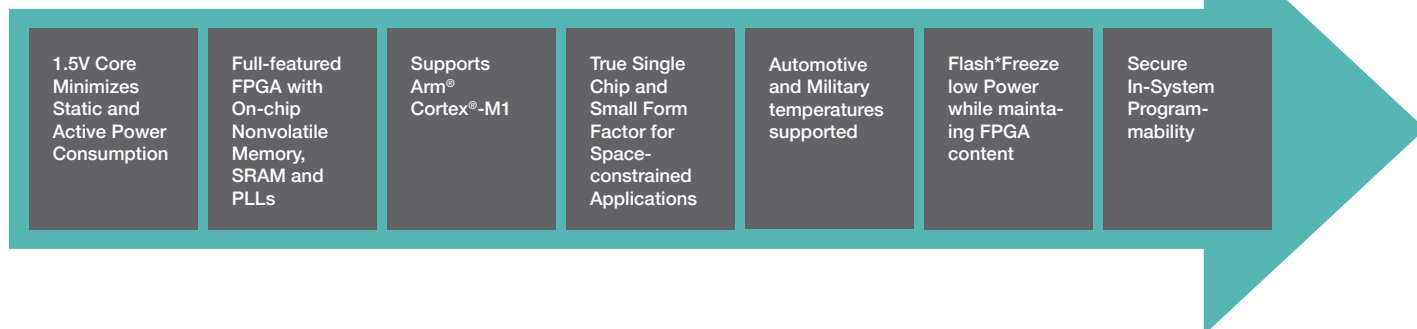
- 1 Kbit of on-chip, programmable, nonvolatile FlashROM storage
- 1.2V to 1.5V operation
- Clock conditioning circuitry based on integrated phase-locked loops (PLLs)
- Up to 36 Kbits of true dual-port SRAM
- Up to 71 user I/Os
- Best design security

IGLOO® nano Devices	AGLN010	AGLN020	AGLN060	AGLN125	AGLN250
System Gates	10,000	20,000	60,000	125,000	250,000
Equivalent LEs	100	200	700	1.5 K	3K
Flash*Freeze Mode (typical, μ W)	2	4	10	16	24
RAM kbits (1,024 bits)			18	36	36
4,608-bit Blocks			4	8	8
FlashROM Bits	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP			Yes	Yes	Yes
Integrated PLLs in CCCs			1	1	1
I/O Banks	2	3	2	2	4
Maximum User I/Os	34	52	71	71	68
Speed Grades	Std.	Std.	Std.	Std.	Std.
Temperature Grades	C, I	C, I	C, I	C, I	C, I
Single-Ended I/Os					
UC36 (3 x 3 mm)	23				
QN48 (6 x 6 mm)	34				
QN68 (8 x 8 mm)		49			
CS81 (5 x 5 mm)		52	60	60	60
VQ100 (14 x 14 mm)			71	71	68

Click the below link for more details on IGLOO family: www.microsemi.com/product-directory/fpgas/1689-igloo#overview

ProASIC3 Flash FPGAs

The ProASIC3 series of FPGAs, which includes ProASIC3/e, ProASIC3 nano, and ProASIC3L, offers breakthrough performance, density, and features in demanding applications. The family temperature range spans industrial and commercial, while also offering automotive qualified and military temperature devices to support diversified applications.



ProASIC3/e

The ProASIC3/e FPGAs support portable, consumer, industrial, communications and medical applications with commercial and industrial temperature devices.

The family also offers AEC-Q100 qualified FPGAs for automotive segment supporting the -40C to 135C temperature range. ProASIC3 nonvolatile flash technology gives automotive system designers the advantage of a secure, low-power, single-chip solution that is Instant-On. Their SEU immune non-volatile Flash technology is ideally suited for demanding applications in powertrain, safety and telematics-based subsystems, where firm-error failure is not an option.

The military ProASIC3 family of Flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50%. These power savings are coupled with performance, density, true single chip, 1.2V to 1.5V core and I/O operation, re-programmability, and advanced features.

- Available in logic densities from 330 LEs to 35K LEs
- 1 kbit of on-chip, programmable, nonvolatile FlashROM storage
- 1.5V operation
- Clock conditioning circuitry based on up to 6 integrated PLLs
- Up to 504 kbits of true dual-port SRAM
- Up to 620 user I/Os
- Best design security

ProASIC ³ Devices	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Cortex [®] -M1 Devices				M1A3P250	M1A3P400	M1A3P600	M1A3P1000
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000
Equivalent LEs	330	700	1.5 K	3K	5K	7K	11K
RAM kbits (1,024 bits)		18	36	36	54	108	144
4,608-bit Blocks		4	8	8	12	24	32
FlashROM Bits	1,024	1,024	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP1		Yes	Yes	Yes	Yes	Yes	Yes
PLLs		1	1	1	1	1	1
I/O Banks	2	2	2	4	4	4	4
Maximum User I/Os	77	96	133	157	178	235	300
Speed Grades	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2
Temperature Grades	C, I	C, I, T	C, I, T	C, I, T, M	C, I	C, I	C, I, T, M
Single-Ended I/Os / Differential I/O Pairs							
QN48	34						
QN68	49						
VQ100	77	71	71	68/13			
TQ144		91	100				
PQ208			133	151/34	151/34	154/35	154/35
FG144		96	97	97/24	97/25	97/25	97/25
FG256				157/382	178/38	177/43	177/44
FG484						235/60	300/74

ProASIC3E and ProASIC3 nano

ProASIC3E

ProASIC [®] 3E Devices	A3PE600	A3PE1500	A3PE3000
Cortex [®] -M1 Devices		M1A3PE1500	M1A3PE3000
System Gates	600,000	1,500,000	3,000,000
Equivalent LEs	7K	16K	35K
RAM kbits (1,024 bits)	108	270	504
4,608-bit Blocks	24	60	112
FlashROM Bits	1,024	1,024	1,024
Secure (AES) ISP	Yes	Yes	Yes
Integrated PLL in CCCs	6	6	6
I/O Banks	8	8	8
Maximum User I/Os	270	444	620
Speed Grades	Std., -1, -2	Std., -1, -2	Std., -1, -2
Temperature Grades	C, I	C, I	C, I
Single-Ended I/O Differential I/O Pairs			
PQ208		147/65	147/65
FG256	165/79		
FG324			221/110
FG484	270/135	280/139	341/168
FG676		444/222	
FG896			620/310

ProASIC3 nano

The ProASIC3 nano family increases the breadth of the ProASIC3 product line by offering smaller densities and packages with enhanced features of the ProASIC3 family. ProASIC3 nano devices offer the advantage of being a secure, low-power, single-chip solution that is Instant On.

- Available in logic densities from 100 LEs to 3K LEs
- 1 Kbit of on-chip, programmable, nonvolatile FlashROM storage
- 1.5V operation
- Clock conditioning circuitry based on integrated phase-locked loops (PLLs)
- Up to 36 Kbits of true dual-port SRAM
- Up to 71 user I/Os
- Best design security

ProASIC [®] 3 nano Devices	A3PN010	A3PN020	A3PN060	A3PN125	A3PN250
System Gates	10,000	20,000	60,000	125,000	250,000
Equivalent LEs	100	200	700	1.5 K	3K
RAM kbits (1,024 bits)			18	36	36
4,608-bit Blocks			4	8	8
FlashROM Bits	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP			Yes	Yes	Yes
Integrated PLLs in CCCs			1	1	1
I/O Banks	2	3	2	2	4
Maximum User I/Os	34	49	71	71	68
Speed Grades	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2
Temperature Grades	C, I	C, I	C, I	C, I	C, I
Single-Ended I/O					
QN48 (6 × 6 mm)	34				
QN68 (8 × 8 mm)		49			
VQ100 (14x14 mm)			71	71	68

ProASIC3L

ProASIC3L low-power FPGAs feature lower dynamic and static power than ProASIC3 FPGAs. The ProASIC3L family also supports the implementation of an FPGA-optimized 32-bit Arm Cortex-M1 Processor, allowing system designers to select the Flash FPGA solution that best meets their speed and power design requirements.

The ProASIC3L family of Microchip Flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50% compared to the equivalent ProASIC3 device. These power savings are coupled with performance, density, true single-chip, I/O operation as low as 1.2V, re-programmability and advanced features. Using Flash*Freeze technology enables users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies while retaining internal states of the device.

- Available in logic densities from 7K LEs to 35K LEs
- 1 Kbit of on-chip, programmable, nonvolatile FlashROM storage
- 1.2V–1.5V operation
- Clock conditioning circuitry based on up to 6 integrated PLLs
- Up to 504 Kbits of true dual-port SRAM
- Up to 620 user I/Os
- Best design security

ProASIC®3L Devices	A3P600L	A3P1000L	A3PE600L	A3PE3000L
Cortex®-M1 Devices	M1A3P600L	M1A3P1000L		M1A3PE3000L
System Gates	600,000	1,000,000	600,000	3,000,000
Equivalent LEs	7K	11K	7K	35K
RAM kbits (1,024 bits)	108	144	108	504
4,608-Bit Blocks	24	32	24	112
FlashROM Bits	1,024	1,024	1,024	1,024
Secure (AES) ISP	Yes	Yes	Yes	Yes
Integrated PLLs in CCCs	1	1	6	6
I/O Banks	4	4	8	8
Maximum User I/Os	235	177	270	620
Typical Static / Flash*Freeze Power (mW) at Vcc = 1.2V	0.66	1.06	TBA	3.3
Speed Grades	Std., -1	Std., -1	Std., -1	Std., -1
Temperature Grades	C, I	C, I	M	C, I, M
Single-Ended I/Os/Differential I/O Pairs				
PQ208				147/65
FG144	97/25	97/25		
FG256		177/44		
FG324				221/110
FG484	235/60		270/135	341/168
FG896				620/310

For more details on ProASIC3 family, visit www.microsemi.com/product-directory/fpgas/1690-proasic3#overview

Libero® SoC Design Software

Microchip's Libero SoC design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools that are used for designing with Microchip's power-efficient flash-based IGLOO and ProASIC3 devices. The suite integrates industry-standard Synopsys Synplify Pro synthesis and Mentor Graphics ModelSim simulation with best-in-class constraints management, debug capabilities, timing analysis, power analysis, secure production programming and push button design flow.

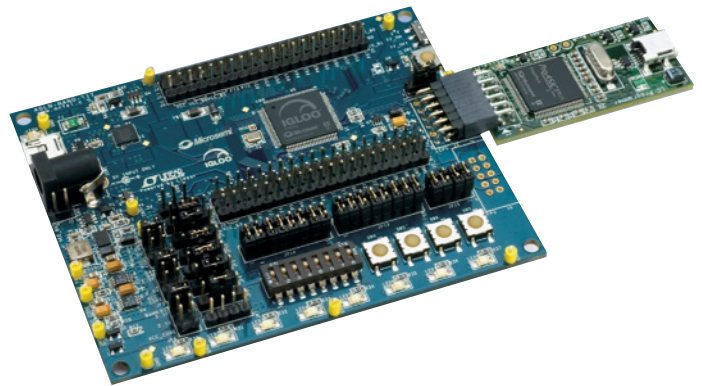
This comprehensive suite features an intuitive design flow with GUI wizards to guide the design process. Its easy-to-adopt single-click synthesis to programming flow integrates industry-standard third-party tools, a rich IP library of DirectCores and Companion-Cores, and supports complete reference designs and development kits.

For more details on Libero design suite visit, www.microsemi.com/product-directory/fpga-soc/1637-design-resources

IGLOO nano Kit

Microchip's IGLOO nano Starter Kit provides a simple board with Microchip's IGLOO nano AGLN250 device in the VQG100 package, Libero System on Chip (SoC), and a Low-Cost Programming Stick (LCPS) for in-system programming. The IGLOO nano Starter Kit is fully RoHS-compliant and enables you to quickly evaluate Microchip's IGLOO family and prototype your design. The following key functions are supported:

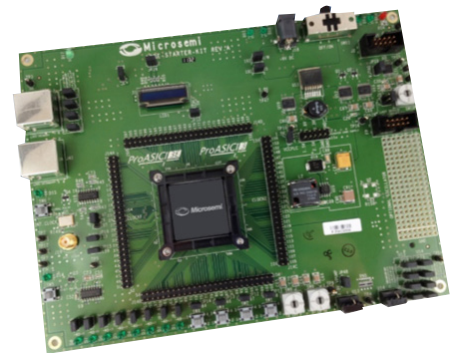
- Detailed current monitoring capabilities of the industry's lowest power FPGAs
- Development with Microchip's Flash*Freeze technology
- Easy experimentation with ISP, device serialization and FlashLock on-chip system security
- USB-to-UART interface for HyperTerminal on PC connected to board
- On-board voltage regulation, enabling independent I/O bank voltages



ProASIC3 Starter Kit

Microchip's ProASIC3 Starter Kit is a complete kit that includes a ProASIC3 starter kit board a Libero Silver software license and a FlashPro4 programmer. The board is socketed and is populated with A3PE1500 silicon. Any device in the ProASIC3 family in the PQ208 package may be placed into the socket. The following key features are supported:

- On-board voltage regulation
- Advanced FlashROM capabilities
- Four high-speed LVDS channels with a ProASIC3E device or two LVDS channels with a ProASIC3 device
- Programming headers



Intellectual Property

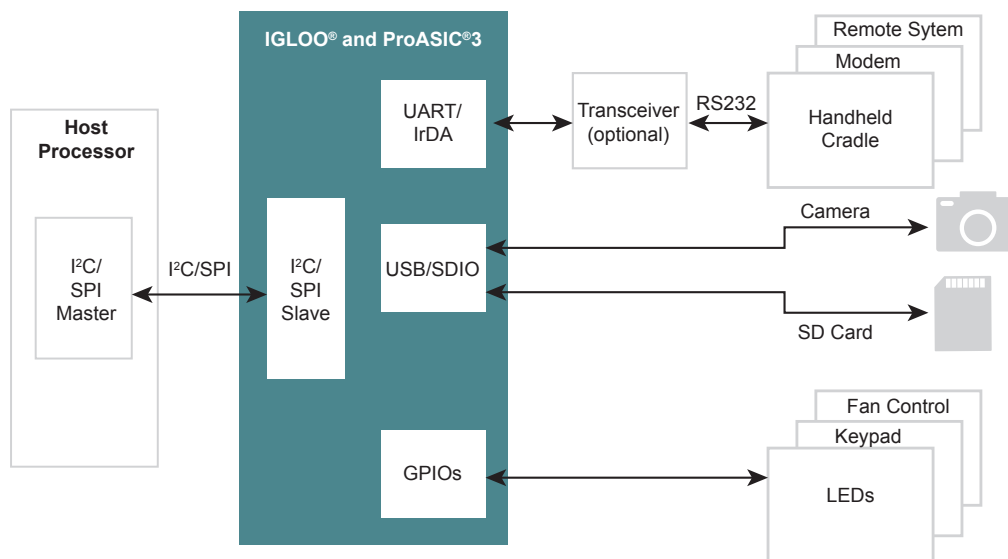
Microchip enhances your design productivity by providing an extensive suite of proven and optimized IP cores for use with Microchip FPGAs. Our extensive suite of IP cores covers all key markets and applications. Our cores are organized as either Microchip-developed DirectCores or third-party-developed CompanionCores. Most DirectCores are available for free within our Libero tool suite and include common communications interfaces, peripherals, and processing elements.

For more details on IP Cores, visit <https://www.microsemi.com/product-directory/design-resources/5092-ip-cores>

Solutions

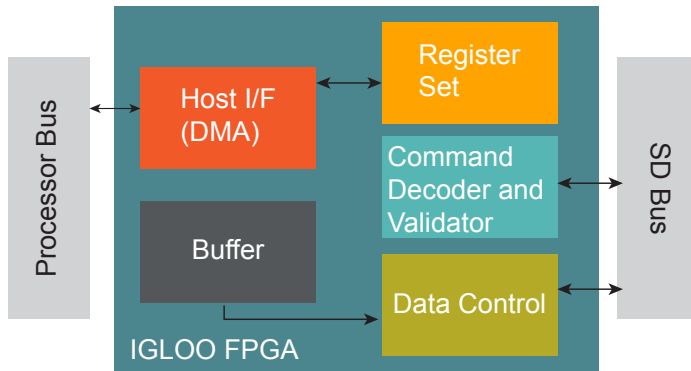
Interface Bridging

Translate bus protocols and voltages between incompatible devices at the lowest possible cost.



Storage

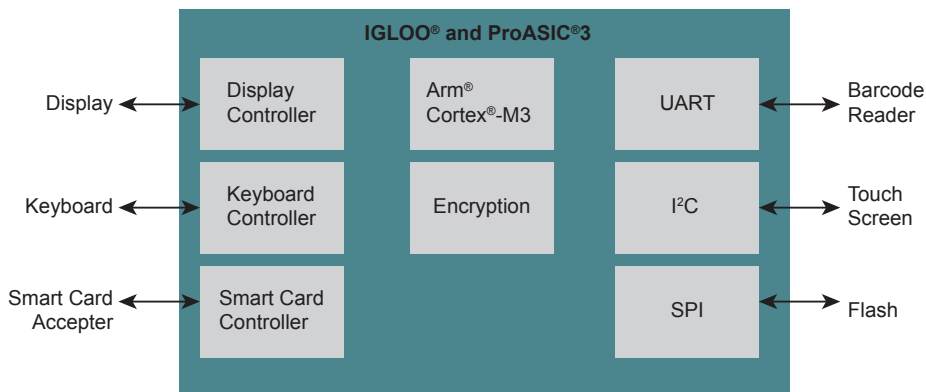
Controllers for popular storage interface standards such as SD, SDIO, microSD, MMC, etc. which are optimized for low power.



SD Controller

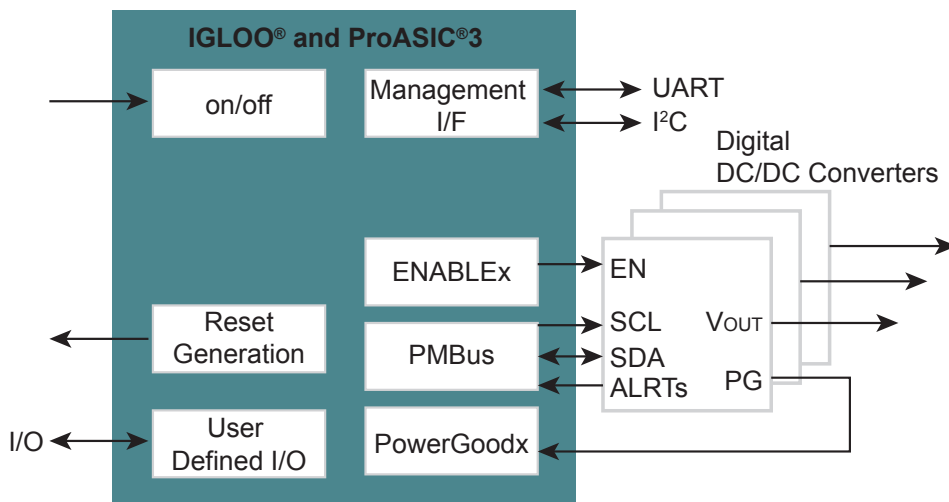
Human Machine Interface (HMI) and Display Interface

Manage various protocols interfaces for multiple devices to be connected.



Power Management Control

Manage the power-up sequencing and monitoring of other devices on the board.



Support

Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. For more information, please visit www.microchip.com:

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- Developer Help Website: www.microchip.com/developerhelp
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