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Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

PRELIMINARY

CYW20745

ROM-Based Single Microphone Headset IC With Voice Command Recognition

Cypress CYW20745 is a Bluetooth 3.0 monolithic IC solution for single microphone mono headset applications with radio, baseband, application ROM, power management, mono single microphone codec, and many other components typically required for low-cost headset designs, making it ideal for low-cost, footprint-challenged headset designs. This device is the world's first ROM-based design to support voice command recognition and multilanguage voice prompts without needing to add large expensive memory in the external BOM.

The CYW20745 also delivers differentiating features, including enhanced audio quality and reduced charging times, A2DP, and multipoint connections, through the integration of various noise suppression technologies, circuitry, and application profiles. It is a ROM-based noise and echo reduction headset, enabling a revolutionary reduction in the bill of materials (BOM) for high-end, midrange, and low-cost mono headsets.

The CYW20745 is designed for enabling features and audio quality that are usually available only for high-end products, but at a fraction of the cost of existing solutions.

The CYW20745 supports the Bluetooth 3.0 standard, adding enhanced power control, simple and secure pairing, and enhanced inquiry response as value-added features for Bluetooth headsets.

All major functional blocks required for a mono headset, including PMU, charger, and audio codec are integrated into a single package providing low system cost, ease of implementation, and high product yields.

This device uses 65 nm process that provides significant power reduction compared to older processes.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20745	CYW20745
BCM20745A0KMLGT	CYW20745A0KMLGT
BCM20745A0KMLG	CYW20745A0KMLG
BCM20745A0KFBGT	CYW20745A0KFBGT
BCM20745A0KFBG	CYW20745A0KFBG

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to:
http://www.cypress.com/glossary

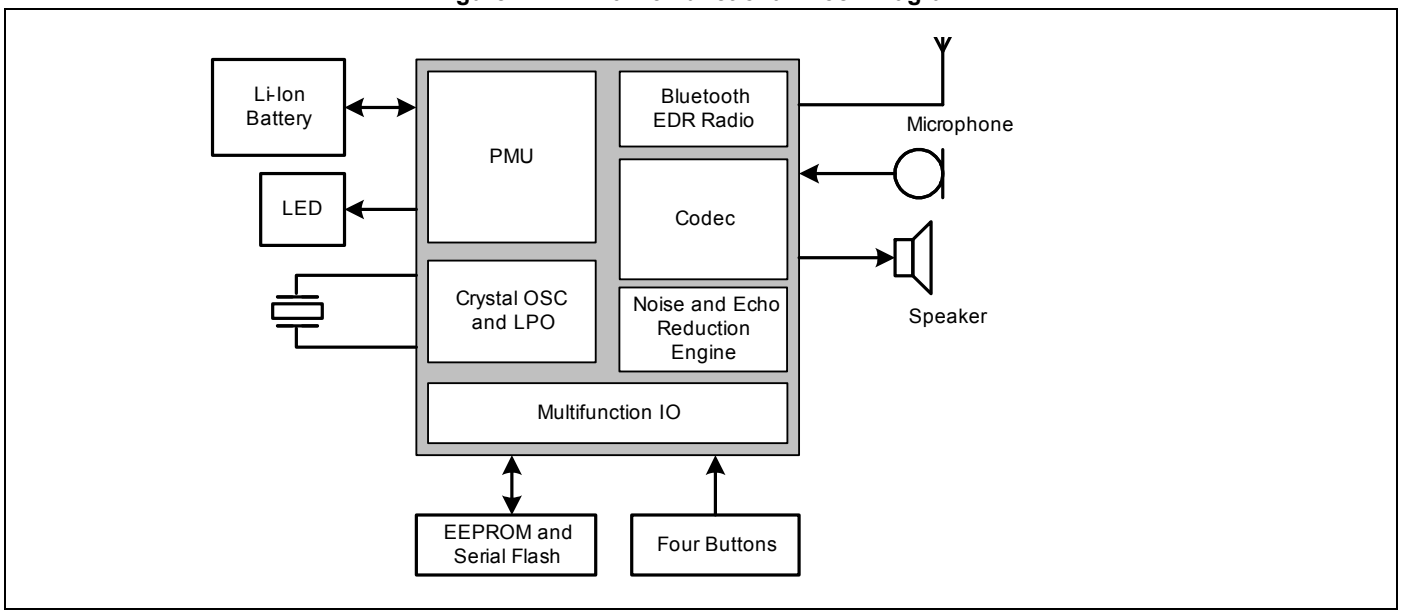
Applications

■ The CYW20745 is fully optimized for mono headset products.

Features

- Single-chip Bluetooth 3.0 transceiver supporting Bluetooth 2.1 + Enhanced Data Rate (EDR) and Bluetooth 2.0, 1.2, and 1.1 backward compatibility
- Best-in-class Bluetooth radio with 8 dBm transmit power and –91 dBm receive sensitivity
- Support for side tone and digital microphones
- Supports microphone and speaker equalization
- High-performance ARM Cortex™-M3 processor
- On-chip SRAM and ROM
- Extensive configuration tool for application differentiation and audio path tuning
- Integrated SmartAudio® speech enhancement algorithms
  - Noise suppression
  - Echo suppression
  - Wind-noise suppression
  - Packet-loss concealment
  - Bit-error concealment
  - Speech-intelligibility enhancement
  - Automatic gain control (AGC) and automatic volume control (AVC)
- UART and UART over USB adapter for test and configuration
- Switching regulator, battery charger, and power management unit
- Supports fast charging, power dissipation monitoring, and optional charger voltage regulation
- High quality 8 kHz and 16 kHz audio codec with a single microphone interface
- Low power operation
- 5.5 mm × 4.5 mm, 66-ball WFBGA package with a 0.5 mm pitch and a 7 mm x 8 mm, 52-pin QFN package with a 0.5 mm pitch
- Pin-to-pin compatible with the CYW20740/CYW20741/CYW20742
- Full-featured and configurable mono headset application firmware built on Cypress's Bluetooth for embedded (BTE) audio stack
- Infinite Shelf Life Extension support
- Multilanguage voice prompt
- Advanced multipoint
- Pairing enhancements
- A2DP over mono
- Voice command recognition

Figure 1. CYW20745 Functional Block Diagram



IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Contents

1. Overview

The Cypress CYW20745 is a monolithic, single-chip, Bluetooth 3.0-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. It is a ROM-based, single microphone, mono headset IC with noise and echo reduction. The CYW20745 features the highest level of integration and eliminates all critical external components, thereby minimizing the footprint and reducing the system cost associated with implementing a Bluetooth audio solution.

1.1 Features

The features supported by the CYW20745 are listed below:

- Fully supports Bluetooth 3.0 and 2.1+EDR features and is Bluetooth 2.0, 1.2, and 1.1 backward compatible. Feature support includes the following:
  - Bluetooth Enhanced Data Rate (EDR)
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - eSCO
  - Fast connect
  - Enhanced power control
- Integrated SmartAudio® speech enhancement algorithms which include:
  - Noise suppression
  - Echo suppression
  - Wind-noise suppression
  - Packet-loss concealment
  - Bit-error concealment
  - A speech-intelligibility enhancement
  - Automatic gain control and automatic volume control
  - An echo cancellation enhancement for a carkit
- Best in class Bluetooth radio with 8 dBm transmit power and –91 dBm receive sensitivity
- A2DP over mono
- Voice command recognition
- Support for side tone and digital microphones
- Supports microphone and speaker equalization
- High-performance ARM Cortex-M3 processor
- On-chip SRAM and ROM
- Extensive configuration tool for application differentiation and audio path tuning
- UART and UART over USB adapter for test and configuration
- Maximum UART baud rates of 1.5 Mbps
- Built-in transmit/receive switch and balun
- High-quality 8 kHz and 16 kHz audio codec with a single microphone interface
- Switching regulator, battery charger, and power management unit
- Automatic power saving modes
- Built-in low power oscillator to support deep sleep
- Supports fast charging, power dissipation control, and optional charger voltage regulation
- Built-in Low-Dropout (LDO) regulators
- Independent software-controlled regulator shutdown
- 5.5 mm × 4.5 mm, 66-ball WFBGA package with a 0.5 mm pitch, and a 7 mm × 8 mm, 52-pin QFN package with a 0.5 mm pitch
- Full-featured and configurable mono headset application firmware built on the Cypress BTE audio stack including application enhancements like multilanguage voice prompts, advance multipoint, and pairing enhancements

1.2 Configuration Parameters

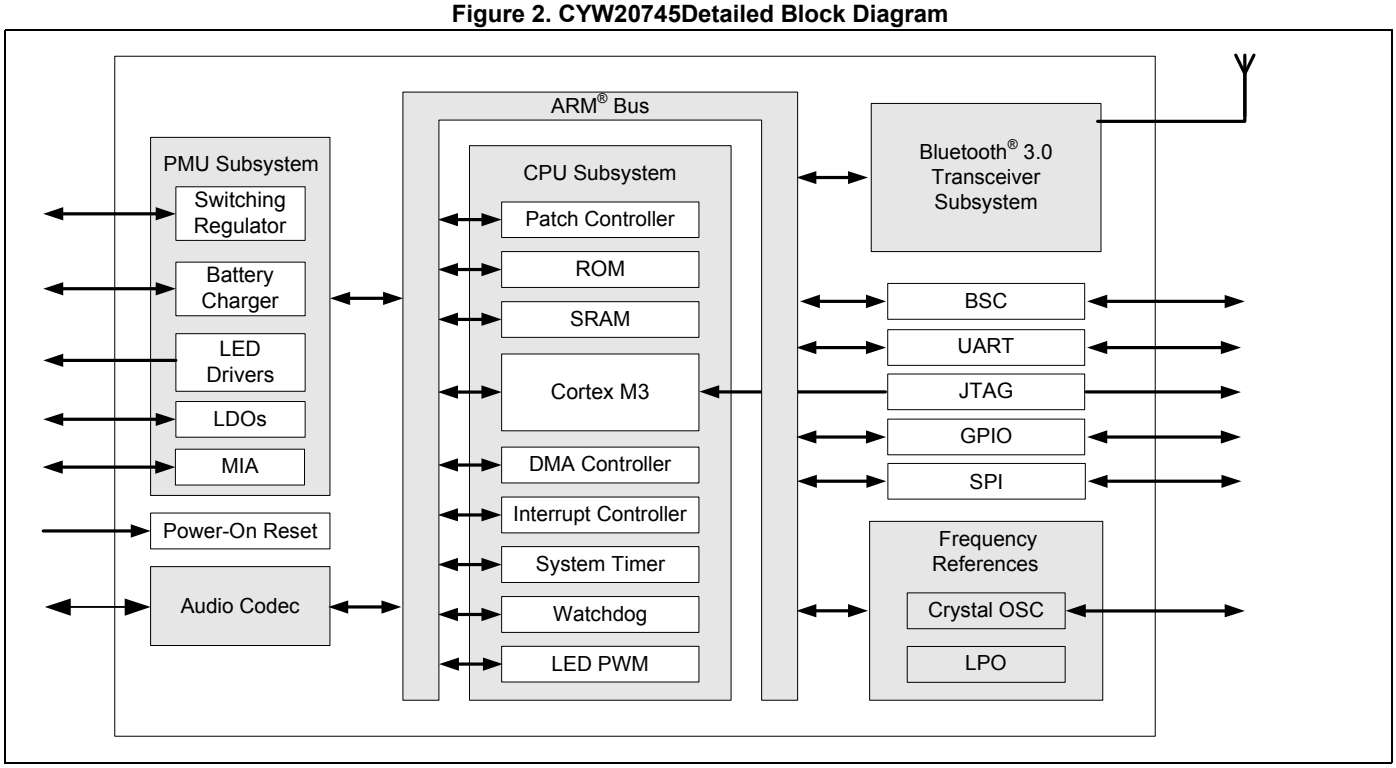
The following features can be configured using a simple GUI-based configuration tool. These features are programmed into the EEPROM using a PC attached to the CYW20745 UART port.

- Power Management Unit (PMU) parameters
- LED states (duty cycle, events, brightness, etc.)
- Speech path gain settings
- Event-based tone generation
  - Ring tone selections
  - Events definition
- General-Purpose Input/Output (GPIO) mask
- Button functionality (timing and sequence definition)
- Bluetooth parameters
  - Pairing timeout
  - Hands-Free Profile (HFP) features
  - Network time
  - Auto reconnect
- Power saving modes
  - Power on/off timer
  - Automatic switch-off timer
- Friendly device name
- Bluetooth Device (BD) address

1.3 Detailed Block Diagram

Figure 2 illustrates the major internal components of the CYW20745.

Figure 2. CYW20745Detailed Block Diagram



Major subsystems are described in the following sections:

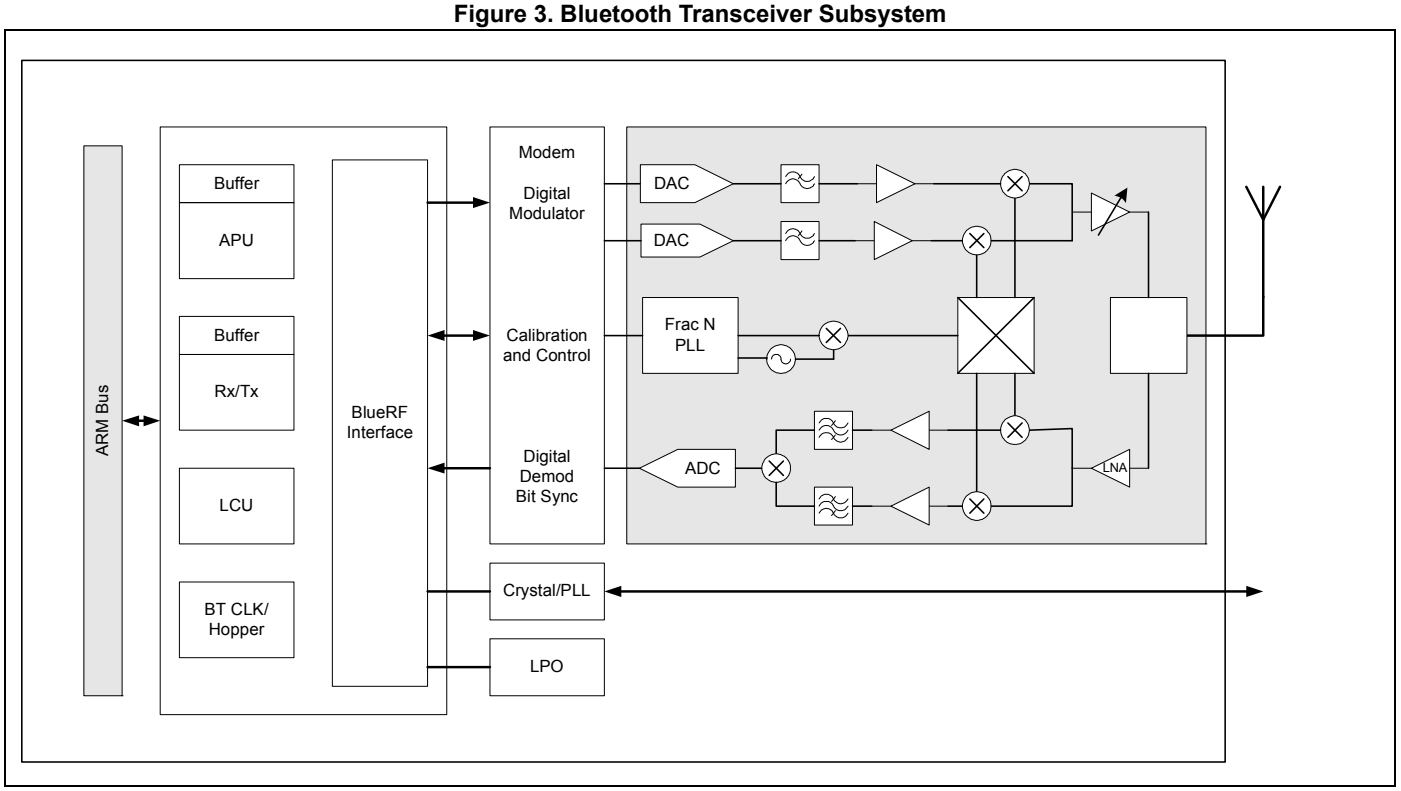
- Section 2.: “Bluetooth Transceiver,” on page 7
- Section 3.: “CPU Subsystem,” on page 9
- Section 4.: “Power Management Unit,” on page 11
- Section 5.: “Peripherals,” on page 14
- Section 6.: “Audio,” on page 16
- Section 7.: “Frequency References,” on page 18

CYW20745 modes of operation are described in Section 8.: “Operation,” on page 19.

2. Bluetooth Transceiver

The CYW20745 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed Industrial, Scientific, and Medical (ISM) band. It is fully compliant with the Bluetooth Radio Specification and EDR specification, and meets or exceeds the requirements to provide the highest communication link QoS. Figure 3 shows the individual components within the Bluetooth transceiver.

Figure 3. Bluetooth Transceiver Subsystem



2.1 EDR Radio Transmitter Path

The CYW20745 features a fully integrated zero-IF transmitter. The baseband transmits GFSK data that is digitally modulated in the modem block, and then upconverts the data to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filters, I/Q upconverters, output Power Amplifiers (PAs), and RF filters. It also incorporates π/4-DQPSK modulation for 2 Mbps and 8-DPSK modulation for 3 Mbps to support EDR.

2.1.1 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signals. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

2.1.2 Power Amplifier

The fully integrated PA is configurable for Class 2 operation as well as Class 1 operation with higher supply voltage to the power amplifier, using a highly linearized, temperature-compensated design. This feature provides the user with greater flexibility and options in the type of front-end matching and filtering to use with the CYW20745.

2.2 EDR Radio Receiver Path

The receiver path uses a low-IF architecture to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW20745 to be used in most applications with no off-chip filtering.

2.2.1 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

2.2.2 Receiver Signal Strength Indicator

The radio portion of the CYW20745 provides a Received Signal Strength Indication (RSSI) signal to the baseband so that the controller can participate in a Bluetooth power-controlled link. This occurs by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

2.3 EDR Radio Local Oscillator Generation

Local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW20745 uses an internal RF and IF loop filter.

2.4 EDR Radio Calibration

The CYW20745 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user intervention is required during normal operation or during manufacturing, to provide for optimal performance. Calibration optimizes all major blocks in the radio to within 2 percent of optimal performance. The calibration process accounts for process variation and temperature variation. Calibration occurs transparently during normal operation and during the setting time of hops. The transceiver then calibrates temperature variations as the device cools and heats during normal operation within its environment.

2.5 Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operations. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes Host Controller Interface (HCI) packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before data is sent over the air:

- Symbol timing recovery, data deframing, Forward Error Correction (FEC), Header Error Control (HEC), Cyclic Redundancy Check (CRC), data decryption, and data dewhitening in the receiver
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter

2.5.1 Frequency Hopping Generator

The frequency hopping sequence generator supports AFH by selecting the correct hopping channel number depending on the link controller state, Bluetooth clock, and device address.

2.5.2 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller to perform the link control tasks. There are two major states: STANDBY and CONNECTION. In addition, there are six substates: PAGE, PAGE SCAN, INQUIRY, INQUIRY SCAN, SNIFF, and HOLD.

3. CPU Subsystem

3.1 Cortex-M3™

The CYW20745 uses a Cortex M3. The CPU is clocked at up to 48 MHz. During idle time, the CPU is placed in a low-power state.

3.2 On-Chip Memories

The CYW20745 includes TBD KB of ROM and 120 KB of RAM. The ROM stores firmware for the headset application. The RAM stores temporary variables. An external EEPROM is used to store configuration and nonvolatile variables.

3.3 Watchdog Timer

The hardware incorporates a watchdog timer capable of resetting the chip. The watchdog timer ensures correct system operation.

3.4 General-Purpose Timer

The general-purpose timer can be configured to operate either from the high-speed clock source or the Low-Power Oscillator (LPO). When operating from the LPO, the timer can wake the hardware from deep sleep when a timer event occurs.

3.5 ARM® JTAG

The test mode pins can be configured to switch the CYW20745 to operate in ARM JTAG mode as shown in Table 2.

Table 2. Enabling ARM JTAG with the TM Pins

Function	TM1	TM2
Normal operation	0	0
ARM JTAG	1	0
Reserved	x	1

The I/O assignments in the ARM JTAG mode are provided in Table 3.

Table 3. JTAG Connections

Signal	Pin
TCK	GPIO5
TDI	GPIO8
TDO	GPIO7
TMS	GPIO6
TRSTN	RST_N

3.6 External Reset

The CYW20745 has an integrated Power-On Reset (POR) circuit that resets all circuits to a known power-on state. This action can also be driven by an external reset signal that can be used to externally control the device, forcing it into a power-on reset state. The $\overline{RST}$ signal input is active low and has an internally programmable pull-up resistor (no connection is required in most applications).

When the reset signal is asserted (100 µsec low on $\overline{RST}$), the GPIOs are in the following states:

- GPIO_13 = pulled down
- GPIO_12 = pulled down
- GPIO_11 = pulled up
- GPIO_10 = pulled down
- GPIO_9 = pulled down
- GPIO_8 = pulled down
- GPIO_7 = pulled up
- GPIO_6 = pulled up
- GPIO_5 = pulled up
- GPIO_4 = pulled up
- GPIO_3 = pulled up
- GPIO_2 = pulled down
- GPIO_1 = pulled down
- GPIO_0 = pulled down

4. Power Management Unit

To reduce the external bill of materials, the CYW20745 integrated power management unit includes the following key features:

- Switching regulator
- Optimized for lithium-ion and Lithium Polymer batteries
- LDO regulators for noise isolation
- Battery charger
- LED drivers
- Low-battery detection
- Undervoltage lockout
- Short circuit protection
- On-chip temperature sensor
- Charger watchdog

	**Caution!** The CYW20745 is designed for use with lithium secondary cell batteries. These batteries can become unsafe and ignite, rupture, explode, reach high temperatures, and leak acid. Special caution must be exercised in the design, manufacture, test, and use of the end product that incorporates this device. The CYW20745 has built-in features that are intended to reduce, but not eliminate, the chance of an unsafe condition. When using lithium batteries, it is strongly recommended that an external battery protection IC be used to manage charger overvoltage, discharge undervoltage, charger overcurrent, and discharge overcurrent. In addition, the lithium cells should have an integrated PTC, thermal fuse, vent, and or a separator. Consult the battery manufacturer for safety suggestions. Due to these system level usage and safety protections, Cypress accepts no responsibility for any injuries or damages sustained as a result of using this device. The customer assumes all attendant risk.

4.1 Switching Regulator

The CYW20745 includes an integrated high-performance, buck-mode switching regulator optimized to work with single-cell lithium-ion batteries.

The switching regulator includes the following capabilities and features:

- Direct power from a lithium-ion battery
- Programmable output voltage
- Programmable switching frequency
- Burst mode for a low quiescent current
- Pulse-Width Modulation (PWM) mode for a clean supply voltage in active mode
- Fast switching between burst and PWM modes
- Soft start-up
- Low start-up voltage (external enable with battery undervoltage lockout)
- Duty cycle limiting, up to 90% duty cycle
- Overcurrent protection
- Snubber to eliminate ringing or oscillation
- High efficiency
- Low quiescent current with no load

4.2 LDO Regulators

Multiple LDO regulators are included, each individually tailored to provide all of the required low-noise supply voltages for driving critical on-chip circuits.

There are four major linear regulators in the CYW20745—BT core/RF circuits, I/Os, audio codec, and speaker driver. A low-noise microphone bias supply is also provided.

4.3 Battery Charger

The CYW20745 includes an integrated battery charger optimized for use with lithium-ion and lithium polymer batteries.

The battery charger's operation is based on a hardware state machine that runs separately from the CYW20745 baseband logic and Central Processing Unit (CPU). The charging algorithm parameters are configurable and can be tuned to optimize the charger's performance for specific batteries and charging power supplies. These parameters are stored in off-chip EEPROM or serial flash and are loaded into the charger state machine once the CPU boots and starts running.

Battery charger capabilities and features include:

- System operation while the battery is charging.
- A four-stage battery charge algorithm (pre-charge0, constant current, constant voltage, and recharge). The constant current phase supports programmable voltage and current levels. The number of programmable voltage and current levels is also programmable.
- Internal pass transistor for low-cost systems.
- Optional charger voltage regulation using external bipolar transistor for high-voltage charging systems
- Safety timers for each charge stage.
- Continuously running fault detectors (including battery overcurrent, battery overvoltage, and charger voltage errors)
- Temperature and voltage drop safety detectors
- Internal temperature sensor
- Low-power UVLO mode
- Fuel-gauge monitoring
- Power dissipation control
- Charger type detection
- Handles standard charge batteries from 30 mAh to 200 mAh and 3C fast charge batteries from 30 mAh to 130 mAh. Possibility of fast charging at 5C for batteries below 80 mAH.
- Handles standard carkit batteries (0.5C charge) from 30 mAh to 800 mAh.
- Can preserve the battery health by reducing recharge cycles (the CYW20745 chip sinks limited/reduced current from the battery when the charger is plugged in and the battery is fully charged).
- Integrated ADC for monitoring battery, temperature, and charger voltage.

4.3.1 Charger Watchdog

A watchdog circuit in the charger block has been included to automatically reset the CYW20745 in the event of a firmware crash. The following details apply to watchdog timer operation:

- The watchdog timer is disabled at POR.
- By default, firmware will enable the watchdog timer during bootup. Once enabled, the watchdog timer cannot be disabled.
- The watchdog timer countdown starts immediately after a charger is plugged in.
- Once started, the watchdog countdown continues until a watchdog time-out triggers a baseband POR, unless firmware stops the watchdog before the timer completes its countdown.
- As long as a charger remains attached, the watchdog will remain inactive after a POR or after firmware stops the watchdog. The watchdog will be reactivated if a charger is removed and then reattached.
- The default setting for the watchdog timer is two seconds.

4.4 LED Drivers

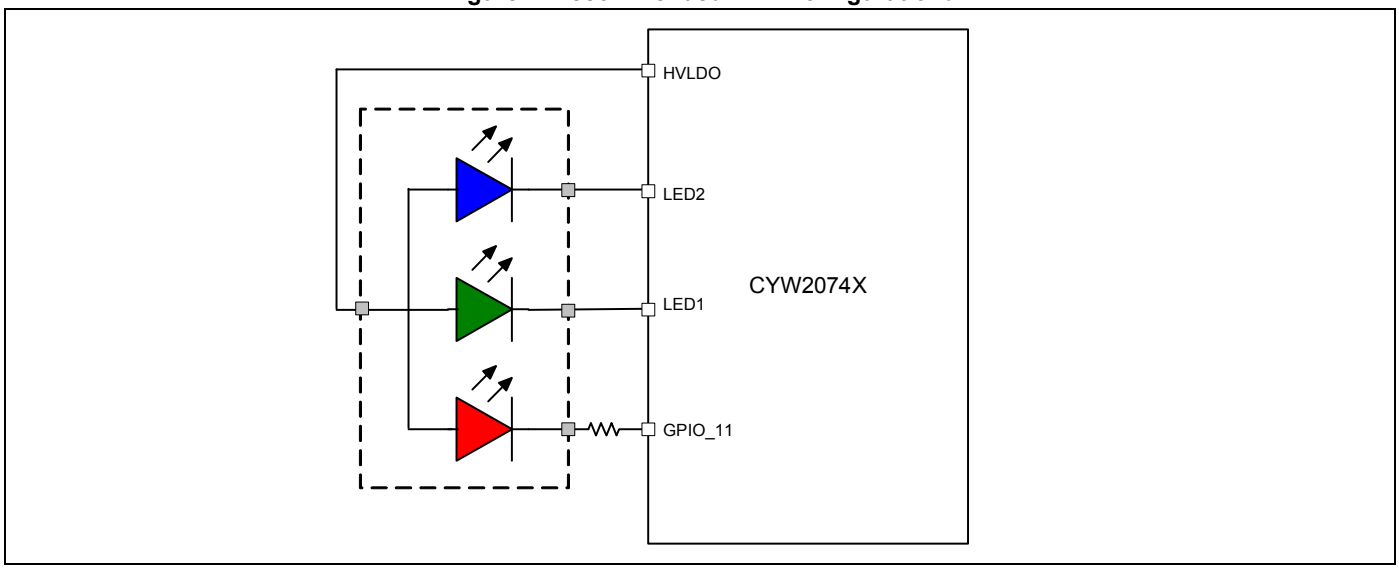
The CYW20745 includes two integrated, constant-current LED drivers and one GPIO with PWM voltage control that can be used as a third LED driver.

LED driver capabilities and features include:

- Programmable drive current
- Low dropout voltage
- Current sinking driver with high voltage tolerance to allow connecting LEDs to the I/O power supply.

Figure 4 illustrates recommended LED connections to the CYW20745.

Figure 4. Recommended LED Configuration[6]



5. Peripherals

5.1 UART Interface

The UART physical interface is a standard, 4-wire interface (RX,TX, RTS, CTS) with a 9600 bps to 1.5 Mbps adjustable baud rate. The interface features an automatic baud rate detection capability to establish a proper baud rate selection. Alternatively, the baud rate may be preconfigured in the firmware. The CYW20745 has a 480-byte receive FIFO and a 480-byte transmit FIFO to support high data rates.

Note: By default, the UART is configured to operate over the USB connector (UART over USB). For more information on how to implement UART over USB, refer to *UART Communication Over USB Connector*, document number 2074X-AN60x-R.

Table 4. GPIO Assignment for the UART Interface

Signal	Pin
RXD	GPIO0
TXD	GPIO1
CTS	GPIO2
RTS	GPIO13

The CYW20745 has the capability to perform XON/XOFF flow control and has hardware support for Serial Line Internet Protocol (SLIP). It also has the capability to perform wake-on-activity. When the chip is in a low-power sleep mode, activity on the RX or CTS inputs can wake the chip.

The baud rate of the CYW20745 UART is controlled by two registers. The first, called the DLBR register, is a UART clock divisor that divides the 24 MHz reference clock by an integer multiple of 16. The second, called the DHBR register, is a baud rate adjustment that is used to specify a number of 24 MHz clock cycles to stuff in the first or second half of each bit time. Up to eight 24 MHz clock cycles can be inserted into the first half of each bit time, and up to eight 24 MHz clock cycles can be inserted into the second half of each bit time.

When setting the baud rate manually, the UART clock divisor is an 8-bit value that is stored as 256 – *desired divisor*. For example, a desired divisor of 13 is stored as 256 – 13 = 243 = 0xF3.

The baud rate adjustment is also an 8-bit value, of which the 4 most significant bits are the number of additional clock cycles to insert in the first half of each bit time, and the 4 least significant bits are the number of clock cycles to insert in the second half of each bit time. If either of these two values exceeds 8, they are rounded to 8.

Table 5 contains example values to generate common baud rates.

Table 5. Common Baud Rate Examples

Desired Baud Rate in bps	UART Clock Divisor (256 – Desired Divisor)	Baud Rate Adjustment (High Nibble)	Baud Rate Adjustment (Low Nibble)	Actual CYW20745 Baud Rate in bps	Percentage Error
1500000	0xFF	0x00	0x00	1500000	0.00
921600	0xFF	0x05	0x05	923077	0.16
460800	0xFD	0x02	0x02	461538	0.16
230400	0xFA	0x04	0x04	230796	0.17
115200	0xF3	0x00	0x00	115385	0.16
57600	0xE6	0x00	0x00	57692	0.16
38400	0xD9	0x01	0x00	38400	0.00
28800	0xCC	0x00	0x00	28846	0.16
19200	0xB2	0x01	0x01	19200	0.00
14400	0x98	0x00	0x00	14423	0.16
9600	0x64	0x02	0x02	9600	0.00

Normally, the UART baud rate is set by the parameters stored in the EEPROM or serial flash, or by automatic baud rate detection, and the host does not need to adjust the baud rate. The CYW20745 UART will operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

5.2 BSC Interface

The CYW20745 includes dedicated hardware for implementing a 2-wire interface used to connect to an off-chip serial EEPROM. The EEPROM is required to store configuration parameters as well as pairing information. Support is available for 100 Kbps and 400 Kbps data rate configurations. The default data rate is 100 Kbps. In this context, Kbps = 1000 bits per second.

Note: The Broadcom Serial Control (BSC) bus is Philips® I^2C compatible.

5.3 SPI Interface

The Serial Peripheral Interface (SPI) is a high-speed, synchronous serial interface that can be used for interfacing with other devices. A full-duplex DMA channel is available for low overhead SPI control. The SPI interface supports several modes of operation:

- 4-wire mode—interface includes clock, chip select, data in, and data out. This is the standard mode of operation.
- 3-wire mode—interface includes clock, chip select, and one bidirectional data line for devices that support 3-wire mode of operation on SPI.
- Master mode—the SPI can be configured for master mode operation up to a maximum frequency of 24 MHz.
- Slave mode—the SPI can be configured for slave mode operation up to 48 MHz.

5.4 GPIO

The CYW20745 has three GPIOs for the user interface input. This allows for up to three buttons on the headset.

Table 6. GPIO Assignment for Buttons

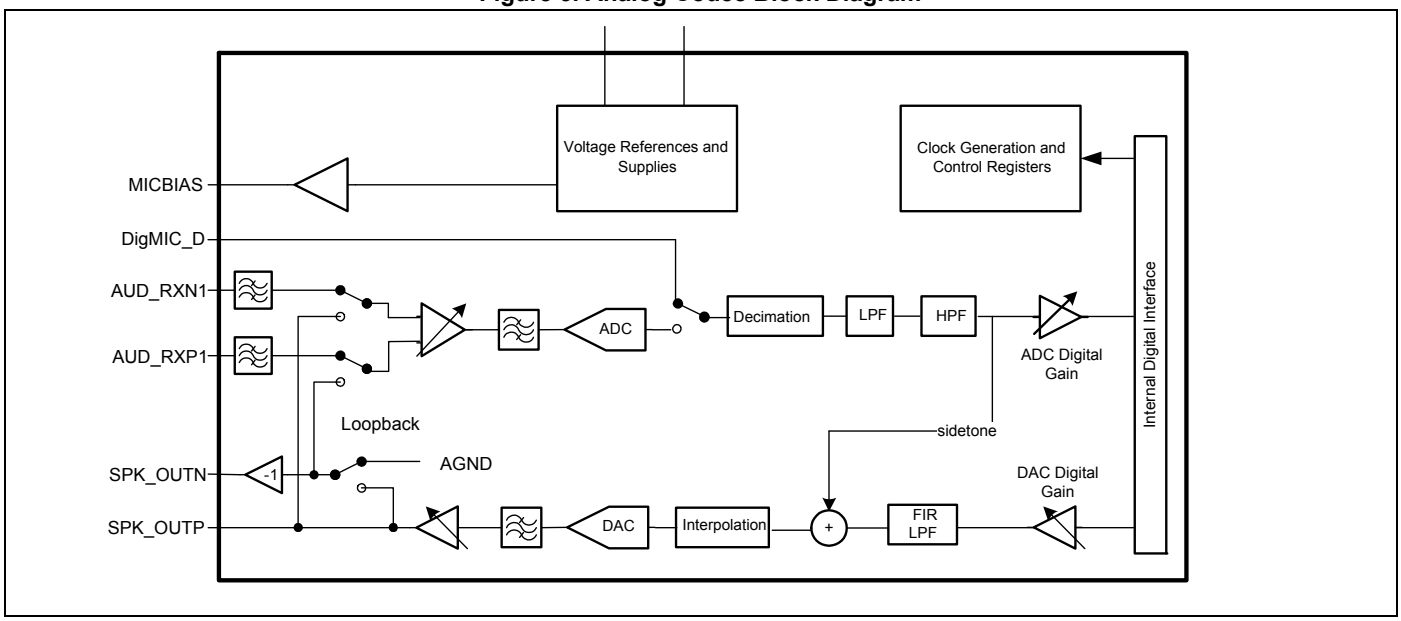
Signal	Pin
Multifunction	GPIO3/WAKEB
Volume up	GPIO8
Volume down	GPIO9

6. Audio

6.1 Codec

Figure 5 shows the analog codec block diagram.

Figure 5. Analog Codec Block Diagram



6.1.1 DAC and Headset Amplifier

The CYW20745 DAC and headset amplifiers include the following capabilities and features:

- 32Ω and 16Ω speaker-impedance support
- Differential load connections
- 18 dB analog gain control
- Pop reduction circuit at power-up/down
- Several power modes
- 8 kHz and 16 kHz sample rates

6.1.2 Preamplifier and ADC

The CYW20745 preamplifier and ADC include the following capabilities and features:

- Wide dynamic range
- Optional in-band analog High-Pass Filter (HPF) for increased wind noise tolerance
- Differential and single-ended modes
- Microphone preamplifier
- Low-noise microphone bias generator
- Configurable HPF in the microphone path
- 8 kHz and 16 kHz sample rates

6.1.3 Sample Rate Adaptation

The digital rate adapter allows for up to a 5 percent adjustment and is automatically controlled by a sophisticated rate tracking and adaptation algorithm.

6.2 Speech Codecs

In addition to pass-through (no compression/decompression), the CYW20745 supports the following speech codecs:

- 8 kHz CVSD
- 8 kHz A-law
- 8 kHz μ-law

6.3 A2DP Codec

The CYW20745 supports the following A2DP codec settings:

- SBC Sampling Frequency—48 kHz, 44.1 kHz, 32 kHz, and 16 kHz are the supported sampling frequencies.
- Channel Mode—Mono, Dual, Stereo, and Joint Stereo modes are supported.
- Bit Pools:
  - Joint Stereo: 30–249
  - Dual: 16–75
  - Mono: 14–128
  - Stereo: 30–250

6.4 Digital Microphone Support

The interface drawing and definition of the microelectromechanical systems (MEMS) digital microphone is shown in Figure 6. The output from the digital microphone is a binary bit sequence. A 3 MHz clock must be supplied to the digital microphone from the CYW20745. L/R select is used to define the clock edge on which the data from the microphone is output. L/R select is tied to ground because the interface is designed to support only a single digital microphone.

Figure 6. MEMS Digital Microphone Interface

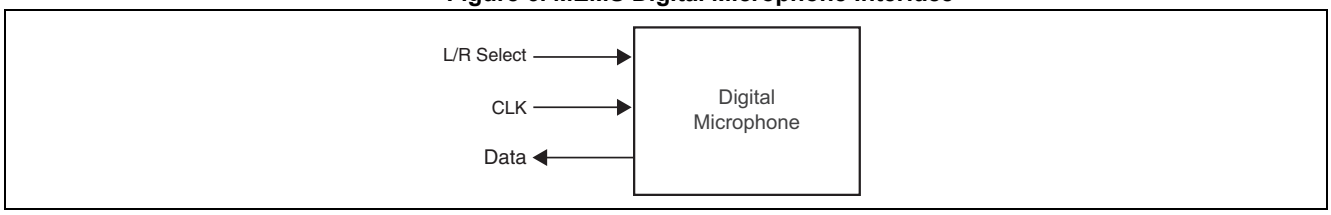


Table 7. MEMS Digital Microphone Interface

Signal Name	Description
Data	Microphone binary data output (connect to GPIO)
CLK	Microphone external clock input (connect to GPIO, 3 MHz, 50% duty cycle)
L/R select	Microphone input that defines which edge of the clock signal will be used to trigger data output; typically connected to ground.

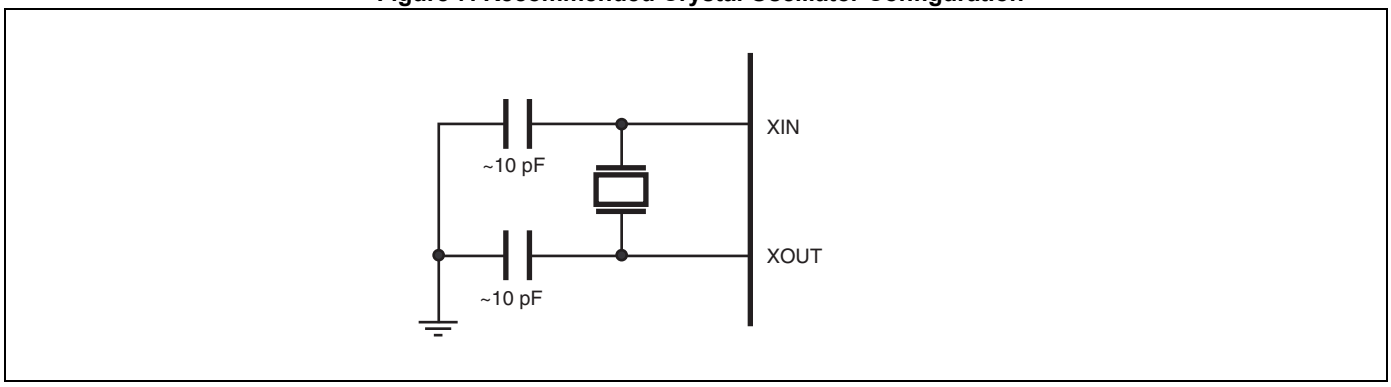
7. Frequency References

The CYW20745 uses two different frequency references for normal and low-power operational modes. An external crystal is used to generate all radio frequencies and clocks used during normal operation. A fully integrated internal LPO is used to supply the clock during low-power modes.

7.1 Crystal Interface and Clock Generation

The CYW20745 uses a 26 MHz crystal as the primary reference frequency. Figure 7 illustrates the recommended configuration for the crystal oscillator, including all external components.

Figure 7. Recommended Crystal Oscillator Configuration



7.2 Low-Power Oscillator

To enable low-power operating modes, an internal LPO is included on the CYW20745. The oscillator is calibrated automatically by the hardware.

8. Operation

8.1 CYW20745 Modes of Operation

Specific user, and other monitored system events, determine the mode in which the CYW20745 operates. Each supported operating mode is designed to perform the desired function, while minimizing power consumption.

The CYW20745 supports the following operating modes:

Active mode	The fully functional mode of the chip in which the headset is in a connected state and has an active call.
Standby mode	In standby mode, HS is in a connected state, and there is no active call, but the HS is waiting for an incoming or outgoing call.
Sleep mode	This is a temporary chip mode in which certain blocks are switched off (for example, radio, codec, and so on), but the software is in a state where it can quickly turn on all blocks and enter a fully functional mode. Typically software switches to this mode between bursts of activity (radio or signal processing) to conserve power in active or standby modes.
Deep Sleep (off) mode	In this mode, leakage current flows from the battery, and the chip performs no functions. To escape this mode, a user button-press event or charger plug-in event must occur.
Charging mode	The CYW20745 operates in the charging mode when the charger is plugged in. All activities related to battery charging, monitoring, and safety features are performed in this mode.

9. Pin Assignments

Table 8 lists pin assignments on the CYW20745 for the WFBGA package.
Table 9 lists pin assignments on the CYW20745 for the QFN package.

Table 8. CYW20745 Pin Assignments (WFBGA Package)

Pin Name	Pin Number	I/O	Power Domain	Description
AUD_AVDD	E6	I	AUD_AVDD	Audio codec analog power
AUD_AVSS	F5, G4, H4, H8	I	AUD_AVSS	Audio codec analog ground
AUD_RXN1	H5	I	AUD_AVDD	Audio codec microphone differential negative input channel.
AUD_RXP1	G5	I	AUD_AVDD	Audio codec microphone differential positive input channel.
NC	H6	–	–	No connect
NC	G6	–	–	No connect
AUD_AVSS	B8	I	AVSS	Charger. Analog ground
NPNCNTL	C7	O	VCHG	Base control for external PNP driver transistor through an NPN transistor, used for handling high charging voltage.
GPIO_0	F8	I/O	VDDO	General-purpose I/O
GPIO_1	E7	I/O	VDDO	General-purpose I/O
GPIO_2	C8	I/O	VDDO	General-purpose I/O
GPIO_3	F10	I/O	VDDO	General-purpose I/O
GPIO_4	E9	I/O	VDDO	General-purpose I/O
GPIO_5	D5	I/O	VDDO	General-purpose I/O
GPIO_6	D7	I/O	VDDO	General-purpose I/O
GPIO_7	F9	I/O	VDDO	General-purpose I/O, or mux into ADC
GPIO_8	D4	I/O	VDDO	General-purpose I/O
GPIO_9	C4	I/O	VDDO	General-purpose I/O
GPIO_10	A1	I/O	VDDO	General-purpose I/O
GPIO_11	B2	I/O	VDDO	General-purpose I/O
GPIO_12	B3	I/O	VDDO	General-purpose I/O
GPIO_13	B5	I/O	VDDO	General-purpose I/O
HVLDO	C10	O	AVDD	Voltage supply for I/Os. Voltage output pin from HVLDO. Analog power supply to drive digital I/O, flash, and LEDs.
LED1	A6	O	VBAT	Output driver for LED. Connect the cathode of LED1. Anode can be connected to HVLDO.
LED2	B6	O	VBAT	Output driver for LED. Connect the cathode of LED2. Anode can be connected to HVLDO.
MICBIAS	G7	O	MICAVDD	Microphone bias output
MICREF	H7	I	ACDAVDD	Microphone reference voltage
RES	G2	O	VDDXO	External calibration resistor (connect 15K, 1% to ground)
RFP	E1	I/O	VDD_RF	RF I/O port, connect to antenna
RST	G10	I	VDDO	Power-on reset, active low
SPK_AVDD	H10	I	SPKAVDD	Speaker analog power
SPK_AVSS	G8	I	SPKAVSS	Speaker ground
SPK_OUTN	H9	O	SPKAVDD	Speaker differential negative output channel
SPK_OUTP	G9	O	SPKAVDD	Speaker differential positive output channel
TM1	C2	I	VDDO	Test mode pin (connect to ground)
TM2	B1	I	VDDO	Test mode pin (connect to ground)

Table 8. CYW20745 Pin Assignments (WFBGA Package) (Cont.)

Pin Name	Pin Number	I/O	Power Domain	Description
VBAT	A7	I	VBAT	Battery positive supply terminal pin
VBAT_AU_AVDD	D9	I	VBAT	Power input for audio LDO and HVLDO—powers from battery as VBAT pin
VCHG	A5	I	VCHG	Charger supply input
VCHGAUX	A4	I	VCHG	Power to the charger control system
VDDC	A3, D10	I	VDDC	1.2V core power input. Tie to V12 on PCB.
VDDIF	C1	I	VDDIF	Power to the IF circuit. Tie to V12 on PCB.
VDDLNA	F1	I	VDDLNA	Power to the LNA. Tie to V12 on PCB.
VDDO	A2, E10	I	VDDO	3.3V digital I/O power input. Tie to AVDD on PCB.
VDDPX	H1	I	VDDPLL	RF PLL supply voltage. Tie to V12 on PCB.
VDDTF	D1	I	VDDTF	PA supply voltage. Tie on PCB to V12 pin for Class 2 or to external power source up to 2.5V for Class 1.
VDDRF	G1	I	VDDRF	RF and VCO power supply. Tie to V12 on PCB.
VDDXO	H2	I	VDDXO	Crystal oscillator power supply. Tie to V12 on PCB.
VFSW	A10	I	VBAT	PMU switching regulator output voltage feedback. Feedback network input of regulated switcher output voltage.
VIOMLDO	B9	O	V12	Main LDO supply decoupling pin
VLXSWG	A9	O	VBAT	PMU switching regulator inductor terminal. SWREG inductor terminal.
V12	B10	O	V12	Main LDO output 1.2V to digital power
VSS	C9, D2, E3, E8, F2	I	VSS	Digital radio ground
VSSP	A8	I	VSS	PMU ground
WAKEB	B7	I	AVDD_OUT	PMU wake-up and shut-down pin. MIA-LITE wakeup/system power-down signal. Connects to button switch. Internal pull-up with 0 = button activated. Active low level initiates wake-up.
XOUT	G3	O	VDDXO	XTAL out
XIN	H3	I	VDDXO	XTAL in

Figure 8 shows the pin locations on the CYW20745 WFBGA package.

Figure 8. Pin Locations (WFBGA Package)

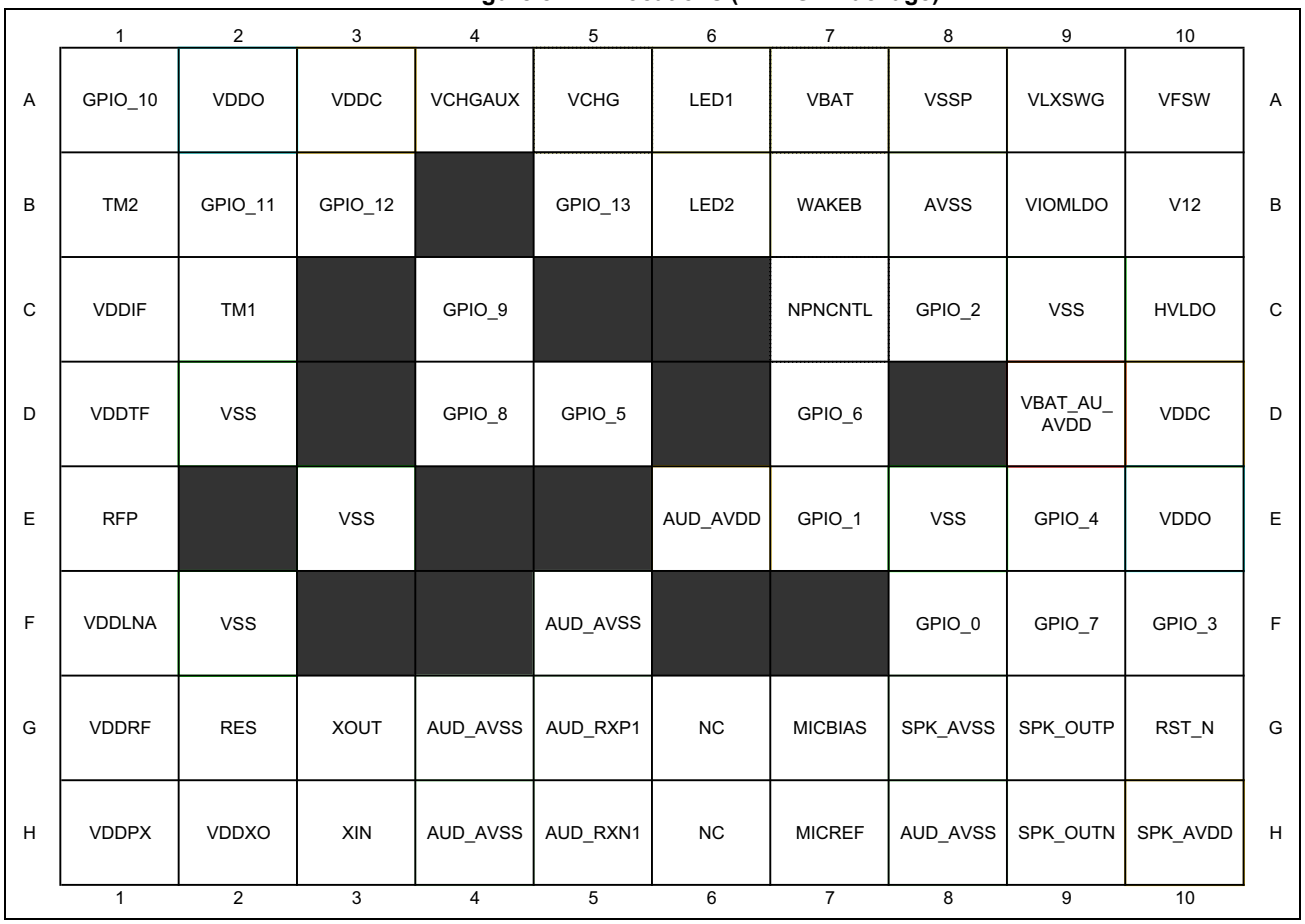


Table 9. CYW20745 Pin Assignments (QFN Package)

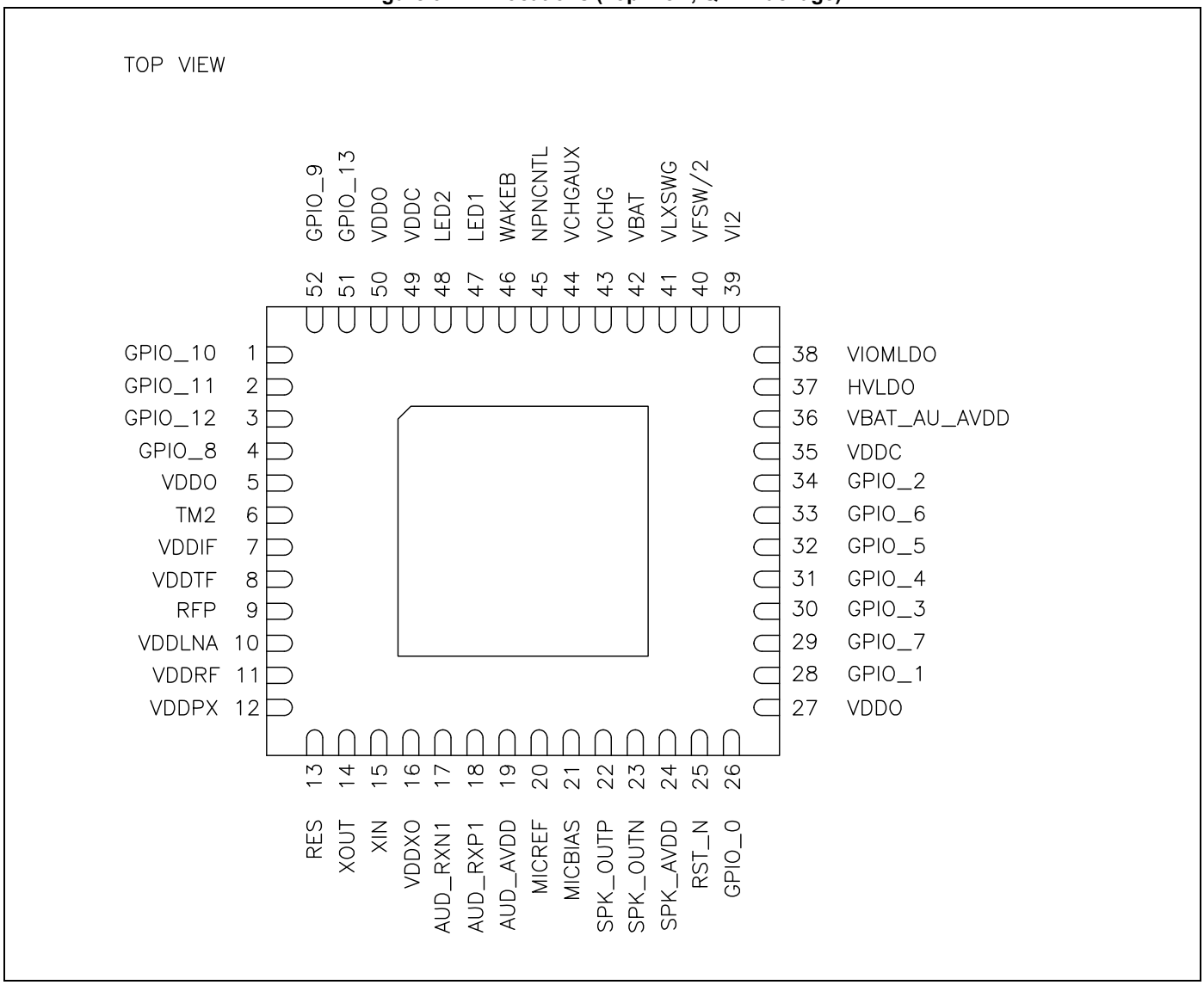
Pin Name	Pin Number	I/O	Power Domain	Description
AUD_AVDD	19	I	AUD_AVDD	Audio codec analog power
AUD_RXN1	17	I	AUD_AVDD	Audio codec microphone differential negative input channel.
AUD_RXP1	18	I	AUD_AVDD	Audio codec microphone differential positive input channel.
NPNCNTL	45	O	VCHG	Base control for external PNP driver transistor through an NPN transistor, used for handling high charging voltage.
GPIO_0	26	I/O	VDDO	General purpose I/O
GPIO_1	28	I/O	VDDO	General purpose I/O
GPIO_2	34	I/O	VDDO	General purpose I/O
GPIO_3	30	I/O	VDDO	General purpose I/O
GPIO_4	31	I/O	VDDO	General purpose I/O
GPIO_5	32	I/O	VDDO	General purpose I/O
GPIO_6	33	I/O	VDDO	General purpose I/O
GPIO_7	29	I/O	VDDO	General purpose I/O, or mux into ADC
GPIO_8	4	I/O	VDDO	General purpose I/O
GPIO_9	52	I/O	VDDO	General purpose I/O
GPIO_10	1	I/O	VDDO	General purpose I/O
GPIO_11	2	I/O	VDDO	General purpose I/O
GPIO_12	3	I/O	VDDO	General purpose I/O
GPIO_13	51	I/O	VDDO	General purpose I/O
HVLDO	37	O	AVDD	Voltage supply for I/Os. Voltage output pin from HVLDO. Analog power supply to drive digital I/O, flash, and LEDs.
LED1	47	O	VBAT	Output driver for LED. Connect the cathode of LED1. Anode can be connected to HVLDO.
LED2	48	O	VBAT	Output driver for LED. Connect the cathode of LED2. Anode can be connected to HVLDO.
MICBIAS	21	O	MICAVDD	Microphone bias output
MICREF	20	I	ACDAVDD	Microphone reference voltage
RES	13	O	VDDXO	External calibration resistor (connect 15K, 1% to ground)
RFP	9	I/O	VDD_RF	RF I/O port, connect to antenna
RST	25	I	VDDO	Power-on reset, active low
SPK_AVDD	24	I	SPKAVDD	Speaker analog power
SPK_OUTN	23	O	SPKAVDD	Speaker differential negative output channel
SPK_OUTP	22	O	SPKAVDD	Speaker differential positive output channel
TM2	6	I	VDDO	Test mode pin (connect to ground)
VBAT	42	I	VBAT	Battery positive supply terminal pin
VBAT_AU_AVDD	36	I	VBAT	Power input for audio LDO and HVLDO—powers from battery as VBAT pin
VCHG	43	I	VCHG	Charger supply input
VCHGAUX	44	I	VCHG	Power to the charger control system
VDDC	35, 49	I	VDDC	1.2V core power input. Tie to V12 on PCB.
VDDIF	7	I	VDDIF	Power to the IF circuit. Tie to V12 on PCB.
VDDLNA	10	I	VDDLNA	Power to the LNA. Tie to V12 on PCB.
VDDO	5,27,50	I	VDDO	3.3V digital I/O power input. Tie to AVDD on PCB.
VDDPX	12	I	VDDPLL	RF PLL supply voltage. Tie to V12 on PCB.

Table 9. CYW20745 Pin Assignments (QFN Package) (Cont.)

Pin Name	Pin Number	I/O	Power Domain	Description
VDDTF	8	I	VDDTF	PA supply voltage. Tie on PCB to V12 pin for Class 2 or to external power source up to 2.5V for Class 1.
VDDRF	11	I	VDDRF	RF and VCO power supply. Tie to V12 on PCB.
VDDXO	16	I	VDDXO	Crystal oscillator power supply. Tie to V12 on PCB.
VFSW	40	I	VBAT	PMU switching regulator output voltage feedback. Feedback network input of regulated switcher output voltage.
VIOMLDO	38	O	V12	Main LDO supply decoupling pin
VLXSWG	41	O	VBAT	PMU switching regulator inductor terminal. SWREG inductor terminal.
V12	39	O	V12	Main LDO output 1.2V to digital power
VSS	Center PAD	I	VSS	Digital radio ground
WAKEB	46	I	AVDD_OUT	PMU wake-up and shut-down pin. MIA-LITE wakeup/system power-down signal. Connects to button switch. Internal pull-up with 0 = button activated. Active low level initiates wake-up.
XOUT	14	O	VDDXO	XTAL out
XIN	15	I	VDDXO	XTAL in

Figure 9 shows the pin locations on the CYW20745 QFN package.

Figure 9. Pin Locations (Top View, QFN Package)



10. Specifications

10.1 Environmental Specifications

Environmental specifications for the CYW20745 are listed below:

- Operating temperature range (see "Ordering Information" on page 41)
- Storage temperature range: –40°C to +125°C
- RoHS lead-free compliance

10.2 Maximum Rating Specifications

Note: All data reported in this section are derived from system characterization.

Table 10. Absolute Maximum Electrical Ratings

Rating	Symbol	Value	Unit
Maximum DC supply voltage for I/O	VDDO	3.8	V
Maximum DC supply voltage for charger	VCHG	6.5	V
Maximum voltage on input or output pin	Vimax	Domain supply voltage [a] + 10%	V
Maximum transient voltage on input or output pin, 10% maximum duty time	Vimaxt	4.1	V
Minimum voltage on input or output pin	Vimin	VSS – 0.3v	V
Maximum voltage on LED 2 pin	VLED2-max	4.1	V
Storage temperature range	Tstg	–40 to +125	°C
Maximum battery input voltage	VBAT	4.5	V
Maximum charger power dissipation	Pmax(VCHG – VBAT)	390	mW

a. Refer to Table 8: "CYW20745 Pin Assignments (WFBGA Package)," on page 20, for the appropriate power domain.

Caution! Voltage should never be applied to any I/O pins if VDDO is not applied. I/O pins (pins listed with VDDO as the power domain) should never be actively driven high or externally pulled high.

10.3 PMU Specifications

Note: All data reported in this section are derived from system characterization.

Table 11. Typical Power Supply Output Voltage

Power Outputs	Description	Condition	Typical	Unit
VLXSWG	Switching regulator output looping back through the VFSW pin as the system power input	Programmable	1.2, 1.3–1.6	V
AUD_AVDD/ SPK_AVDD	Audio and speaker power supply and decoupling	–	2.7	V
V12	RF, XTAL, and core power supply output	–	1.2	V
AVDD	Voltage supply for charger PMU analog circuits and MIC bias	–	3.3	V

Table 12. Switching Regulator Characteristics

Property	Conditions	Minimum	Typical	Maximum	Unit
Input voltage range	Operating range	3.1	3.7	4.2	V
Switching frequency	–	–	2.8	–	MHz
Quiescent current	Burst mode	–	80	–	µA
Power-down current	–	–	500	–	nA
Output current burst mode efficiency	3 mA load	80	–	–	%
Output current PWM mode, peak	–	–	10	24.2	mA
Output current PWM mode efficiency	30 mA	–	90	–	%
Start-up input voltage	0–5 mA load	–	2.5	–	V
External output inductor	–	–	10	–	µH
External output capacitor	–	–	4.7	–	µF
Output voltage ripple	PWM mode	–	–	20	mVpp
Output voltage ripple	Burst mode	–	–	100	mVpp

Table 13. Battery Charger

Property	Condition(s)/Description	Minimum	Typical/ Default	Maximum	Unit
Charging temperature range	–	–	0–45[a]	–	°C
Charger active power supply consumption without battery charge current	Vch > 4.2V	–	–	2	mA
Vch to Vbat leakage	Charger input is 0V. Vbat is 3.6V.	–	113	–	µA
Charger input voltage	Average voltage	4.5	5.0	6.5	V
Battery overvoltage threshold	Programmable in 100 mV steps	–	4.3	–	V
Constant voltage regulation	Programmable in 100 mV steps	–	4.2	–	V
Voltage regulation accuracy	After trimming, 25°C	–	±1	–	%
Constant current accuracy	–	±20	–	–	%
Precharge safety timer, T0	–	–	60	–	minutes
Constant current[b]	Programmable to values from 10 mA to 400 mA	–	50	–	mA
Constant current safety timer, T2	Programmable from 20 minutes to 300 minutes	–	120	–	minutes
Constant voltage safety timer, T3	Programmable from 30 minutes to 4 hours	–	105	–	minutes
Taper current	Programmable	–	20	–	mA
Timer accuracy	–	–	±25	–	%
Shutoff offset	Minimum difference with battery voltage for starting the charge: Vcharger > Vbat + offset	–	340	–	mV

a. Charging temperature range can be configured through firmware. High and low threshold are configured separately: minimum up to -11°C, maximum up to +58°C. Refer to Broadcom application note 2074X-AN70x-R for information on configuring the charging temperature range.
b. Refer to Broadcom application note 2074X-AN70x-R for information on configuring the constant current.

Table 14. Charger UVLO/POR

Property	Conditions	Minimum	Typical	Maximum	Unit
Charger UVLO low-voltage threshold	Decreasing voltage	–	3.98	–	V
Charger UVLO high-voltage threshold	Increasing voltage	–	4.17	–	V

Table 15. Battery UVLO

Property	Conditions	Minimum	Typical	Maximum	Unit
Vbat undervoltage low threshold, lithium	Decreasing voltage	–	3.0	–	V

Table 16. Low Battery Interrupt[a]

Property	Conditions	Typical	Unit
Low-battery threshold	Programmable	3.40	V
Critical low-battery threshold	Programmable	3.16	V

a. Refer to Broadcom application note 2074X-AN70x-R for information on configuring the threshold.

Table 17. LED Driver 1 and 2

Property	Conditions	Minimum	Typical	Maximum	Unit
Output sink current	Programmable in 0.8 mA steps	0.8	2.3	6	mA
Current tolerance	–	–20	–	20	%

10.4 General I/O

Note: All data reported in this section are derived from system characterization.

Table 18. General I/O Electrical Characteristics

Symbol	Property	Minimum	Typical	Maximum	Unit	Test Conditions
VIL	Low-level input voltage	–	–	0.8	V	For 3.0–3.3V
VIH	High-level input voltage	2	–	–	V	For 3.0–3.3V
VOL	Low-level output voltage	–	–	0.4	V	IOL = 2 mA
VOH	High-level output voltage	VDDO – 0.4	–	–	V	IOH = 2 mA
IOL	Low-level output current	–	–	3	mA	VOL = 0.25V
IOH	High-level output current	–	–	3	mA	VOH = IOVDD – 0.1
II	Input leakage current	–	–	0.25	µA	–
RPU	Pull-up resistor	–	60	–	kΩ	–
RPD	Pull-down resistor	–	60	–	kΩ	–

10.5 RF Specifications

Note: All data reported in this section are derived from system characterization.

10.5.1 Receiver

Table 19. Receiver RF Specifications

Property	Minimum	Typical[a]	Maximum[b]	Unit
Receiver Section				
Frequency range	2402	–	2480	MHz
Rx Sensitivity				
GFSK, 0.1% BER, 1 Mbps	–	–89.5	–	dBm
pi/4-DQPSK, 0.01% BER, 2Mbps	–	–91.5	–	dBm
8-DPSK, 0.01% BER, 3 Mbps	–	–85.5	–	dBm
Maximum input	–	–	–10.0[c]	dBm
Interference Performance				
C/I co-channel (GFSK, 0.1% BER)	–	–	11.0	dB
C/I 1 MHz adjacent channel (GFSK, 0.1% BER)	–	–	0.0	dB
C/I 2 MHz adjacent channel (GFSK, 0.1% BER)	–	–	–30.0	dB
C/I ³ 3 MHz adjacent channel (GFSK, 0.1% BER)	–	–	–40.0	dB
C/I image channel (GFSK, 0.1% BER)	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel (GFSK,0.1% BER)	–	–	–20.0	dB
C/I co-channel (pi/4-DQPSK, 0.1% BER)	–	–	13.0	dB
C/I 1 MHz adjacent channel (pi/4-DQPSK, 0.1% BER)	–	–	0.0	dB
C/I 2 MHz adjacent channel (pi/4-DQPSK, 0.1% BER)	–	–	–30.0	dB
C/I ³ 3 MHz adjacent channel (8-DPSK, 0.1% BER)	–	–	–40.0	dB
C/I image channel (pi/4-DQPSK, 0.1%BER)	–	–	–7.0	dB
C/I 1 MHz adjacent to image channel (pi/4-DQPSK,0.1% BER)	–	–	–20.0	dB
C/I co-channel (8-DPSK, 0.1% BER)	–	–	21.0	dB
C/I 1 MHz adjacent channel (8-DPSK, 0.1% BER)	–	–	5.0	dB
C/I 2 MHz adjacent channel (8-DPSK, 0.1% BER)	–	–	–25.0	dB
C/I ³ 3 MHz adjacent channel (8-DPSK, 0.1% BER)	–	–	–33.0	dB
C/I image channel (8-DPSK, 0.1% BER)	–	–	0.0	dB
C/I 1 MHz adjacent to image channel (8-DPSK,0.1% BER)	–	–	–13.0	dB
Out-of-Band Blocking Performance (CW)				
30 MHz to 2000 MHz, 0.1% BER	–	–10.0	–	dBm
2000 MHz to 2400 MHz, 0.1% BER	–	–27.0	–	dBm
2500 MHz to 3000 MHz, 0.1% BER	–	–27.0	–	dBm
3000 MHz to 12.75 GHz, 0.1% BER	–	–10.0	–	dBm

Table 19. Receiver RF Specifications (Cont.)

Property	Minimum	Typical[a]	Maximum[b]	Unit
Out-of-Band Blocking Performance (Modulated Interferer) Without Band-Pass Filter				
776 MHz to 794 MHz (CDMA)	–	–26.0	–	dBm
824 MHz to 850 MHz (CDMA)	–	–35.0	–	dBm
1850 MHz to 1910 MHz (CDMA)	–	–30.0	–	dBm
824 MHz to 850 MHz (EDGE/GSM)	–	–27.0	–	dBm
880 MHz to 915 MHz (EDGE/GSM)	–	–27.0	–	dBm
1710 MHz to 1785 MHz (EDGE/GSM)	–	–30.0	–	dBm
1850 MHz to 1910 MHz (EDGE/GSM)	–	–25.0	–	dBm
1920 MHz to 1980 MHz (WCDMA)	–	–31.0	–	dBm
1850 MHz to 1910 MHz (WCDMA)	–	–31.0	–	dBm
2500 MHz to 2570 MHz (WCDMA)	–	–35.0	–	dBm
Intermodulation Performance[d]				
BT, Delta f = 5 MHz	–39.0	–	–	dBm
Out-of-Band Spurious Emissions[e]				
30 MHz to 1 GHz	–	–85.0	–57.0	dBm
1 GHz to 12.75 GHz	–	–60.0	–47.0	dBm
Out-of-Band Spurious Emission Noise Floor[e]				
824 MHz to 850 MHz (EDGE/GSM)	–	–140.0	–	dBm/Hz
880 MHz to 915 MHz (EDGE/GSM)	–	–140.0	–	dBm/Hz
1710 MHz to 1785 MHz (EDGE/GSM)	–	–140.0	–	dBm/Hz
1850 MHz to 1910 MHz (EDGE/GSM)	–	–140.0	–	dBm/Hz
1920 MHz to 1980 MHz (WCDMA)	–	–140.0	–	dBm/Hz

a. Typical conditions are 1.2V operating voltage and 25°C ambient temperature.
b. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 2.1+EDR specification.
c. Applies for GFSK mode. Bluetooth specification is –20.0 dBm.
d. f0 = –64 dBm Bluetooth modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n × 1 MHz, where n is 3, 4, or 5. For the typical case, n = 5.
e. Conducted (RBW = 100 kHz), including baseband-radiated emissions.

10.5.2 Transmitter

Note: All data reported in this section are derived from system characterization.

Table 20. Transmitter RF Specifications[a]

Property	Minimum	Typical	Maximum	Unit
Transmitter Section				
Frequency range	2402	–	2480	MHz
Maximum output power (Class 2 with V12 pin power to VDDTF pin, with TCA and TSSI)	–3	2	4	dBm
Maximum output power (Class 1 with 3.3V to VDDTF pin, with TCA and TSSI)[b]	5	8	12	dBm
In-Band Spurious Emission				
±500 kHz	–	–	–20.0	dBc
1.0 MHz < |M – N| < 1.5 MHz (EDR only)	–	–	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz (EDR only)	–	–	–20.0	dBm
|M – N| > 2.5 MHz (EDR only)	–	–	–40.0[c]	dBm
Out-of-Band Spurious Emission				
30 MHz to 1 GHz	–	–80.0	–36.0[d]	dBm
1 GHz to 12.75 GHz	–	–	–30.0[e]	dBm
1.8 GHz to 1.9 GHz	–	–80.0	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–90.0	–47.0	dBm
GPS Band Spurious Emissions and Noise Floor[f]				
1572.92 MHz to 1577.92 MHz (without SAW filter)	–	–150	–124	dBm/Hz
1572.92 MHz to 1577.92 MHz (with SAW filter)	–	–162	–146	dBm/Hz
Out-of-Band Noise and Spurious Emission without Band-pass Filter at Front End[f]				
746 MHz to 764 MHz (CDMA)	–	– 78	–	dBm
851 MHz to 894 MHz (CDMA)	–	– 68	–	dBm
925 MHz to 960 MHz (GSM)	–	– 68	–	dBm
1805 MHz to 1880 MHz (GSM)	–	– 70	–	dBm
1930 MHz to 1990 MHz (CDMA)	–	– 73	–	dBm
2110 MHz to 2170 MHz (WCDMA)	–	– 73	–	dBm
Out-of-Band Spurious Emission Noise Floor[f]				
746 MHz to 764 MHz	–	–140	–130	dBm/Hz
851 MHz to 894 MHz	–	–140	–130	dBm/Hz
925 MHz to 960 MHz	–	–140	–130	dBm/Hz
1805 MHz to 1880 MHz	–	–140	–130	dBm/Hz
1930 MHz to 1990 MHz	–	–140	–130	dBm/Hz
2110 MHz to 2170 MHz	–	–140	–130	dBm/Hz

Table 20. Transmitter RF Specifications[a] (Cont.)

Property	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	130	180	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency drift				
DH1 packet	–	±20	±25	kHz
DH3 packet	–	±20	±40	kHz
DH5 packet	–	±20	±40	kHz
Drift rate	–	10	20	kHz/50 µs
Frequency deviation				
00001111 sequence in payload[g]	140	–	175	kHz
10101010 sequence in payload[h]	115	–	–	kHz
Channel spacing	–	1	–	MHz

a. Class 1 numbers are not tested in production screening.
b. For basic rate only.
c. Class 1 operation may need exceptions as allowed by Bluetooth specification.
d. Maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the 2.1+EDR specification. The spurious emissions during Idle Mode are the same as specified in Table 19 on page 29.
e. Filter may be needed for 2nd harmonic of RF.
f. Conducted (RBW = 100 kHz), including baseband-radiated emissions.
g. Average deviation in payload.
h. Maximum deviation in payload, for 99.9% of all frequency deviations.

10.6 Audio Specifications

Note: All data reported in this section are derived from system characterization.

10.6.1 Audio DAC

Table 21. Audio DAC Path Performance Specifications, 8 kHz Sample Rate

Property	Conditions	Minimum	Typical	Maximum	Unit
Full-scale output signal level	0 dB driver gain 1 kHz tone at 0 dBFS 32Ω line load	–	3.2	–	Vppd
Output driver capability	0 dB driver gain 1 kHz tone at 0 dBFS 32Ω load	–	30	–	mW (rms)
Output load impedance	Nominal speaker load	16	32	–	Ω
Driver gain range	Adjustable gain	–18	–	0	dB
Driver step sizes	–	–	3	–	dB
Absolute gain error	Over 0 to –18 dB driver gain 1 kHz tone	–	1	–	dB
Idle channel tone	0 dB driver gain, no signal 32Ω load	–	–	–95	dBc
SNR	0 dB driver gain A-weight 20 kHz BW 32Ω load	80	85	–	dB
Dynamic range	0 dB driver gain A-weight, 20 kHz BW 1 kHz tone at –60 dBFS 32Ω load	80	85	–	dB
Total harmonic distortion (THD) + N	Po= 24 mW 0 dB driver gain A-weight, 20 kHz BW 32Ω load	–	–	–70	dB
	Po= 3 mW, 0 dB driver gain A-weight 20 kHz BW 32Ω load	–	–	–62	dB

Notes:

- 2.7V analog supplies
- Fs = 8 kHz
- Entire DAC path, digital baseband input and differential analog output unless stated in the conditions.
- SNR is a measure of the difference in level between the full-scale output and the output with no signal applied. No auto-zero function is applied.
- Dynamic range is a measure of the difference between the highest and the lowest portion of a signal. Normally this is a THD + N measurement at 60 dB below full scale (referred to output). The measured signal is then corrected by adding 60 dB (for example, THD + N @ –60).
- THD + N is the ratio of the RMS values of noise + distortion and the signal.
- Idle channel tone is the relative power of the highest tone with respect to full-scale output when no signal is present at the input.

10.6.2 Audio ADC

Note: All data reported in this section are derived from system characterization.

Table 22. Audio ADC Performance—Microphone Path Specifications

Property	Conditions	Minimum	Typical	Maximum	Unit
Full-scale differential input voltage	Preamplifier gain = 42 dB, 1 kHz tone	–	16	–	mVppd
	Preamplifier gain = 21 dB, single-ended input, 1 kHz tone	–	180	–	Vppd
Input impedance, differential	From 21 dB to 42 dB gain settings, microphone mode	26	60	732	kΩ
Input capacitance	–	–	10	–	pF
Preamplifier gain	Gain adjustable	21	–	42	dB
Input referred noise voltage	Preamplifier gain = 42 dB, A-weight, 4 kHz BW	–	–	3	µVrms
	Preamplifier gain = 21 dB, A-weight, 4 kHz BW	–	–	4	dBc
Idle channel tone	Preamplifier gain = 42 dB, no input	–	–	–80	dBc
	Preamplifier gain = 21 dB, no input	–	–	–90	dBc
SNR	Preamplifier gain = 42 dB, A-weight, 4 kHz BW	–	69	–	dB
	Preamplifier gain = 21 dB, A-weight, 4 kHz BW	–	85	–	dB
Dynamic range	Preamplifier gain = 42 dB, A-weight, 4 kHz BW, 1 kHz tone at –60 dBFS	–	69	–	dB
	Preamplifier gain = 21 dB, A-weight, 4 kHz BW, 1 kHz tone at –60 dBFS	–	85	–	dB
THD + N	Preamplifier gain = 42 dB, A-weight, 4 kHz BW, 1 kHz tone at –10 dBFS	–	–	–55	dB
	Preamplifier gain = 21 dB, A-weight, 20 kHz BW, 1 kHz tone at –10 dBFS	–	–	–70	dB
Microphone bias voltage	3.0V supply available	2.1	–	2.4	V
Microphone bias current	–	–	–	2	mA
Microphone bias noise level	C-message weight	–	–	4	µVrms
Crosstalk between L and R channels	1 kHz tone at –10 dBFS	–	–	–50	dB

- 2.7V analog supplies
- Fs = 8 kHz
- Entire ADC path, differential analog input, and digital baseband output, unless stated in the conditions.

10.7 Timing and AC Specifications

10.7.1 Crystal Characteristics

Table 23. Crystal Requirement Characteristics

Property	Value	Unit
Frequency	26	MHz
Crystal load capacitance	10	pF
ESR	30 (maximum)	Ω
Power dissipation	200 (maximum)	µW
Frequency stability over temperature[a]	±20 PPM over –20 to 75°C	–
Overtone order	Fundamental	–

a. Frequency stability includes both initial tolerance and over temperature tolerance specs. It is combined into the 20 ppm.

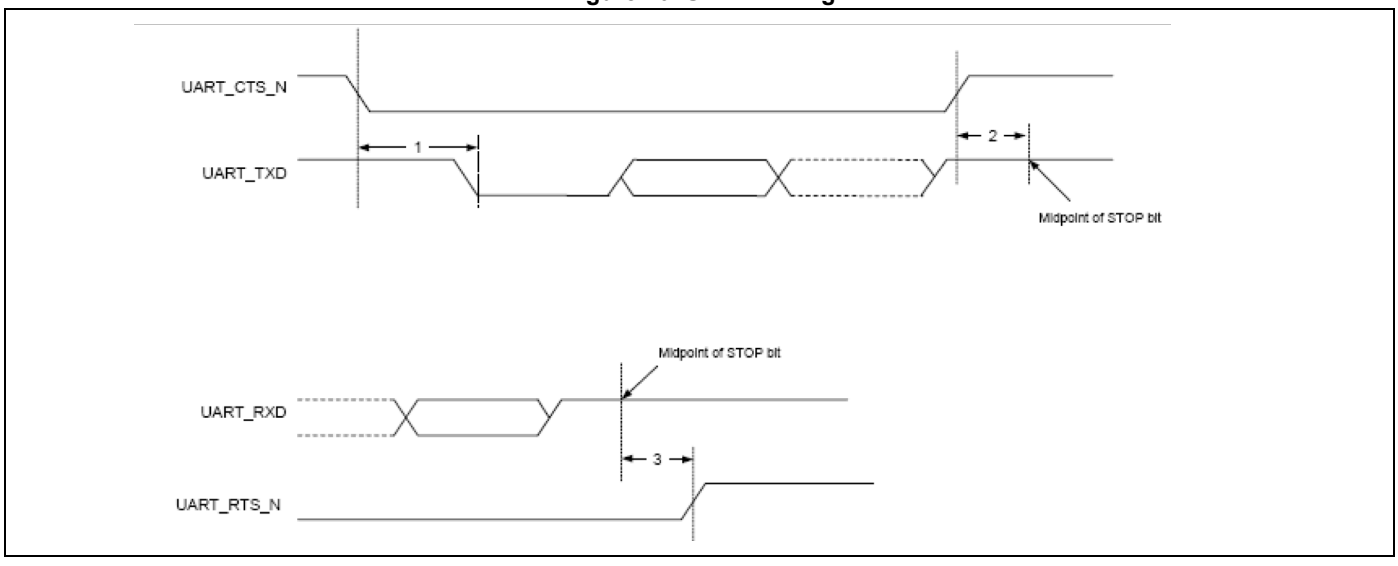
10.7.2 UART Timing

Note: The reference number specified in Table 24 corresponds to the reference numbers identified in Figure 10.

Table 24. UART Timing Specifications

Reference	Number	Conditions	Minimum	Typical	Maximum	Unit
1	Delay time	UART_CTS low to UART_TXD valid	–	–	24	Baudout cycles
2	Setup time	UART_CTS high before midpoint of stop bit	–	–	10	ns
3	Delay time	Midpoint of stop bit to UART_RTS high	–	–	2	Baudout cycles

Figure 10. UART Timing



10.7.3 BSC Interface Timing

Notes:

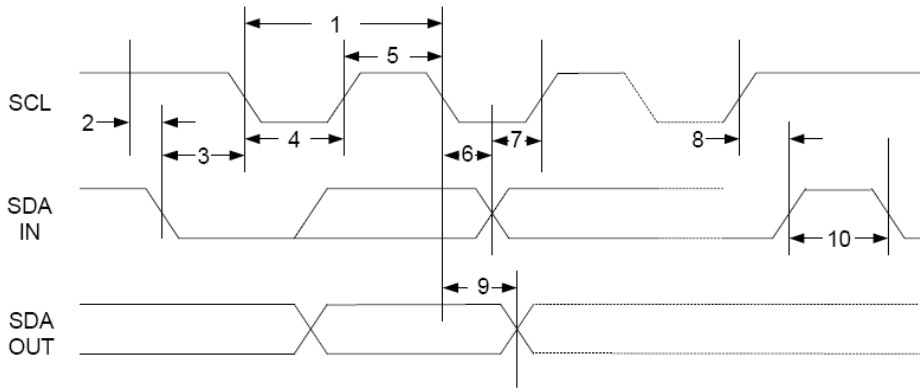
The Broadcom Serial Control (BSC) bus is Philips I^2C compatible.

The reference number specified in Table 25 corresponds to the reference numbers identified in Figure 11.

Table 25. BSC Interface Timing Specifications

Reference	Conditions	Minimum	Typical	Maximum	Unit
1	Clock frequency	–	100	–	kHz
		–	400	–	kHz
2	START condition setup time	650	–	–	ns
3	START condition hold time	280	–	–	ns
4	Clock low time	650	–	–	ns
5	Clock high time	280	–	–	ns
6	Data input hold time (As a transmitter, 300 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.)	0	–	–	ns
7	Data input setup time	100	–	–	ns
8	STOP condition setup time	280	–	–	ns
9	Output valid from clock	–	400	–	ns
10	Bus free time is the time that the cbus must be free before a new transaction can start.	650	–	–	ns

Figure 11. BSC Interface Timing Diagram



10.8 Power Consumption

Table 26. Power Supply Current (with a Nominal 3.7V Battery Voltage)

Operating Mode	Typical	Unit
Active mode (with 500 ms sniff interval)		
■ HV3	8.8	mA
■ 2EV3	7.6	mA
■ EV3	8.8	mA
A2DP active mode		
■ 44.1 kHz sampling rate, SBC (mono, 8 subbands, 16 blocks, 53 bit pool), 2DH5 packet type with 118 byte frame size	10	mA
Wideband speech active mode		
■ 2EV3 eSCO	8.3	mA
Standby mode		
■ Single HFP Sniff (640 ms interval)	200	µA
■ Single HFP Sniff (500 ms interval)	207	µA
■ Dual HFP Sniff (640 ms interval)	286	µA
■ Dual HFP Sniff (500 ms interval)	292	µA
Deep Sleep (off) mode	3.0	µA

Notes:

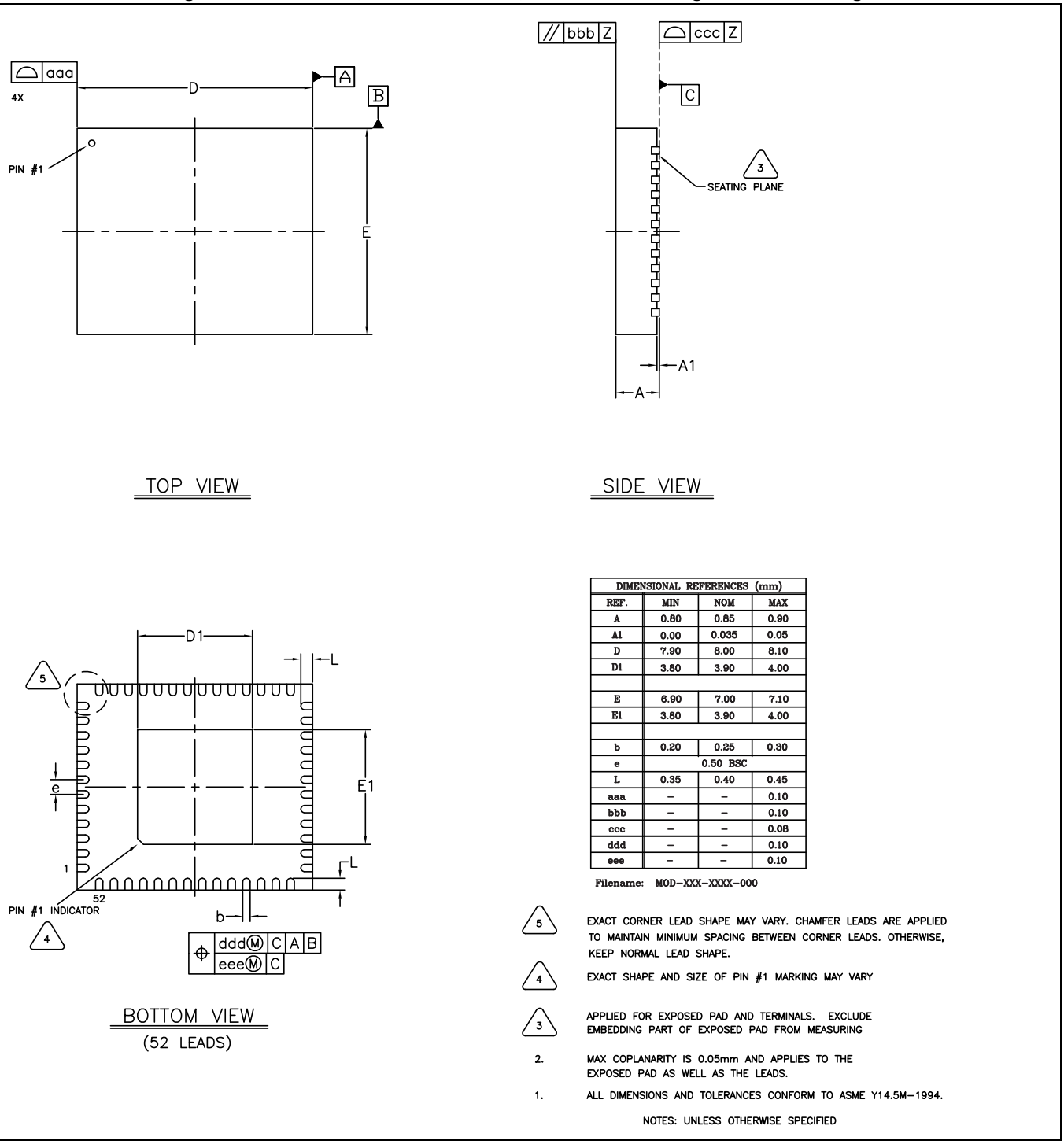
- The currents are measured without audio running.
- The currents are measured with Cypress generic MMI, and LEDs are off.
- The standby current is measured with the device operating in Slave mode.

Note:

For more information about measuring power consumption, refer to Power Consumption Measurements, Broadcom document number 2074X-AN50x-R.

11. Mechanical Specification

Figure 12. CYW20745, 8.0 mm × 7.0 mm, 52-Pin QFN Package Outline Drawing



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
D	7.90	8.00	8.10
D1	3.80	3.90	4.00
E	6.90	7.00	7.10
E1	3.80	3.90	4.00
b	0.20	0.25	0.30
e		0.50 BSC	
L	0.35	0.40	0.45
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.10
eee	–	–	0.10

Filename: MOD–XXX–XXXX–000

5 EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.

4 EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY

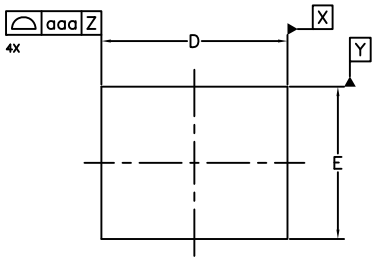
3 APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING

2. MAX COPLANARITY IS 0.05mm AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.

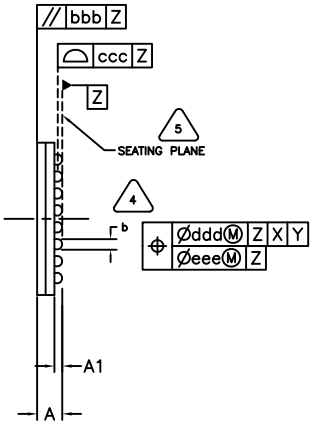
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

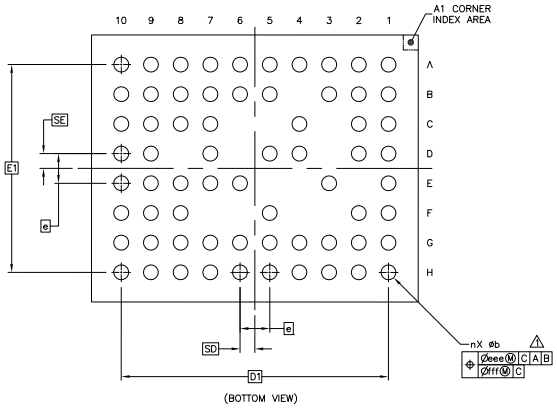
Figure 13. CYW20745, 5.5 mm × 4.5 mm, 66-Ball WFBGA Package Outline DrawingTape and Reel Specification



TOP VIEW



SIDE VIEW



BOTTOM VIEW

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.90
A1	0.15	0.18	0.21
D	5.40	5.50	5.60
D1		4.50 BSC	
E	4.40	4.50	4.60
E1		3.50 BSC	
b	0.20	0.25	0.30
e		0.50 BSC	
f	–	0.5	–
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.05
eee	–	–	0.05

Filename: tbd

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.50mm

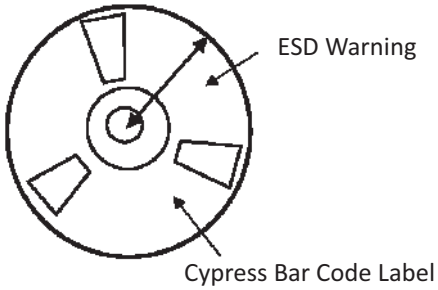
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–207.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

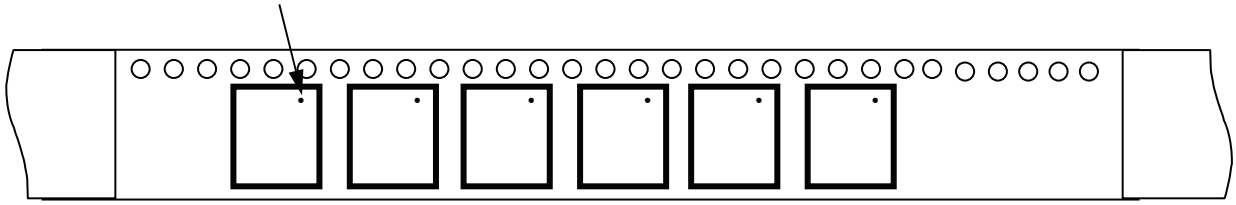
11.1 Tape and Reel Specification

Figure 14. Reel/Labeling/Packing Specification



Device Orientation/Mix Lot Number:
Each reel may contain up to three individual lot numbers; this is independent of date code.
These individual lots must be labeled on the box, moisture barrier bag and reel.

Pin 1: Top right corner, top of package, toward sprocket holes



Moisture Barrier Bag Contents/Label:
Desiccant pouch (minimum 1)
Humidity indicator (minimum 1)
Reel (maximum 1)

12. Ordering Information

Part Number	Description	Delivery	Operating Temperature
CYW20745A0KMLGT	Wireless audio processor	Tape/Reel (2000 K per reel)	–30°C to 85°C
CYW20745A0KMLG	Wireless audio processor	–	–30°C to 85°C
CYW20745A0KFBGT	Wireless audio processor	Tape/Reel (3000 K per reel)	–30°C to 85°C
CYW20745A0KFBG	Wireless audio processor	–	–30°C to 85°C

12.1 References

The references in this section may be used in conjunction with this document.

Note: Cypress provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see IoT Resources).

For Cypress documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Broadcom Number	Cypress Number	Source
Power Consumption Measurement	2074X-AN5xx-R	002-14900	community.cypress.com
UART Communication Over USB Connector	2074X-AN6xx-R	-	community.cypress.com
Bluetooth Headset Charger Design and Tuning	2074X-AN7xx-R	-	community.cypress.com

Document History

Document Title: CYW20745 ROM-Based Single Microphone Headset IC With Voice Command Recognition Document Number: 002-14900				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	9/3/10	20745-DS00-R Initial release
*A	–	–	8/2/11	20745-DS01-R **Added:** • "A2DP Codec" on page 17. **Updated:** • Table 12, "Switching Regulator Characteristics," on page 27. • Table 13, "Battery Charger," on page 27. • Table 20, "Transmitter RF Specifications," on page 31. • Table 23, "Crystal Requirement Characteristics," on page 35. • Table 26, "Power Supply Current (with a Nominal 3.7V Battery Voltage)," on page 37.
*B	5475002	UTSV	10/14/16	Updated to Cypress Template
*C	5962489	AESATMP9	11/09/2017	Updated logo and copyright.

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