# CS8312

# IGBT Ignition Predriver with Dynamic Current Regulation

The CS8312 is a bipolar microprocessor interface IC designed to drive an IGBT (or logic level MOSFETs) powering large inductive loads in harsh operating environments. The IC's dynamic current limit function lets the microprocessor adjust the current limit threshold to the real time needs of the system.

CLI, the current limit input, sets the current limit for the IGBT high or low as directed by the system microprocessor. CLI also raises and lowers the threshold on the diagnostic FLAG output signal. The FLAG output signals the microprocessor when the current level approaches current limit on the IGBT. The CTRL input enables the FLAG function.

### Features

- μP Compatible Inputs
- Adjustable Current Limit Thresholds
- External Sense Resistor
- Flag Signal to Indicate Output Status

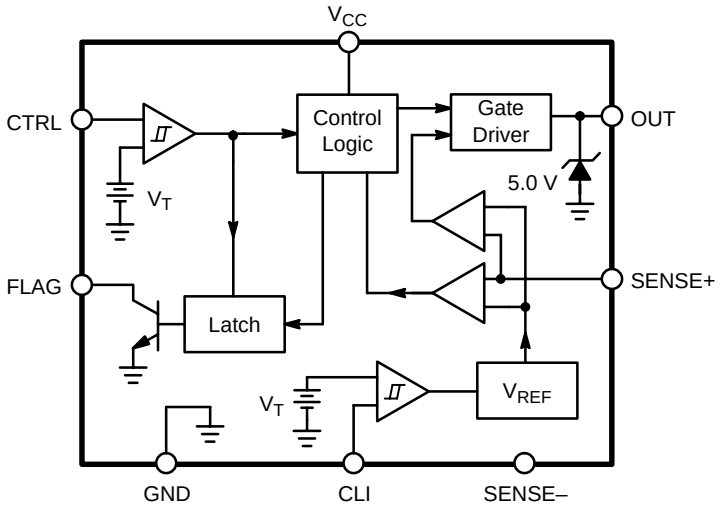
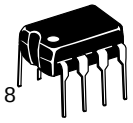



**Figure 1. Block Diagram**

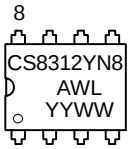
ON Semiconductor™

http://onsemi.com



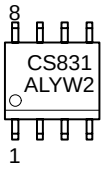

**DIP–8**
**N SUFFIX**
**CASE 626**

**MARKING DIAGRAMS**



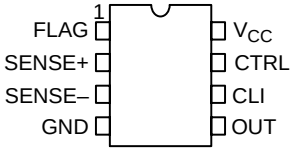


**SO–8**
**D SUFFIX**
**CASE 751**




A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

**PIN CONNECTIONS**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| CS8312YN8 | DIP–8 | 50 Units/Rail |
| CS8312YD8 | SO–8 | 95 Units/Rail |
| CS8312YDR8 | SO–8 | 2500 Tape & Reel |

## ABSOLUTE MAXIMUM RATINGS*

| Rating | | Value | Unit |
|---|---|---|---|
| Supply Voltage | | –0.3 to 12 | V |
| Digital Input Currents | | 2.0 | mA |
| Internal Power Dissipation ($T_A$ = 25°C) | | 700 | mW |
| Junction Temperature Range | | –40 to +150 | °C |
| Storage Temperature Range | | –55 to +165 | °C |
| Electrostatic Discharge (Human Body Model) | | 2.0 | kV |
| Lead Temperature Soldering | Wave Solder (through hole styles only) Note 1.<br>Reflow (SMD styles only) Note 2. | 260 peak<br>230 peak | °C<br>°C |

1. 10 seconds max.
2. 60 seconds max above 183°C

*The maximum package power dissipation must be observed.

## ELECTRICAL CHARACTERISTICS (7.0 V ≤ $V_{CC}$ ≤ 10 V, –40°C ≤ $T_A$ ≤ 125°C, –0.2 V ≤ Differential Ground Voltage ≤ 0.8 V; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Power Supply Including Ripple Voltage | – | 7.0 | – | 10 | V |
| Supply Ripple Frequency | – | 10 | – | 60 | kHz |
| Differential Ground Frequency | – | 10 | – | 60 | kHz |
| Quiescent Current, $I_Q$<br>Turn On<br>Turn Off | <br>$V_{CTRL}$ = 5.5 V<br>$V_{CTRL}$ = –0.3 V | <br>–<br>– | <br>–<br>– | <br>15<br>5.0 | <br>mA<br>mA |
| Supply Voltage Rejection | $V_{CTRL}$ = 5.5 V | 30 | – | – | dB |
| Differential Ground Rejection Ratio | $V_{CTRL}$ = 5.5 V | 30 | – | – | dB |
| Differential Ground Current Ratio | $V_{CTRL}$ = –0.3 V,<br>($V_{SENSE–}$ – $V_{GND}$)DC = 1.0 V<br>($V_{SENSE–}$ – $V_{GND}$)AC = 0.6 V | – | – | 3.0 | mA |
| Unity Gain Bandwidth | $V_{CTRL}$ = 5.5 V | 400 | – | – | kHz |
| Turn On Delay | CTRL Increasing | – | – | 30 | µs |
| Turn Off Delay | CTRL Decreasing | – | – | 30 | µs |
| **Control Function** | | | | | |
| Input Voltage Range | $I_{CTRL}$ = 2.0 mA | –0.3 | – | 5.5 | V |
| Input Threshold<br>Turn On<br>Turn Off<br>Hysteresis | <br>CTRL Increasing<br>CTRL Decreasing | <br>–<br>1.5<br>0.4 | <br>–<br>–<br>– | <br>3.5<br>–<br>2.0 | <br>V<br>V<br>V |
| Voltage | $I_{CTRL}$ = 10 µA max | – | – | 1.1 | V |
| Input Capacitance | – | – | – | 50 | pF |
| **Current Limit Increase Function** | | | | | |
| Input Voltage Range | $I_{CTRL}$ = 2.0 mA | –0.3 | – | 5.5 | V |
| Input Threshold<br>Turn On<br>Turn Off<br>Hysteresis | <br>CLI Increasing<br>CLI Decreasing | <br>–<br>1.5<br>0.4 | <br>–<br>–<br>– | <br>3.5<br>–<br>2.0 | <br>V<br>V<br>V |
| Voltage | $I_{CLI}$ = 10 µA max | – | – | 1.1 | V |

**ELECTRICAL CHARACTERISTICS (continued)** (7.0 V ≤ $V_{CC}$ ≤ 10 V, –40°C ≤ $T_A$ ≤ 125°C, –0.2 V ≤ Differential Ground Voltage ≤ 0.8 V; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Current Limit Increase Function (continued)** | | | | | |
| Input Capacitance | – | – | – | 50 | pF |
| **Output Stage** | | | | | |
| $I_{OUT}$ | – | – | – | 5.0 | mA |
| Clamp Voltage | $V_{CTRL}$ = 5.5 V, $I_{OUT}$ = 1.0 mA | 4.0 | – | 5.5 | V |
| Output Off Voltage | $V_{CTRL}$ = –0.3 V, $I_{OUT}$ = 10 μA<br>$V_{CTRL}$ = –0.3 V, $I_{OUT}$ = 200 μA | –<br>– | –<br>– | 0.5<br>1.2 | V<br>V |
| **Flag Function** | | | | | |
| Output Low | $V_{CTRL}$ = 5.5 V, $I_{FLAG}$ = 1.5 mA | – | – | 0.9 | V |
| Leakage Current | $V_{CTRL}$ = –0.3 V | – | – | 10 | μA |
| Output Capacitance | – | – | – | 50 | pF |
| Turn On ($V_{SENSE+}$ – $V_{SENSE–}$) | $V_{CTRL}$ = 5.5 V, $V_{CLI}$ = –0.3 V<br>$V_{CTRL}$ = 5.5 V, $V_{CLI}$ = 5.5 V | 210<br>300 | 225<br>– | 240<br>350 | mV<br>mV |
| Turn Off Delay | CTRL Decreasing | – | – | 10 | μs |
| Turn On Delay | – | – | – | 10 | μs |
| Disable Time | – | 100 | – | 450 | μs |
| **Sense Function** | | | | | |
| Input Voltage Range | – | –0.3 | – | 2.5 | V |
| Sense Regulation Voltage | $V_{CTRL}$ = 5.5 V, $V_{CLI}$ = –0.3 V<br>$V_{CTRL}$ = 5.5 V, $V_{CLI}$ = 5.5 V | 270<br>380 | 295<br>410 | 320<br>440 | mV<br>mV |
| Input Leakage Current | $V_{CTRL}$ = 5.5 V | – | – | 5.0 | μA |
| Propagation Delay | $V_{CTRL}$ = 5.5 V | – | – | 20 | μs |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN # | | PIN SYMBOL | FUNCTION |
|---|---|---|---|
| DIP–8 | SO–8 | | |
| 1 | 1 | FLAG | Indicates whether current through the IGBT has reached a pre-set level. |
| 2 | 2 | SENSE+ | Positive input to current comparator. |
| 3 | 3 | SENSE– | Ground (SENSE–) for current sense resistor. |
| 4 | 4 | GND | Ground connection. |
| 5 | 5 | OUT | Output voltage to IGBT (MOSFET) gate. |
| 6 | 6 | CLI | Current limit input increase. |
| 7 | 7 | CTRL | Control input. |
| 8 | 8 | $V_{CC}$ | Supply voltage. |

## CIRCUIT DESCRIPTION

### Flag Function (See Figure 2)

The flag indicates when the voltage across the two sense pins is approaching a current limit level that has been determined by the value of the external sense resistor ($R_{SENSE}$) and the state of the CTRL and CLI pins. If the voltage across the sense pins (SENSE+, SENSE–) is less than the flag turn–on voltage, then the FLAG is off. When the voltage between the sense pins equals the FLAG turn on voltage, the FLAG will latch on until the CTRL pin goes low. FLAG is disabled whenever CTRL is low. Changing the CLI pin from low to high will increase nominal FLAG turn on voltage by approximately 45%.

**Table 1. FLAG Timing Sequence**

| State | CONTROL | SENSE+ | FLAG |
|---|---|---|---|
| 0 | Low | X | OFF |
| 1 | High | Below Threshold | OFF |
| 2 | High | Above Threshold | ON |
| 3 | High | X | ON |
| 0 | Low | X | OFF |

### Output Stage

The CS8312 output (OUT) saturates and supplies voltage to the IGBT (or MOSFET) gate once the CTRL switches from low to high. As current through the IGBT (MOSFET) increases and the voltage across the sense resistor passes the flag turn on voltage, the FLAG will turn on. If the current through the sense resistor continues to rise and the sense resistor voltage reaches the regulation sense voltage, then the gate voltage will fall to a level that regulates the driver and maintains the regulation sense voltage at the sense resistor.

### Current Limit Function

Changing the CLI pin from a logic low to a logic high increases the FLAG turn on voltage by approximately 45% and the regulation sense voltage by approximately 39% respectively.

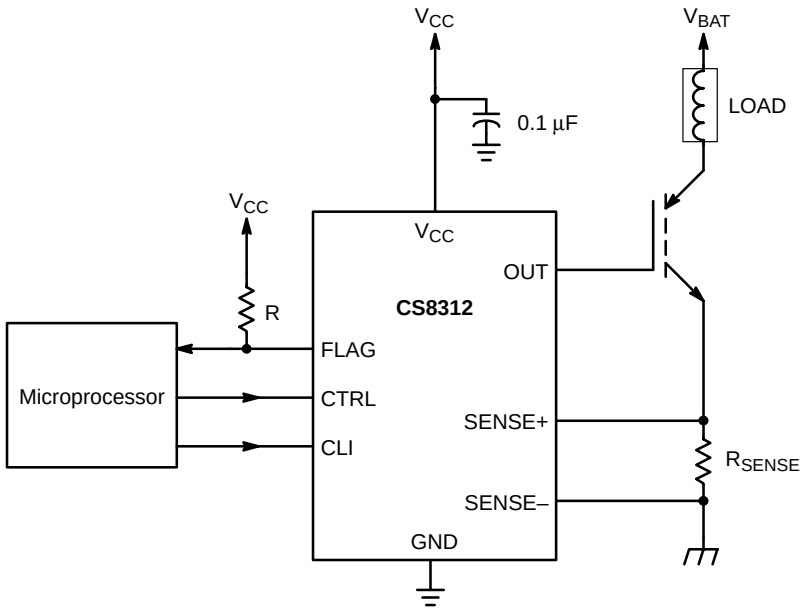



**Figure 2. Application and Test Diagram**

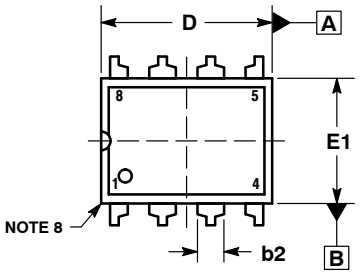
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

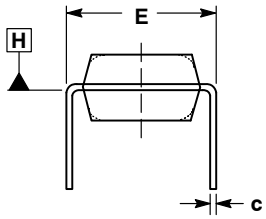
SCALE 1:1

**PDIP–8**
CASE 626–05
ISSUE P

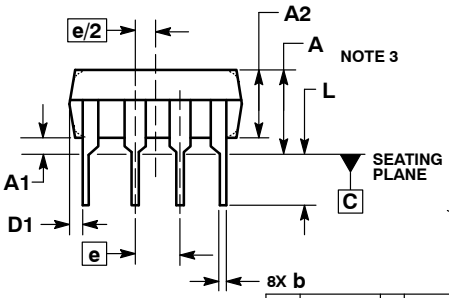
DATE 22 APR 2015



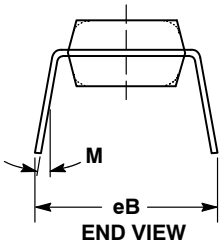

TOP VIEW




END VIEW
WITH LEADS CONSTRAINED
NOTE 5




SIDE VIEW



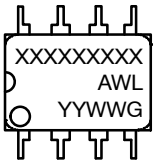

END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | ---- | 0.210 | --- | 5.33 |
| A1 | 0.015 | ---- | 0.38 | --- |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.35 | 0.56 |
| b2 | 0.060 TYP | | 1.52 TYP | |
| C | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.355 | 0.400 | 9.02 | 10.16 |
| D1 | 0.005 | ---- | 0.13 | --- |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| eB | ---- | 0.430 | --- | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| M | ---- | 10° | --- | 10° |

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. $V_{CC}$

### GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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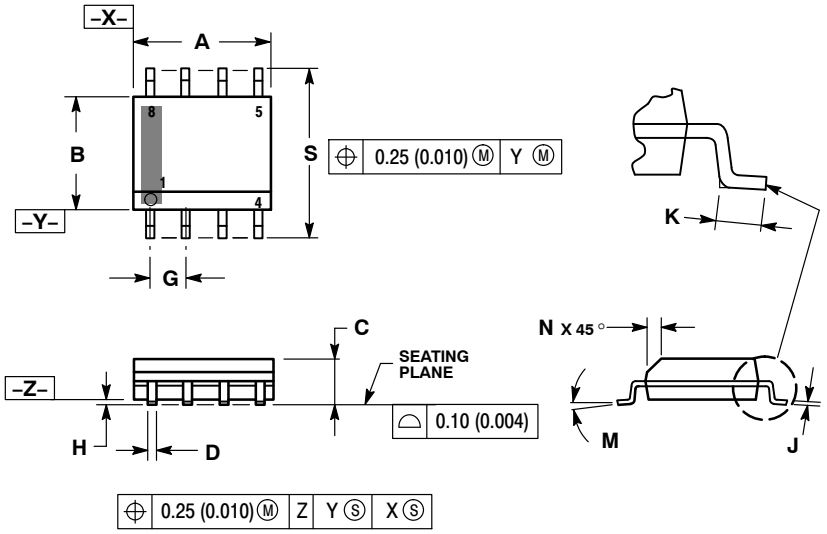
|---|---|---|
| DESCRIPTION: | PDIP–8 | PAGE 1 OF 1 |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

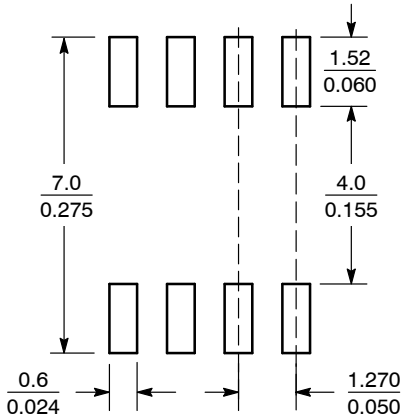
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

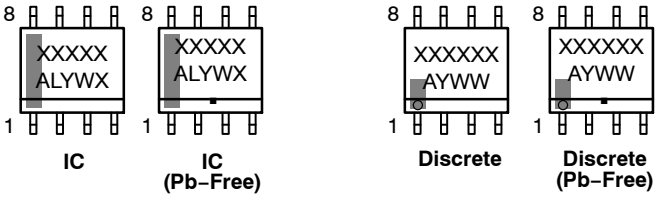
### SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SOIC−8 NB** | **PAGE 1 OF 2** |

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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