Texas Instruments

TMS320 Cross-Platform Daughtercard Adapter

User's Guide

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the TMS320 cross-platform daughtercard adapter. A complete circuit description as well as schematic diagram and bill of materials are included. A newly revised specification, the *TMS320 Cross-Platform Daughtercard Specification* (Document No. SPRA711) has been adopted by the DSP Group. This new specification will ensure that future DSP evaluation board products follow a set standard. The Data Converter Applications Group is committed to follow this new specification when designing data converter *daughtercard* evaluation modules.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Overview
- Chapter 2—Physical Description
- Chapter 3—EVM Operation

Related Documentation

To obtain a copy of the following TI document, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, please identify this booklet by its title and literature number. Updated TI documents can also be obtained through our website at www.ti.com. The Xlinx website is also listed for your convenience in obtaining documentation on the XC9572.

Data Sheets:	**Literature Number:**
XC9572 In-System Programmable CPLD	www.xilinx.com/partinfo/9572.pdf
Application Reports:	
TMS320 Cross-Platform Daughtercard Specification	SPRA711

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If you have questions about this or other Texas Instruments Data Converter evaluation modules, send an e-mail message to the Data Converter Application Team at dataconvapps@list.ti.com. Include product your question concerns in the subject heading.

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Chapter 1

EVM Overview

This chapter provides an overview of the evaluation module.

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1.1 Adapter Card Purpose

As the DSP evaluation platforms from Texas Instruments have evolved, minor differences have developed in the signal chain to the 80-pin interface connectors. A newly revised specification, the *TMS320 Cross-Platform Daughtercard Specification* (Document No. SPRA711) has been adopted by the DSP Group. This new specification will ensure that future DSP evaluation board products follow a set standard. The Data Converter Applications Group is committed to follow this new specification when designing data converter *daughtercard* evaluation modules. The adapter card design allows flexibility in resolving some of the known platform-specific differences. The primary features of the adapter are discussed in the following paragraphs.

1.2 C5402 Users

The *TMS320 Cross-Platform Daughtercard Specification* recommends using address lines DC_A[2:5] for accessing daughtercards. This correlates to A[0:3] on existing C5402 platforms. This requirement poses a problem to C5402 users due to the DSP CPLD which resides in the same area. Parallel data converter EVMs that comply with SPRA711 can use this adapter card to move the daughtercard address lines from DC_A[2:5] to A[12:15] by setting the appropriate switches on the adapter card. The PLD on the adapter card reroutes the address lines from the DSP to the EVM.

1.3 C6211 Users

The C6211 EVM uses the first serial port instance for an onboard codec. Most currently-used data converter evaluation modules that feature a serial interface use the first serial port when interfacing to the DSP. By setting appropriate switches on the adapter card, the seven signals associated with Port 1 are swapped with the seven signals associated with Port 2.

1.4 Additional Adapter Card Features

This EVM features an XC9752-84C in-circuit programmable logic device from Xilinx Corporation. The CPLD allows the adapter card user to swap the serial port signals from several different TMS320 DSP development boards to a data converter EVM.

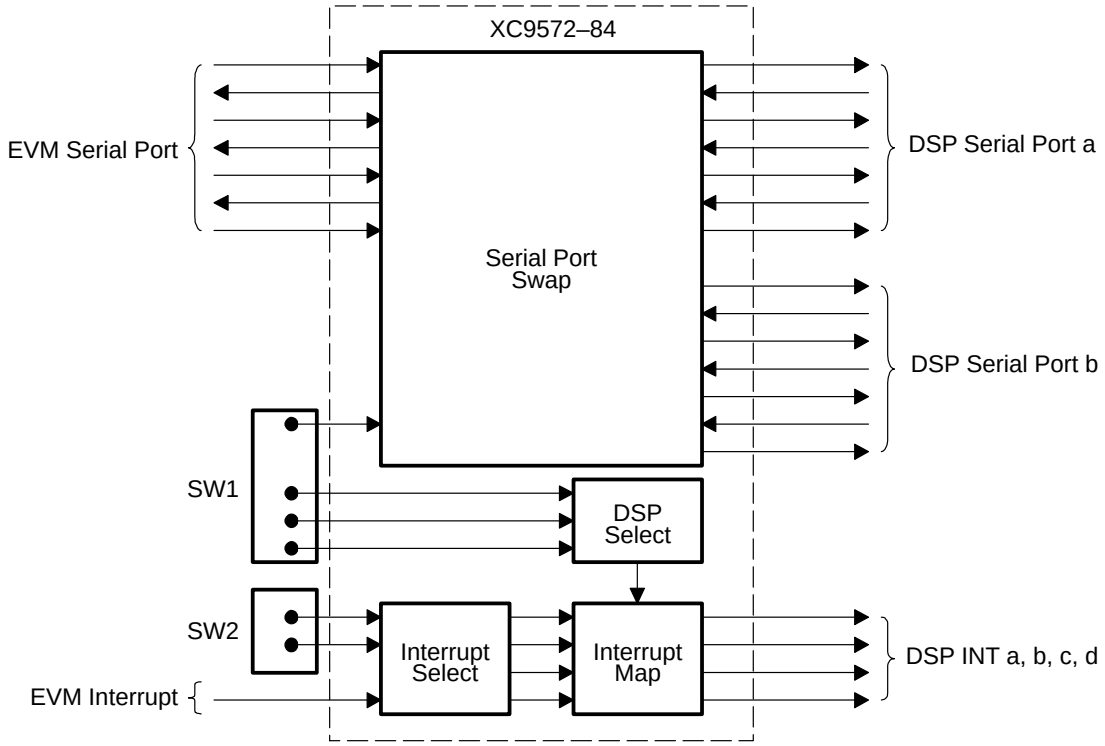
The EVM also features a three-bit DSP selection switch to align the interrupt from the data converter EVM to INT 7 on the C6201, C6202, C6211 and C6711 DSPs, or INT 0 on the C5402 development systems. A two-bit interrupt selection switch allows the interrupt from the data converter EVM to be mapped to interrupts 7, 6, 5, or 4 on the C6XXX or 0, 1, 2, or 3 on the C5402 systems.

Both male and female connectors are installed on the EVM. This allows the adapter card to connect between the DSP and data converter boards. Signals not re-routed by the CPLD are passed directly from the DSP, through the adapter card, to the data converter EVM.

1.5 CPLD Block Diagram

The CPLD on the adapter card contains 3 primary function blocks that control the routing of signals from the DSP connector (bottom side) to the EVM connector (topside). Two switch banks on the card provide the necessary control signals to the PLD. SW1 is a four-bit SPST switch that controls serial port swapping and DSP selection. SW2 is a two-bit SPST switch that provides a one-of-four selection of the incoming interrupt to the DSP for data converters with an interrupt output signal.

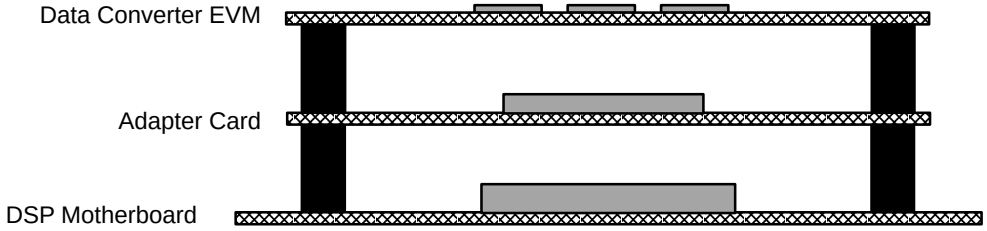
Figure 1–1. Block Diagram



1.6 Board Installation

The TMS320 cross-platform daughtercard adapter is designed to be used in conjunction with the data converter evaluation modules from Texas Instruments. The adapter card has male connectors on the bottom side of the board which plug directly into most DSP Evaluation platforms designed to either the SPRA478 or SPRA711 specifications. Female connectors are located on the top side of the adapter card allowing direct plug-in of a variety of daughtercards.

Figure 1–2. Board Installation



1.7 SW1—Serial Swap

Switch 1, position 1 determines the serial port that is routed to the EVM under test. In the default mode, SW1–1 is in the OFF position and the serial signals associated with DSP Port *a* and Port *b* are fed directly through the adapter card to the EVM under test. Since all seven signals associated with either port are routed through the CPLD, any delay in signal transfer should be uniform.

When SW1–1 is moved to the ON position, the CPLD performs a 1:1 swap of all serial lines associated with ports *a* and *b*. Table 1–1 shows an example of the serial line mapping.

Table 1–1. Port Swap via SW1

SW1–1	Serial Port *a*		Serial Port *b*	
	EVM Connections	**DSP Connections**	**EVM Connections**	**DSP Connections**
OFF	EVM_CLKXa	DC_CLKXa	EVM_CLKXb	DC_CLKXb
	EVM_CLKRa	DC_CLKRa	EVM_CLKRb	DC_CLKRb
	EVM_DXa	DC_DXa	EVM_DXb	DC_DXb
	EVM_DRa	DC_DRa	EVM_DRb	DC_DRb
	EVM_FSXa	DC_FSXa	EVM_FSXb	DC_FSXb
	EVM_FSRa	DC_FSRa	EVM_FSRb	DC_FSRb
	EVM_CLKSa	DC_CLKSa	EVM_CLKSb	DC_CLKSb
ON	EVM_CLKXb	DC_CLKXa	EVM_CLKXa	DC_CLKXb
	EVM_CLKRb	DC_CLKRa	EVM_CLKRa	DC_CLKRb
	EVM_DXb	DC_DXa	EVM_DXa	DC_DXb
	EVM_DRb	DC_DRa	EVM_DRa	DC_DRb
	EVM_FSXb	DC_FSXa	EVM_FSXa	DC_FSXb
	EVM_FSRb	DC_FSRa	EVM_FSRa	DC_FSRb
	EVM_CLKSb	DC_CLKSa	EVM_CLKSa	DC_CLKSb

1.8 SW1—DSP Selection

Switch 1, positions 2, 3, and 4 control the DSP selection. This allows the interrupt from data converter EVMs to default to INT 7 across the C6000 DSP platforms. The C6201 and C6202 DSP EVMs assign interrupt 7 to pin 53 of the peripheral connector, while the C6211 and C6711 assign interrupt 7 to pin 68. The DSP selection switch simply maps the EVM interrupt to INT 7 regardless of the DSP platform. The exception to this is the C5402 DSK. This DSP EVM refers to pin 53 as INT 0.

The schematic for the adapter card refers to the nomenclature used in *The TMS320 Cross-Platform Daughtercard Specification* (Document No. SPRA711). Table 1–2 shows the DSP code and resulting interrupt mapping.

Table 1–2. DSP Selection

EVM	SPRA711	C5402	C6201	C6202	C6211	C6711
INT out (pin 53)	INT *a* (pin 53)	INT 0 (pin 53)	INT 7 (pin 53)	INT 7 (pin 53)	INT 7 (pin 68)	INT 7 (pin 68)
	INT *b* (pin 48)	INT 1 (pin 48)	Hi-Z	INT 6 (pin 48)	INT 6 (pin 67)	INT 6 (pin 67)
	INT *c* (pin 67)	INT 2 (pin 67)	Hi-Z	INT 5 (pin 67)	INT 5 (pin 48)	INT 5 (pin 48)
	INT *d* (pin 68)	INT 3 (pin 68)	Hi-Z	INT 4 (pin 68)	INT 4 (pin 53)	INT 4 (pin 53)
DSP Code	**000**	**001**	**010**	**011**	**100**	**101**

1.8.1 C5402 Selection

When the DSP selection switches are set to 001, the CPLD redirects address lines A15, A14, A13, and A12 from the C5402 DSP expansion connector (pins 7, 8, 9, and 10) to the EVM connector locations A5, A4, A3, and A2 (pins 23, 24, 25, and 26*)*.

Note:

The signals on the expansion connector pins 7, 8, 9, and 10 are referred to as A17, A16, A15, and A14 on the C6000 Series DSP boards.

1.9 SW2—INT Selection

Switch 2 allows the adapter card user to re-map the interrupt from the data converter EVM to any of four possible interrupts on the DSP. Table 3 shows the relative mapping.

Table 1–3. INT Selection

EVM	Code	SPRA711	C5402	C6201	C6202	C6211	C6711
INT *a* (pin 53)	00	INT *a* (pin 53)	INT 0 (pin 53)	INT 7 (pin 53)	INT 7 (pin 53)	INT 7 (pin 68)	INT 7 (pin 68)
	01	INT *b* (pin 48)	INT 1 (pin 48)	Hi-Z	INT 6 (pin 48)	INT 6 (pin 67)	INT 6 (pin 67)
	10	INT *c* (pin 67)	INT 2 (pin 67)	Hi-Z	INT 5 (pin 67)	INT 5 (pin 48)	INT 5 (pin 48)
	11	INT *d* (pin 68)	INT 3 (pin 68)	Hi-Z	INT 4 (pin 68)	INT 4 (pin 53)	INT 4 (pin 53)

1.10 Power Requirements

No external power connections are required for the adapter card. The 5 V DSP supply is used as the VCC source for the CPLD.

1.11 VCC I/O Selection

Jumper W1 provides power to the VCC input/output pins of the CPLD. Placing a shunt jumper across pins 1–2 provides 3.3 V from the DSP motherboard to the VCCI/O pins. Placing the W1 jumper across pins 2–3 provides 5 V to the VCCI/O voltage pins. The default mode is pins 2–3 shorted.

Chapter 2

Physical Description

This chapter describes the PCB layout and provides a bill of material and schematic of the EVM.

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2.1 PCB Layout

The EVM is constructed on a two-layer printed-circuit board using FR-4 material. Dimensions are 203,7-mm (8.02 inch) x 86,1-mm (3.39 inch) x 1,57-mm (0.062 inch) thick. The assembly and individual artwork layers are shown in the following figures.

Figure 2–1. PCB Screen

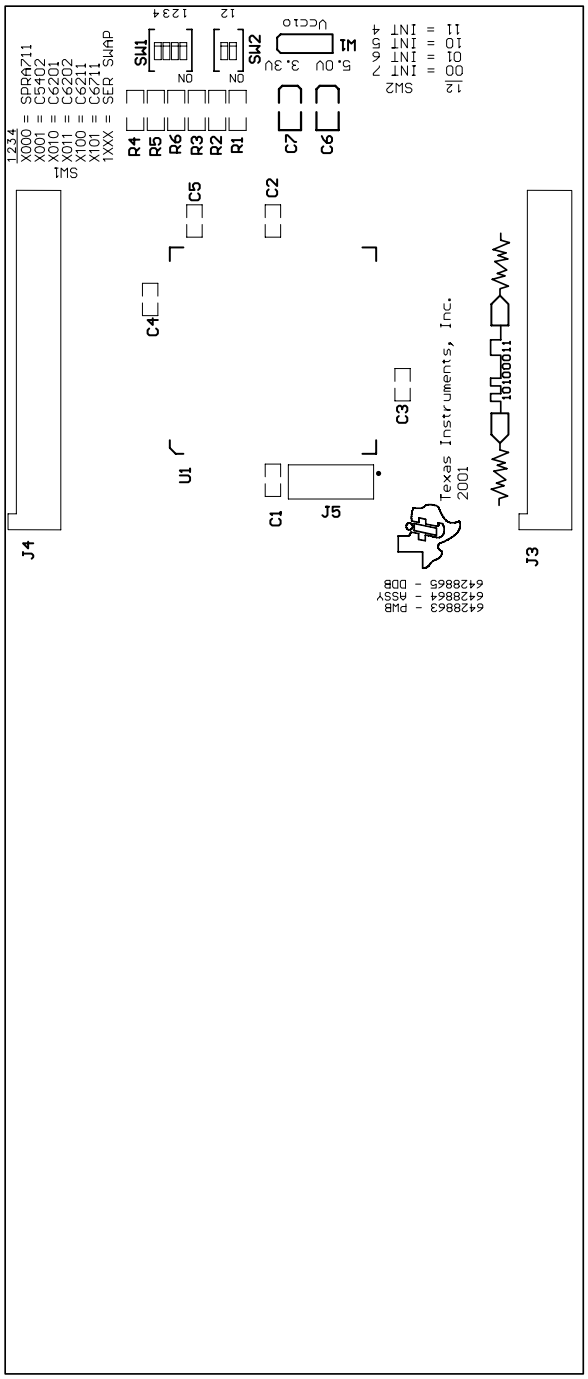


Figure 2–2. PCB Layer 1

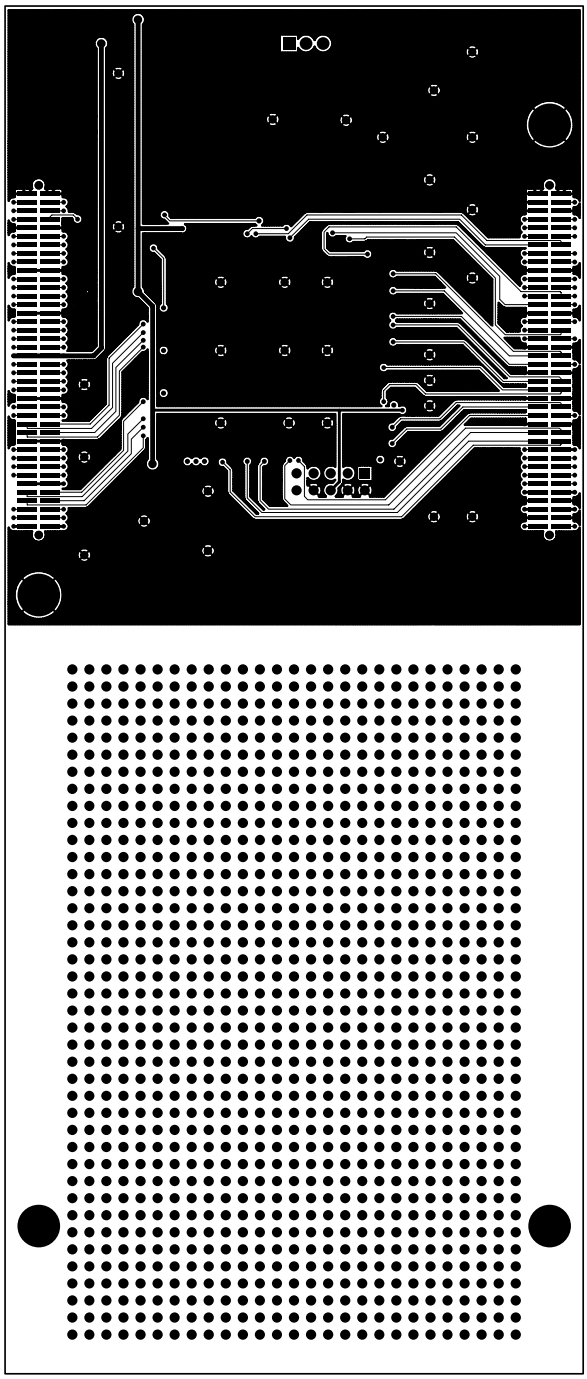
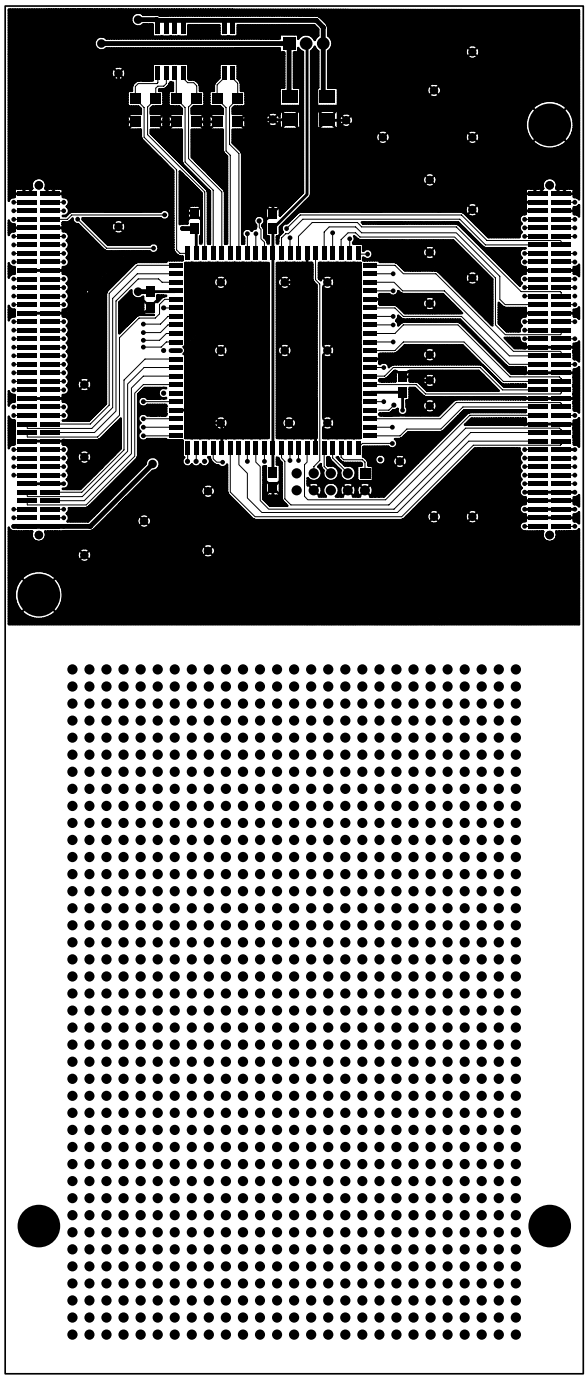


Figure 2–3. PCB Layer 2



2.2 Parts List

Table 2–1 shows the reference designator, manufacturer and part number of the components associated with the adapter card.

Table 2–1. EVM Bill of Materials List

Qty.	Reference Designator	Value	Supplier	Part No.
3	C1 C2 C3 C4 C5	0.1 μF	Panasonic	ECJ–2YB1H103K
4	R1 R2 R3 R4 R5 R6	33 μF	Panasonic	ERJ–8GEYJ103V
2	SW2	2-Position, SPST	CTS	218–2LPST
4	C6 C7	10 μF, 10 V, tantalum	Panasonic	
1	W1	3-Pin jumper	Samtec	TSW–103–07–L–S
15	SW1	4-Position, SPST	CTS	218–4LPST
2	J5	5-Position, dual row header	Samtec	TSW–103–07–L–D
1	U1	CPLD	Xilinx	XC9572–15PC84C
1	J3 J4	80 Pin SMT female	Samtec	SFM–140–L2–S–D–LC
1	J1 J2	80 Pin SMT male	Samtec	TFM–140–32–S–D–LC

Chapter 3

EVM Operation

This chapter describes the operation of the EVM.

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3.1 EVM Operation

The EVM is factory tested and configured for immediate operation with a few simple connections. There is no setup procedure for the end user; simply place the adapter card on the host DSP and plug the data converter EVM into the adapter card. Apply power to the DSP and/or data converter EVM as instructed in the appropriate users guide.

3.1.1 Jumper Settings

Table 3–1 shows the function of each jumper on the EVM.

Table 3–1. Jumper Settings

Reference	Setting	Function
W1	Pin 1–2 Closed	Provides 3.3 V from the DSP motherboard to the CPLD I/O voltage pins
	Pin 2–3 Closed	Provides 5 V from the DSP motherboard to the CPLD I/O voltage pins

3.1.2 I/O Connector Signals

Except for those listed in the tables below, each pair of connectors should be considered as having *pass-through* signals. Consult the respective DSP or EVM user's guide for signal name and/or pin number of any signal not listed.

Table 3–2. Adapter Card Connector Pair J1 and J3

Signal	Pin	Pin	Signal
DC_A17	7	8	DC_A16
DC_A15	9	10	DC_A14
DC_A5	23	24	DC_A4
DC_A3	25	26	DC_A2

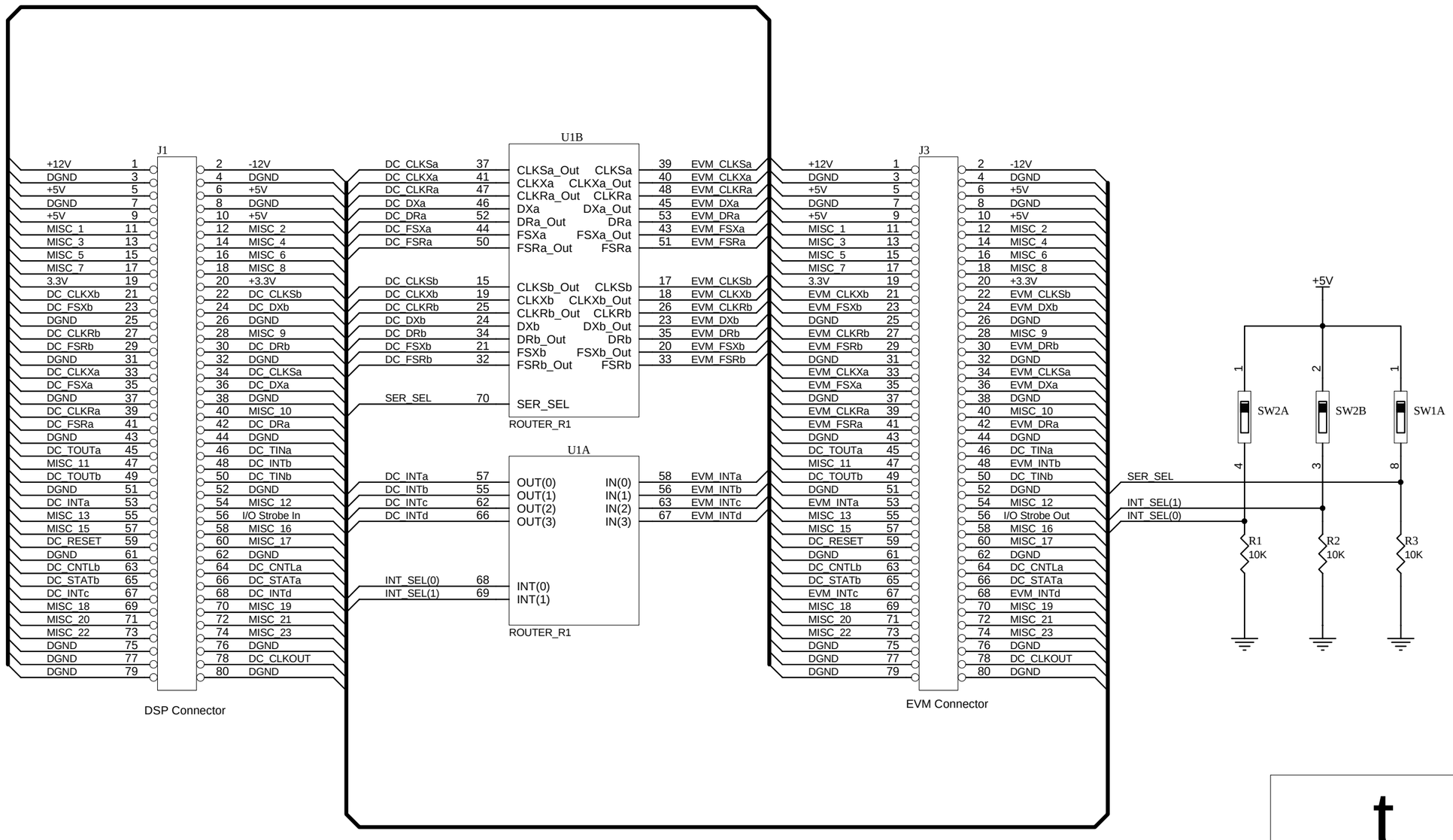
Table 3–3. Adapter Card Connector Pair J2 and J4

Signal	Pin	Pin	Signal
DC_CLKXb	21	22	DC_CLKSb
DC_FSXb	23	24	DC_DXb
DC_CLKRb	27		
DC_FSRb	29	30	DC_DRb
DC_CLKXa	33	34	DC_CLKSa
DC_FSXa	35	36	DC_DXa
DC_CLKRa	39		
DC_FSRa	41	42	DC_DRa
DC_INTa	53	48	DC_INTb
DC_INTc	67	68	DC_INTd

3.2 Schematic Diagrams

The following pages show the complete schematic diagram of the evaluation board.

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH



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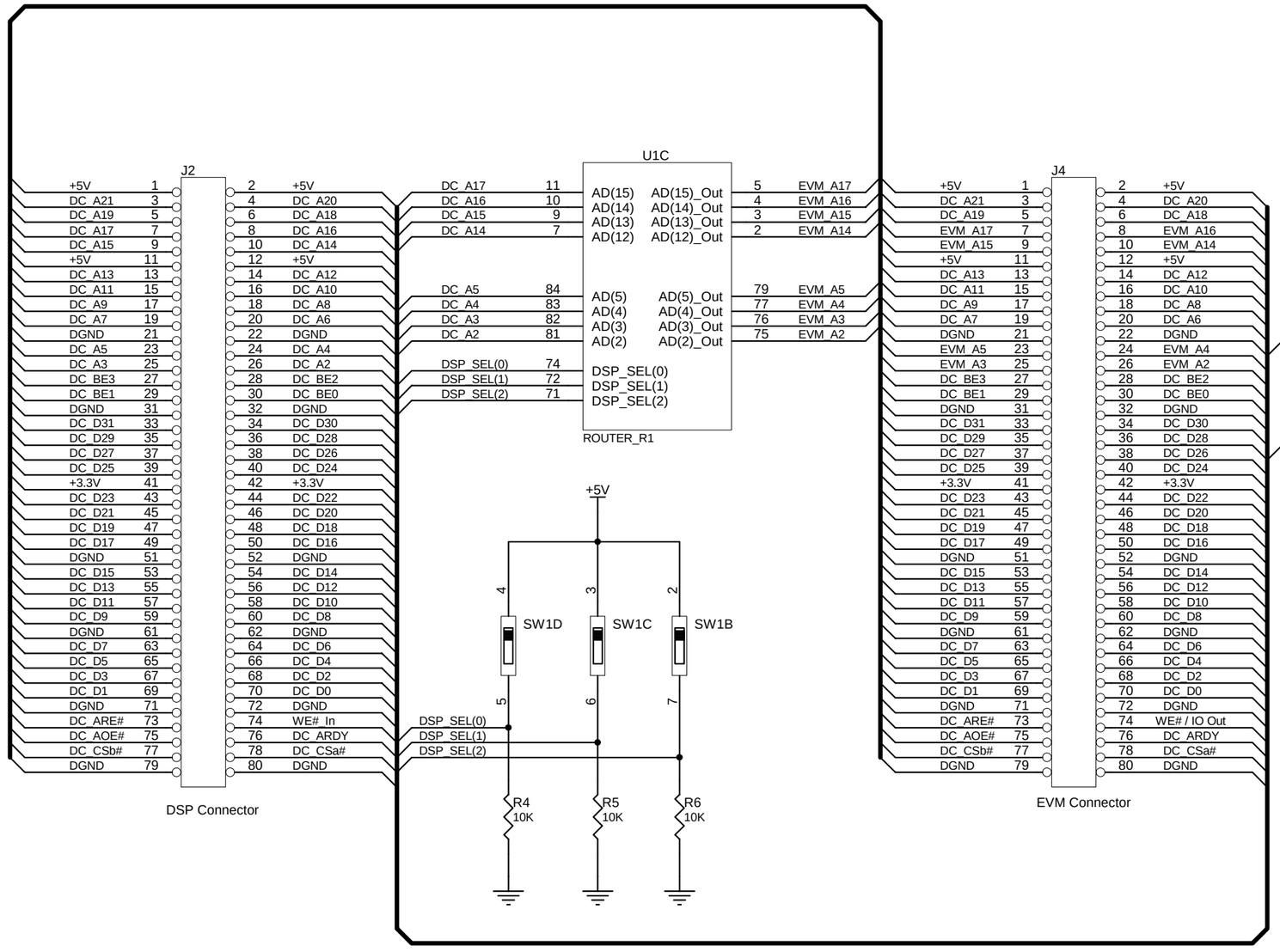
Drawn By: Tom Hendrick	Title: Common Connector Adapter Card Peripheral Connections			
Engineer: Tom Hendrick		SIZE: B	DATE: 16-Mar-2001	REV: A
FILE: 6428865				SHEET: 1 OF: 2

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH



Drawn By: Tom Hendrick			
Engineer: Tom Hendrick	SIZE: B	DATE: 16-Mar-2001	REV: A
FILE: 6428865			SHEET: 2 OF: 2

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Title: Common Connector Adapter Card Expansion Connections