TEXAS INSTRUMENTS
LM74501-Q1
SNOSD87A – JULY 2021 – REVISED FEBRUARY 2022

LM74501-Q1 *TVS Less* Automotive Reverse Battery Protection Controller

1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 3.2-V to 65-V input range (3.9-V start-up)
- –18-V reverse voltage rating
- Charge pump for external N-channel MOSFET
- Gate discharge timer: meets automotive ISO7637-2 pulse 1 transient without additional TVS diode (TVS less)
- 1-µA shutdown current (EN = low)
- 80-µA typical operating quiescent current (EN = high)
- 20-V VDS clamp (EN = low)
- Integrated battery voltage monitoring switch (SW)
- 8-pin SOT-23 package 2.90 mm × 1.60 mm

2 Applications

- Body electronics and lighting
  - Body control module (BCM)
  - Wiper module
- Automotive infotainment and cluster
  - Digital cockpit processing unit
- ADAS domain controller

3 Description

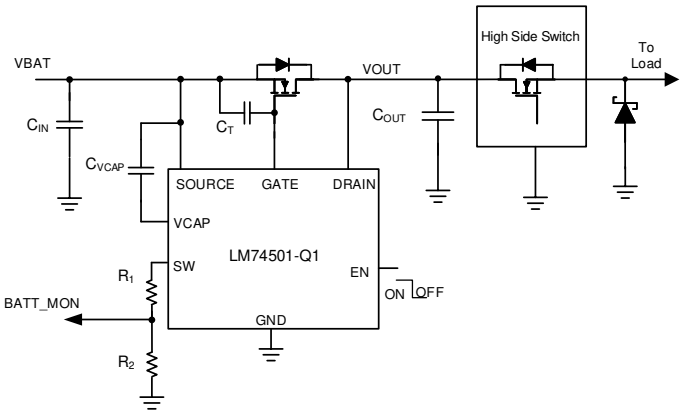
The LM74501-Q1 operates in conjunction with an external N-channel MOSFET as a low loss reverse polarity protection solution. The device supports wide supply input range of 3.2 V to 65 V. The 3.2-V input voltage support is particularly well suited for severe cold crank requirements in automotive systems. The device can withstand and protect the loads from negative supply voltages down to –18 V. The LM74501-Q1 does not have reverse current blocking functionality and is suitable for input reverse polarity protection of loads that can potentially deliver energy back to the input supply such as automotive body control module motor loads.

The LM74501-Q1 controller provides a charge pump gate drive for an external N-channel MOSFET. The LM74501-Q1 has a unique integrated feature that allows systems to meet automotive ISO7637 pulse 1 transient requirements without an additional TVS Diode (TVS less). The LM74501-Q1 features an integrated switch to enable battery voltage monitoring with an external resistor divider. With the enable pin low, the controller is off and draws only around 1 µA of current, thus offering low system current when put into sleep mode.

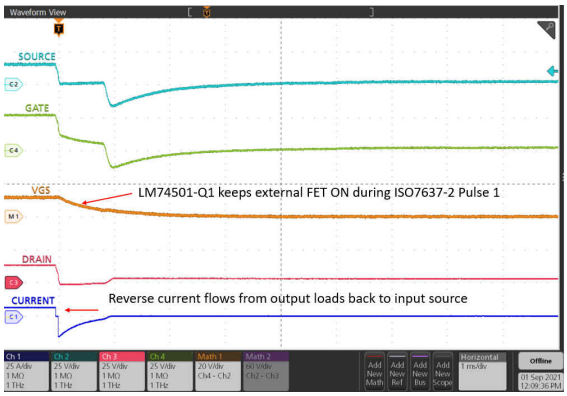
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM74501-Q1	SOT-23 (8)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



LM74501-Q1 Typical Application Schematic for Automotive Battery Reverse Polarity Protection



TVS Less ISO7637-2 Pulse 1 Operation

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (February 2022)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Pin Configuration and Functions

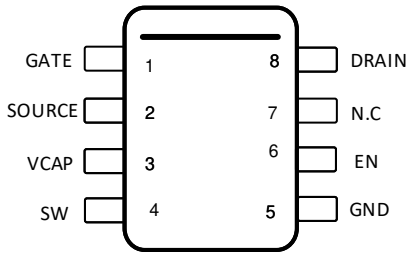


Figure 5-1. DDF Package 8-Pin SOT-23 (LM74501-Q1 Top View)

Table 5-1. LM74501-Q1 Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	GATE	O	Gate drive output. Connect to the gate of the external N-channel MOSFET.
2	SOURCE	I	Connect to the source of the external N-channel MOSFET. This pin also acts as the input supply for the device.
3	VCAP	O	Charge pump output. Connect to an external charge pump capacitor.
4	SW	I	Voltage sensing disconnect switch terminal. SOURCE and SW are internally connected through a switch when EN is high. A resistor ladder from this pin to GND can be used to monitor battery voltage. When EN is pulled low, the switch is OFF, disconnecting the resistor ladder from the battery line, thereby cutting off the leakage current.
5	GND	G	Ground pin
6	EN	I	Enable pin. Can be connected to SOURCE for always ON operation.
7	N.C	NA	No connect. Keep this pin floating.
8	DRAIN	I	Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input pins	SOURCE to GND	$-(V_{CLAMP} - 1)$	65	V
	EN, SW to GND, $V_{(SOURCE)} > 0$ V	–0.3	65	V
	EN to GND, $V_{(SOURCE)} \leq 0$ V	$V_{(SOURCE)}$	65 + $V_{(SOURCE)}$	V
	SW to GND, $V_{(SOURCE)} \leq 0$ V	$V_{(SOURCE)}$	0.3 + $V_{(SOURCE)}$	V
	I_{SW}	–1	10	mA
Output pins	GATE to SOURCE	–0.3	15	V
	VCAP to SOURCE	–0.3	15	V
Output pins	DRAIN to SOURCE	–5	V_{CLAMP}	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (GATE, SW, GND, DRAIN)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input pins	SOURCE to GND	–18		60	V
	EN to GND	–18		60	
Input pins	DRAIN to GND			60	V
Input to output pins	SOURCE to DRAIN	$-V_{CLAMP}$		5	V
External capacitance	SOURCE	0.1			µF
	VCAP to SOURCE	0.1			µF
External MOSFET maximum V_{GS} rating	GATE to SOURCE	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		DDF (SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W

THERMAL METRIC(1)		DDF (SOT)	UNIT
		8 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(SOURCE)}$ = 12 V, C_{IN} = $C_{(VCAP)}$ = C_{OUT} = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SOURCE} SUPPLY VOLTAGE						
V_{CLAMP}	V_{DS} clamp voltage	$V_{(EN)}$ = 0 V	19		24	V
$V_{(SOURCE)}$	Operating input voltage		4		60	V
$V_{(SOURCE\ POR)}$	VSOURCE POR rising threshold				3.9	V
	VSOURCE POR falling threshold		2.2	2.8	3.1	V
$V_{(SOURCE\ POR(Hys))}$	VSOURCE POR hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown supply current	$V_{(EN)}$ = 0 V		0.9	1.5	µA
$I_{(Q)}$	Operating quiescent current			80	130	µA
ENABLE INPUT						
$V_{(EN\_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN\_IH)}$	Enable input high threshold		1.06	2	2.6	
$V_{(EN\_Hys)}$	Enable hysteresis		0.52		1.35	V
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		3	5	µA
GATE DRIVE						
$I_{(GATE)}$	Peak source current	Enable (low to high) $V_{(GATE)} – V_{(SOURCE)}$ = 5 V	3	11		mA
RDS_{ON}	discharge switch RDS_{ON}	$V_{(EN)}$ = 0 V, $V_{(GATE)} – V_{(SOURCE)}$ = 100 mV	24	30	36	kΩ
SW						
$R_{(SW)}$	Battery sensing disconnect switch resistance	4 V < $V_{(SOURCE)}$ ≤ 60 V	10	19.5	46	Ω
CHARGE PUMP						
$I_{(VCAP)}$	Charge pump source current (charge pump on)	$V_{(VCAP)} – V_{SOURCE}$ = 7 V	162	300	600	µA
	Charge pump sink current (charge pump off)	$V_{(VCAP)} – V_{SOURCE}$ = 14 V		5	10	µA
$V_{(VCAP)} – V_{(SOURCE)}$	Charge pump voltage at $V_{(SOURCE)}$ = 3.2 V	$I_{(VCAP)}$ ≤ 30 µA	8			V
	Charge pump turn-on voltage		10.3	11.6	13	V
	Charge pump turn-off voltage		11	12.4	13.9	V
	Charge pump enable comparator hysteresis		0.4	0.8	1.2	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(SOURCE)}$ UV release at rising edge	$V_{SOURCE} – V_{DRAIN}$ = 100 mV	5.7	6.5	7.5	V
	$V_{(VCAP)} – V_{(SOURCE)}$ UV threshold at falling edge	$V_{SOURCE} – V_{DRAIN}$ = 100 mV	5.05	5.4	6.2	V
DRAIN						

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(SOURCE)}$ = 12 V, C_{IN} = $C_{(VCAP)}$ = C_{OUT} = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(DRAIN)}$	DRAIN sink current	$V_{(SOURCE)}$ = $V_{(EN)}$ = –14 V, $V_{(DRAIN)}$ = 0 V			4	µA

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(SOURCE)}$ = 12 V, C_{IN} = $C_{(VCAP)}$ = C_{OUT} = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to gate turn-on delay	$V_{(VCAP)}$ > $V_{(VCAP\ UVLOR)}$		75	110	µs

6.7 Typical Characteristics

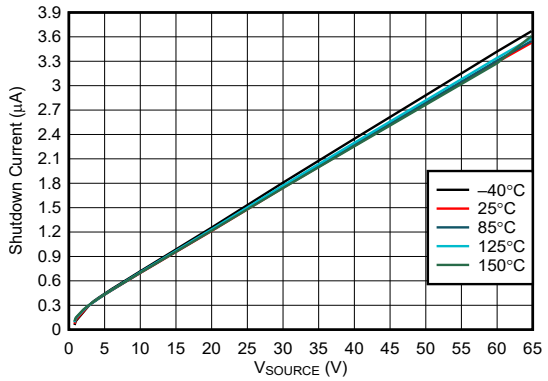


Figure 6-1. Shutdown Supply Current vs Supply Voltage

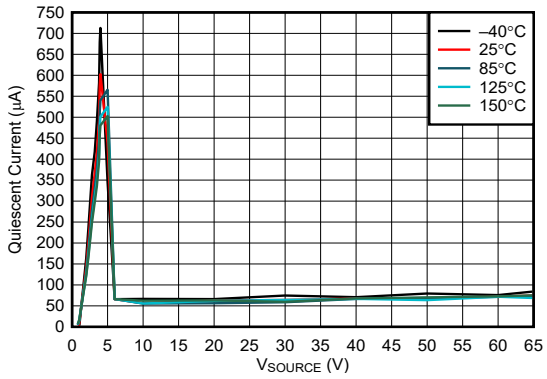


Figure 6-2. Operating Quiescent Current vs Supply Voltage

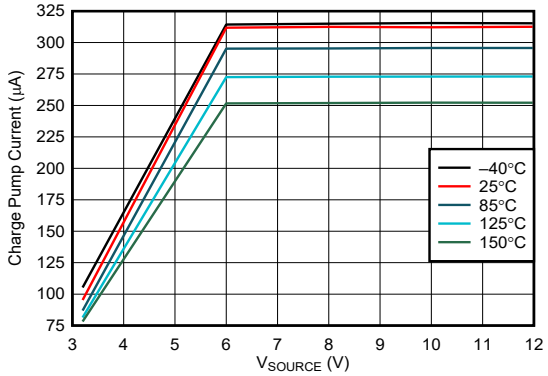


Figure 6-3. Charge Pump Current vs Supply Voltage at VCAP = 6 V

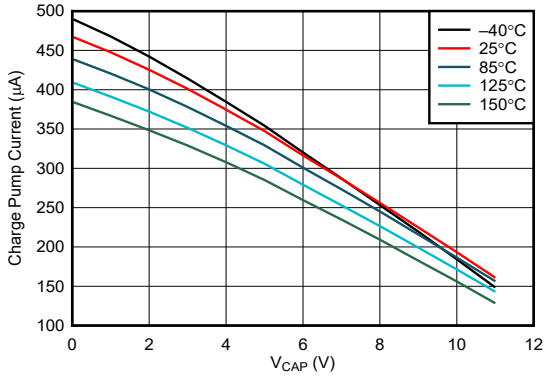


Figure 6-4. Charge Pump V-I Characteristics at VSOURCE > = 12 V

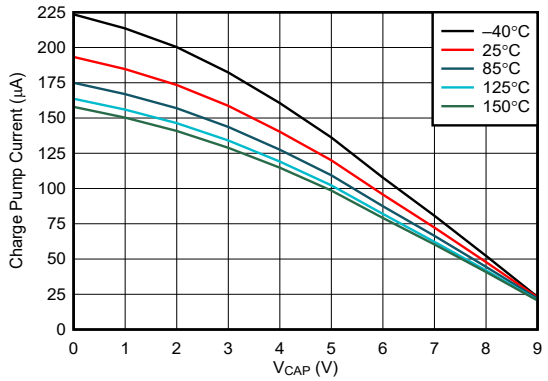


Figure 6-5. Charge Pump V-I Characteristics at VSOURCE = 3.2 V

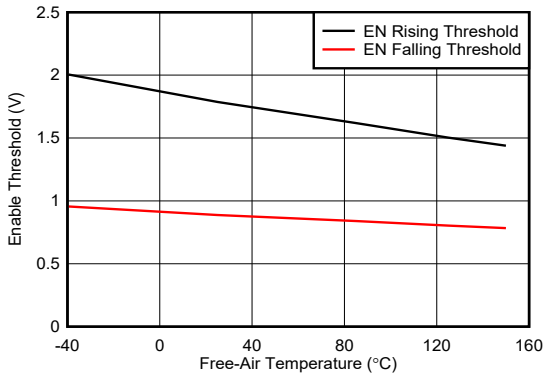


Figure 6-6. Enable Threshold vs Temperature

6.7 Typical Characteristics (continued)

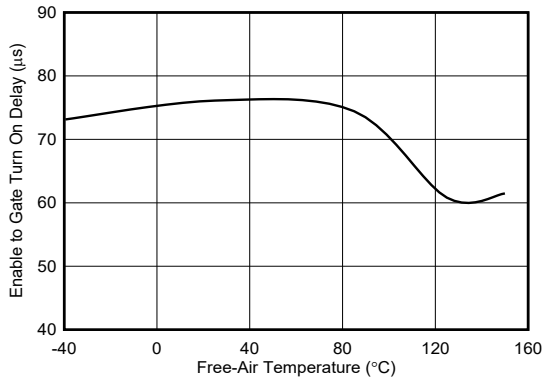


Figure 6-7. Enable to Gate Turn On Delay vs Temperature

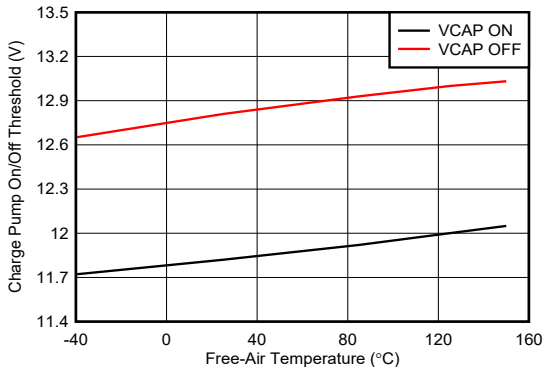


Figure 6-8. Charge Pump ON/OFF Threshold vs Temperature

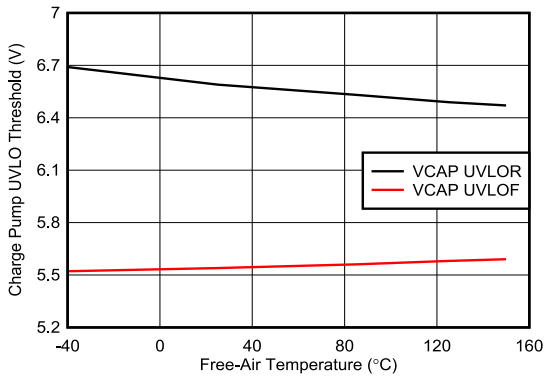


Figure 6-9. Charge Pump UVLO Threshold vs Temperature

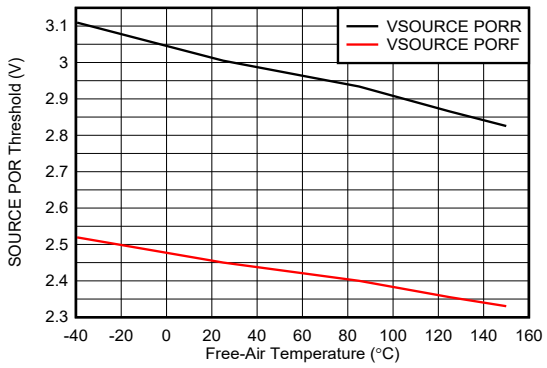


Figure 6-10. VSOURCE POR Threshold vs Temperature

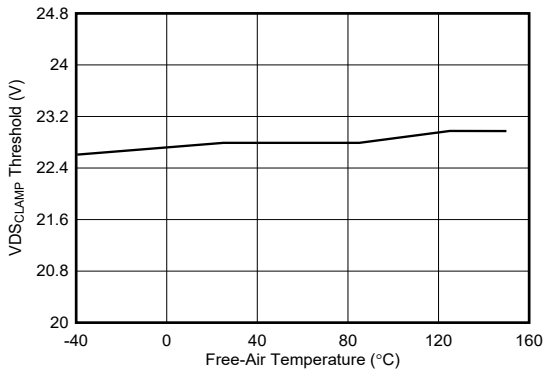


Figure 6-11. VDS_{CLAMP} Threshold vs Temperature

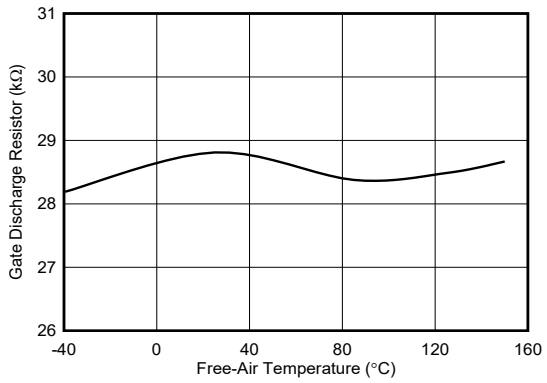


Figure 6-12. Gate Discharge Resistor vs Temperature

7 Parameter Measurement Information

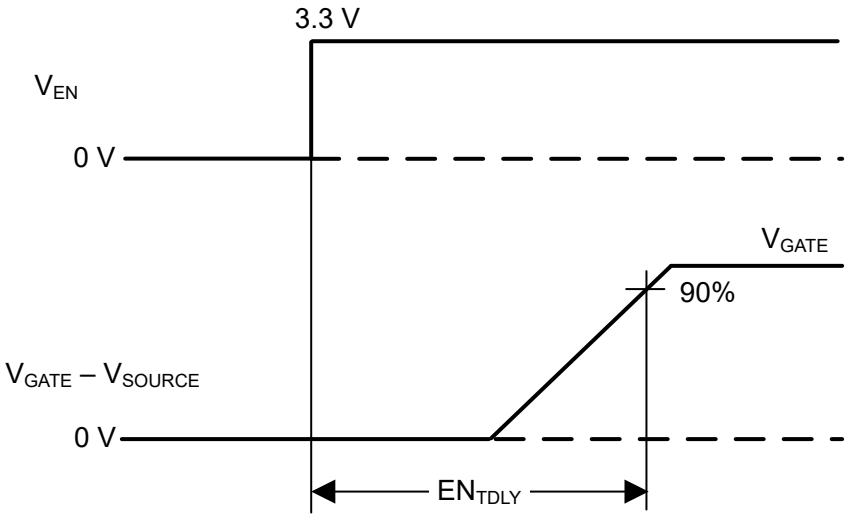


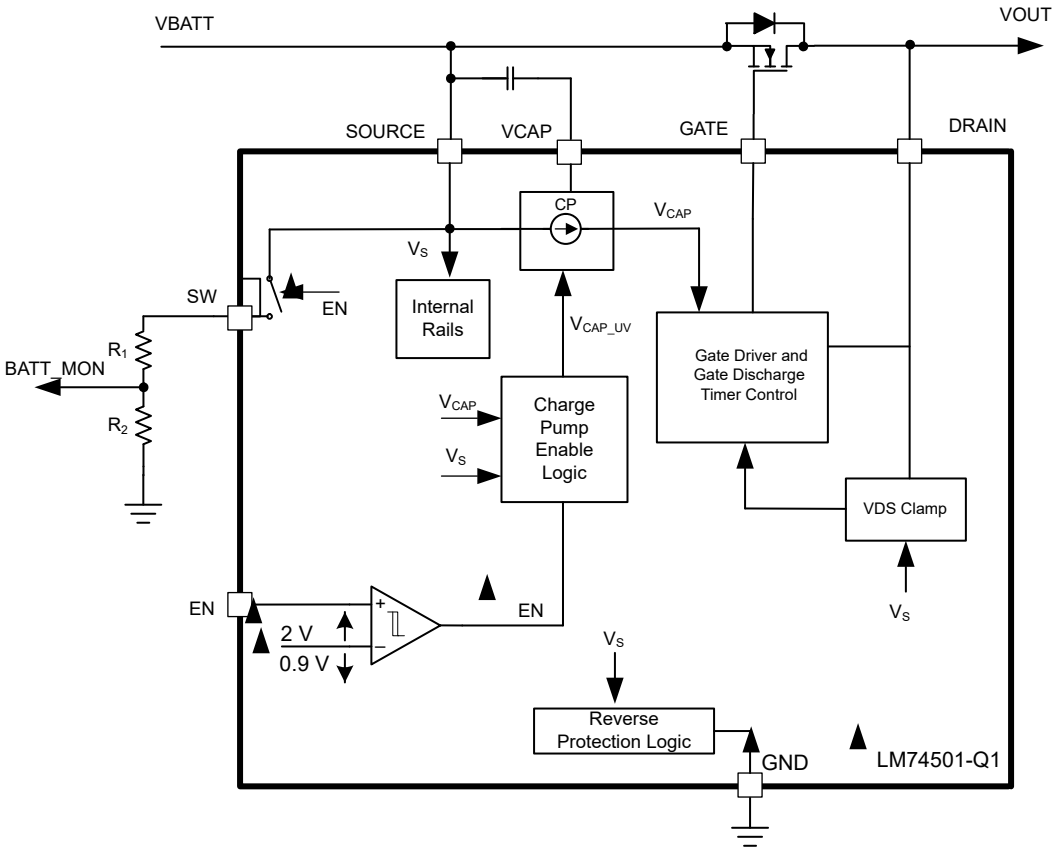
Figure 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

The LM74501-Q1 controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit. This easy-to-use reverse polarity protection controller is paired with an external N-channel MOSFET to replace other reverse polarity protection schemes such as a P-channel MOSFET. An internal charge pump is used to drive the external N-Channel MOSFET with a typical gate drive voltage of 12 V. The Gate Discharge Timer feature of the device enables meeting automotive ISO7637 pulse 1 transient requirements without an additional TVS Diode (TVS less) under certain load conditions. The LM74501-Q1 has integrated switch (SW), which enables input battery voltage monitoring by connecting an external resistor divider from the SW pin to GND. An enable pin, EN, is available to place the LM74501-Q1 in shutdown mode, disabling the N-Channel MOSFET and minimizing the quiescent current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage

The SOURCE pin is used to power the internal circuitry of the LM74501-Q1, typically drawing 80 µA when enabled and 1 µA when disabled. If the SOURCE pin voltage is greater than the POR rising threshold, the LM74501-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The LM74501-Q1 can withstand input reverse voltage up to –18 V.

8.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and SOURCE pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor, the EN pin voltage must be above the specified input high threshold, $V_{(EN\_IH)}$. When enabled, the charge pump sources a charging current of 300 µA (typical). If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external

MOSFET can be driven above its specified threshold voltage, the VCAP-to-SOURCE voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 75\ \mu s + C_{(VCAP)} \times \frac{V_{(VCAP\_UVLOR)}}{300\ \mu A} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across SOURCE and VCAP pins.
- $V_{(VCAP\_UVLOR)}$ is 6.5 V (typical).

To remove any chatter on the gate drive, approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP-to-SOURCE voltage reaches 12.4 V (typical), at which point the charge pump is disabled decreasing the current draw on the SOURCE pin. The charge pump remains disabled until the VCAP-to-SOURCE voltage is below to 11.6 V (typical), at which point the charge pump is enabled. The voltage between VCAP and SOURCE continues to charge and discharge between 11.6 V and 12.4 V as shown in Figure 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74501-Q1 is reduced. When the charge pump is disabled, it sinks 5 µA (typical).

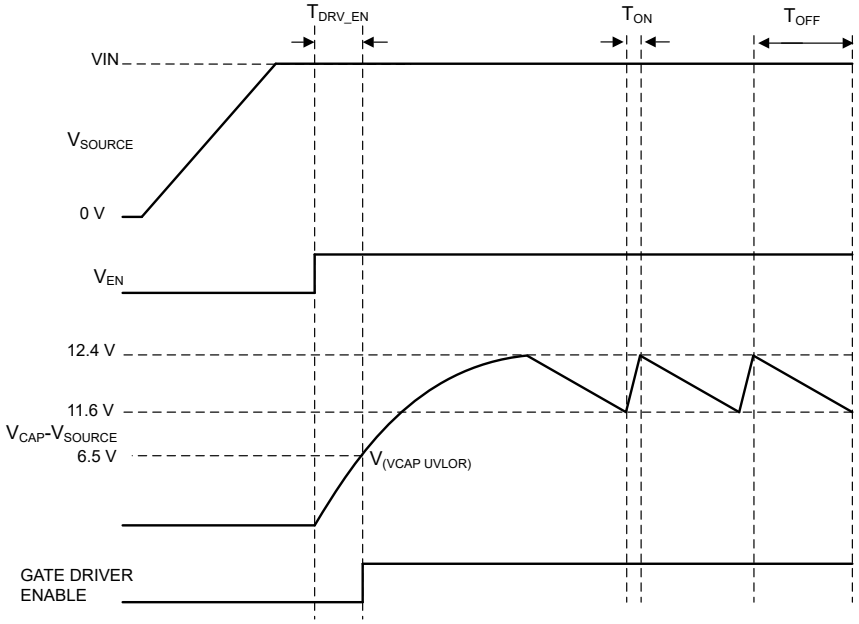


Figure 8-1. Charge Pump Operation

8.3.3 Enable

The LM74501-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74501-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –18 V. This feature allows for the EN pin to be connected directly to the SOURCE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 1 µA pulls the EN pin low and disables the device.

8.3.4 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the appropriate GATE-to-SOURCE voltage.

Before the gate driver is enabled, the following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to SOURCE voltage must be greater than the undervoltage lockout voltage.
- The SOURCE voltage must be greater than the VSOURCE POR rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the SOURCE pin, assuring that the external MOSFET is disabled. After these conditions are achieved, the gate driver operates in the full conduction mode.

8.3.5 SW (Battery Voltage Monitoring)

The LM74501-Q1 has an SW pin to enable battery voltage monitoring in automotive systems. When the device is enabled, an internal switch connects the SW pin to SOURCE. This connection enables monitoring battery voltage using an external resistor divider connected from SW pin to GND. When LM74501-Q1 is put in shutdown mode by pulling down the EN pin to ground, an internal switch between SW and SOURCE pin is disconnected. This disconnection ensures there is no quiescent current drawn by the resistor ladder when system is put into low power shutdown mode. When not used, the SW pin can be left floating.

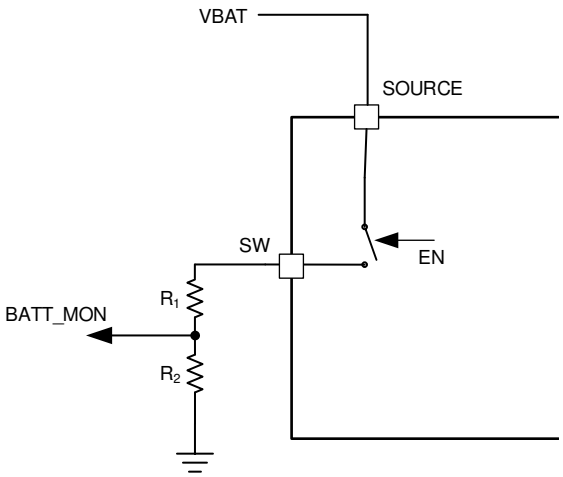


Figure 8-2. LM74501-Q1 SW Functionality

8.3.6 Gate Discharge Timer

The LM74501-Q1 has a unique gate discharge timer feature, which enables TVS less reverse polarity protection solution in case of ISO7637-2 pulse 1 event. An additional capacitor (C_T) across external N-FET's GATE to SOURCE terminal keeps external N-FET on for specific time window even when input voltage falls below V_{PORF} threshold of SOURCE pin or when the EN pin is pulled low. This gate discharge feature allows reverse current back to input source by keeping external MOSFET on for extended time duration set by gate discharge timer capacitor (C_T) and enables automotive systems to meet TVS less ISO 7637-2 pulse 1 operation. Use Equation 2 to calculate the typical gate discharge time.

$$t_D = -[R_D \times (C_T + Ciss) \times \ln (V_T / V_{GATE})] \quad (2)$$

Where

- R_D is the LM74501-Q1 internal GATE discharge resistor (typically 30 kΩ).
- Ciss is the external MOSFET input capacitance.
- C_T is the timer capacitor connected between GATE and SOURCE of an external MOSFET.
- V_T is the gate-to-source threshold voltage of an external MOSFET.
- V_{GATE} is the nominal GATE pin voltage of LM74501-Q1 (12.4-V typical).

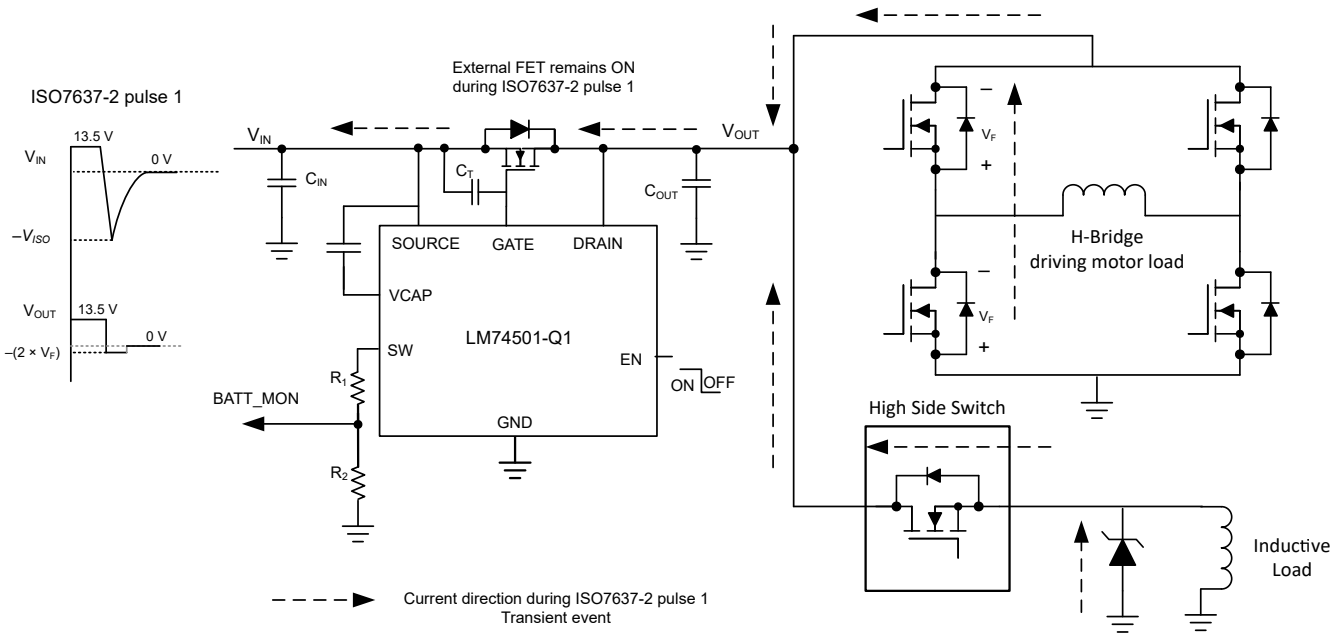


Figure 8-3. Typical Application Scenario During ISO7637-2 Pulse 1 Events

Figure 8-3 shows equivalent the LM74501-Q1 circuit operation during an ISO7637-2 pulse 1 event. Note that reverse current flows back to the input source from output loads such as a high-side switch followed by schottky diode or MOSFET H-bridge driving motor load. Thus, to achieve TVS less operation during ISO7637-2 pulse 1 events, output loads must be capable of withstanding the peak reverse current during ISO7637-2 pulse 1 event.

Figure 8-4 shows the TVS-less ISO7637-2 pulse 1 performance of the LM74501-Q1 with output loads capable of handling reverse current during an ISO7637-2 pulse 1 event, similar to loads configuration shown in Figure 8-4.

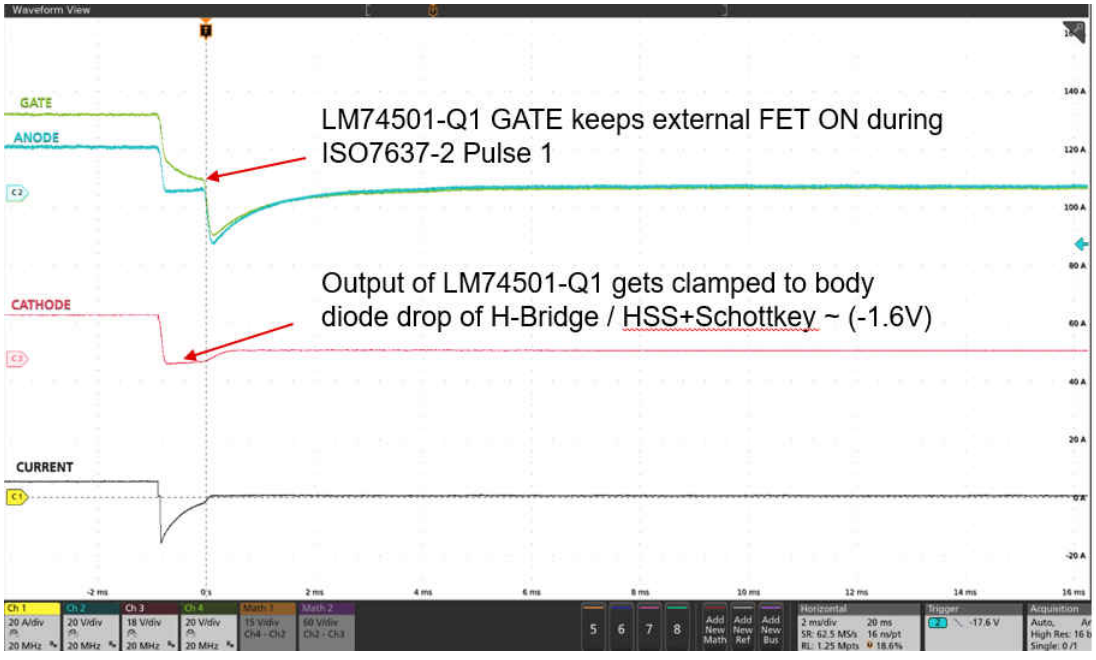


Figure 8-4. TVS Less Operation During ISO7637-2 Pulse 1

The other short duration transient events such as ISO7637-2 pulse 2A, 3A, or 3B usually get filtered out by input and output capacitors and do not affect the system performance.

For the loads that cannot handle peak reverse current during an ISO 7637-2 pulse 1 transient event but can handle negative voltage for a short duration, a schottky diode capable of handling peak reverse current can be placed from output to ground to clamp the output voltage to negative forward voltage drop of the Schottky diode ($-V_F$).

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74501-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN\_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode, the LM74501-Q1 enters low I_Q operation with the SOURCE pin only sinking 1 µA. When the LM74501-Q1 is in shutdown mode, forward current flowing through the external MOSFET is not interrupted but is conducted through the body diode of the MOSFET.

8.4.2 Full Conduction Mode

For the LM74501-Q1 to operate in full conduction mode the gate driver must be enabled as described in the *Gate Driver* section. If these conditions are achieved, the GATE pin is internally connected to the VCAP pin, resulting in the GATE to SOURCE voltage being approximately the same as the VCAP to SOURCE voltage. By connecting VCAP to GATE, the external MOSFET is fully enhanced reducing the power loss of the external MOSFET.

8.4.3 VDS Clamp

The LM74501-Q1 has an integrated VDS clamp feature that turns on an external MOSFET whenever voltage difference between DRIAN and SOURCE exceeds VDS clamp threshold (20 V typical) when enable pin is pulled low. This use case scenario is specially true when the LM74501-Q1 is used to drive inductive loads and overshoot can happen at the DRAIN pin due to regenerative action of the motor load. Also, if the gate discharge timer designed to keep external MOSFET on during an ISO7637-2 pulse 1 event expires within stipulated time window due to component level tolerances, the LM74501-Q1 VDS clamp feature provides second level of protection to keep maximum voltage across FET to 20 V.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM74501-Q1 is used with an N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in Figure 9-2 where the LM74501-Q1 is used to drive a MOSFET Q1 in series with a battery. The LM74501-Q1 enables TVS-less operation with its integrated gate discharge timer feature.

9.1.1 Reverse Battery Protection

P-FET based reverse polarity protection is a very commonly used scheme in automotive applications to achieve low insertion loss protection solution. A low loss reverse polarity protection solution can be realized using the LM74501-Q1 with an external N-FET to replace P-FET based solution. The LM74501-Q1-based reverse polarity protection solution offers input TVS-less performance during ISO7637-2 pulse 1 event, better cold crank performance (low VIN operation) and smaller solution size compared to P-FET based solution. Figure 9-1 compares the performance benefits of LM74501-Q1 + N-FET over a traditional P-FET based reverse polarity protection solution.

- As shown in Figure 9-1, a given power level LM74501-Q1 + N-FET solution can be 50% smaller than a similar power rated P-FET solution.
- The second advantage that the LM74501-Q1 offers over a traditional P-FET is TVS-less operation for the body control module load driving paths where reverse current blocking is not a must-have feature and output loads are capable of handling negative voltage and reverse current for a short duration of the time.
- As PFET is self biased by simply pulling its gate pin low, P-FET shows poorer cold crank performance (low VIN operation) compared to the LM74501-Q1. During severe cold crank where battery voltage falls below 4 V, P-FET series resistance increases drastically as shown in Figure 9-1. This increase leads to higher voltage drop across the PFET. Also, with a higher gate-to-source threshold (V_T), this can sometimes lead to system reset due to turning off of the P-FET. On the other side, the LM74501-Q1 has excellent severe cold crank performance. The LM74501-Q1 keeps the external FET completely enhanced even when input voltage falls to 3.2 V during severe cold crank operation.

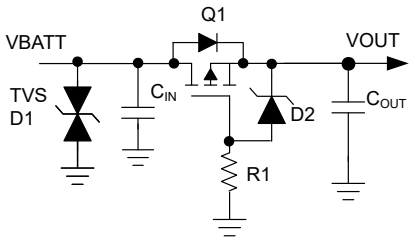
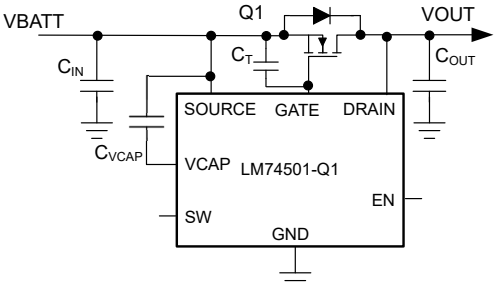
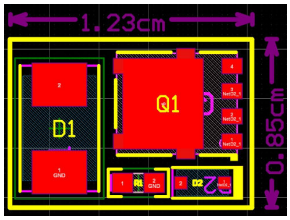
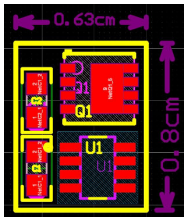
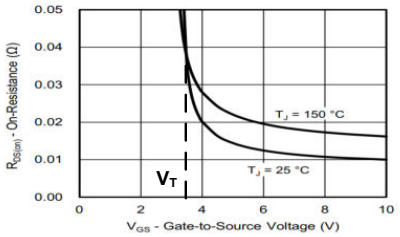
Parameter	P-channel MOSFET	LM74501-Q1 + N-channel MOSFET
Typical Application Diagram		
Solution Size (Load current > 6 A)	**PFET (Q1) +TVS (D1) + Zener (D2) + Resistor (R1)** 12.3 mm × 8.5 mm (104.5 mm^2) 	**LM74501 + NFET (Q1) + C_{CVCAP} + C_T** 6.3 mm × 8 mm (50.4 mm^2) TVS Less solution with 50% reduction in size 
Low V_{IN} / Cold-Crank Performance		Better cold crank performance compared to PFET based solution. External N-FET remains fully enhanced even if input voltage falls to 3.2 V.

Figure 9-1. PFET vs LM74501-Q1 Reverse Polarity Protection Solution Comparison

9.2 Typical Application

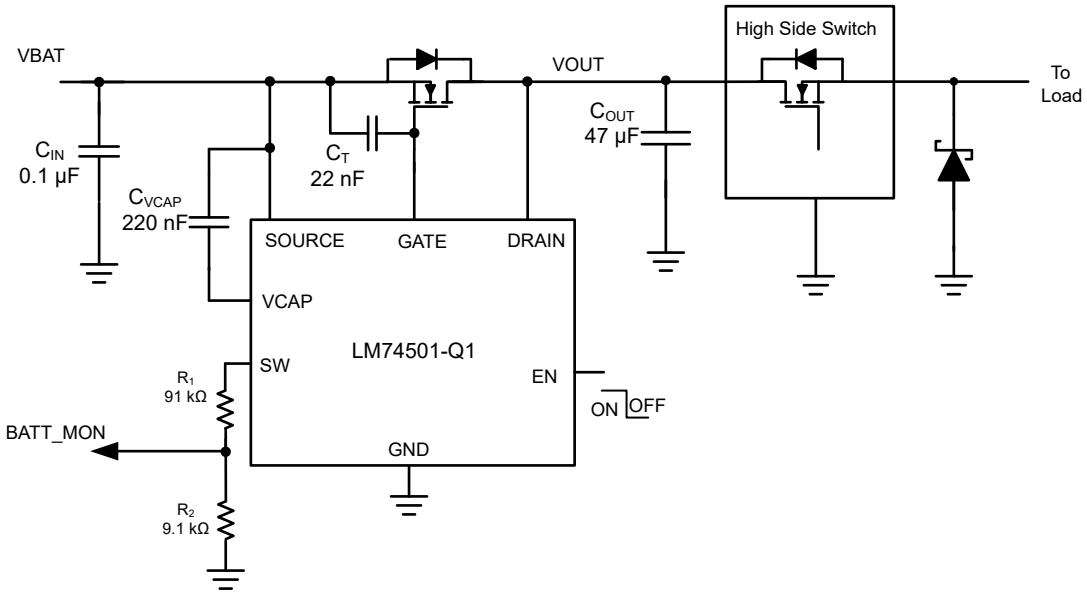


Figure 9-2. Typical Application Circuit

9.2.1 Design Requirements

A design example, with system design parameters, is presented in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V battery, 12-V nominal with 3.2-V cold crank, and 35-V load dump
Output voltage	3.2-V during cold crank to 35-V load dump
Output current range	3-A nominal, 5-A maximum
Output capacitance	47-µF typical holdup capacitance
Automotive EMC compliance	ISO 7637-2 and ISO 16750-2

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

9.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current, I_D, the maximum drain-to-source voltage, $V_{DS(MAX)}$, the maximum source current through body diode, and the drain-to-source on resistance, R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. As the LM74501-Q1 has an integrated VDS clamp control with threshold of 20 V (typical), MOSFETs with voltage rating of 40 V can be used with the LM74501-Q1. The maximum GATE pin voltage of the LM74501-Q1 can drive is 13.9 V, so a MOSFET with 15-V minimum V_{GS} must be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a Zener diode can be used to clamp V_{GS} to safe level. During start-up, inrush current flows through the body diode to charge the bulk holdup capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, the lowest possible $R_{DS(ON)}$ is preferred. Selecting a MOSFET with forward voltage drop of < 50 mV is a good starting point and gives good trade off between power dissipation and cost.

The BUK7Y3R0-40H MOSFET is selected to meet this 12-V reverse battery protection design requirements and it is rated at:

- 40-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 2.55 mΩ (typical) and 3-mΩ maximum rated at 10-V V_{GS}

Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

9.2.2.3 Gate Discharge Timer Capacitor Selection (C_T)

A gate discharge timer decides the time duration for which external MOSFET is kept on after the LM74501-Q1 fall below its PoR threshold (V_{PORF}) or when EN pin is pulled low. A ISO7637-2 pulse 1 transient lasts for typically 2 ms. At the end of 2-ms ISO7637-2 pulse 1, amplitude has already fallen to 10% of its peak value. Assuming a ISO7637-2 pulse 1 transient with amplitude of –150 V, at the end of 2 ms, the voltage seen by the LM74501-Q1 is around –15 V. With a VDS rating of external MOSFET of 40 V, the gate discharge timer capacitor, C_T, can be selected such that external FET remains on for less than 2 ms. A C_T timer capacitor value of 22 nF is selected for the given MOSFET as per Equation 2.

9.2.2.4 Charge Pump VCAP, Input and Output Capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

- VCAP: minimum recommended value of VCAP (µF) ≥ 10 × ($C_{ISS(MOSFET)}$ + C_T) µF
- C_{IN}: minimum 100 nF of input capacitance
- C_{OUT}: typical 10 µF to 47 µF of output capacitance

9.2.3 Application Curves

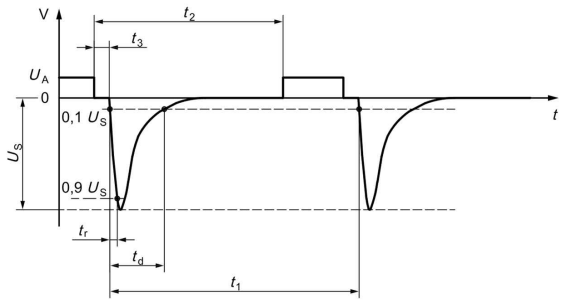
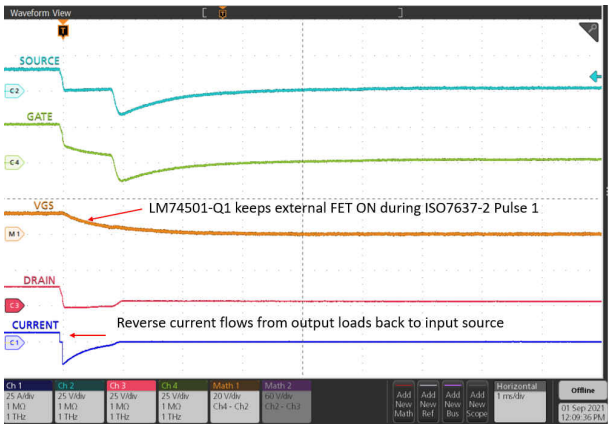
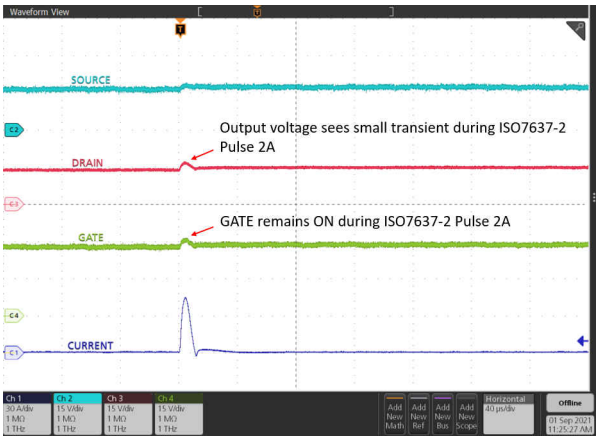


Figure 9-3. ISO 7637-2 Pulse 1



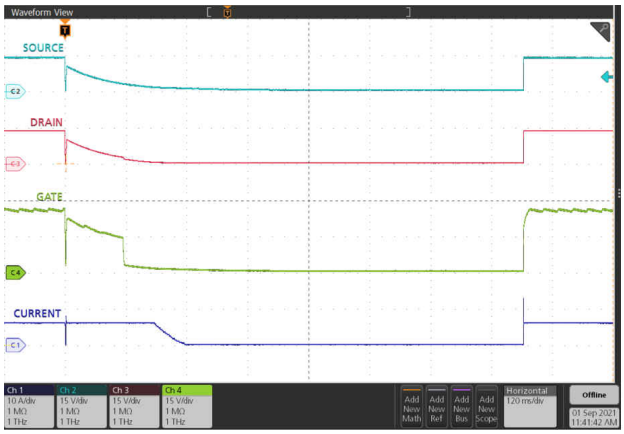
Time (1 ms/DIV)

Figure 9-4. Response to ISO 7637-2 Pulse 1



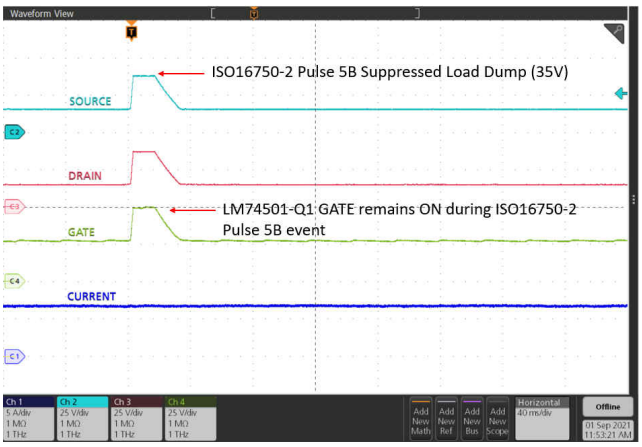
Time (40 µs/DIV)

Figure 9-5. Response to ISO7637-2 Pulse 2A



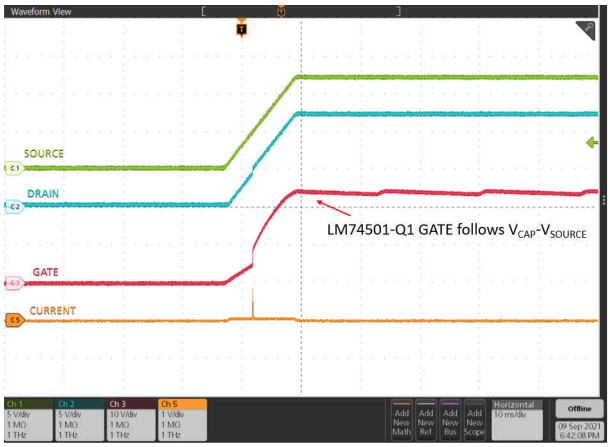
Time (120 ms/DIV)

Figure 9-6. Response to ISO7637-2 Pulse 2B



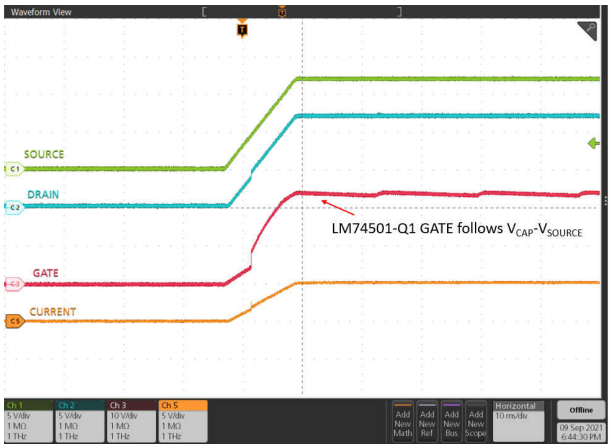
Time (40 ms/DIV)

Figure 9-7. Response to ISO16750-2 Pulse 5B



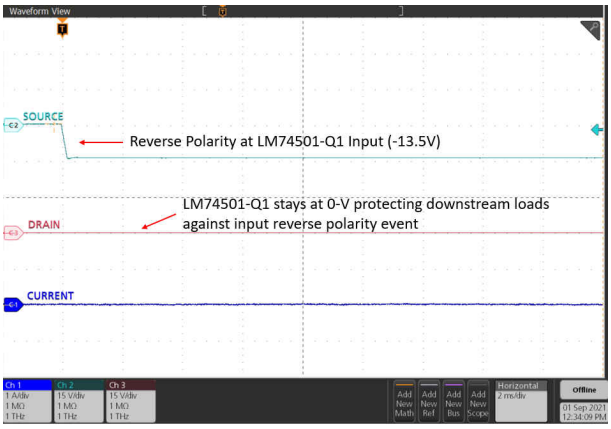
Time (10 ms/DIV)

Figure 9-8. Start-up with No Load



Time (10 ms/DIV)

Figure 9-9. Start-up with 5-A Load



Time (20 ms/DIV)

Figure 9-10. Input Reverse Polarity Hot Plug

10 Power Supply Recommendations

The LM74501-Q1 controller is designed for the supply voltage range of 3.2 V ≤ V_{SOURCE} ≤ 65 V. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 100 nF placed close to SOURCE pin to GND. To prevent Lthe M74501-Q1 and surrounding components from damage under the conditions of a direct output short circuit, use a power supply having overload and short-circuit protection.

11 Layout

11.1 Layout Guidelines

- Connect SOURCE, GATE, and DRAIN pins of LM74501-Q1 close to the MOSFET's SOURCE, GATE, and DRAIN pins.
- Use thick traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this solution is through the MOSFET.
- Place the input capacitor close to the SOURCE pin to Ground (GND) to minimize long ground loop.
- Keep the charge pump capacitor across VCAP and SOURCE pins away from the MOSFET to lower the thermal effects on the capacitance value.
- Avoid excessively thin and long trace for the gate pin connection. The Gate pin of the LM74501-Q1 must be connected to the MOSFET gate with short trace.
- Use of series gate resistor (typical 10 Ω) can help with better EMI performance.

11.2 Layout Example

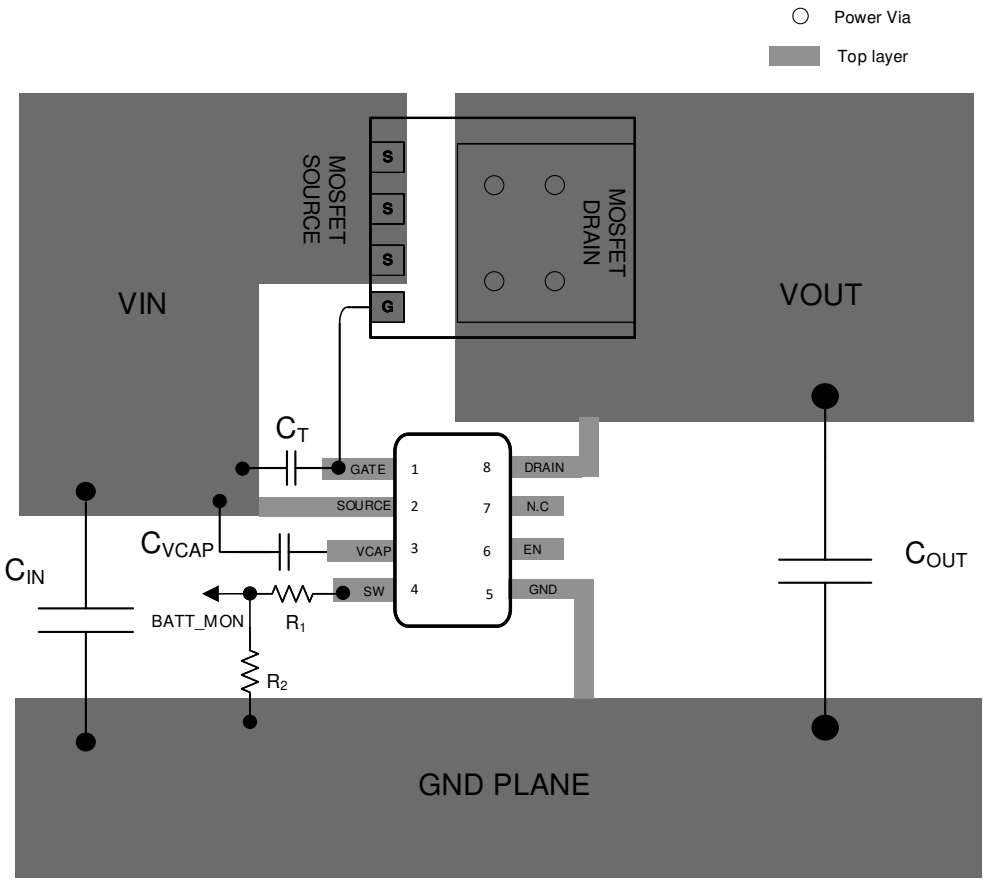


Figure 11-1. LM74501-Q1 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74501QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L7501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

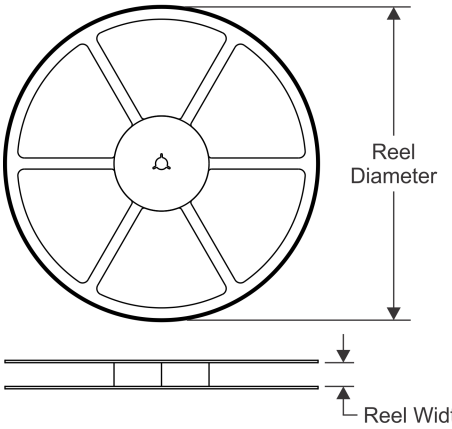
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

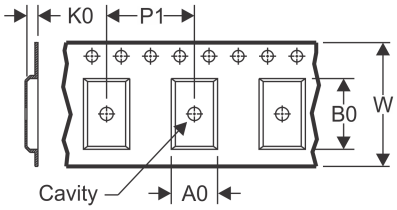
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

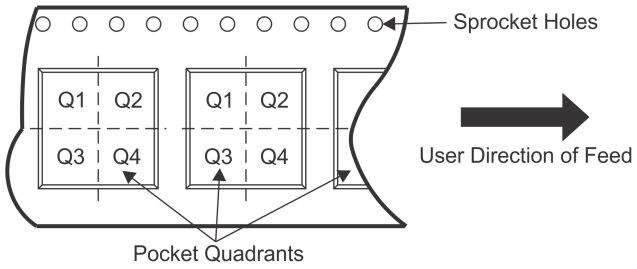


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

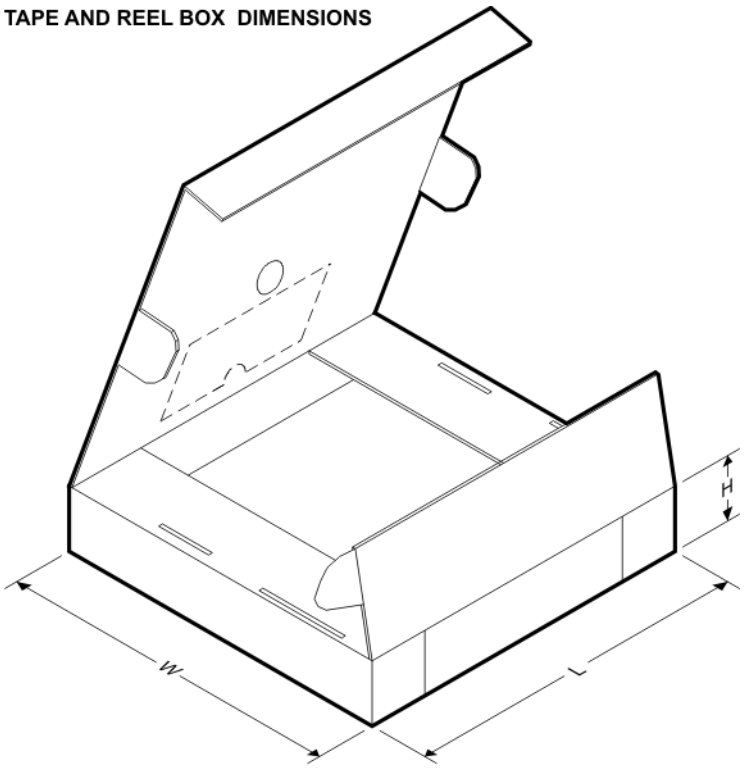
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74501QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

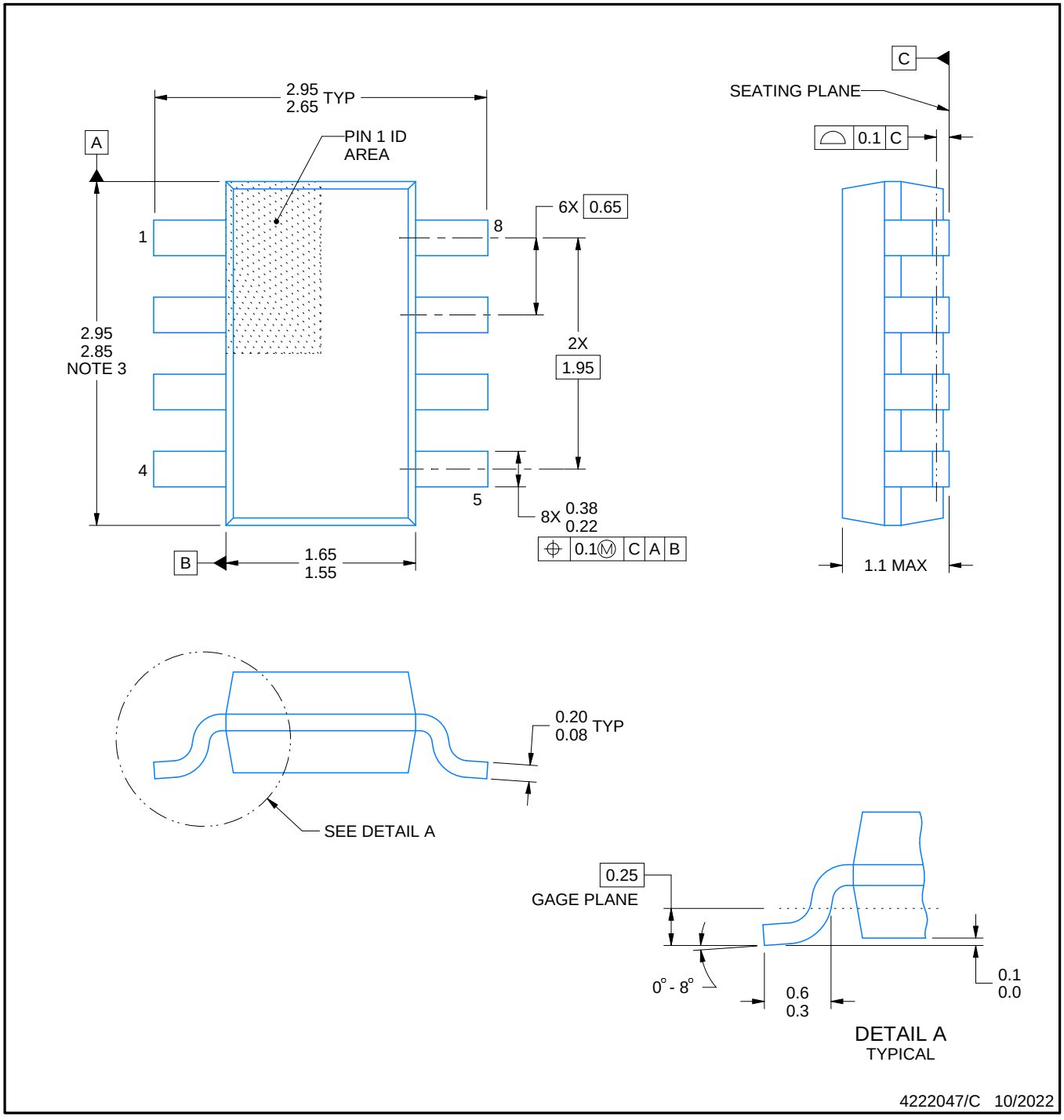
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74501QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

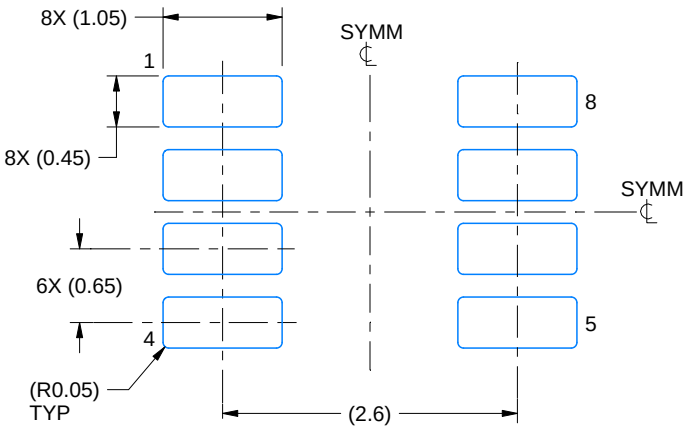
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

NON SOLDER MASK
DEFINED

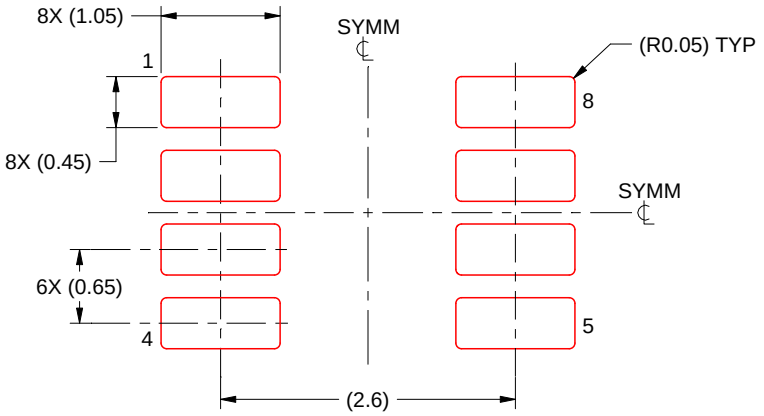
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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