SN54F86, SN74F86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

● **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54F86 . . . J PACKAGE
SN74F86 . . . D OR N PACKAGE
(TOP VIEW)

```
        ┌───┬─∪─┬───┐
  1A  [ │ 1     14 │ ]  V_CC
  1B  [ │ 2     13 │ ]  4B
  1Y  [ │ 3     12 │ ]  4A
  2A  [ │ 4     11 │ ]  4Y
  2B  [ │ 5     10 │ ]  3B
  2Y  [ │ 6      9 │ ]  3A
 GND  [ │ 7      8 │ ]  3Y
        └──────────┘
```

description

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.
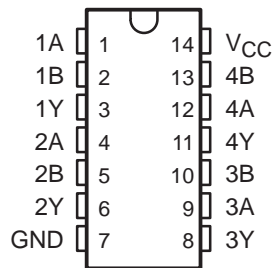
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54F86 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F86 is characterized for operation from 0°C to 70°C.
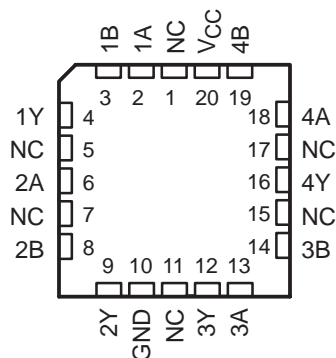
SN54F86 . . . FK PACKAGE
(TOP VIEW)

```
            1B 1A NC V_CC 4B
             3  2  1  20 19
  1Y  [  4               18  ]  4A
  NC  [  5               17  ]  NC
  2A  [  6               16  ]  4Y
  NC  [  7               15  ]  NC
  2B  [  8               14  ]  3B
             9 10 11 12 13
            2Y GND NC 3Y 3A
```

NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†

```
 1A  1 ──┐   ┌──────────┐
         │   │   = 1    │   3
 1B  2 ──┤   │          ├──────  1Y
         │   │          │
 2A  4 ──┤   │          │   6
         │   │          ├──────  2Y
 2B  5 ──┤   │          │
         │   │          │
 3A  9 ──┤   │          │   8
         │   │          ├──────  3Y
 3B 10 ──┤   │          │
         │   │          │
 4A 12 ──┤   │          │  11
         │   │          ├──────  4Y
 4B 13 ──┘   └──────────┘
```
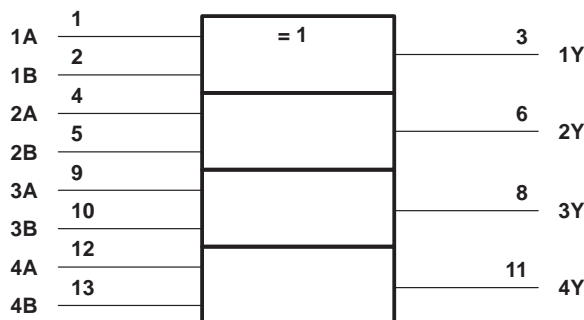
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

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TEXAS INSTRUMENTS

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SN54F86, SN74F86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.
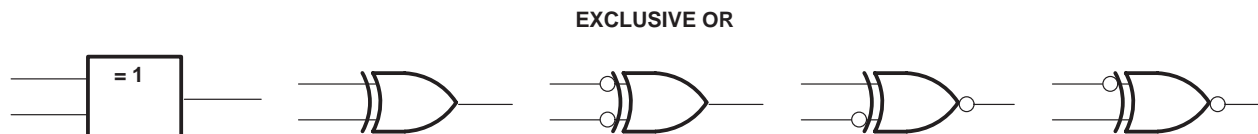
EXCLUSIVE OR

These are five equivalent exclusive-OR symbols valid for an 'F86 gate in positive logic; negation may be shown at any two ports.
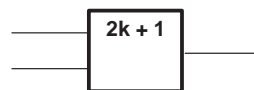
LOGIC-IDENTITY ELEMENT	EVEN-PARITY ELEMENT	ODD-PARITY ELEMENT
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).	The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.	The output is active (high) if an odd number of outputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−1.2 V to 7 V
Input current range	−30 mA to 5 mA
Voltage range applied to any output in the high state	−0.5 V to V_{CC}
Current into any output in the low state	40 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
N package	78°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54F86			SN74F86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F86 MIN	SN54F86 TYP†	SN54F86 MAX	SN74F86 MIN	SN74F86 TYP†	SN74F86 MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5$ V,	$I_{OH} = -1$ mA	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75$ V,	$I_{OH} = -1$ mA				2.7			
V_{OL}	$V_{CC} = 4.5$ V,	$I_{OL} = 20$ mA		0.3	0.5		0.3	0.5	V
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	µA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.5$ V			-0.6			-0.6	mA
I_{OS}‡	$V_{CC} = 5.5$ V,	$V_O = 0$	-60		-150	-60		-150	mA
I_{CCH}	$V_{CC} = 5.5$ V,	See Note 3		15	23		15	23	mA
I_{CCL}	$V_{CC} = 5.5$ V,	$V_I = 4.5$ V		18	28		18	28	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: I_{CCH} is measured with outputs open, and the A or B input (not both) at 4.5 V. Remaining inputs are grounded.

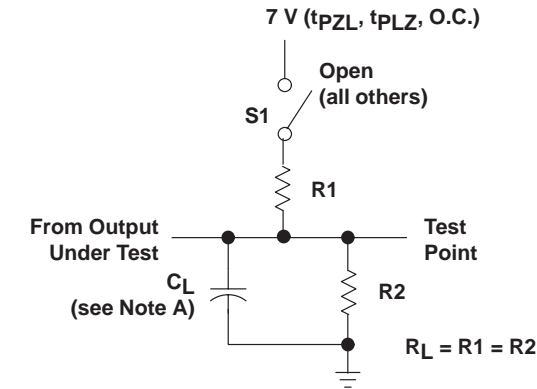## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $C_L = 50$ pF, $R_L = 500$ Ω, $T_A = 25°C$ 'F86 MIN	'F86 TYP	'F86 MAX	$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_L = 500$Ω, T_A = MIN to MAX§ SN54F86 MIN	SN54F86 MAX	SN74F86 MIN	SN74F86 MAX	UNIT
t_{PLH}	A or B (other input low)	Y	3	4	5.5	3	7	3	6.5	ns
t_{PHL}			3	4.2	5.5	2.6	8	3	6.5	
t_{PLH}	A or B (other input high)	Y	3.5	5.3	7	3.5	10	3.5	8	ns
t_{PHL}			3	4.7	6.5	3	8	3	7.5	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
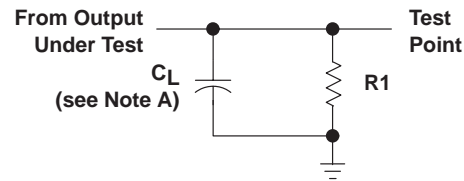
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INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

7 V (t_{PZL}, t_{PLZ}, O.C.)

Open (all others)

S1

R1

From Output Under Test

Test Point

C_L (see Note A)

R2

R_L = R1 = R2

LOAD CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR OUTPUTS

From Output Under Test

Test Point

C_L (see Note A)

R1

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

Timing Input (see Note C)

1.5 V

3 V

0 V

t_{su}

t_h

Data Input (see Note C)

1.5 V

1.5 V

3 V

0 V
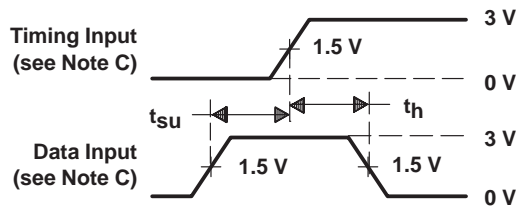
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

High-Level Pulse (see Note C)

1.5 V

1.5 V

3 V

0 V

t_w

Low-Level Pulse

1.5 V

1.5 V

3 V

0 V
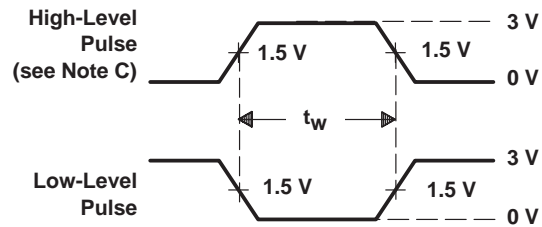
VOLTAGE WAVEFORMS PULSE DURATION

Input (see Note C)

1.5 V

1.5 V

3 V

0 V

t_{PLH}

t_{PHL}

In-Phase Output (see Note E)

1.5 V

1.5 V

V_{OH}

V_{OL}

t_{PHL}

t_{PLH}

Out-of-Phase Output (see Note E)

1.5 V

1.5 V

V_{OH}

V_{OL}
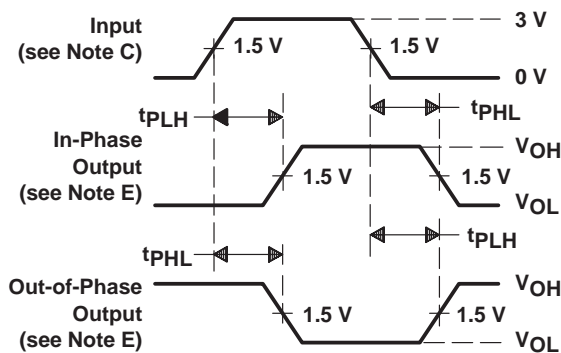
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)

Output Control (low-level enable)

1.5 V

1.5 V

3 V

0 V

t_{PZL}

t_{PLZ}

Waveform 1 (see Notes B and E)

1.5 V

3.5 V

V_{OL}

0.3 V

t_{PZH}

t_{PHZ}

Waveform 2 (see Notes B and E)

1.5 V

V_{OH}

0.3 V

0 V
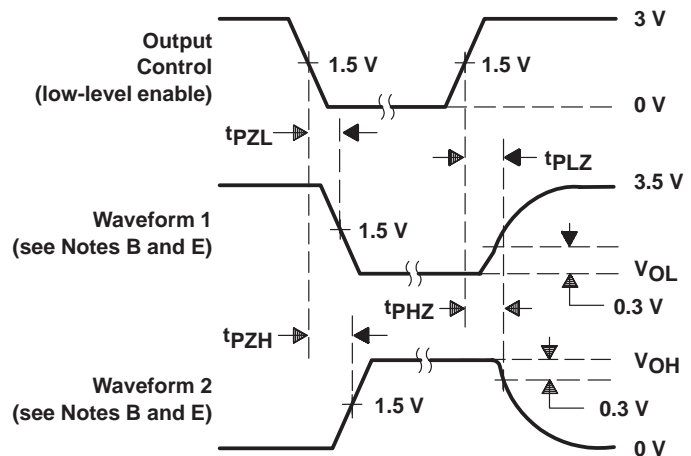
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, t_r = t_f $\leq$ 2.5 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F86D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F86	Samples
SN74F86DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F86	Samples
SN74F86DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F86	Samples
SN74F86N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F86N	Samples
SN74F86NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F86N	Samples
SN74F86NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F86	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74F86NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F86DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74F86NSR	SO	NS	14	2000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74F86D	D	SOIC	14	50	506.6	8	3940	4.32
SN74F86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F86N	N	PDIP	14	25	506	13.97	11230	4.32
SN74F86NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74F86NE4	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03
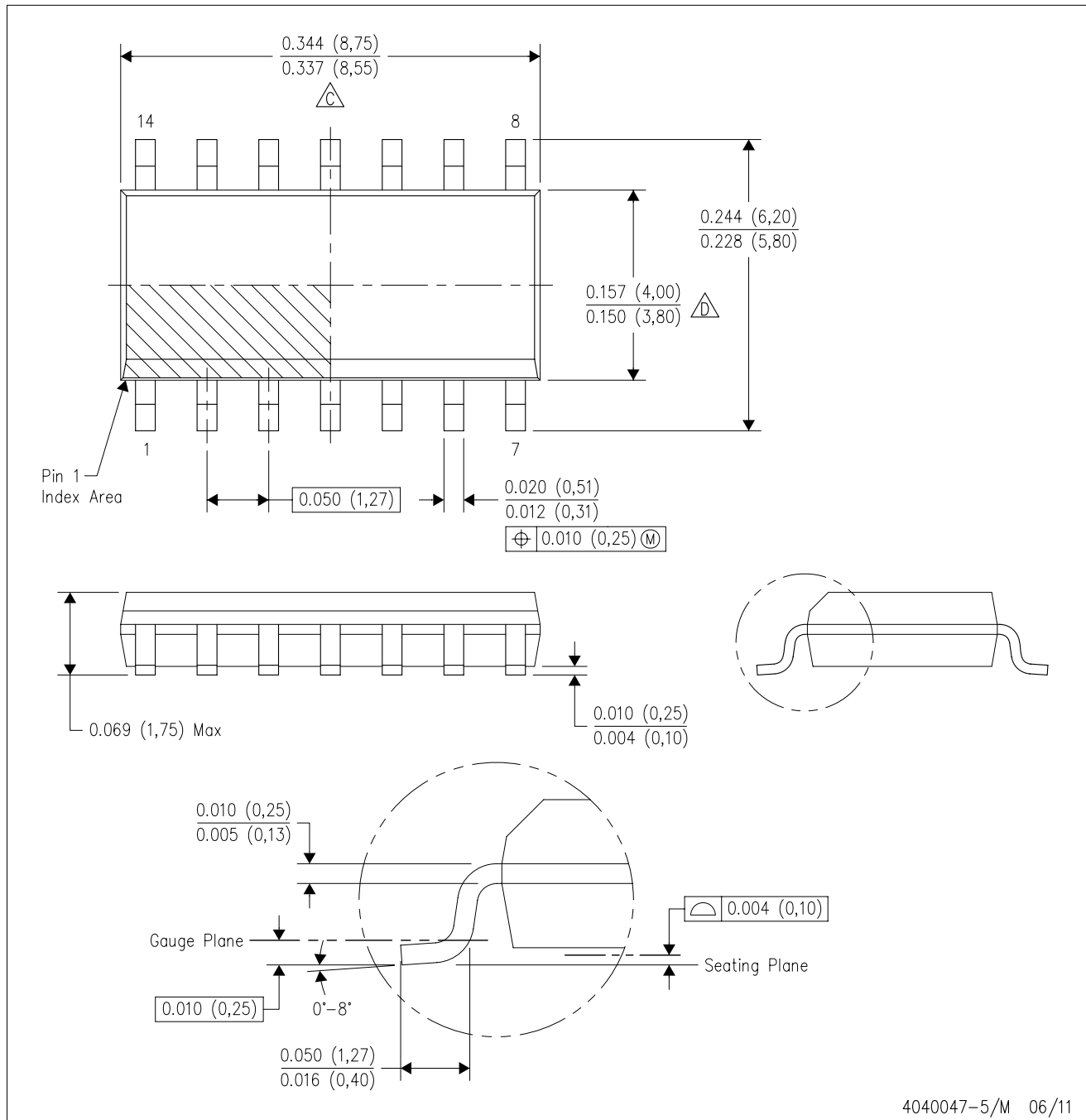
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
△C

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
         △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AB.

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D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0.07

All Around

Example
Solder Mask Opening
(See Note E)

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16　　　　　　9

0.260 (6,60)
0.240 (6,10)

1　　　　　　8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES:　A.　All linear dimensions are in inches (millimeters).
　　　　　B.　This drawing is subject to change without notice.
　　　⚠C　Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
　　　⚠D　The 20 pin end lead shoulder width is a vendor option, either half or full width.

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