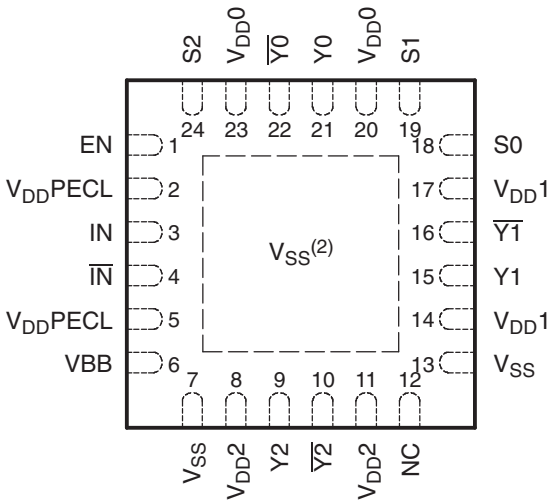
1:3 LVPECL CLOCK BUFFER WITH PROGRAMMABLE DIVIDER

FEATURES

- **Distributes One Differential Clock Input to Three LVPECL Differential Clock Outputs**
- **Programmable Output Divider for Two LVPECL Outputs**
- **Low-Output Skew 15 ps (Typical)**
- **V_{CC} Range 3 V–3.6 V**
- **Signaling Rate Up to 800-MHz LVPECL**
- **Differential Input Stage for Wide Common-Mode Range**
- **Provides VBB Bias Voltage Output for Single-Ended Input Signals**
- **Receiver Input Threshold ±75 mV**
- **24-Terminal QFN Package (4 mm × 4 mm)**
- **Accepts Any Differential Signaling: LVDS, HSTL, CML, VML, SSTL-2, and Single-Ended: LVTTL/LVCMOS**

RGE PACKAGE
(TOP VIEW)



(2) Thermal pad must be connected to V_{SS}.

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SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Additional temperature ranges available - contact factory

DESCRIPTION/ORDERING INFORMATION

The CDCP1803 clock driver distributes one pair of differential clock inputs to three pairs of LVPECL differential clock outputs Y[2:0] and $\overline{Y}$[2:0] with minimum skew for clock distribution. The CDCP1803 is specifically designed for driving 50-Ω transmission lines.

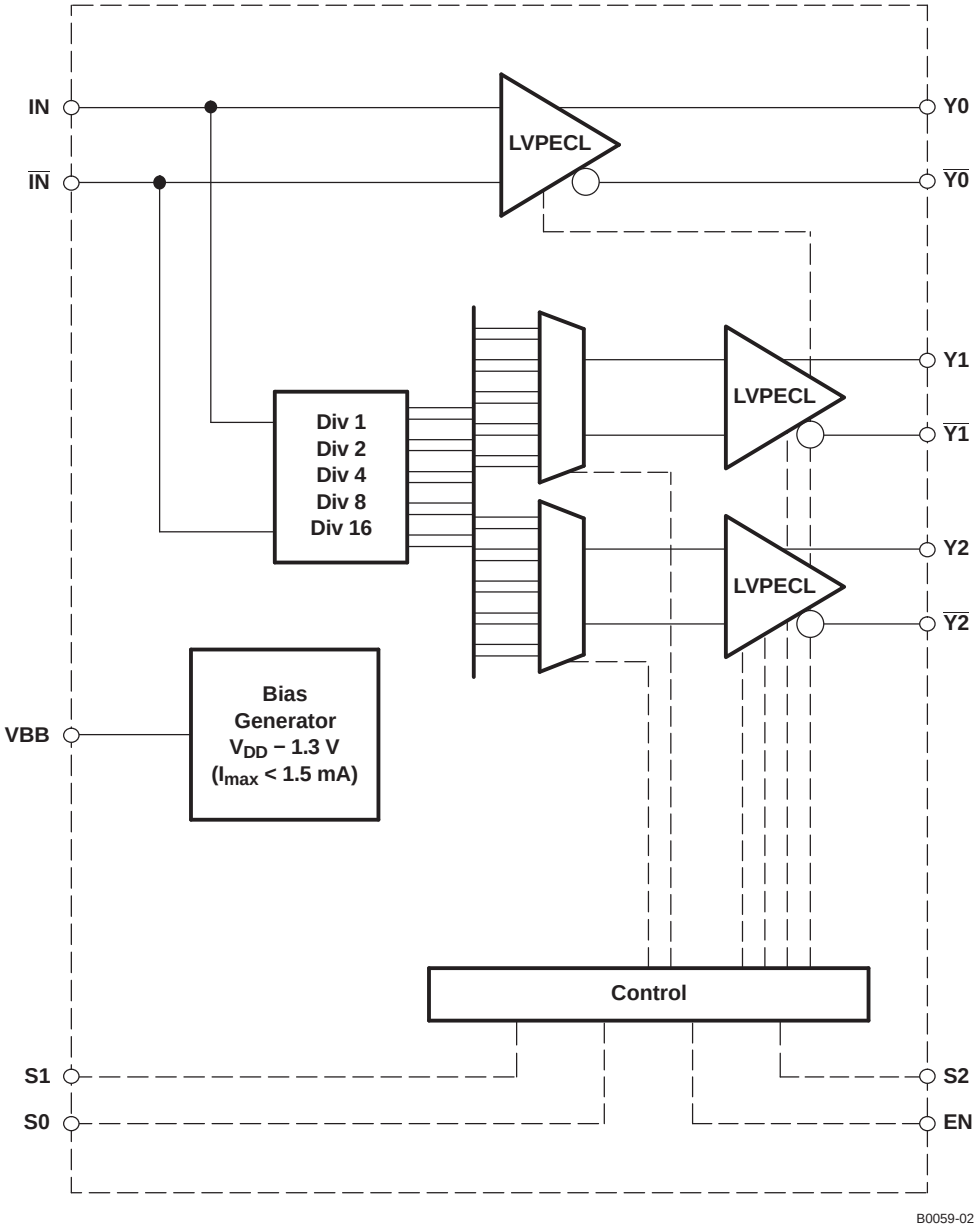
The CDCP1803 has three control terminals, S0, S1, and S2, to select different output mode settings; see Table 1 for details. The CDCP1803 is characterized for operation from –55°C to 125°C. For use in single-ended driver applications, the CDCP1803 also provides a VBB output terminal that can be directly connected to the unused input as a common-mode voltage reference.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	VQFN-RGE	Reel of 250	CDCP1803MRGETEP	CDCP1803EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	1	I (with 60-kΩ pullup)	ENABLE: Enables or disables all outputs simultaneously. EN = 1: outputs on according to S[2:0] settings EN = 0: outputs Y[2:0] off (high impedance) See Table 1 for details.
IN, $\overline{IN}$	3, 4	I (differential)	Differential input clock. Input stage is sensitive and has a wide common-mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Because the input is high-impedance, it is recommended to terminate the PCB transmission line before the input (e.g., with 100 Ω across input). Input can also be driven by a single-ended signal if the complementary input is tied to VBB. A more-advanced scheme for single-ended signals is given in the *Application Information* section near the end of this document. The inputs employ an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than ~0.7 V. Reverse biasing of the IC through these inputs is possible and must be prevented by limiting the input voltage < V_{DD}.
NC	12		No connect. Leave this terminal open or tie to ground.
S[2:0]	24, 19, 18	I (with 60-kΩ pullup)	Select mode of operation. Defines the output configuration of Y[2:0], see Table 1 for configuration.
VBB	6	O	Bias voltage output can be used to bias unused complementary input $\overline{IN}$ for single-ended input signals. The output voltage of VBB is V_{DD} – 1.3 V. When driving a load, the output current drive is limited to about 1.5 mA.
V_{DD}PECL	2, 5	Supply	Supply voltage PECL input + internal logic
V_{DD}[2:0]	8, 11, 14, 17, 20, 23	Supply	PECL output supply voltage for output Y[2:0]. Each output can be disabled by pulling the corresponding V_{DD}x to GND. **CAUTION:** In this mode, no voltage from outside may be forced, because internal diodes could be forced in forward direction. Thus, it is recommended to disconnect the output if it is not being used.
V_{SS}	7, 13	Supply	Device ground
$\overline{Y[2:0]}$ Y[2:0]	9, 15, 21 10, 16, 22	O (LVPECL)	LVPECL clock outputs. These outputs provide low-skew copies of IN or down-divided copies of clock IN based on selected mode of operation S[2:0]. If an output is unused, the output can simply be left open to save power and minimize noise impact to the remaining outputs.

CONTROL TERMINAL SETTINGS

The CDCP1803 has three control terminals (S0, S1, and S2) and an enable terminal (EN) to select different output mode settings.

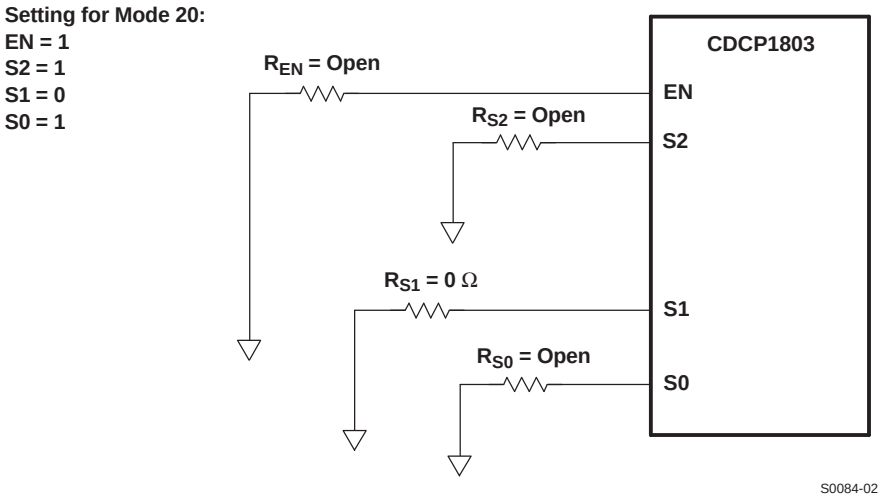


Figure 1. Control Terminal Setting for Example

Table 1. Selection Mode Table

					LVPECL[1]		
MODE	**EN**	**S2**	**S1**	**S0**	**Y0**	**Y1**	**Y2**
0	0	x	x	x	Off (high-z)		
1	1	0	0	0	÷ 1	÷ 1	÷ 1
2	1	0	0	$V_{DD}/2$	÷ 1	Off (high-z)	Off (high-z)
3	1	0	0	1	÷ 1	÷ 1	Off (high-z)
4	1	0	$V_{DD}/2$	0	÷ 1	÷ 2	Off (high-z)
5	1	0	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 4	Off (high-z)
6	1	0	$V_{DD}/2$	1	÷ 1	÷ 8	Off (high-z)
7	1	0	1	0	÷ 1	Off (high-z)	÷ 1
8	1	0	1	1	÷ 1	÷ 2	÷ 1
9	1	$V_{DD}/2$	0	0	÷ 1	÷ 4	÷ 1
10	1	$V_{DD}/2$	0	$V_{DD}/2$	÷ 1	÷ 8	÷ 1
11	1	$V_{DD}/2$	0	1	÷ 1	Off (high-z)	÷ 2
12	1	$V_{DD}/2$	$V_{DD}/2$	0	÷ 1	÷ 1	÷ 2
13	1	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 2	÷ 2
14	1	$V_{DD}/2$	$V_{DD}/2$	1	÷ 1	÷ 4	÷ 2
15	1	$V_{DD}/2$	1	0	÷ 1	÷ 8	÷ 2
16	1	$V_{DD}/2$	1	$V_{DD}/2$	÷ 1	Off (high-z)	÷ 4
17	1	$V_{DD}/2$	1	1	÷ 1	÷ 1	÷ 4
18	1	1	0	0	÷ 1	÷ 2	÷ 4
19	1	1	0	$V_{DD}/2$	÷ 1	÷ 4	÷ 4
20	1	1	0	1	÷ 1	÷ 8	÷ 4
21	1	1	$V_{DD}/2$	0	÷ 1	Off (high-z)	÷ 8
22	1	1	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 1	÷ 8
23	1	1	$V_{DD}/2$	1	÷ 1	÷ 2	÷ 8
24	1	1	1	0	÷ 1	÷ 4	÷ 8
25	1	1	1	$V_{DD}/2$	÷ 1	÷ 8	÷ 8
26	1	1	1	1	÷ 1	Off (high-z)	÷ 16
27	$V_{DD}/2$	0	0	0	÷ 1	÷ 1	÷ 16
28	$V_{DD}/2$	0	0	$V_{DD}/2$	÷ 1	÷ 2	÷ 16
29	$V_{DD}/2$	0	0	1	÷ 1	÷ 4	÷ 16
30	$V_{DD}/2$	0	$V_{DD}/2$	0	÷ 1	÷ 8	÷ 16
Rsv	$V_{DD}/2$	1	$V_{DD}/2$	1	Reserved	Reserved	Reserved
Rsv	$V_{DD}/2$	1	1	0	N/A	Low	Low

(1) The LVPECL outputs are open-emitter stages. Thus, if the unused LVPECL outputs Y0, Y1, or Y2 are left unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding V_{DD} input to GND.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

V_{DD}	Supply voltage	–0.3 V to 3.8 V
V_I	Input voltage	–0.2 V to (V_{DD} + 0.2 V)
V_O	Output voltage	–0.2 V to (V_{DD} + 0.2 V)
	Differential short-circuit current, Yn, $\overline{Yn}$, I_{OSD}	Continuous
	Electrostatic discharge (HBM 1.5 kΩ, 100 pF), ESD	>2000 V
	Moisture level 24-terminal QFN package (solder reflow temperature of 235°C) MSL	2
T_{stg}	Storage temperature	–65°C to 150°C
T_J	Maximum junction temperature	150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

LVPECL INPUT IN, $\overline{IN}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Input frequency		0		800	MHz
V_{CM}	High-level input common mode		1		V_{DD} – 0.3	V
V_{IN}	Input voltage swing between IN and $\overline{IN}$(1)		500		1300	mV
	Input voltage swing between IN and $\overline{IN}$ (2)		125		1300	
I_{IN}	Input current	V_I = V_{DD} or 0 V			±10	µA
R_{IN}	Input impedance		300			kΩ
C_I	Input capacitance at IN, $\overline{IN}$			1		pF

(1) Is required to maintain ac specifications
(2) Is required to maintain device functionality

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

LVPECL OUTPUT DRIVER Y[2:0], $\overline{Y[2:0]}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Output frequency, see Figure 3.		0		800	MHz
V_{OH}	High-level output voltage	Termination with 50 Ω to V_{DD} – 2 V	V_{DD} – 1.18		V_{DD} – 0.81	V
V_{OL}	Low-level output voltage	Termination with 50 Ω to V_{DD} – 2 V	V_{DD} – 1.98		V_{DD} – 1.55	V
V_O	Output voltage swing between Y and $\overline{Y}$, see Figure 3.	Termination with 50 Ω to V_{DD} – 2 V	500			mV
I_{OZL}	Output 3-state current	V_{DD} = 3.6 V, V_O = 0 V			5	µA
I_{OZH}		V_{DD} = 3.6 V, V_O = V_{DD} – 0.8 V			10	
t_r/t_f	Rise and fall times	20% to 80% of V_{OUTPP}, see Figure 8.	170		400	ps
$t_{skpecl(o)}$	Output skew between any LVPECL output Y[2:0] and $\overline{Y[2:0]}$	See Note A in Figure 7.		15	70	ps
t_{Duty}	Output duty-cycle distortion(1)	Crossing point-to-crossing point distortion	–50		50	ps
$t_{sk(pp)}$	Part-to-part skew	Any Y, see Note B in Figure 7.		50		ps
C_O	Output capacitance	V_O = V_{DD} or GND		1		pF
LOAD	Expected output load			50		Ω

(1) For an 800-MHz signal, the 50-ps error would result in a duty cycle distortion of ±4% when driven by an ideal clock input signal.

LVPECL INPUT-TO-LVPECL OUTPUT PARAMETERS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(lh)}$	Propagation delay, rising edge	VOX to VOX	320		600	ps
$t_{pd(hl)}$	Propagation delay, falling edge	VOX to VOX	320		600	ps
$t_{sk(p)}$	LVPECL pulse skew	VOX to VOX, see Note C in Figure 7.			100	ps

JITTER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
JITTER CHARACTERISTICS						
$t_{jitterLVPECL}$	Additive phase jitter from input to LVPECL output Y[2:0], see Figure 2.	12 kHz to 20 MHz, f_{out} = 250 MHz to 800 MHz, divide-by-1 mode		0.15		ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz to 800 MHz, divide-by-1 mode		0.25		

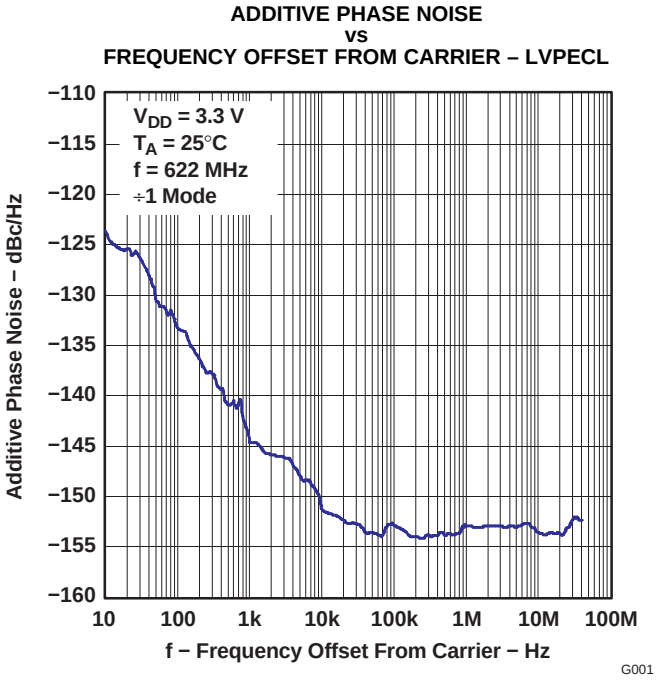


Figure 2.

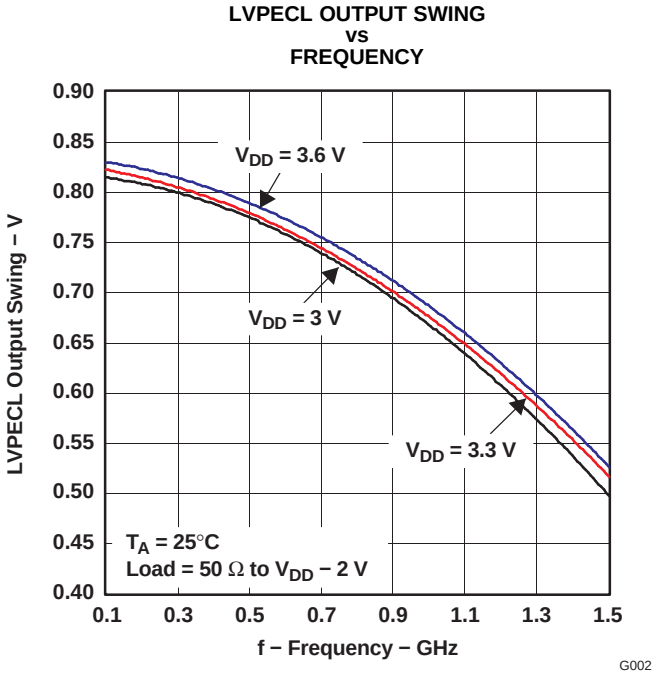


Figure 3.

SUPPLY CURRENT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Full load	All outputs enabled and terminated with 50 Ω to V_{DD} – 2 V on LVPECL outputs, f = 800 MHz for LVPECL outputs, V_{DD} = 3.3 V		140		mA
		No load	Outputs enabled, no output load, f = 800 MHz for LVPECL outputs, V_{DD} = 3.6 V			90	
	Supply current saving per LVPECL output stage disabled, no load		f = 800 MHz for LVPECL output, V_{DD} = 3.3 V		10		
I_{DDZ}	Supply current, 3-state		All outputs in high-impedance state by control logic, f = 0 Hz, V_{DD} = 3.6 V			0.5	mA

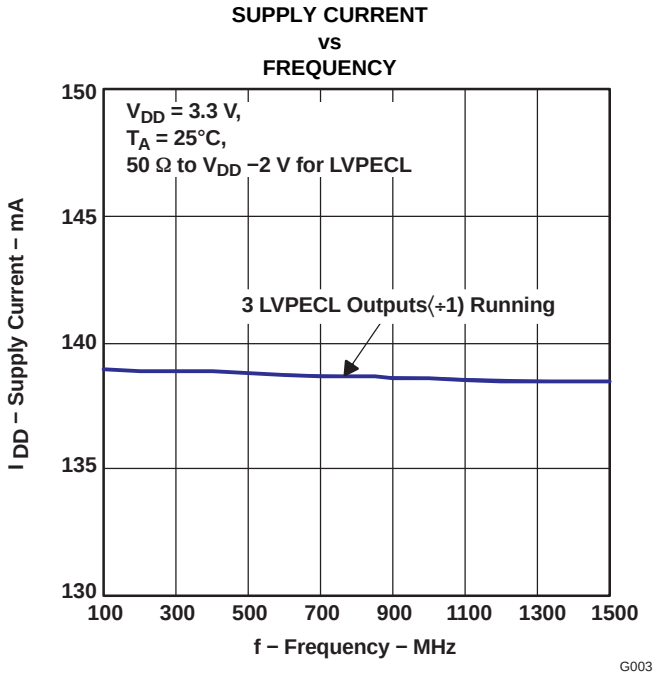


Figure 4.

PACKAGE THERMAL RESISTANCE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA-1}$	QFN-24 package thermal resistance(1)	4-layer JEDEC test board (JESD51-7), airflow = 0 ft/min		106.6		°C/W
$R_{\theta JA-2}$	QFN-24 package thermal resistance with thermal vias in PCB(1)	4-layer JEDEC test board (JESD51-7) with four thermal vias of 22-mil diameter each, airflow = 0 ft/min		55.4		°C/W

(1) It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

Example:

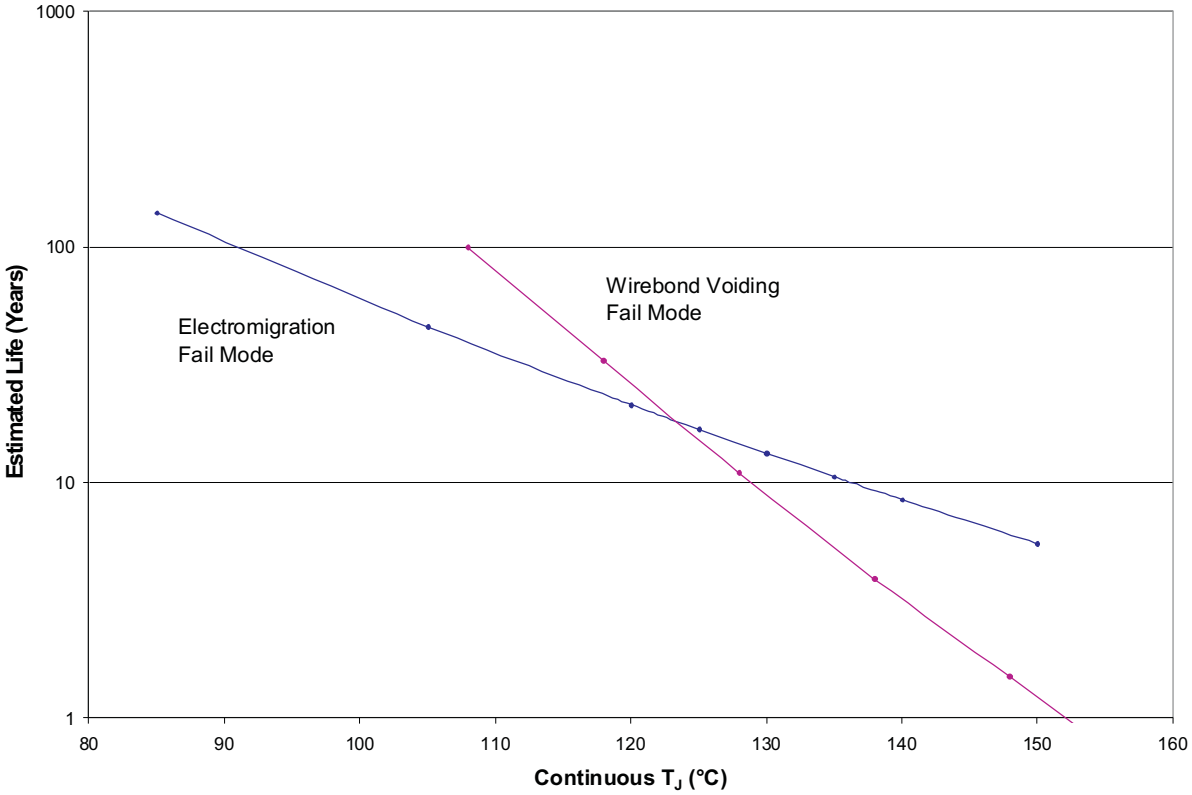
Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

$T_{Chassis}$ = 125°C (temperature of the chassis)

$P_{effective} = I_{max} \times V_{max}$ = 90 mA × 3.6 V = 324 mW (max power consumption inside the package)

$\theta T_{Junction} = \theta_{JA-2} \times P_{effective}$ = 55.45°C/W × 324 mW = 17.97°C

$T_{Junction} = \theta T_{Junction} + T_{Chassis}$ = 17.97°C + 125°C = 143°C (see Figure 5 for expected life with continuous 125°C operation)



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 5. Operating Life Derating Chart

CONTROL INPUT CHARACTERISTICS

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	Setup time, S0, S1, S2, and EN terminals before clock IN		25			ns
t_h	Hold time, S0, S1, S2, and EN terminals after clock IN		0			ns
$t_{(disable)}$	Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)			10		ns
$t_{(enable)}$	Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals)			1		µs
Rpullup	Internal pullup resistor on S[2:0] and EN input			60		kΩ
$V_{IH(H)}$	Three-level input high, S0, S1, S2, and EN terminals(1)		0.9 V_{DD}			V
$V_{IL(L)}$	Three-level low, S0, S1, S2, and EN terminals				0.1 V_{DD}	V
I_{IH}	Input current, S0, S1, S2, and EN terminals	$V_I = V_{DD}$			–5	µA
I_{IL}		V_I = GND	38		85	µA

(1) Leaving this terminal floating automatically pulls the logic level high to V_{DD} through an internal pullup resistor of 60 kΩ.

BIAS VOLTAGE VBB

over operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBB	Output reference voltage	V_{DD} = 3 V–3.6 V, I_{BB} = –0.2 mA	V_{DD} – 1.4		V_{DD} – 1.1	V

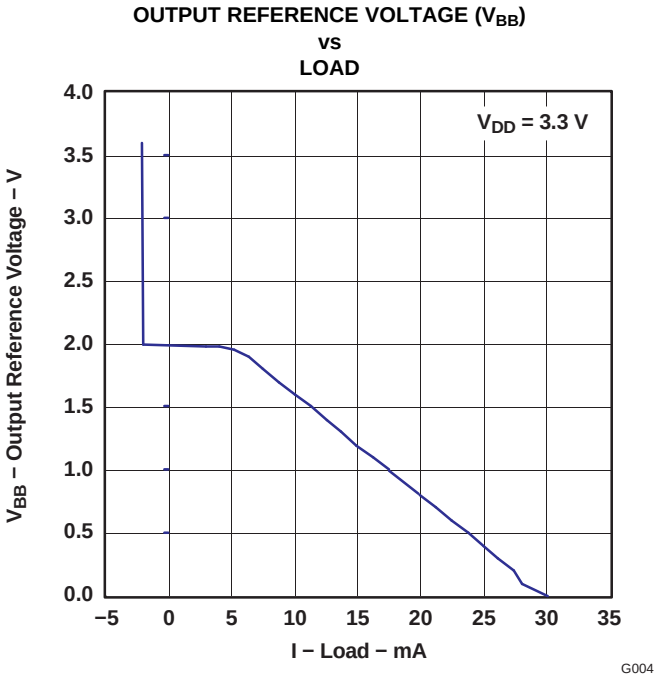
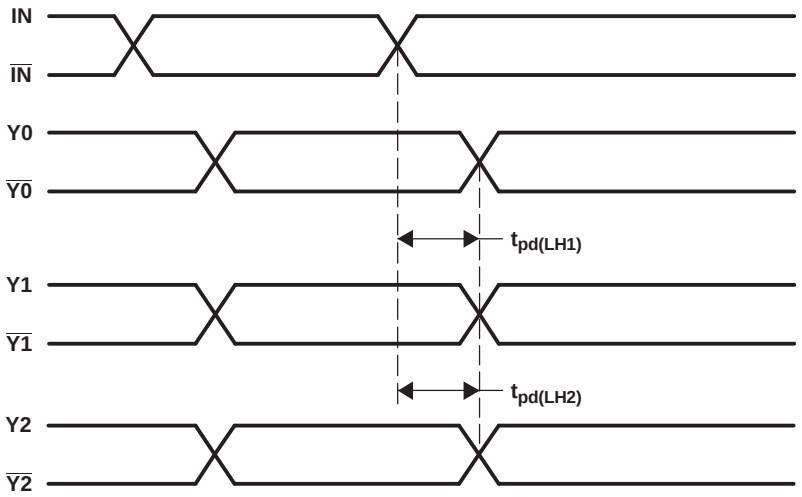


Figure 6.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ (n = 0…2)
- The difference between the fastest and the slowest $t_{pd(HL)n}$ (n = 0…2)

B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ (n = 0…2 for LVPECL, n = 3 for LVCMOS) across multiple devices
- The difference between the fastest and the slowest $t_{pd(HL)n}$ (n = 0…2 for LVPECL, n = 3 for LVCMOS) across multiple devices

C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd(HL)}$) and the low-to-high ($t_{pd(LH)}$) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = | t_{pd(HL)} - t_{pd(LH)} |$. Pulse skew is sometimes referred to as *pulse width distortion or duty cycle skew.*

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Figure 7. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

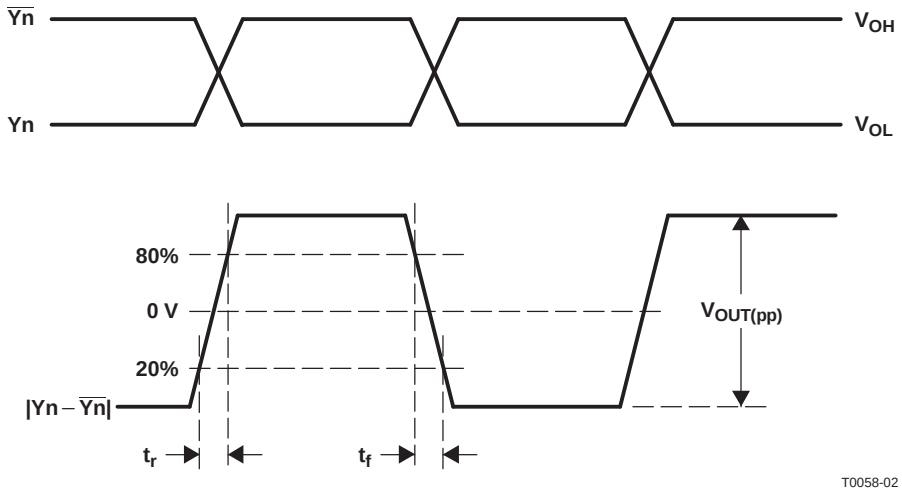


Figure 8. LVPECL Differential Output Voltage and Rise/Fall Time

PCB DESIGN FOR THERMAL FUNCTIONALITY

It is recommended to take special care of the PCB design for good thermal flow from the QFN 24-terminal package to the PCB.

Due to the three LVPECL outputs, the current consumption of the CDCP1803 is fixed.

JEDEC JESD51-7 specifies thermal conductivity for standard PCB boards.

PARAMETER MEASUREMENT INFORMATION (continued)

Modeling the CDCP1803 with a standard 4-layer JEDEC board results in a 59.5°C maximum temperature with $R_{\theta JA}$ of 106.62°C/W for 25°C ambient temperature.

When deploying four thermal vias (one per quadrant), the thermal flow improves significantly, yielding 42.9°C maximum temperature with $R_{\theta JA}$ of 55.4°C/W for 25°C ambient temperature.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications enabling all four outputs at once.

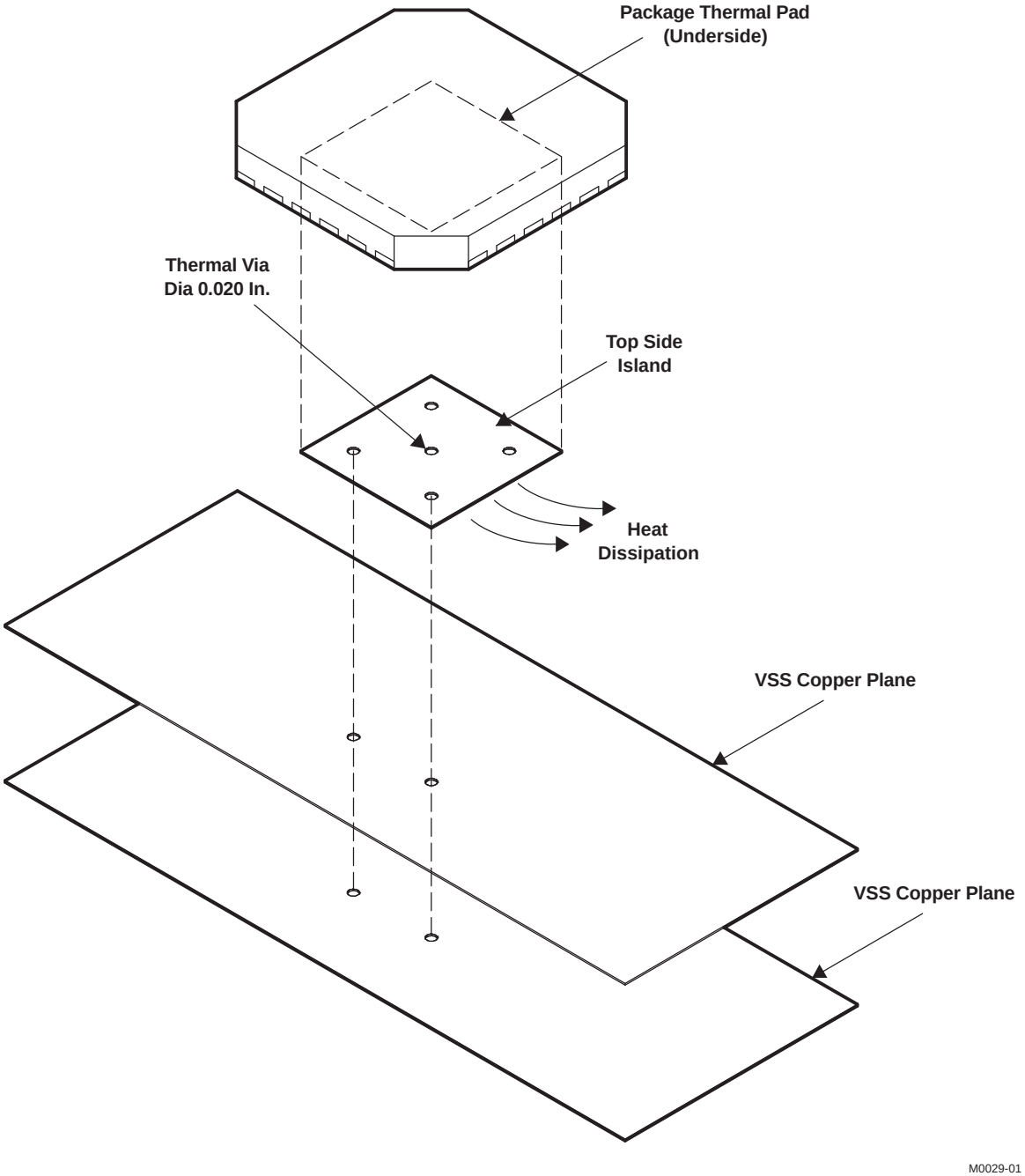


Figure 9. Recommended Thermal Via Placement

See the *Quad Flatpack No-Lead Logic Packages* (SCBA017) and *QFN/SON PCB Attachment* (SLUA271) application reports for further package-related information.

APPLICATION INFORMATION

LVPECL RECEIVER INPUT TERMINATION

The input of the CDCP1803 has a high impedance and comes with a large common-mode voltage range.

For optimized noise performance, it is recommended to properly terminate the PCB trace (transmission line). If a differential signal drives the CDCP1803, then a 100-Ω termination resistor is recommended to be placed as close as possible across the input terminals. An even better approach is to install 2 × 50-Ω resistors, with the center tap connected to a capacitor (C) to terminate odd-mode noise and make up for transmission line mismatches. The VBB output can also be connected to the center tap to bias the input signal to (V_{DD} – 1.3 V) (see Figure 10).

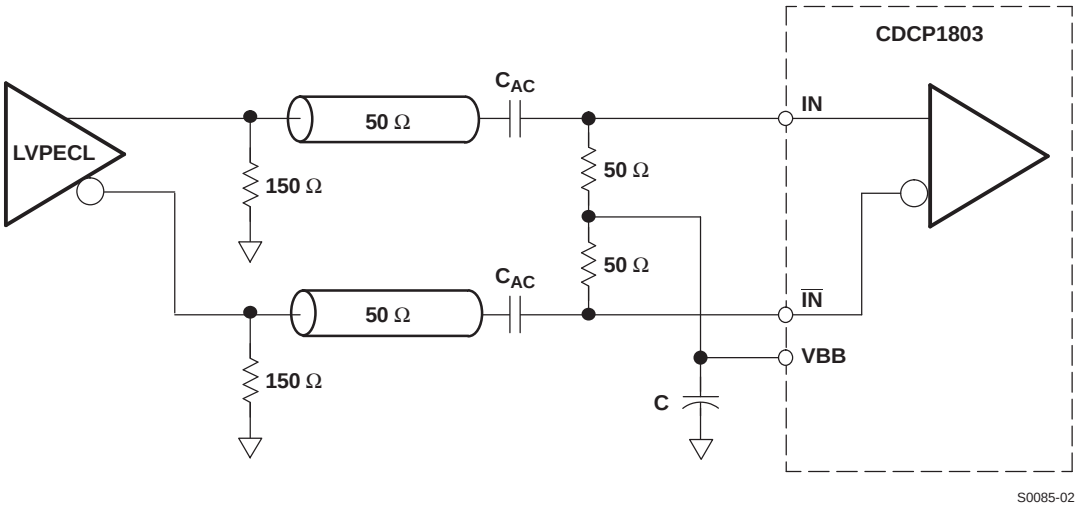


Figure 10. Recommended AC-Coupling LVPECL Receiver Input Termination

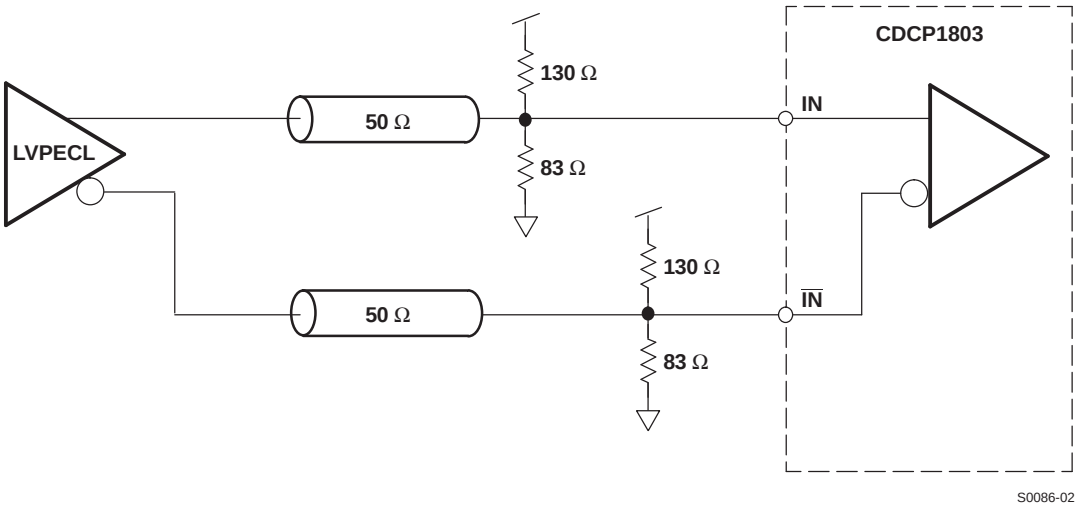
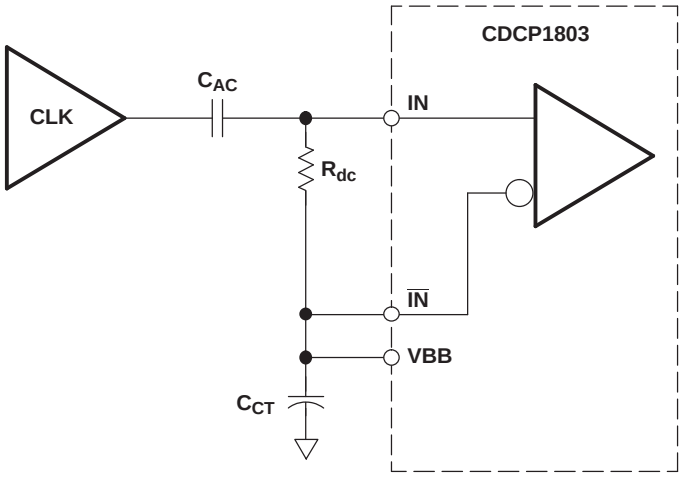


Figure 11. Recommended DC-Coupling LVPECL Receiver Input Termination

The CDCP1803 can also be driven by single-ended signals. Typically, the input signal becomes connected to one input, while the complementary input must be properly biased to the center voltage of the incoming input signal. For LVCMOS signals, this would be $V_{CC}/2$, realized by a simple voltage divider (e.g., two 10-kΩ resistors). The best option (especially if the dc offset of the input signal might vary) is to ac-couple the input signal and then rebias the signal using the VBB reference output. See Figure 12.



NOTE: C_{AC} − AC-coupling capacitor (e.g., 10 nF)
C_{CT} − Capacitor keeps voltage at $\overline{IN}$ constant (e.g., 10 nF)
R_{dc} − Load and correct duty cycle (e.g., 50 Ω)
VBB − Bias voltage output

S0087-02

Figure 12. Typical Application Setting for Single-Ended Input Signals Driving the CDCP1803

DEVICE BEHAVIOR DURING RESET AND CONTROL-TERMINAL SWITCHING

Output Behavior From Enabling the Device (EN = 0 → 1)

In disable mode (EN = 0), all output drivers are switched in high-Z mode. The S[2:0] control inputs are also switched off. In the same mode, all flip-flops are reset. The typical current consumption is below 500 µA.

When the device is enabled again, it takes typically 1 µs for the settling of the reference voltage and currents. During this time, the outputs Y[2:0] and $\overline{Y}$[2:0] drive a high signal. After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device is as shown in Figure 13. The inverting input and output signal is not included. The Y:/1 waveform is the undivided output driver state.

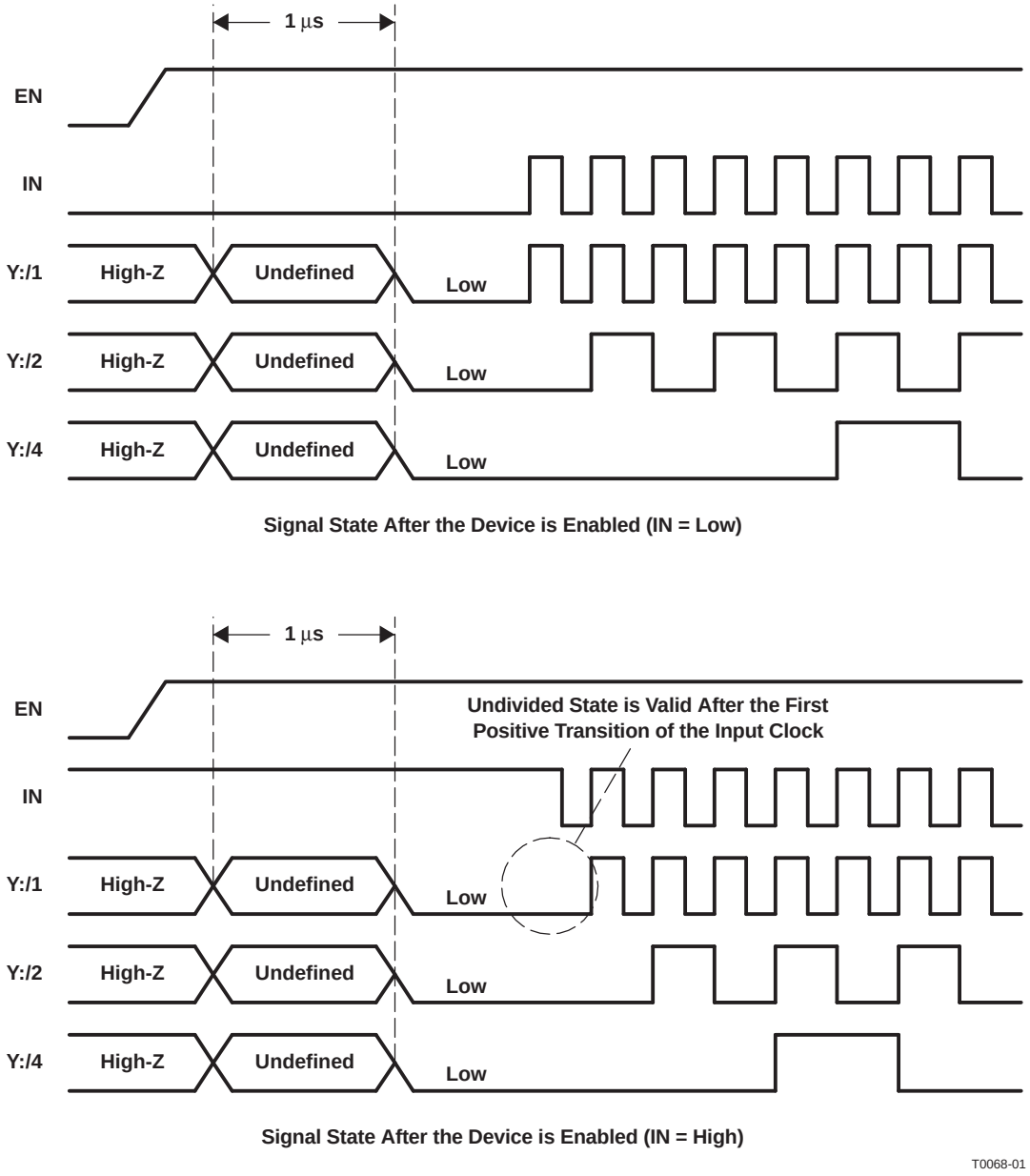


Figure 13. Waveforms

Enabling a Single Output Stage

If a single output stage becomes enabled:

- Y[2:0] is either low or high (undefined).
- $\overline{Y[2:0]}$ is the inverted signal of Y[2:0].

With the first positive clock transition, the undivided output becomes the input clock state. The divided output states are equal to the actual internal divider. The internal divider is not reset while enabling single output drivers.

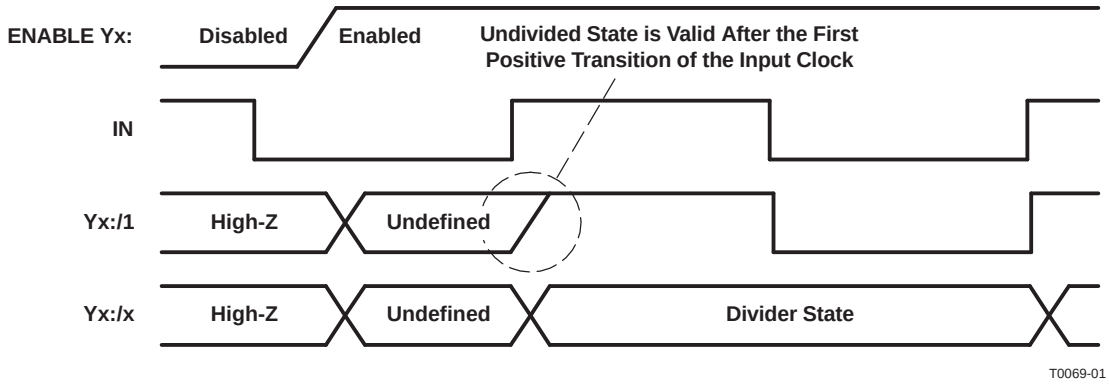


Figure 14. Signal State After an Output Driver Becomes Enabled While IN = 0

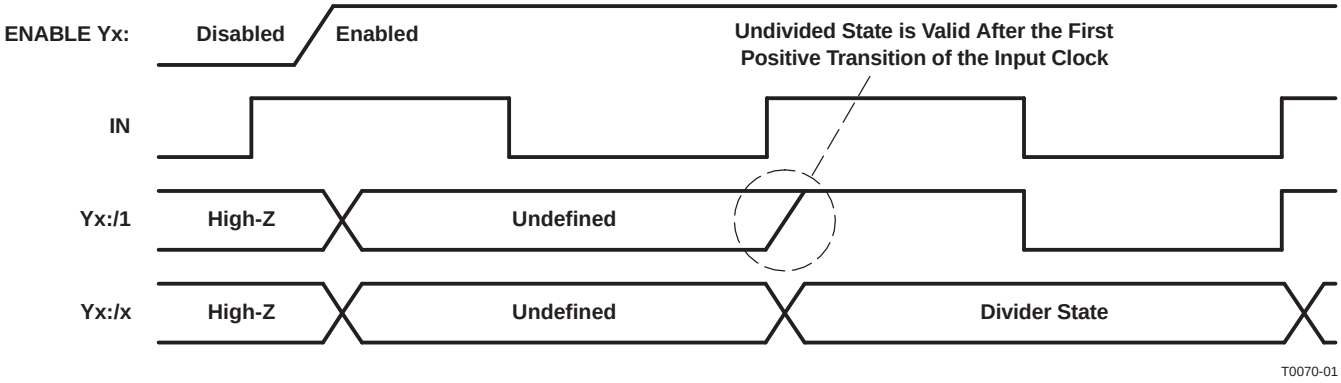


Figure 15. Signal State After an Output Driver Becomes Enabled While IN = 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCP1803MRGETEP	LIFEBUY	VQFN	RGE	24		TBD	Call TI	Call TI	-55 to 125	CDCP 1803EP	
V62/09619-01XE	LIFEBUY	VQFN	RGE	24		TBD	Call TI	Call TI	-55 to 125	CDCP 1803EP	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CDCP1803-EP :

- Catalog: CDCP1803

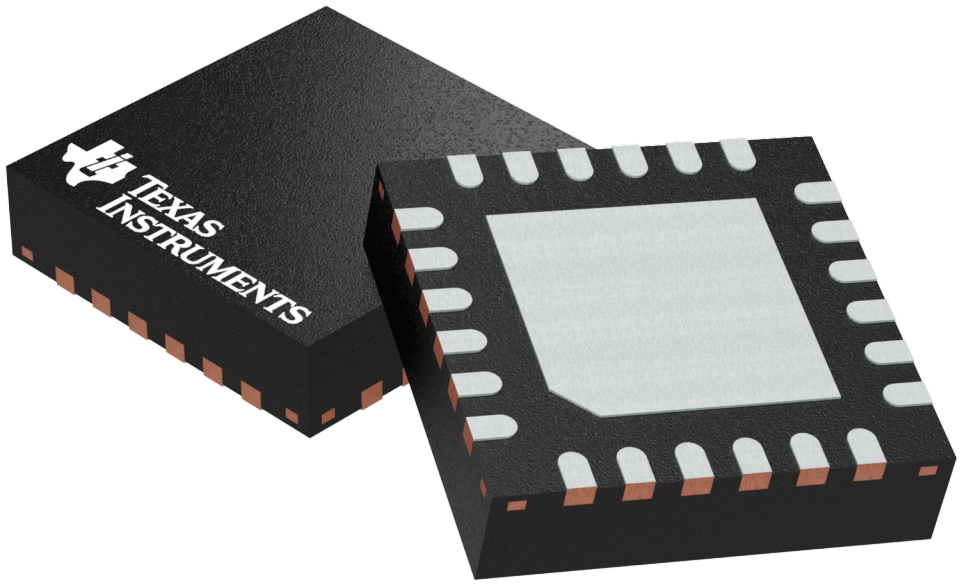
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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