# Onsemi

## **High-Current, Half-Bridge, Gate-Driver IC** FAN73912

#### Description

The FAN73912 is a monolithic half bridge gate-drive IC designed for high-voltage and high-speed driving for MOSFETs and IGBTs that operate up to +1200 V.

The advanced input filter of HIN provides protection against short-pulsed input signals caused by noise.

An advanced level-shift circuit offers high-side gate driver operation up to VS = -9.8 V (typical) for VBS = 15 V. The UVLO circuit prevents malfunction when VCC and VBS are lower than the specified threshold voltage.

Output drivers typically source and sink 2 A and 3 A, respectively.

#### Features

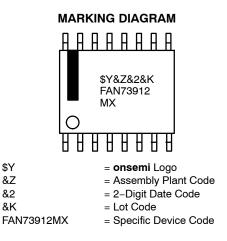
- Floating Channel for Bootstrap Operation to +1200 V
- Typically 2 A/ 3 A Sourcing/Sinking Current Driving Capability for Both Channels
- Gate Driver Supply (VCC) Range from 12 V to 20 V
- Separate Logic Supply (VDD) Range from 3 V to 20 V
- Extended Allowable Negative VS Swing to -9.8 V for Signal Propagation at VCC = VBS = 15 V
- Built-in Cycle-by-Cycle Edge-Triggered Shutdown Logic
- Built-in Shoot-Through Protection Logic
- Common–Mode dv/dt Noise Canceling Circuit
- UVLO Functions for Both Channels
- Built-in Advanced Input Filter
- Matched Propagation Delay Below 50 ns
- Outputs in-Phase with Input Signal
- Logic and Power Ground +/- 10 V Offset
- This Device is Pb-Free and Halogen Free

#### **Typical Application**

- Electrical Contactor
- UPS
- Solar Inverter
- Ballast
- General-Purpose Half-Bridge Topology



SOIC-16W CASE 751BH



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#### **ORDERING INFORMATION**

Device	e Package Shipping	
FAN73912MX	Wide-16	1,000/
(Note 1)	SOIC	Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. This device passed wave-soldering test by JESD22A-111

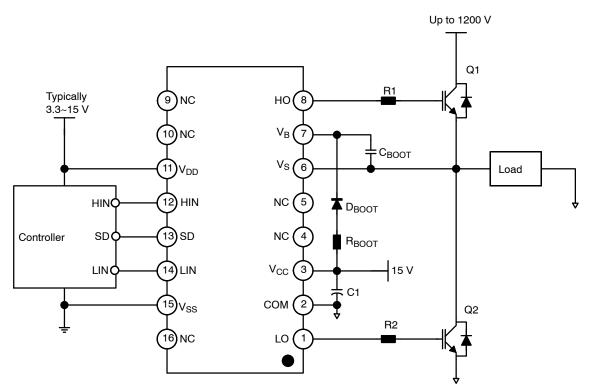


Figure 1. Application Schematic – Adjustable Option

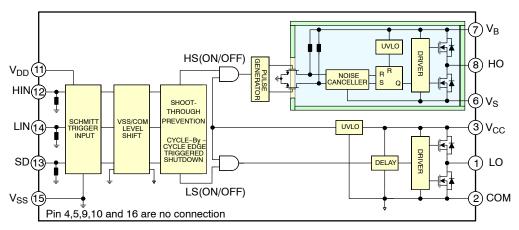


Figure 2. Simplified Block Diagram

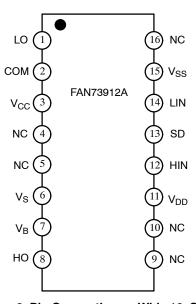


Figure 3. Pin Connections – Wide 16–SOIC (Top View)

#### Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description	
1	LO	Low-Side Driver Output	
2	COM	Low-Side Driver Return	
3	VCC	Low-Side Supply Voltage	
4	NC	No Connection	
5	NC	No Connection	
6	V <sub>S</sub>	High-Voltage Floating Supply Return	
7	V <sub>B</sub>	High-Side Floating Supply	
8	НО	High-Side Driver Output	
9	NC	No Connection	
10	NC	No Connection	
11	V <sub>DD</sub>	Logic Supply Voltage	
12	HIN	Logic Input for High-Side Gate Driver Output	
13	SD	Logic Input for Shutdown	
14	LIN	Logic Input for Low-Side Gate Driver Output	
15	V <sub>SS</sub>	Logic Ground	
16	NC	No Connection	

### FAN73912

Table 2. MAXIMUM RATINGS ( $T_J$ = 25°C, unless otherwise specified. All voltage parameters are referenced to COM unless	
otherwise stated in the table.)	

Symbol	Parameter	Min	Max	Unit
VB	High-Side Floating Supply Voltage	-0.3	1225.0	V
VS	High-Side Floating Offset Voltage	V <sub>B</sub> –25	V <sub>B</sub> +0.3	V
V <sub>HO</sub>	High-Side Floating Output Voltage	V <sub>S</sub> –0.3	V <sub>B</sub> +0.3	V
V <sub>CC</sub>	Low-Side Supply Voltage	-0.3	25	V
$V_{LO}$	Low-Side Floating Output Voltage	-0.3	V <sub>CC</sub> +.0.3	V
$V_{DD}$	Logic Supply Voltage	V <sub>SS</sub> -0.3 -0.3	V <sub>SS</sub> +25 25	V
V <sub>SS</sub>	Logic GND	V <sub>DD</sub> –25	V <sub>DD</sub> +0.3	V
V <sub>IN</sub>	Logic Input Voltage (HIN, LIN and SD)	V <sub>SS</sub> + V <sub>DD</sub> -25.3 -0.3	V <sub>DD</sub> +0.3 25	V
dV <sub>S</sub> /dt	Allowable Offset Voltage Slew Rate	-	±50	V/ns
P <sub>D</sub> (Note 2, 3, 4)	Power Dissipation	-	1.3	W
$\theta_{JA}$	Thermal Resistance	-	95	°C/W
TJ	Junction Temperature	-	150	°C
T <sub>STG</sub>	Storage Temperature	-55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 2. Mounted on  $76.2 \times 114.3 \times 1.6$  mm PCB (FR-4 glass epoxy material).

Refer to the following standards: З.

JESD51-2: Integral circuit's thermal test method environmental conditions, natural convection;

JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.

4. Do not exceed maximum power dissipation (PD) under any circumstances.

Table 3. RECOMMENDED OPERATING CONDITIONS (All voltage parameters are referenced to COM unless otherwise stated in the table)

Symbol	Parameter	Min	Мах	Unit
VB	High-Side Floating Supply Voltage	V <sub>S</sub> + 12	V <sub>S</sub> + 20	V
VS	High-Side Floating Supply Offset Voltage (Note 6)	8 – V <sub>CC</sub>	1200	V
V <sub>HO</sub>	High-Side (HO) Output Voltage	V <sub>S</sub>	V <sub>B</sub>	V
V <sub>CC</sub>	Low-Side Supply Voltage	12	20	V
$V_{LO}$	Low-Side (LO) Output Voltage	0	V <sub>CC</sub>	V
$V_{DD}$	Logic Supply Voltage	V <sub>SS</sub> + 3 0	V <sub>SS</sub> + 20 20	V
$V_{SS}$	Logic Ground (Note 5)	-10	10	V
V <sub>IN</sub>	Logic Input Voltage (HIN, LIN, SD)	$V_{SS} + V_{DD} - 20$	V <sub>DD</sub> 20	V
TJ	Junction Temperature	-40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability. 5. When  $V_{DD} < 10$  V, the minimum  $V_{SS}$  offset is limited to  $-V_{DD}$ .

6. Referenced to  $T_J = 25^{\circ}C$ .

**Table 4. STATIC ELECTRICAL CHARACTERISTICS**  $(V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15.0 \text{ V}, T_J = 25^{\circ}\text{C}$ , unless otherwise specified. The V<sub>IH</sub>, V<sub>IL</sub> and I<sub>IN</sub> parameters are referenced to V<sub>SS</sub> and are applicable to respective input leads: HIN, LIN and SD. The V<sub>O</sub> and I<sub>O</sub> parameters are referenced to V<sub>S</sub> and COM and are applicable to the respective output leads: HO and LO. The V<sub>DDUV</sub> parameters are referenced to COM. The V<sub>BSUV</sub> parameters are referenced to V<sub>S1, 2, 3</sub>.)

LOW-SIDE POWER SUPPLY SECTION     VIN = 0 V or VDD     -     170     300 $\mu$ A       IGDD     Quiescent VDC Supply Current     VIN = 0 V or VDD     -     170     300 $\mu$ A       IPCD     Operating VoC Supply Current     FIN = 20 KHz, rms VIN = 15 VPP     -     22     - $\mu$ A       IPDD     Operating VoC Supply Current     FIN = 20 KHz, rms VIN = 15 VPP     -     30     50 $\mu$ A       VoCUV,     Voc Supply Under-Voltage     Voc = Sweep     9.7     11.0     12     V       VocUV,     Voc Supply Under-Voltage     Voc = Sweep     9.2     10.5     1.1     V       VocUV,     Voc Supply Under-Voltage     Voc = Sweep     -     0.5     -     V       VocUV,     Voc Supply Under-Voltage     Voc = Sweep     -     0.5     10.0 $\mu$ A       VocUV,     Voc Supply Under-Voltage     Voc = Sweep     9.2     10.5     11.4     V       VBBNU,     Vag Supply Under-Voltage     Vag = Sweep     9.2     10.5     1.4     V       VBBUV,	Symbol	Parameter	Conditions	Min	Тур	Max	Units
$ \begin{array}{ c c c c } \begin{tabular}{ c c c c } \hline $V_{DD} & Quiescent $V_{DD} & V_{CC} $V_{DD} & V_{DC} $V_{DD} & V_{CC} $V_{DD} & V_{DC} $V_{DD} & V_{DD} $V_{DD} & V_{DC} $V_{DD} & V_{DD} $V_{DD} $V_{DD} & V_{DD} $V_{DD} & V_{DD} $V_{DD} $V_{DD} & V_{DD} $V_{DD} & V_{DD} $V_{DD} & V_{DD} $V_{DD} $V_{DD} $V_{DD} & V_{DD} $V_{DD} $V_{DD$	LOW-SIDE	POWER SUPPLY SECTION					
$\begin{array}{c ccc} \mbox{Operating } V_{CC} \mbox{Supply Current} & f_N = 20 \ kHz, rms } V_{IN} = 15 \ V_{PP} & - & 650 & 950 & \muA \\ \hline I_{PDD} \mbox{Operating } V_{DD} \ Supply Current & S_D = V_{DD} & - & 2 & - & \muA \\ \hline I_{SD} \mbox{Supply Current } & S_D = V_{DD} & - & 30 & 50 & \muA \\ \hline V_{CCUV_1} \ V_{CC} \ Supply Under-Voltage \\ Positive-Going Threshold Voltage \\ \hline V_{CCUV_2} \ V_{CC} \ Supply Under-Voltage Colored \\ \hline V_{CCUV_1} \ V_{CC} \ Supply Under-Voltage Colored \\ \hline V_{CCUV_2} \ V_{CC} \ Supply Under-Voltage Colored \\ \hline V_{CC} \ Supply Under-Voltage Colored \\ \hline V_{CCUV_2} \ V_{CC} \ Supply Under-Voltage Colored \\ \hline V_{PS} \ Supply Under-Voltage Colored \\ \hline V_{PS} \ Supply Under-Voltage \\ \hline V_{PS} \ Supply Under-Voltage \\ \hline V_{PS} \ Supply Under-Voltage \\ \hline V_{SS} \ Supply Under-Voltage \\ \hline V_{S$	I <sub>QCC</sub>	Quiescent V <sub>CC</sub> Supply Current	$V_{IN} = 0 V \text{ or } V_{DD}$	-	170	300	μA
$ \begin{array}{ c c c c c c c } \hline \mbox{Up} & \mbox{Up} U current & \mbox{Up} & \mbox{Up} U current & \mbox{Up} $	I <sub>QDD</sub>	Quiescent V <sub>DD</sub> Supply Current	V <sub>IN</sub> = 0 V or V <sub>DD</sub>	-	-	10	μA
$ \begin{array}{ c c c c c c } & Shutdown Supply Current & S_{D} = V_{DD} & - & 30 & 50 & \muA \\ V_{CCUV_{+}} & V_{CC} Supply Under-Voltage & V_{CC} = Sweep & 9.7 & 11.0 & 12 & V \\ V_{CC} Supply Under-Voltage & V_{CC} = Sweep & 9.2 & 10.5 & 11.4 & V \\ V_{CC} Supply Under-Voltage Lockout & V_{CC} = Sweep & - & 0.5 & - & V \\ W_{CS} Supply Under-Voltage Lockout & V_{CC} = Sweep & - & 0.5 & - & V \\ W_{CS} Supply Under-Voltage Lockout & V_{CC} = Sweep & - & 50 & 100 & \muA \\ V_{BS} & Quiescent V_{BS} Supply Current & V_{IN} = 0 V or V_{DD} & - & 550 & 850 & \muA \\ V_{BS} & Quiescent V_{BS} Supply Current & I_{IN} = 20  kHz  rm value & - & 550 & 850 & \muA \\ V_{BS} & Quiescent V_{BS} Supply Current & I_{IN} = 20  kHz  rm value & - & 550 & 850 & \muA \\ V_{BS} & V_{PS} Supply Under-Voltage & V_{BS} = Sweep & 9.7 & 11.0 & 12.0 & V \\ V_{BS} V_{VP} & V_{BS} Supply Under-Voltage & V_{BS} = Sweep & 9.2 & 10.5 & 11.4 & V \\ V_{BS} V_{VP} & V_{BS} Supply Under-Voltage & V_{BS} = Sweep & 9.2 & 10.5 & 11.4 & V \\ V_{BS} V_{VP} & V_{BS} Supply Under-Voltage & V_{BS} = Sweep & - & 0.5 & - & V \\ V_{BS} V_{VP} & V_{SS} Supply Under-Voltage & V_{BS} = 1200 V (\Gamma_{J} = 25^{\circ}C) & - & - & 100 \\ \hline V_{IL} & Offset Supply Leakage Current & V_{B} = V_{S} = 1200 V (\Gamma_{J} = -26^{\circ}C)  (Note 7) & - & - & 100 \\ \hline V_{DL} & V_{DD} = 5 V & 9.5 & - & - \\ V_{DD} = 5 V & 0.5 & - & - & 6.0 \\ \hline V_{DD} = 15 V & 0.5 & - & - & 6.0 \\ \hline V_{DD} = 15 V & 0.5 & - & - & 6.0 \\ \hline V_{DD} = 15 V & 0.5 & - & - & 6.0 \\ \hline V_{DD} = 15 V & 0.5 & - & - & 0.0 \\ \hline I_{IN} & Logic ~1^n Input Voltage & V_{DD} = 5 V & - & - & 500 & - & K2 \\ \hline CATE DIVET DUSETION \\ \hline V_{DL} & H_{DI} - Level Output Voltage, & V_{D} = 0 A & - & - & 500 & - & K2 \\ \hline CATE DIVET USETION \\ \hline V_{OL} & Low-Level Output Voltage, & V_{0} = 0 A & - & - & 0.1 & V \\ \hline V_{OL} & U_{OL} + UICH SH Sent-Circuit Pulse & V_{0} = 0 V, V_{IN} = 5 V with PW \le 10  \muS & - & 0.0 & - & A \\ \hline V_{OL} & Qutput H[GH Short-Circuit Pulse & V_{0} = 0 V, V_{IN} = 5 V with PW \le 10  \muS & - & 0.0 & - & A \\ \hline V_{OL} & Qutput H[GH Short-Circuit Pul$	I <sub>PCC</sub>	Operating V <sub>CC</sub> Supply Current	f <sub>IN</sub> = 20 kHz, rms V <sub>IN</sub> = 15 V <sub>PP</sub>	-	650	950	μA
$ \begin{array}{ c c c c c } \hline V_{CCUV_+} & V_{CC} Supply Under-Voltage Positive-Going Threshold Voltage V_{CC} = Sweep 9.7 11.0 12 V \\ \hline V_{CCUV} & V_{CC} Supply Under-Voltage Intershold Voltage V_{CC} = Sweep 9.2 10.5 11.4 V \\ \hline V_{CCUV_+} & V_{CC} Supply Under-Voltage Lockout V_{CC} = Sweep 0.5 - V \\ \hline V_{CCUV_+} & V_{CC} Supply Under-Voltage Lockout V_{CC} = Sweep 0.5 - V \\ \hline V_{CCUV_+} & V_{CC} Supply Under-Voltage Lockout V_{CC} = Sweep 0.5 - V \\ \hline V_{CC} Supply Under-Voltage Lockout V_{CC} = Sweep 50 100 \muA \\ \hline V_{DS} & Operating V_{DS} Supply Current & I_{IN} = 0 V or V_{DD} - 550 850 \muA \\ \hline V_{DS} & Operating V_{DS} Supply Current & I_{IN} = 0 V or V_{DD} - 550 850 \muA \\ \hline V_{DS} & V_{PO} Subve-Going Threshold Voltage V_{DS} = Sweep 9.7 11.0 12.0 V \\ \hline V_{DS} & V_{DS} Supply Under-Voltage Positive-Going Threshold Voltage V_{DS} = Sweep 9.2 10.5 11.4 V \\ \hline V_{DS} & V_{DS} Supply Under-Voltage Lockout V_{DS} = Sweep 9.2 10.5 11.4 V \\ \hline V_{BS} & V_{PO} Subve-Going Threshold Voltage V_{DS} = Sweep 0.5 - V \\ \hline V_{BS} & V_{DS} & V_{DI} Order-Voltage Lockout V_{DS} = Sweep 9.2 10.5 11.4 V \\ \hline V_{BS} & V_{DS} & V_{DI} & V_{DS} = 1200 V (T_J = 25^{\circ}C) 50 100 \\ \hline V_{B} & V_{S} & Supply Under-Voltage Dockout V_{DS} = 1100 V (T_J = -40^{\circ}C) (Note 7) 100 \\ \hline V_{B} & V_{S} & V_{DD} = 3 V 0.5 V \\ \hline V_{DL} & Logic *1^{\circ} Input Voltage V_{DD} = 3 V 0.5 V \\ \hline V_{DD} & = 15 V - 0.5 0.8 \\ \hline V_{DD} & = 15 V - 0.5 0.8 \\ \hline V_{DD} & = 15 V - 0.5 - 0 & - 0.8 \\ \hline V_{DD} & = 15 V - 0.5 - 0 & - 0.8 \\ \hline V_{DD} & = 15 V - 0.5 - 0 & - 0.8 \\ \hline V_{DD} & = 15 V - 0.5 & - 0 & - 0.8 \\ \hline V_{DD} & = 15 V & - 0 & - 0.8 \\ \hline V_{DD} & = 15 V & - 0 & - 0.8 \\ \hline V_{DL} & Logic *1^{\circ} Input Voltage V_{D} &  _{D} = 0 A & - 0 & - 0.8 \\ \hline V_{DL} & Logic *1^{\circ} Input Voltage V_{D} &  _{D} = 0 A & - 0 & - 0.8 \\ \hline V_{DL} & Logic Unput Voltage, V_{D} &  _{D} = 0 A & - 0 & - 0.1 \\ \hline V_{OL} & Low-Level Output Voltage, V_{D} &  _{D} = 0 A & - 0 & - 0.1 \\ \hline V_{OL} & Low-Level Output Voltage, V_{D} &  _{D} = 0 V \\ \hline$	I <sub>PDD</sub>	Operating V <sub>DD</sub> Supply Current	f <sub>IN</sub> = 20 kHz, rms V <sub>IN</sub> = 15 V <sub>PP</sub>	-	2	-	μA
$ \begin{array}{ c c c c c } \hline Positive-Going Threshold Voltage \\ \hline V_{CC} Supply Under-Voltage Agative-Going Threshold Voltage \\ \hline V_{CC} = Sweep \\ \hline Positive-Going Threshold Voltage \\ \hline V_{CC} = Sweep \\ \hline Positive-Supply Under-Voltage Lockout \\ \hline Hystersis Voltage \\ \hline V_{DC} = Sweep \\ \hline Positive-Scrino \\ \hline H_{PS} \\ \hline Derating V_{BS} Supply Current \\ \hline I_{N} = 0 V or V_{DD} \\ \hline Positive-Going Threshold Voltage \\ \hline V_{BS} \\ \hline V_{BS} \\ V_{DD} \\ V_{BS} \\ V_{BS} \\ V_{BS} \\ V_{DS} \\ V_{DD} \\ V_{BS} \\ V_{DS} \\ V_{DD} $	I <sub>SD</sub>	Shutdown Supply Current	$S_D = V_{DD}$	-	30	50	μA
	V <sub>CCUV+</sub>	V <sub>CC</sub> Supply Under-Voltage Positive-Going Threshold Voltage	V <sub>CC</sub> = Sweep	9.7	11.0	12	V
$ \begin{array}{ c c c c c } \hline W_{DD} & U_{DD} & U$	V <sub>CCUV-</sub>	V <sub>CC</sub> Supply Under-Voltage Negative-Going Threshold Voltage	V <sub>CC</sub> = Sweep	9.2	10.5	11.4	V
$ \begin{array}{ c c c c c c } \hline U_{DBS} & Quiescent V_{BS} Supply Current & V_{IN} = 0 \ V or V_{DD} & - & 50 & 100 & \muA \\ \hline I_{BS} & Operating V_{BS} Supply Current & f_{N} = 20 \ kHz, \ rms \ value & - & 550 & 850 & \muA \\ \hline V_{BS} V_{VB} & V_{BS} \ Supply \ Under-Voltage \\ Positive-Going Threshold Voltage & V_{BS} = Sweep & 9.7 & 11.0 & 12.0 & V \\ \hline V_{BS} \ Supply \ Under-Voltage \ Logar Threshold Voltage & V_{BS} = Sweep & 9.2 & 10.5 & 11.4 & V \\ \hline V_{BS} \ Supply \ Under-Voltage \ Logar Threshold Voltage & V_{BS} = Sweep & - & 0.5 & - & V \\ \hline V_{BS} \ V_{BS} \ Supply \ Under-Voltage \ Logar Threshold Voltage & V_{BS} = Sweep & - & 0.5 & - & V \\ \hline V_{BS} \ V_{BS} \ Supply \ Under-Voltage \ Logar Threshold Voltage \ V_{BS} = 1200 \ V \ (T_J = 25^{\circ}C) & - & - & 50 & P \\ \hline V_{B} \ V_{B} \$	V <sub>CCUVH</sub>		V <sub>CC</sub> = Sweep	_	0.5	_	V
$ \begin{array}{ c c c c c } \hline P_{BS} & Operating V_{BS} Supply Current & f_{IN} = 20 kHz, rms value & - & 550 & 850 & \muA \\ \hline V_{BS} UV_{\mu} & V_{BS} Supply Under-Voltage \\ Positive-Going Threshold Voltage \\ \hline V_{BS} UV_{\mu} & V_{BS} Supply Under-Voltage \\ \hline V_{BS} UV_{\mu} & V_{BS} Supply Under-Voltage \\ \hline V_{BS} UV_{\mu} & V_{BS} Supply Under-Voltage Lockout \\ \hline V_{BS} UV_{\mu} & V_{BS} Supply Under-Voltage Lockout \\ \hline V_{BS} UV_{\mu} & V_{BS} Supply Under-Voltage Lockout \\ \hline V_{BS} UV_{\mu} & V_{BS} Supply Under-Voltage Lockout \\ \hline V_{BS} V_{DS} & V_{DS} Supply Under-Voltage Lockout \\ \hline V_{BS} = V_{S} = 1200 V (T_{J} = 25^{\circ}C) & - & - & 50 \\ \hline V_{B} = V_{S} = 1200 V (T_{J} = 25^{\circ}C) & - & - & 100 \\ \hline V_{B} = V_{S} = 1200 V (T_{J} = -40^{\circ}C) (Note 7) & - & - & 100 \\ \hline V_{B} = V_{S} = 1200 V (T_{J} = -40^{\circ}C) (Note 7) & - & - & 100 \\ \hline V_{B} = V_{S} = 1100 V (T_{J} = -40^{\circ}C) (Note 7) & - & - & 100 \\ \hline V_{B} = V_{S} = 1100 V (T_{J} = -40^{\circ}C) (Note 7) & - & - & 100 \\ \hline V_{DD} = 15 V & 9.5 & - & - & V \\ \hline V_{DD} = 15 V & 9.5 & - & - & 0.8 \\ \hline V_{DD} = 15 V & - & & - & 0.8 \\ \hline V_{DD} = 15 V & - & & - & 0.8 \\ \hline V_{DD} = 15 V & - & & - & 0.0 \\ \hline I_{IN} & Logic "0" Input Voltage & V_{IN} = 15 V & - & & - & 0.0 \\ \hline I_{IN} & Logic "0" Input Pul-down Resistance & & - & - & 500 & - & k\Omega \\ \hline R_{IN} & Logic "0" Input Pul-down Resistance & & - & 500 & - & k\Omega \\ \hline Catter OUTPUT SECTION \\ \hline V_{OH} & High-Level Output Voltage, & & I_{O} = 0 A & & - & - & 0.1 & V \\ \hline V_{OH} & High-Level Output Voltage, & & I_{O} = 0 A & & - & - & 0.1 & V \\ \hline V_{OH} & Current & V_{O} = 0 V, V_{IN} = 5 V with PW \le 10 \ \mu S & - & & 2.0 & - & A \\ \hline V_{OL} & Output HIGH Short-Circuit Pulse & V_{O} = 0 V, V_{IN} = 0 V with PW \le 10 \ \mu S & - & & 3.0 & - & A \\ \hline V_{S} & Allowable Negative V_{S} Pin Voltage & & - & - & -9.8 & -7.0 & V \\ \hline \end{array}$	BOOTSTRA	APPED SUPPLY SECTION					
	I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	$V_{IN} = 0 V \text{ or } V_{DD}$	-	50	100	μA
$ \begin{array}{ c c c c } \mbox{Positive-Going Threshold Voltage} & V_{BS} = Sweep & 9.2 & 10.5 & 11.4 & V \\ \hline V_{BS UV-H} & V_{BS Supply Under-Voltage Lockout} & V_{BS} = Sweep & - & 0.5 & - & V \\ \hline V_{BS UVH} & V_{BS Supply Under-Voltage Lockout} & V_{BS} = Sweep & - & 0.5 & - & V \\ \hline V_{BS UVH} & V_{BS Supply Leakage Current} & V_{B} = V_{S} = 1200 V (T_{J} = 25^{\circ}C) & - & - & 50 & V \\ \hline V_{B} = V_{S} = 1200 V (T_{J} = 125^{\circ}C) (Note 7) & - & - & 100 & V \\ \hline V_{B} = V_{S} = 1100 V (T_{J} = -40^{\circ}C) (Note 7) & - & - & 100 & V \\ \hline V_{B} = V_{S} = 1100 V (T_{J} = -40^{\circ}C) (Note 7) & - & - & 0.5 & V \\ \hline V_{DD} = V_{S} = 1100 V (T_{J} = -40^{\circ}C) (Note 7) & - & - & 0.6 & V \\ \hline V_{DD} = 15 V & 9.5 & - & - & V \\ \hline V_{DD} = 15 V & 9.5 & - & - & 0.8 & V \\ \hline V_{DD} = 15 V & 0.5 & - & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & 0.1 & \mu A \\ \hline I_{IN-} & Logic "0" Input Voltage & V_{IN} = 0 V & - & - & 11 & \mu A \\ \hline I_{IN-} & Logic "0" Input bias Current & V_{IN} = 0 V & - & - & 500 & - & K \\ \hline GATE DRIVER OUTPUT SECTION & & & & & & & & & & & & & & & & & & &$	I <sub>PBS</sub>	Operating V <sub>BS</sub> Supply Current	f <sub>IN</sub> = 20 kHz, rms value	-	550	850	μA
$ \frac{1}{\text{Negative-Going Threshold Voltage}} = \frac{1}{10000000000000000000000000000000000$	$V_{BSUV+}$	V <sub>BS</sub> Supply Under-Voltage Positive-Going Threshold Voltage	V <sub>BS</sub> = Sweep	9.7	11.0	12.0	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	V <sub>BSUV-</sub>	V <sub>BS</sub> Supply Under–Voltage Negative–Going Threshold Voltage	V <sub>BS</sub> = Sweep	9.2	10.5	11.4	V
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	V <sub>BSUVH</sub>		V <sub>BS</sub> = Sweep	-	0.5	-	V
$\begin{tabular}{ c c c c c c } \hline V_B = V_S = 1100 \ V(T_J = -40^\circ C) \ (Note \ 7) & - & - & 100 \end{tabular}$	I <sub>LK</sub>	Offset Supply Leakage Current	$V_{B} = V_{S} = 1200 \text{ V} (T_{J} = 25^{\circ}\text{C})$	-	-	50	μA
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $			$V_{B} = V_{S} = 1200 \text{ V} (T_{J} = 125^{\circ}\text{C}) \text{ (Note 7)}$	-	-	100	
$ \begin{array}{c c c c c c c c } V_{IH} & Logic "1" Input Voltage & V_{DD} = 3 V & 2.4 & - & - & V \\ \hline V_{DD} = 15 V & 9.5 & - & - & V \\ \hline V_{DD} = 15 V & - & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & - & 6.0 & V \\ \hline V_{DD} = 15 V & - & - & 6.0 & V \\ \hline V_{DD} = 15 V & - & - & 0.8 & V \\ \hline V_{DD} = 15 V & - & - & 0.8 & V \\ \hline V_{IN} = 15 V & - & - & 0.8 & V \\ \hline V_{IN} = 0 V & - & - & 0.0 & V \\ \hline V_{IN} = 0 V & - & - & 0.0 & V \\ \hline V_{IN} = 0 V & - & - & 0.0 & V \\ \hline V_{IN} = 0 V & - & - & 0.1 & \mu A \\ \hline V_{IN} & Logic "0" Input bias Current & V_{IN} = 0 V & - & - & 0.1 & \mu A \\ \hline R_{IN} & Logic Input Pull-down Resistance & & - & 500 & - & k\Omega \\ \hline GATE DRIVER OUTPUT SECTION & & & & & & \\ \hline V_{OH} & \begin{array}{c} High-Level Output Voltage, \\ V_{BIAS}-V_O & & I_O = 0 A & - & - & 0.1 & V \\ \hline V_{OL} & Low-Level Output Voltage, V_O & I_O = 0 A & - & - & 0.1 & V \\ \hline I_{O+} & \begin{array}{c} Output HIGH Short-Circuit Pulse \\ Current & & V_O = 0 V, V_{IN} = 5 V with PW \le 10 \ \mu s & - & 2.0 & - & A \\ \hline I_{O-} & \begin{array}{c} Output LOW Short-Circuit Pulsed \\ V_O = 15 V, V_{IN} = 0 V with PW \le 10 \ \mu s & - & 3.0 & - & A \\ \hline V_{S} & Allowable Negative V_S Pin Voltage & & & & & & & & & & & & & & & & & & &$			$V_B = V_S = 1100 \text{ V} (T_J = -40^{\circ}\text{C}) \text{ (Note 7)}$	-	-	100	
$\begin{tabular}{ c c c c c } \hline $V_{DD}$ = 15 V & $9.5$ & $-$ & $-$ & $-$ \\ \hline $V_{DD}$ & $Logic "0" Input Voltage & $V_{DD}$ = 3 V & $-$ & $-$ & $0.8$ \\ \hline $V_{DD}$ = 15 V & $-$ & $-$ & $6.0$ \\ \hline $V_{DD}$ = 15 V & $-$ & $-$ & $6.0$ \\ \hline $V_{DD}$ = 15 V & $-$ & $-$ & $30$ & $50$ & $\mu$A \\ \hline $V_{IN}$ & $Logic "0" Input bias Current & $V_{IN}$ = 15 V & $-$ & $-$ & $30$ & $50$ & $\mu$A \\ \hline $I_{IN}$ & $Logic "0" Input bias Current & $V_{IN}$ = 0 V & $-$ & $-$ & $-$ & $1$ & $\mu$A \\ \hline $I_{IN}$ & $Logic Input Pull-down Resistance & $-$ & $500$ & $-$ & $k\Omega$ \\ \hline $GATE DRIVER OUTPUT SECTION & $V_{OH}$ & $High-Level Output Voltage, $V_O$ & $I_O$ = 0 A & $-$ & $-$ & $0.1$ & $V$ \\ \hline $V_{OL}$ & $Low-Level Output Voltage, $V_O$ & $I_O$ = 0 A & $-$ & $-$ & $0.1$ & $V$ \\ \hline $V_{OL}$ & $Low-Level Output Voltage, $V_O$ & $I_O$ = 0 A & $-$ & $-$ & $0.1$ & $V$ \\ \hline $V_{OL}$ & $Low-Level Output Voltage, $V_O$ & $I_O$ = 0 V, $V_{IN}$ = 5 V with $PW $\le 10 $\mu$s & $-$ & $2.0$ & $-$ & $A$ \\ \hline $V_O$ & $U_{OTTUT}$ & $V_O$ = 0 V, $V_{IN}$ = 5 V with $PW $\le 10 $\mu$s & $-$ & $3.0$ & $-$ & $A$ \\ \hline $V_S$ & $Allowable Negative $V_S$ Pin Voltage & $V_O$ = 15 V, $V_{IN}$ = 0 V with $PW $\le 10 $\mu$s & $-$ & $-$ & $-$ & $-$ & $0.5$ & $-$ & $-$ & $-$ & $0.5$ \\ \hline $V_S$ & $Allowable Negative $V_S$ Pin Voltage & $V_O$ = 15 V, $V_{IN}$ = 0 V with $PW $\le 10 $\mu$s & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $-$ & $$	NPUT LOG	IC SECTION (HIN.LIN AND AD)					
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	V <sub>IH</sub>	Logic "1" Input Voltage	V <sub>DD</sub> = 3 V	2.4	-	-	V
$\begin{tabular}{ c c c c c c c } \hline V_{DD} = 15 \ V & - & - & 6.0 \\ \hline V_{DD} = 15 \ V & - & 30 & 50 & \mu A \\ \hline I_{IN+} & Logic "1" Input bias Current & V_{IN} = 15 \ V & - & 30 & 50 & \mu A \\ \hline I_{IN-} & Logic "0" Input bias Current & V_{IN} = 0 \ V & - & - & 1 & \mu A \\ \hline R_{IN} & Logic Input Pull-down Resistance & & - & 500 & - & k\Omega \\ \hline GATE DRIVER OUTPUT SECTION & & & & & & & & & & & & & & & & & & &$			V <sub>DD</sub> = 15 V	9.5	-	-	
Image: Non-algorithm of the section of the sectio	V <sub>IL</sub>	Logic "0" Input Voltage	V <sub>DD</sub> = 3 V	-	-	0.8	V
I <sub>IN-</sub> Logic "0" Input bias Current $V_{IN} = 0$ V $   1$ $\mu A$ R <sub>IN</sub> Logic Input Pull-down Resistance $ 500$ $ k\Omega$ GATE DRIVER OUTPUT SECTION $V_{OH}$ High-Level Output Voltage, $V_{O}$ $I_{O} = 0$ A $   1.2$ V $V_{OL}$ Low-Level Output Voltage, $V_{O}$ $I_{O} = 0$ A $  0.1$ V $I_{O+}$ Output HIGH Short-Circuit Pulse $V_{O} = 0$ V, $V_{IN} = 5$ V with PW $\leq 10$ $\mu$ s $ 2.0$ $-$ A $I_{O-}$ Output LOW Short-Circuit Pulsed $V_{O} = 15$ V, $V_{IN} = 0$ V with PW $\leq 10$ $\mu$ s $ 3.0$ $-$ A $V_{S}$ Allowable Negative $V_{S}$ Pin Voltage $ -9.8$ $-7.0$ V			V <sub>DD</sub> = 15 V	-	-	6.0	
RinLogic Input Pull-down Resistance-500-k $\Omega$ GATE DRIVER OUTPUT SECTIONVOHHigh-Level Output Voltage, VBIAS-VOIO = 0 A1.2VVOLLow-Level Output Voltage, VOIO = 0 A0.1VIO+Output HIGH Short-Circuit Pulse CurrentVO = 0 V, VIN = 5 V with PW ≤ 10 $\mu$ s-2.0-AIO-Output LOW Short-Circuit Pulsed CurrentVO = 15 V, VIN = 0 V with PW ≤ 10 $\mu$ s-3.0-AVSAllowable Negative VS Pin VoltageVO = 15 V, VIN = 0 V with PW ≤ 10 $\mu$ s9.8-7.0V	I <sub>IN+</sub>	Logic "1" Input bias Current	V <sub>IN</sub> = 15 V	-	30	50	μA
GATE DRIVER OUTPUT SECTION $V_{OH}$ High-Level Output Voltage, $V_{BIAS}$ - $V_O$ $I_O = 0 A$ $  1.2$ $V$ $V_{OL}$ Low-Level Output Voltage, $V_O$ $I_O = 0 A$ $  0.1$ $V$ $I_{O+}$ Output HIGH Short-Circuit Pulse Current $V_O = 0 V$ , $V_{IN} = 5 V$ with $PW \le 10 \ \mu s$ $ 2.0$ $ A$ $I_{O-}$ Output LOW Short-Circuit Pulsed Current $V_O = 15 V$ , $V_{IN} = 0 V$ with $PW \le 10 \ \mu s$ $ 3.0$ $ A$ $V_S$ Allowable Negative $V_S$ Pin Voltage $V_O = 15 V$ , $V_{IN} = 0 V$ with $PW \le 10 \ \mu s$ $ -9.8$ $-7.0$ $V$	I <sub>IN-</sub>	Logic "0" Input bias Current	V <sub>IN</sub> = 0 V	-	-	1	μΑ
$V_{OH}$ High-Level Output Voltage, $V_{BIAS}-V_O$ $I_O = 0 A$ $  1.2$ $V$ $V_{OL}$ Low-Level Output Voltage, $V_O$ $I_O = 0 A$ $  0.1$ $V$ $I_{O+}$ Output HIGH Short-Circuit Pulse Current $V_O = 0 V, V_{IN} = 5 V$ with $PW \le 10 \ \mu s$ $ 2.0$ $ A$ $I_{O-}$ Output LOW Short-Circuit Pulsed Current $V_O = 15 V, V_{IN} = 0 V$ with $PW \le 10 \ \mu s$ $ 3.0$ $ A$ $V_S$ Allowable Negative $V_S$ Pin Voltage $ -9.8$ $-7.0$ $V$	R <sub>IN</sub>	Logic Input Pull-down Resistance		-	500	-	kΩ
VBIAS-VOImage: NOImage: Image:	GATE DRIV	ER OUTPUT SECTION					
$ \begin{array}{ c c c c c } I_{O+} & Output HIGH Short-Circuit Pulse \\ Current & V_{O} = 0 \ V, \ V_{IN} = 5 \ V \ with \ PW \leq 10 \ \mu s & - & 2.0 & - & A \\ \hline I_{O-} & Output LOW Short-Circuit Pulsed \\ Current & V_{O} = 15 \ V, \ V_{IN} = 0 \ V \ with \ PW \leq 10 \ \mu s & - & 3.0 & - & A \\ \hline V_{S} & Allowable \ Negative \ V_{S} \ Pin \ Voltage & & - & -9.8 & -7.0 \ V \\ \end{array} $	V <sub>OH</sub>		I <sub>O</sub> = 0 A	-	-	1.2	V
CurrentCurrentImage: CurrentImage: Current <td>V<sub>OL</sub></td> <td>Low-Level Output Voltage, VO</td> <td>I<sub>O</sub> = 0 A</td> <td>-</td> <td>-</td> <td>0.1</td> <td>V</td>	V <sub>OL</sub>	Low-Level Output Voltage, VO	I <sub>O</sub> = 0 A	-	-	0.1	V
Current     -     -9.8     -7.0     V	I <sub>O+</sub>		$V_O$ = 0 V, $V_{IN}$ = 5 V with PW $\leq$ 10 $\mu s$	-	2.0	-	A
V <sub>S</sub> Allowable Negative V <sub>S</sub> Pin Voltage9.8 -7.0 V for HIN Signal Propagation to HO	I <sub>O-</sub>		$V_O$ = 15 V, $V_{IN}$ = 0 V with PW $\leq$ 10 $\mu s$	-	3.0	_	A
	VS	Allowable Negative V <sub>S</sub> Pin Voltage for HIN Signal Propagation to HO		-	-9.8	-7.0	V

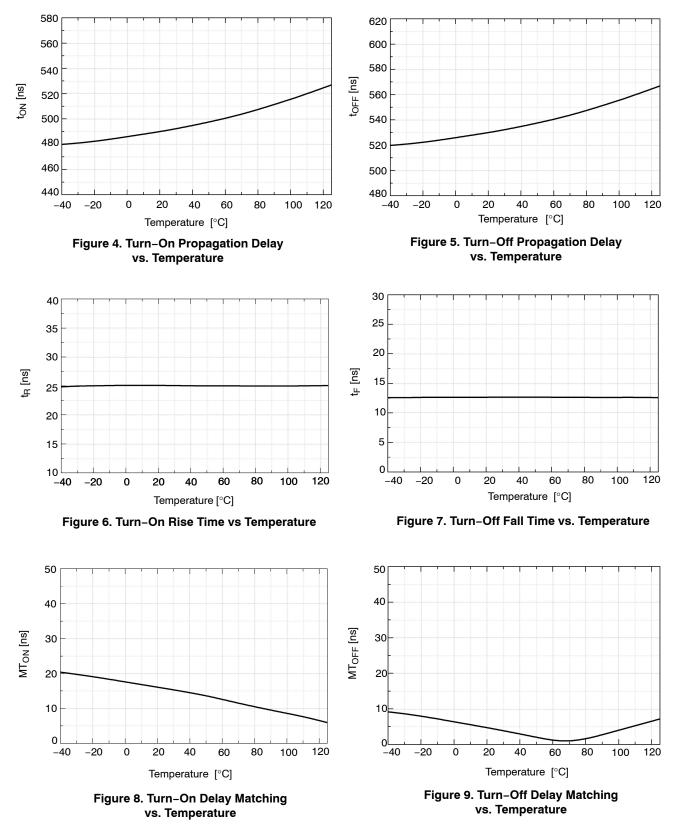
7. These parameters are guaranteed by design.

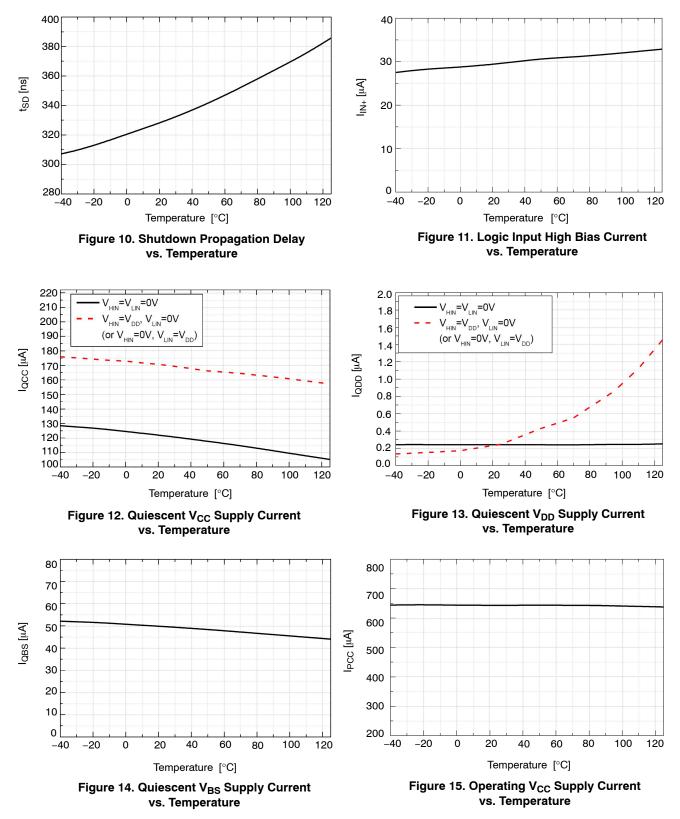
Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS (V <sub>BIAS</sub> (V <sub>CC</sub> , V <sub>BS</sub> , V <sub>DD</sub> ) = 15.0 V, V <sub>S</sub> = V <sub>SS</sub> = COM, C <sub>L</sub> = 1000	pF and
$T_J = 25^{\circ}C$ , unless otherwise specified.)	

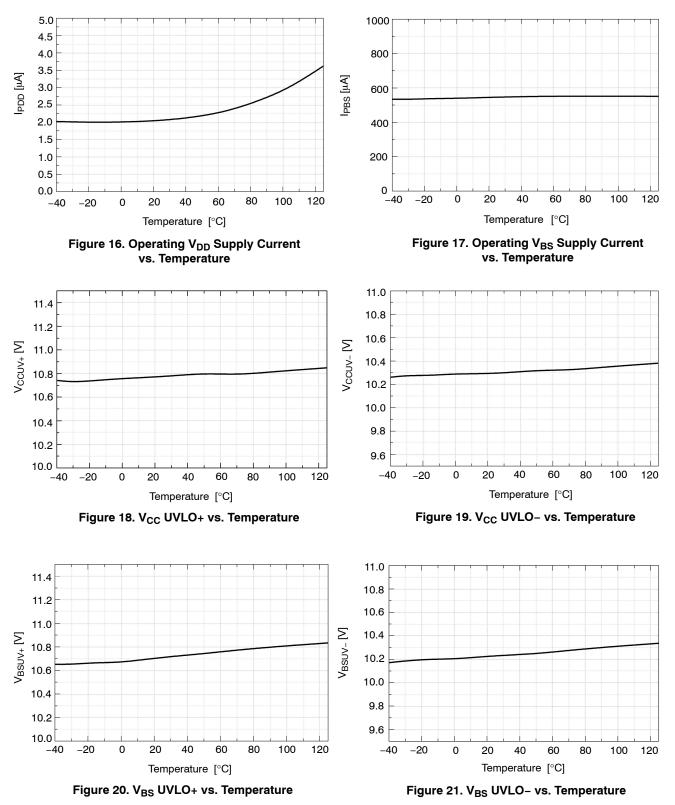
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
LOW-SIDE	LOW-SIDE POWER SUPPLY SECTION						
t <sub>ON</sub>	Turn-On Propagation Delay	V <sub>S</sub> = 0 V	-	500	-	ns	
t <sub>OFF</sub>	Turn-Off Propagation Delay	V <sub>S</sub> = 0 V	-	550	-	ns	
t <sub>FLTIN</sub>	Input Filtering Time (HIN, LIN) (Note 8)		80	150	220	ns	
t <sub>FLTSD</sub>	Input Filtering Time (SD)		-	30	-	ns	
t <sub>SD</sub>	Shutdown Propagation Delay Time		260	330	400	ns	
t <sub>R</sub>	Turn-On Rise Time		-	25	-	ns	
t <sub>F</sub>	Turn-Off Fall Time		-	15	-	ns	
DT	Dead Time		200	330	450	ns	
MDT	Dead Time Matching (Note 9)		-	-	50	ns	
MT	Delay Matching , HO & LO Turn-On/OFF (Note 10)		-	-	50	ns	
РМ	Output Pulse–Width Matching (Note 11)	PW <sub>IN</sub> > 1 μs	-	50	100	ns	

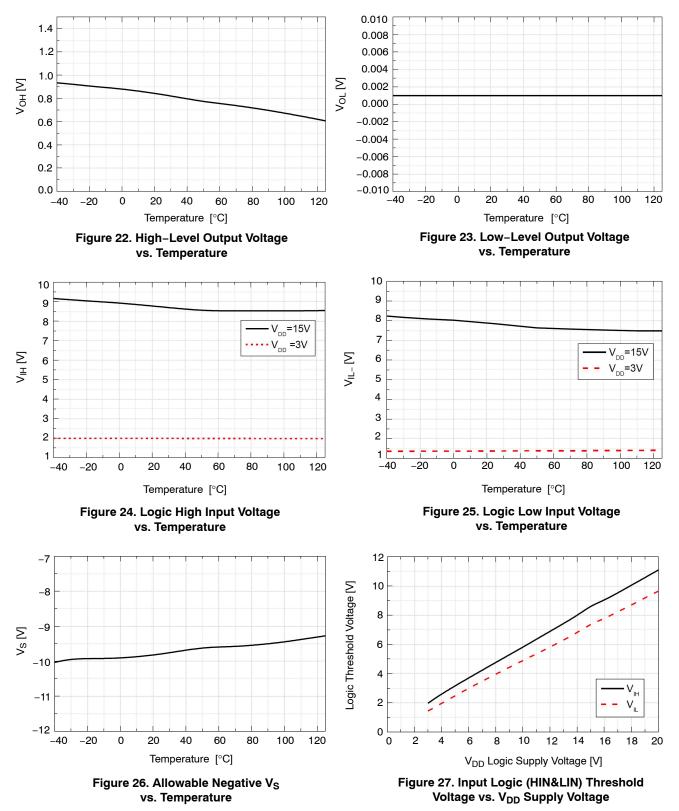
The minimum width of the input pulse should exceed 500 ns to ensure the filtering time of the input filter is exceeded.
MDT is defined as | DT<sub>HO-LO</sub>-DT<sub>LO-HO</sub> | referenced to Figure 40.
MT is defined as an absolute value of matching delay time between High-side and Low-Side.
PM is defined as an absolute value of matching pulse-width between Input and Output.

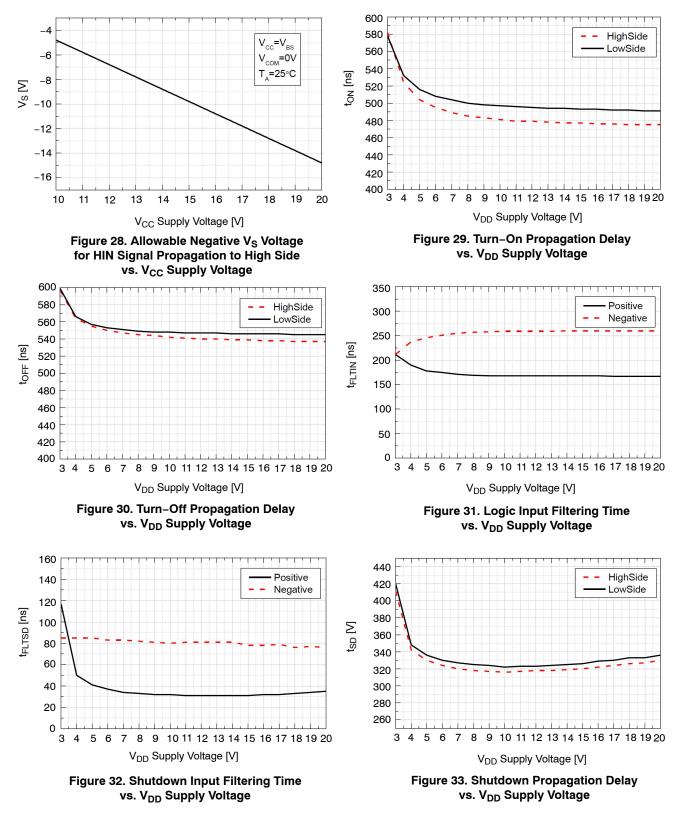












#### TYPICAL CHARACTERISTICS (continued)

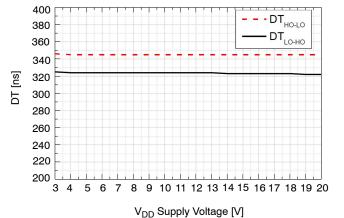
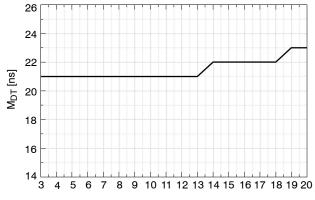


Figure 34. Dead Time vs. V<sub>DD</sub> Supply Voltage



V<sub>DD</sub> Supply Voltage [V]

Figure 35. Dead-Time Matching vs. V<sub>DD</sub> Supply Voltage

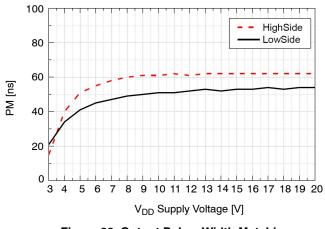


Figure 36. Output Pulse–Width Matching vs. V<sub>DD</sub> Supply Voltage

#### SWITCHING TIME DEFINITIONS

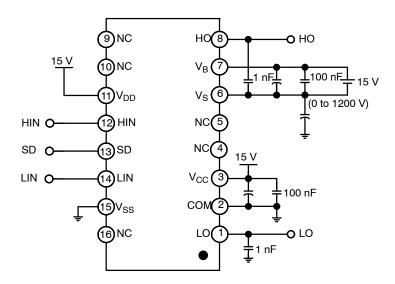
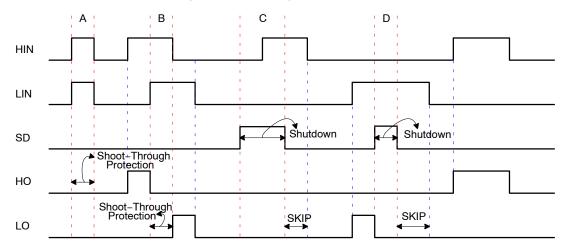


Figure 37. Switching Time Test Circuit



#### Figure 38. Input/Output Timing Diagram

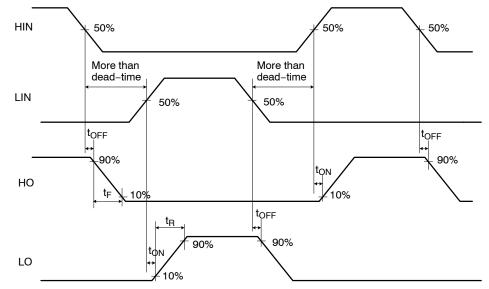
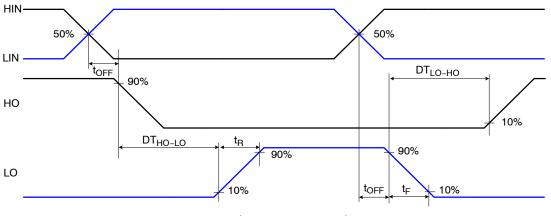


Figure 39. Switching Time Definition

#### SWITCHING TIME DEFINITIONS (continued)



 $\mathsf{MDT} = \left| \mathsf{DT}_{\mathsf{HO}-\mathsf{LO}} - \mathsf{DT}_{\mathsf{LO}-\mathsf{HO}} \right|$ 



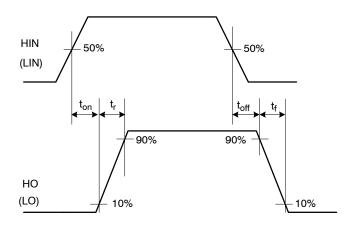


Figure 41. Switching Time Waveform Definitions

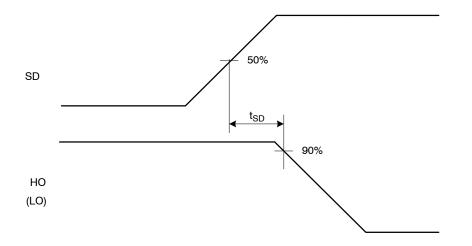


Figure 42. Switching Time Definitions

#### **APPLICATIONS INFORMATION**

#### **Dead Time**

Dead time is automatically inserted whenever the dead time of the external two input signals (between HIN and LIN signals) is shorter than internal fixed dead times (DT1 and DT2). Otherwise, external dead times larger than internal dead times are not modified by the gate driver and internal dead–time waveform definition is shown in Figure 43.

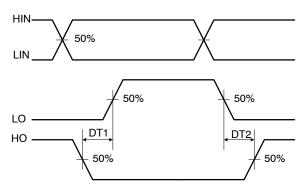


Figure 43. Internal Dead–Time Definitions

#### **Protection Function**

#### Shoot-Through Protection

The shoot-through protection circuitry prevents both high- and low-side switches from conducting at the same time, as shown in Figure 44.

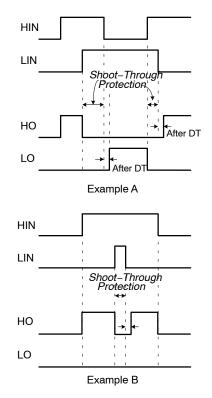


Figure 44. Shoot-Through Protection

#### Shutdown Input

When the SD pin is in LOW state, the gate driver operates normally. When a condition occurs that should shut down the gate driver, the SD pin should be HIGH. The Shutdown circuitry has an input filter; the minimum input duration is specified by  $t_{FLTIN}$  (typically 250 ns).

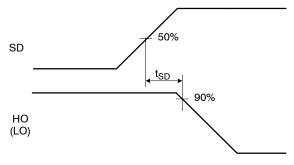


Figure 45. Output Shutdown Timing Waveform

#### **Noise Filter**

#### Input Noise Filter

Figure 46 shows the input noise filter method, which has symmetry duration between the input signal ( $t_{INPUT}$ ) and the output signal ( $t_{OUTPUT}$ ) and helps to reject noise spikes and short pulses. This input filter is applied to the HIN, LIN, and EN inputs. The upper pair of waveforms (Example A) shows an input signal duration ( $t_{INPUT}$ ) much longer than input filter time ( $t_{FLTIN}$ ); it is approximately the same duration between the input signal time ( $t_{INPUT}$ ) and the output signal time ( $t_{OUTPUT}$ ). The lower pair of waveforms (Example B) shows an input signal time ( $t_{INPUT}$ ) slightly longer than input filter time ( $t_{FLTIN}$ ); it is approximately the same duration between input signal time ( $t_{INPUT}$ ) and the output signal time ( $t_{OUTPUT}$ ).

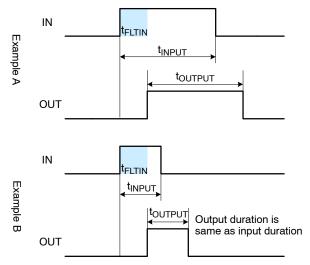


Figure 46. Input Noise Filter Definition

#### Short-Pulsed Input Noise Rejection Method

The input filter circuitry provides protection against short–pulsed input signals (HIN, LIN, and SD) on the input signal lines by applied noise signal. If the input signal duration is less than input filter time ( $t_{FLTIN}$ ), the output does not change states. Example A and B of the Figure 47 show the input and output waveforms with short–pulsed noise spikes with a duration less than input filter time; the output does not change states.

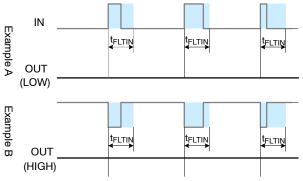


Figure 47. Noise Rejecting Input Filter Definition

#### **Negative VS Transient**

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations. The biggest difficulty with this circuit is the negative voltage present at the emitter of the high–side switching device when high–side switch is turned–off in half–bridge application. If the high–side switch, Q1, turns–off while the load current is flowing to an inductive load, a current commutation occurs from high–side switch, Q1, to the diode, D2, in parallel with the low–side switch of the same inverter leg. Then the negative voltage present at the emitter of the high–side switching device, just before the freewheeling diode, D2, starts clamping, causes load current to suddenly flow to the low–side freewheeling diode, D2, as shown in Figure 48.

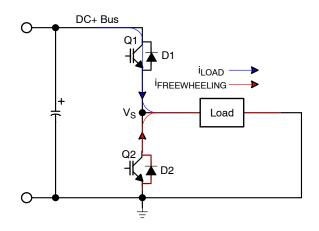


Figure 48. Half–Bridge Application Circuits

This negative voltage can be trouble for the gate driver's output stage, there is the possibility to develop an overvoltage condition of the bootstrap capacitor, input signal missing and latch-up problems because it directly affects the source VS pin of the gate driver, shown in Figure 49. This undershoot voltage is called "negative VS transient".

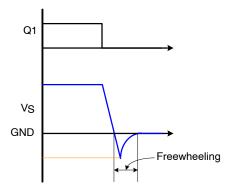
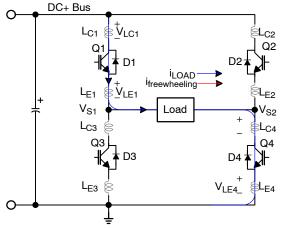


Figure 49. V<sub>S</sub> Waveforms during Q1 Turn-Off

Figure 50 and Figure 51 show the commutation of the load current between high-side switch, Q1, and low-side freewheeling diode, D3, in same inverter leg. The parasitic inductances in the inverter circuit from the die wire bonding to the PCB tracks are jumped together in  $L_C$  and  $L_E$  for each IGBT. When the high-side switch, Q1, and low-side switch, Q4, are turned on, the  $V_{S1}$  node is below DC+ voltage by the voltage drops associated with the power switch and the parasitic inductances of the circuit due to load current is flows from Q1 and Q4, as shown in Figure 50. When the high-side switch, Q1, is turned off and Q4, remained turned on, the load current to flows the low-side freewheeling diode, D3, due to the inductive load connected to VS1 as shown in Figure 51. Q1 Turn-Off and D3 Conducting. The current flows from ground (which is connected to the COM pin of the gate driver) to the load and the negative voltage present at the emitter of the high-side switching device. In this case, the COM pin of the gate driver is at a higher potential than the V<sub>S</sub> pin due to the voltage drops associated with freewheeling diode, D3, and parasitic elements, L<sub>C3</sub> and LE3.





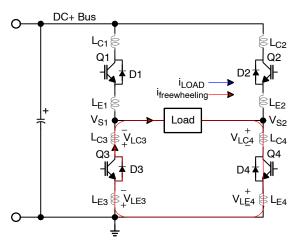
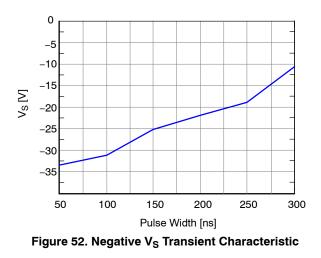


Figure 51. Q1 Turn-Off and D3 Conducting

The FAN73912 has a typical negative VS transient characteristics, as shown in Figure 52.



Even though the FAN73912 has been shown able to handle these negative V<sub>S</sub> transient conditions, it is strongly recommended that the circuit designer limit the negative VS transient as much as possible by careful PCB layout to minimize the value of parasitic elements and component use. The amplitude of negative V<sub>S</sub> voltage is proportional to the parasitic inductances and the turn–off speed, di/dt, of the switching device.

#### **General Guidelines**

#### Printed Circuit Board Layout

The layout recommended for minimized parasitic elements is as follows:

- Direct tracks between switches with no loops or deviation.
- Avoid interconnect links. These can add significant inductance.
- Reduce the effect of lead-inductance by lowering package height above the PCB.
- Consider co-locating both power switches to reduce track length.
- To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.
- To reduce the EM coupling and improve the power switch turn-on/off performance, the gate drive loops must be reduced as much as possible.

#### Placement of Components

The recommended placement and selection of component as follows:

• Place a bypass capacitor between the  $V_{CC}$  and  $V_{SS}$  pins. A ceramic 1  $\mu$ F capacitor is suitable for most applications. This component should be placed as close as possible to the pins to reduce parasitic elements.

- The bypass capacitor from V<sub>CC</sub> to V<sub>SS</sub> supports both the low-side driver and bootstrap capacitor recharge. A value at least ten times higher than the bootstrap capacitor is recommended.
- The bootstrap resistor,  $R_{BOOT}$ , must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that  $V_B$  does not fall below COM (ground). Recommended use is typically 5 ~ 10  $\Omega$  that increase the  $V_{BS}$  time constant. If the voltage drop of bootstrap resistor and diode is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra-fast recovery diode can be used.
- The bootstrap capacitor, C<sub>BOOT</sub>, uses a low-ESR capacitor, such as ceramic capacitor. It is strongly

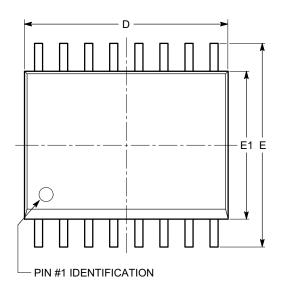
recommended that the placement of components is as follows:

- Place components tied to the floating voltage pins ( $V_B$  and  $V_S$ ) near the respective high–voltage portions of the device and the FAN73912. Not Connected (NC) pins in this package maximize the distance between the high–voltage and low–voltage pins (see Figure 3).
- Place and route for bypass capacitors and gate resistors as close as possible to gate drive IC.
- Locate the bootstrap diode, D<sub>BOOT</sub>, as close as possible to bootstrap capacitor, C<sub>BOOT</sub>.
- The bootstrap diode must use a lower forward voltage drop and minimal switching time as soon as possible for fast recovery or ultra-fast diode.



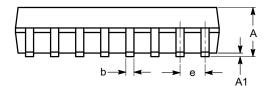
SOIC-16, 300 mils CASE 751BH-01 ISSUE A

DATE 18 MAR 2009



SYMBOL	MIN	NOM	МАХ
A	2.36	2.49	2.64
A1	0.10		0.30
b	0.33	0.41	0.51
с	0.18	0.23	0.28
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
е		1.27 BSC	
h	0.25		0.75
L	0.38	0.81	1.27
θ	0°		8°

TOP VIEW

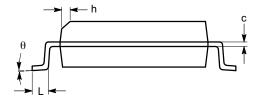


SIDE VIEW



(1) All dimensions are in millimeters. Angles in degrees.

(2) Complies with JEDEC MS-013.



END VIEW

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