

DESCRIPTION

The F2915 is a high reliability, low insertion loss, 50 Ω SP5T absorptive RF switch designed for a multitude of RF applications including wireless communications. This device covers a broad frequency range from 50 MHz to 8000 MHz. In addition to providing low insertion loss, the F2915 also delivers excellent linearity and isolation performance while providing a 50 Ω termination to the unused RF input ports. The F2915 also includes a patent pending constant impedance (K_z) feature. K_z improves system hot switching ruggedness, minimizes LO pulling in VCOs, and reduces phase and amplitude variations in distribution networks. It is also ideal for dynamic switching/selection between two or more amplifiers while avoiding damage to upstream /downstream sensitive devices such as PAs and ADCs.

The F2915 uses a single positive supply voltage supporting three logic control pins using either 3.3 V or 1.8 V control logic. Connecting a negative voltage to pin 20 disables the internal negative voltage generator and becomes the negative supply.

COMPETITIVE ADVANTAGE

The F2915 provides constant impedance in all RF ports during transitions improving a system's hot-switching ruggedness. The device also supports high power handling, and high isolation; particularly important for DPD receiver use.

- ✓ Constant impedance K_z during switching transition
 - ✓ RFX to RFC Isolation = 50 dB*
 - ✓ Insertion Loss = 1.1 dB*
 - ✓ IIP3: +60.5 dBm*
 - ✓ Extended temperature: -40 °C to +105 °C
- * 4 GHz

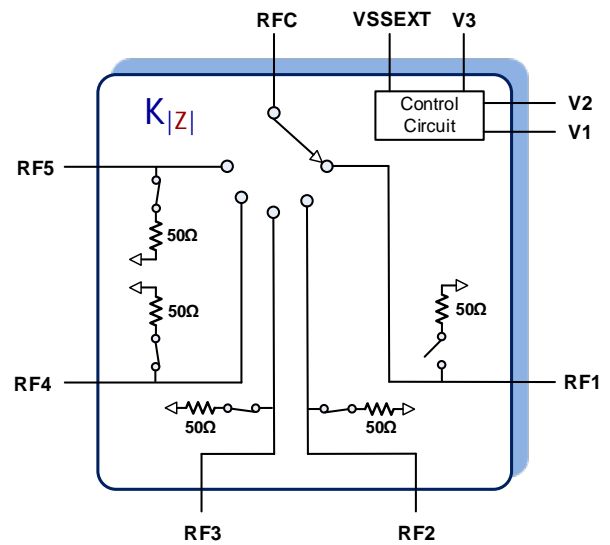
APPLICATIONS

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- Military Systems, JTRS radios
- Cable Infrastructure
- Test / ATE Equipment

FEATURES

- Five symmetric, absorptive RF ports
- High Isolation: 50 dB @ 4000 MHz
- Low Insertion Loss: 1.1 dB @ 4000 MHz
- High Linearity:
 - IIP2 of 114 dBm @ 2000 MHz
 - IIP3 of 60.5 dBm @ 4000 MHz
- High Operating Power Handling:
 - 33 dBm CW on selected RF port
 - 27 dBm on terminated ports
- Single 2.7 V to 5.5 V supply voltage
- External Negative Supply Option
- 3.3 V and 1.8 V compatible control logic
- Operating Temperature -40 °C to +105 °C
- 4 mm x 4 mm 24 pin QFN package
- Pin compatible with competitors

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

F2915NBGK8
 ↓
 Green
 ↗ Tape & Reel

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Units |
|---|----------------------|------|--|-------|
| V _{DD} to GND | V _{DD} | -0.3 | +6.0 | V |
| V1, V2, V3 to GND | V _{CNTL} | -0.3 | Lower of (3.6, V _{DD} + 0.3) | V |
| RF1, RF2, RF3, RF4, RF5, RFC to GND | V _{RF} | -0.3 | +0.3 | V |
| V _{SSEXT} to GND | V _{EXT} | -4.0 | +0.3 | V |
| Input Power for any one selected RF through port. (V _{DD} applied @ 2 GHz and T _C = +85 °C) | P _{MAXTHRU} | | 37 | dBm |
| Input Power for any one selected RF terminated port .(V _{DD} applied @ 2 GHz and T _C = +85 °C) | P _{MAXTERM} | | 30 | dBm |
| Input Power for RFC when in the all off state. (V _{DD} applied @ 2 GHz and T _C = +85 °C) | P _{MAXCOM} | | 33 | dBm |
| Continuous Power Dissipation (T _C = 95 °C Max) | | | 3 | W |
| Maximum Junction Temperature | T _{Jmax} | | +140 | °C |
| Storage Temperature Range | T _{ST} | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | T _{LEAD} | | +260 | °C |
| ESD Voltage– HBM (Per JESD22-A114) | V _{ESDHBM} | | Class 1C (1500V) | |
| ESD Voltage – CDM (Per JESD22-C101) | V _{ESDCDM} | | Class C3 (1000V) | |

T_C = Temperature of the exposed paddle

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

| | |
|---|----------|
| θ _{JA} (Junction – Ambient) | 41 °C/W |
| θ _{JC} (Junction – Case) [The Case is defined as the exposed paddle] | 6.4 °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | MSL1 |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | |
|--|--------------------|---------------------------------------|---|------|------|-------|-----|
| Supply Voltage (s) | V _{DD} | Pin 20 grounded | 2.7 | | 5.5 | V | |
| | | Pin 20 Driven with VSS _{EXT} | 2.7 | | 5.5 | | |
| | VSS _{EXT} | Negative Supply ¹ | -3.6 | -3.4 | -3.2 | | |
| Operating Temp Range | T _{CASE} | Exposed Paddle Temperature | -40 | | +105 | °C | |
| RF Frequency Range | F _{RF} | | 50 | | 8000 | MHz | |
| RF Continuous Input CW Power ² | P _{RF} | Selected Port | | | 33 | dBm | |
| | | Terminated Ports ³ | | | 27 | | |
| RF Continuous Input CW Power for Hot RF Switching ² | P _{RFSW} | RFC as the input | Switch to RF1 thru RF5. | | | 27 | dBm |
| | | | Switched into or out of all off state. | | | 24 | |
| | | RF1 thru RF5 as the inputs | Switched to RFC or into Term ³ . | | | 27 | |
| | | | Switch into or out of all off condition. | | | 27 | |
| RF1 - 5 Port Impedance | Z _{RFX} | | | 50 | | Ω | |
| RFC Port Impedance | Z _{RFc} | | | 50 | | | |

Note 1: For normal operation, connect VSS_{EXT} = 0 V (pin 20) to GND to enable the internal negative voltage generator. By applying VSS_{EXT} to pin 20, the negative voltage generator is disabled completely eliminating any generator spurious responses.

Note 2: Levels based on T_C ≤ 85C. See Figure 1 power de-rating curve for higher case temperatures.

Note 3: In any of the insertion loss modes or switching into any insertion loss mode, any 3 of the 4 remaining terminated port paths may be each exposed to the maximum stated power level during continuous or hot switching operation.

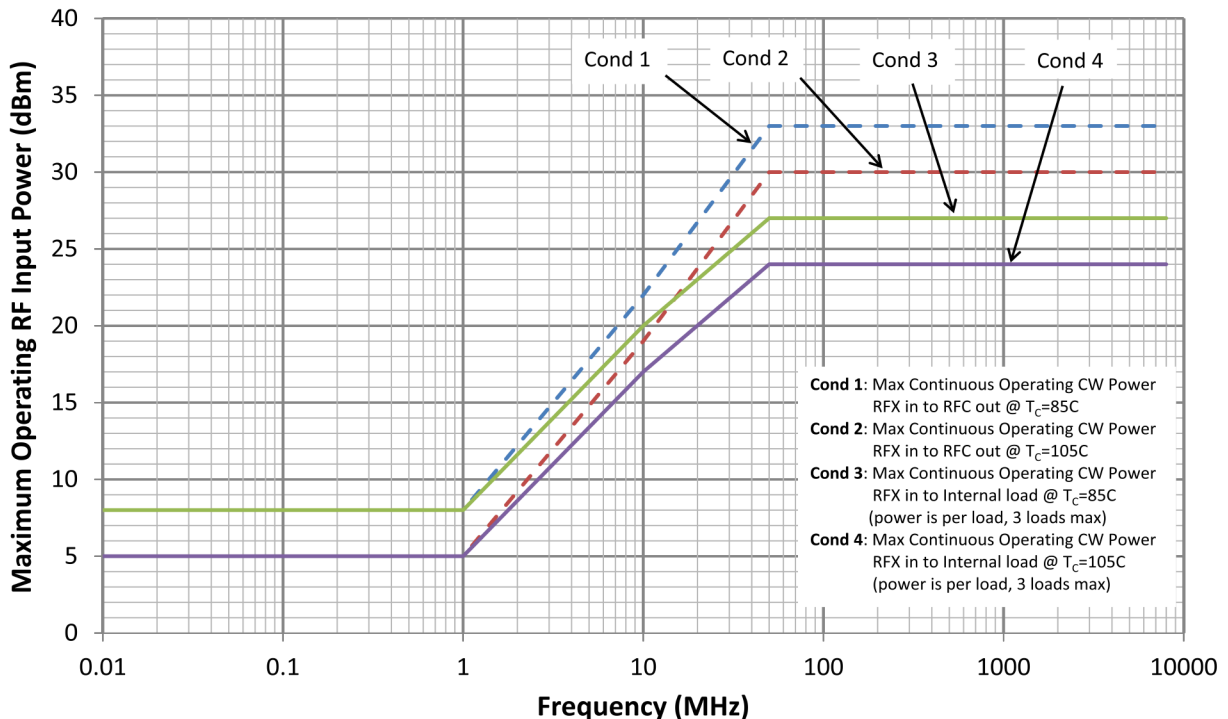


Figure 1 - MAXIMUM RF OPERATING INPUT POWER vs. RF FREQUENCY

SPECIFICATIONS

Typical Application Circuit, Normal mode ($V_{DD}= 3.3\text{ V}$, $V_{SS_{EXT}}= 0\text{ V}$) or Bypass mode ($V_{DD}= 3.3\text{ V}$, $V_{SS_{EXT}}= -3.3\text{ V}$), $T_C = +25\text{ }^\circ\text{C}$, $F_{RF} = 2000\text{ MHz}$, Input power = 0 dBm, $Z_S = Z_L = 50\ \Omega$, RFX = one of the five input ports, PCB board trace and connector losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Units |
|---|------------------|---|---------------------|----------------------------|--------|------------------------------|---------------|
| Logic Input High Threshold | V_{IH} | | | 1.1 | | Lower of (3.6, V_{DD}) | V |
| Logic Input Low Threshold | V_{IL} | | | -0.3 | | 0.6 | V |
| Logic Current | I_{IH}, I_{IL} | For each control pin | | -2 | | +2 | μA |
| DC Current (V_{DD}) | I_{DD} | Normal Mode | 3.3 V or 1.8V Logic | | 290 | 360 | μA |
| | | Bypass Mode | 3.3 V or 1.8V Logic | | 270 | 340 | |
| DC Current ($V_{SS_{EXT}}$) | I_{VSS} | $V_{SS_{EXT}} = -3.3\text{ V}$ | | | -46 | -60 | μA |
| Insertion Loss RFX to RFC | IL | 900 MHz | | | 0.93 | 1.4¹ | dB |
| | | 2100 MHz | | | 1.1 | 1.5 | |
| | | 2700 MHz | | | 1.2 | 1.6 | |
| | | 2700 MHz – 4000 MHz | | | 1.1 | 1.65² | |
| | | 4000 MHz – 8000 MHz | | | 2.3 | | |
| Minimum Isolation RFX to RFC | ISOC | 400 MHz – 900 MHz | | 57.5 | 62 | | dB |
| | | 900 MHz – 2100 MHz | | 51 | 56 | | |
| | | 2100 MHz – 2700 MHz | | 49.5 | 54 | | |
| | | 2700 MHz – 4000 MHz | | 45 | 50 | | |
| | | 4000 MHz – 8000 MHz | | 31 | 36.5 | | |
| Minimum Isolation RFX to RFX | ISOX | 400 MHz – 900 MHz | | 56.5 | 61.5 | | dB |
| | | 900 MHz – 2100 MHz | | 50 | 55 | | |
| | | 2100 MHz – 2700 MHz | | 48 | 53 | | |
| | | 2700 MHz – 4000 MHz | | 44.5 | 49.5 | | |
| | | 4000 MHz – 8000 MHz | | 30.5 | 36.5 | | |
| Insertion Loss Flatness | IL_{FLAT} | 400 MHz – 3800 MHz Any 400 MHz range | | | 0.1 | 0.4 | dB |
| VSWR RFC | $VSWR_{RFC}$ | RF1 through RF5 selected | | | 1.25:1 | 1.78:1 | - |
| VSWR RFX (On Ports) | $VSWR_{ON}$ | RF1 through RF5 selected | | | 1.33:1 | 1.78:1 | - |
| VSWR RFX (Term Ports) | $VSWR_{TERM}$ | RF1 through RF5 unselected | | | 1.15:1 | 1.58:1 | - |
| Maximum RFX Port VSWR During Switching | $VSWR_T$ | From RFX Active to RFX Term | | | 1.7:1 | | - |
| | | From RFX Term to RFX Active | | | 2:1 | | |
| Minimum Return Loss (RFC Port) | RFC_{RL} | RF1 through RF5 selected 400 MHz – 4000 MHz | | 10 | 16 | | dB |
| Minimum Return Loss (RFX Port) | RFX_{RL} | 400 MHz – 4000 MHz | | | | | dB |
| | | | | Active | 9 | 13 | |
| | | | | Terminated | 11 | 15 | |
| Input 1dB Compression ³ | ICP_{1dB} | | | 34 | 36.5 | | dBm |
| Input 0.1dB Compression ³ | $ICP_{0.1dB}$ | | | 28 | 35 | | dBm |
| Input IP2 | IIP2 | $F_{RF1} = 2000\text{ MHz}$, $F_{RF2} = 2010\text{ MHz}$ RF Input = RFX, $P_{IN} = +20\text{ dBm / tone}$ $F_{RF1} + F_{RF2}$ Term | | | 114 | | dBm |
| Input IP3 | IIP3 | $\Delta F = 1\text{ MHz}$ | | | | | dBm |
| | | RF Input = RFX | | $F_{RF} = 400\text{ MHz}$ | 45 | 60.5 | |
| | | $P_{IN} = +20\text{ dBm/ tone}$ | | $F_{RF} = 2000\text{ MHz}$ | 56 | 60 | |
| | | | | $F_{RF} = 4000\text{ MHz}$ | | 60.5 | |

Note 1 – Items in min/max columns in **bold italics** are Guaranteed by Test.

Note 2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

Note 3 – The input 0.1dB and 1dB compression points are linearity figures of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power and Figure 1 for maximum operating RF input power.

Typical Application Circuit, Normal mode ($V_{DD}= 3.3\text{ V}$, $V_{SS_{EXT}}= 0\text{ V}$) or Bypass mode ($V_{DD}= 3.3\text{ V}$, $V_{SS_{EXT}}= -3.3\text{ V}$), $T_C = +25\text{ }^\circ\text{C}$, $F_{RF} = 2000\text{ MHz}$, Input power = 0 dBm, $Z_S = Z_L = 50\ \Omega$, RFX = one of the five input ports, PCB board trace and connector losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--|--------------|--|---|------|-----|-------|
| Group Delay | GD | | | 0.43 | 1 | ns |
| Switching Time ⁴ | T_{SW} | Bypass Mode | 50% CTRL to 90% RF | 256 | 345 | ns |
| | | | 50% CTRL to 10% RF | 256 | 345 | |
| | | | 50% CTRL to RF settled within +/- 0.1 dB of I.L. value. | 285 | | |
| Maximum Switching Rate ⁵ | SW_{RATE} | Pin 20 = GND | | 25 | | kHz |
| | | Pin 20 = $V_{SS_{EXT}}$ applied | | 290 | | |
| Maximum spurious level on any RF port ⁶ | $Spur_{MAX}$ | RF ports terminated into 50 Ω RFX connected to RFC | | -120 | | dBm |

Note 1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test.

Note 2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

Note 3 – The input 0.1dB and 1dB compression points are linearity figures of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power and Figure 1 for maximum operating RF input power.

Note 4 – $F_{RF} = 1\text{GHz}$.

Note 5 – Minimum time required between switching of states = 1/ (Maximum Switching Rate).

Note 6 – Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.

Typical Application Circuit, Normal mode ($V_{DD}= 3.3\text{ V}$, $V_{SS_{EXT}}= 0\text{ V}$), $T_C = +105\text{ }^\circ\text{C}$, Input power = 0 dBm, $Z_S = Z_L = 50\ \Omega$, RFX = one of the five input ports, PCB board trace and connector losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-----------------------------------|-------------------|---------------------|------------|------|-----|-------|
| Insertion Loss RFX to RFC | IL | 50 MHz - 900 MHz | | 1.2 | 1.7 | dB |
| | | 900 MHz - 2100 MHz | | 1.3 | 1.7 | |
| | | 2100 MHz - 2700 MHz | | 1.4 | 1.8 | |
| | | 2700 MHz – 4000 MHz | | 1.4 | 2.0 | |
| | | 4000 MHz – 8000 MHz | | 2.7 | | |
| Minimum Isolation RFX to RFC | ISOC | 50 MHz – 900 MHz | 57 | 61.5 | | dB |
| | | 900 MHz – 2100 MHz | 50.5 | 55.5 | | |
| | | 2100 MHz – 2700 MHz | 49 | 53.5 | | |
| | | 2700 MHz – 4000 MHz | 44.5 | 49.5 | | |
| | | 4000 MHz – 8000 MHz | 30.5 | 36 | | |
| Minimum Isolation RFX to RFX | ISOX | 50 MHz – 900 MHz | 56 | 61 | | dB |
| | | 900 MHz – 2100 MHz | 49.5 | 54.5 | | |
| | | 2100 MHz – 2700 MHz | 47.5 | 52.5 | | |
| | | 2700 MHz – 4000 MHz | 44 | 49 | | |
| | | 4000 MHz – 8000 MHz | 30 | 36 | | |
| Minimum Return Loss (RFC Port) | RFC _{RL} | 50 MHz – 4000 MHz | 9 | 15 | | dB |
| Minimum Return Loss (RFX Port) | RFX _{RL} | 50 MHz – 4000 MHz | Active | 8 | 12 | dB |
| | | | Terminated | 10 | 14 | |

Note – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

TABLE 1: SWITCH CONTROL TRUTH TABLE

| Mode | V3 | V2 | V1 |
|---------|----|----|----|
| All off | 0 | 0 | 0 |
| RF1 on | 0 | 0 | 1 |
| RF2 on | 0 | 1 | 0 |
| RF3 on | 0 | 1 | 1 |
| RF4 on | 1 | 0 | 0 |
| RF5 on | 1 | 0 | 1 |
| All off | 1 | 1 | 0 |
| All off | 1 | 1 | 1 |

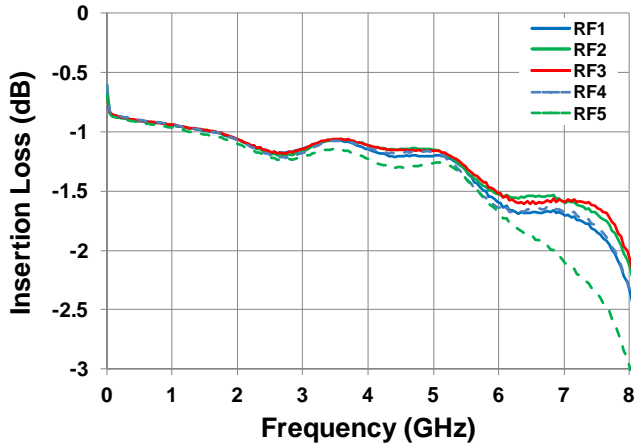
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

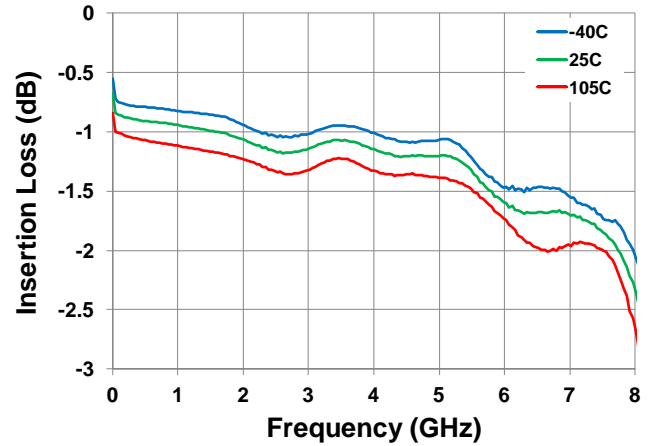
- $V_{DD} = 3.3 \text{ V}$.
- $T_{CASE} = +25 \text{ }^{\circ}\text{C}$ (T_{CASE} = Temperature of exposed paddle).
- $F_{RF} = 2000 \text{ MHz}$.
- RFX is the driven RF port and RFC is the output port.
- $P_{in} = 10 \text{ dBm}$ for all small signal tests.
- $P_{in} = +15 \text{ dBm/}$ tone applied to selected RFX port for two tone linearity tests.
- Two tone frequency spacing = 5 MHz.
- $Z_S = Z_L = 50 \text{ ohms}$.
- All unused RF ports terminated into 50 ohms.
- For Insertion Loss and Isolation plots, RF trace and connector losses are de-embedded (see EVKIT Board and Connector loss plot).
- Plots for Isolation and Insertion Loss over temperature and voltage are for a typical path. For performance of a specific path, refer to the online S-Parameter file.

TYPICAL OPERATING CONDITIONS (- 1 -)

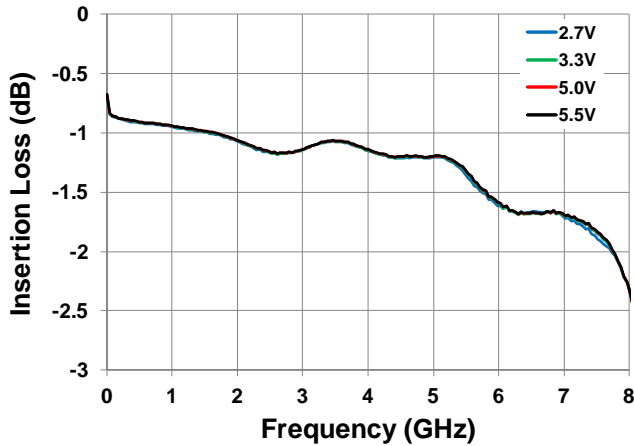
Insertion Loss vs. Selected Switch Path



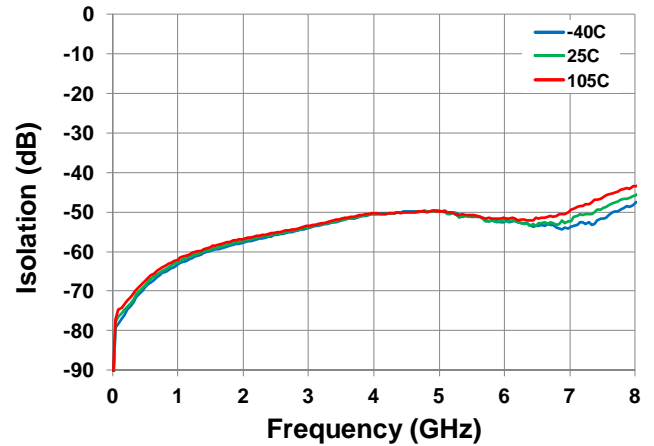
Insertion Loss vs. Temperature



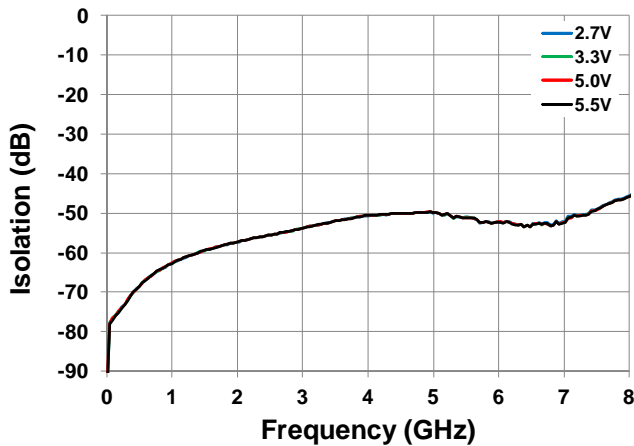
Insertion Loss vs. Voltage



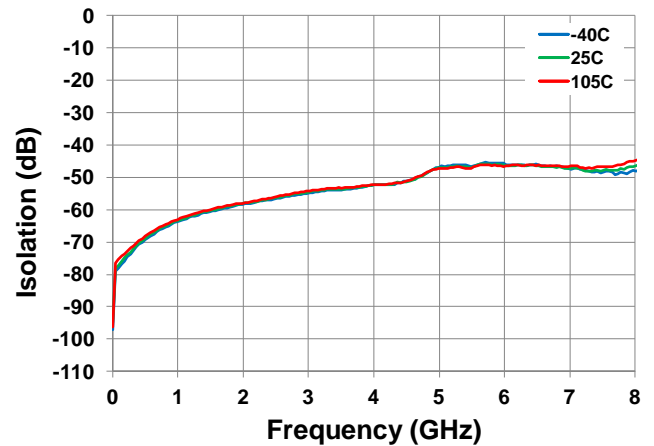
RFX → RFC Isolation vs. Temperature



RFX → RFC Isolation vs. Voltage

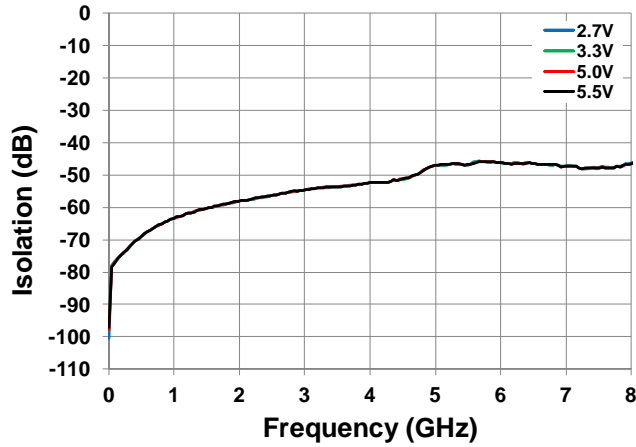


RFX → RFX Isolation vs. Temperature

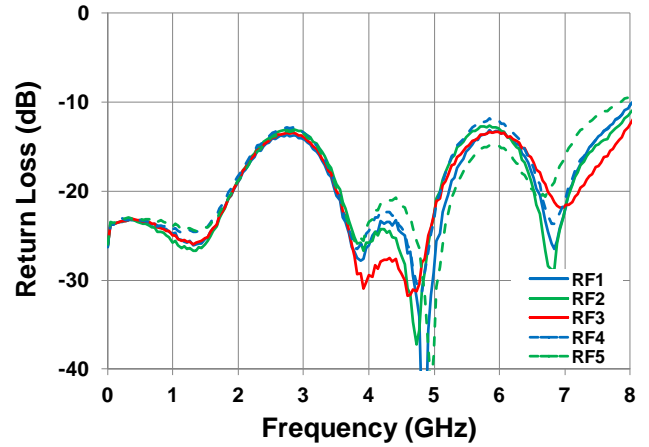


TYPICAL OPERATING CONDITIONS (- 2 -)

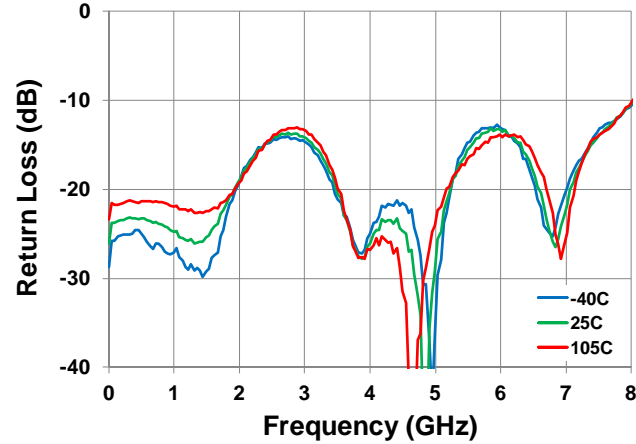
RFX → RFX Isolation vs. Voltage



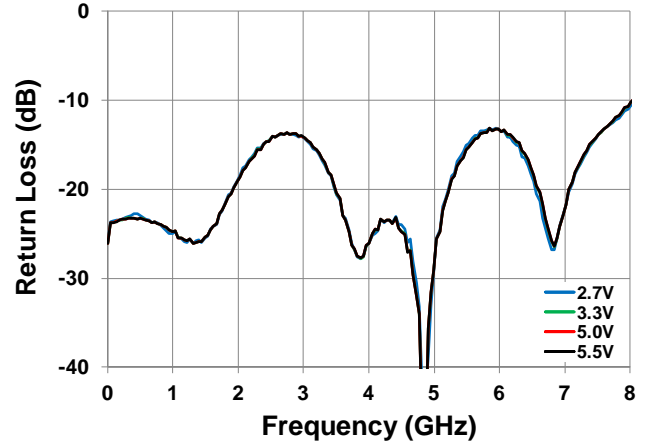
RFX Return Loss vs. Selected RFX Port



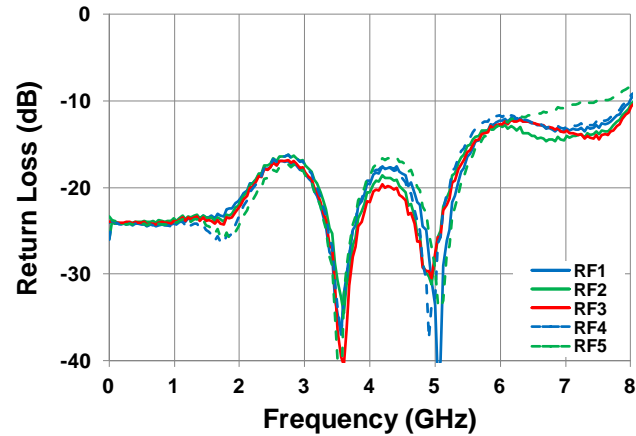
RFX Selected Return Loss vs. Temperature



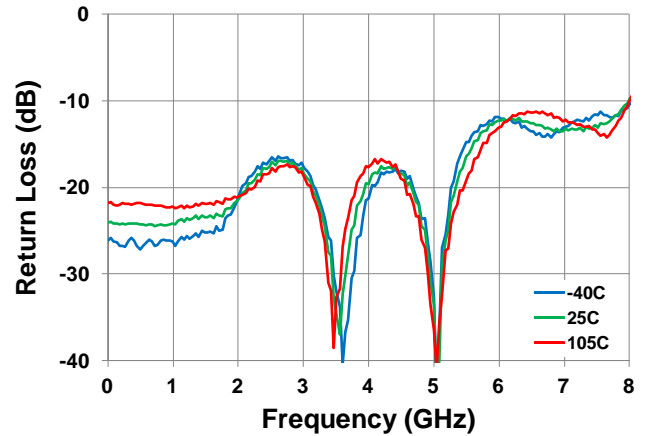
RFX Selected Return Loss vs. Voltage



RFC Return Loss vs. Selected RFX Port

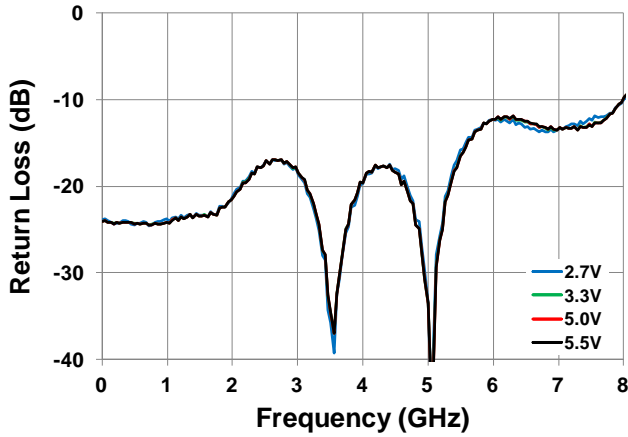


RFC Return Loss with RFX Selected vs. Temperature

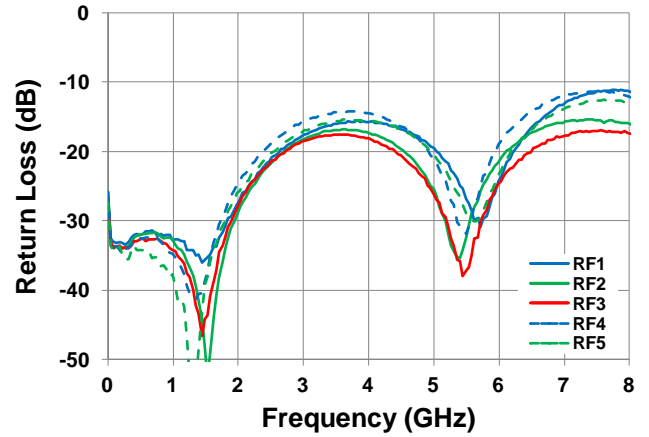


TYPICAL OPERATING CONDITIONS (- 3 -)

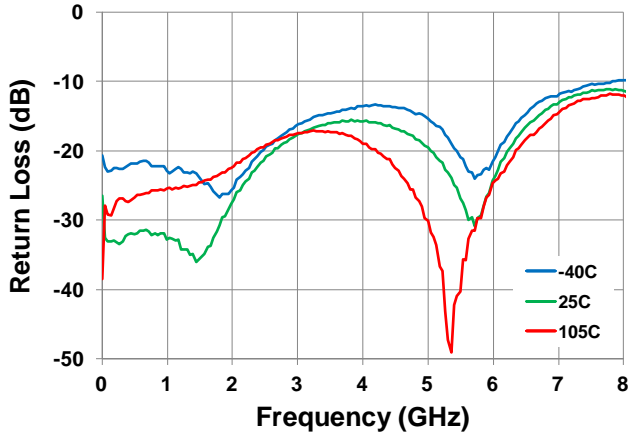
RFC Return Loss with RFX Selected vs. Voltage



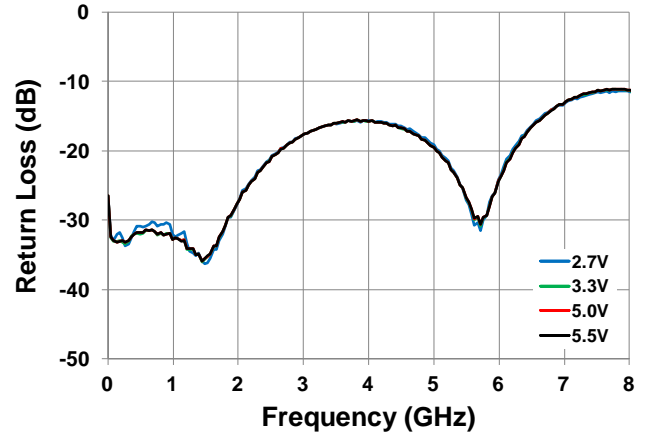
RFX Terminated Return Loss vs. RFX Port



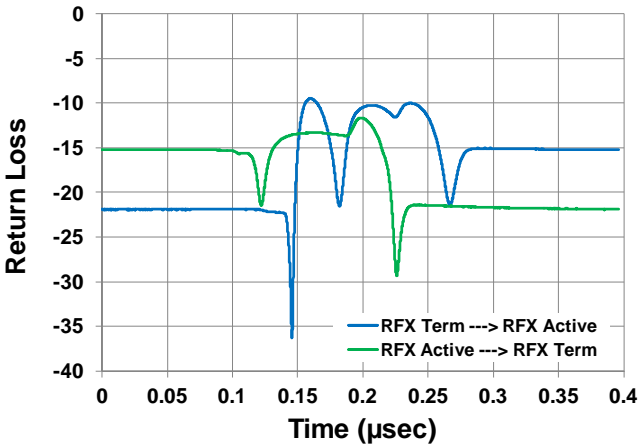
RFX Terminated Return Loss vs. Temperature



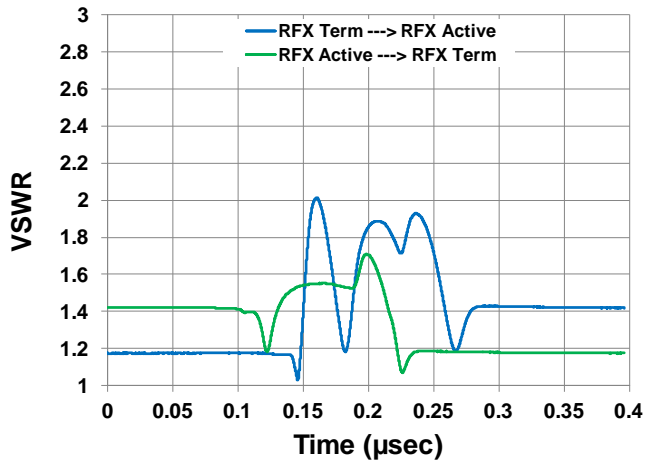
RFX Terminated Return Loss vs. Voltage



Return Loss (During Switching) vs. Time

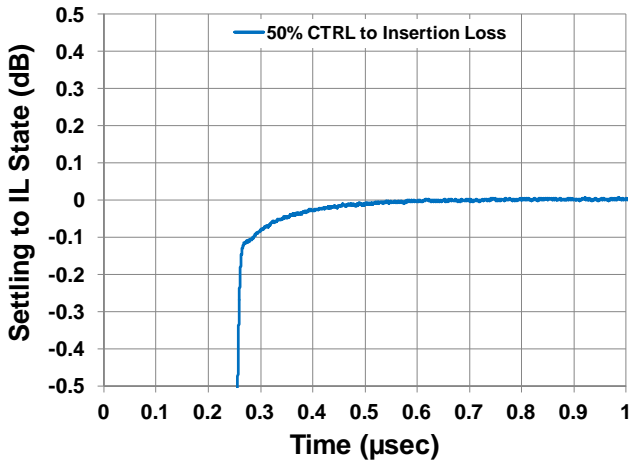


VSWR (During Switching) vs. Time

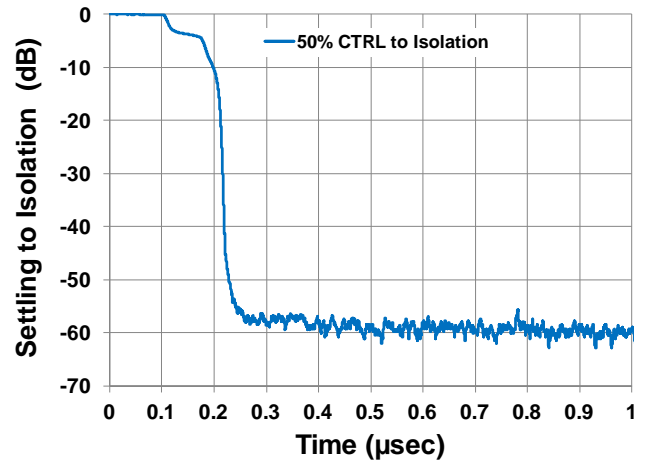


TYPICAL OPERATING CONDITIONS (- 4 -)

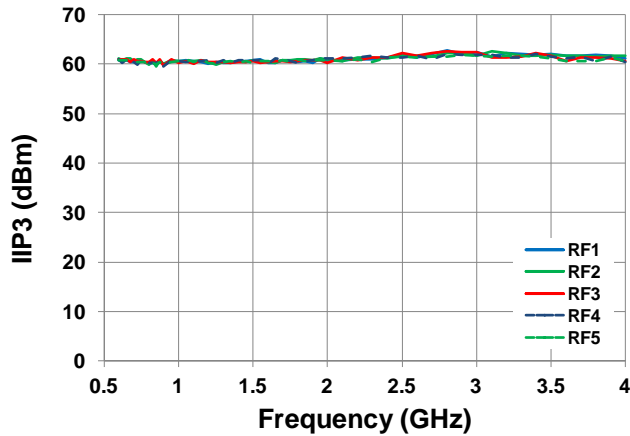
RFX Switching Time [RFX Terminated to RFX Active]



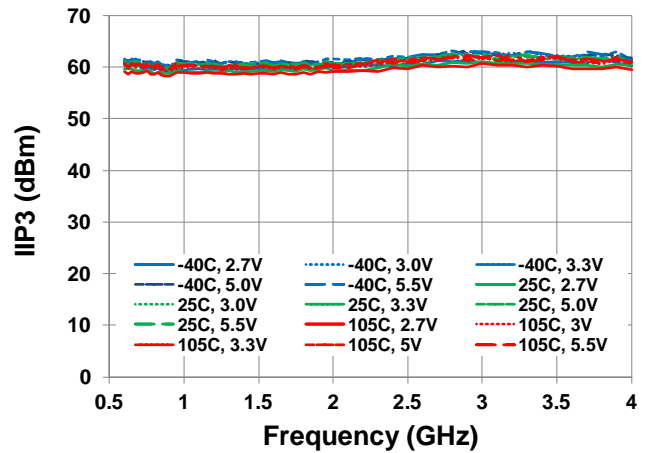
RFX Switching Time [RFX Active to RFX Terminated]



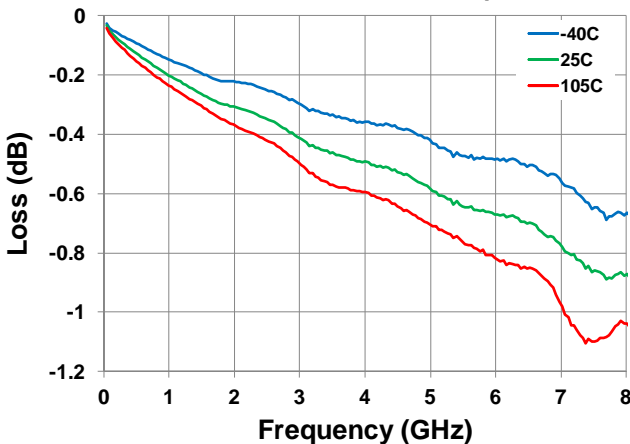
RFX IIP3 vs. Selected RFX Port



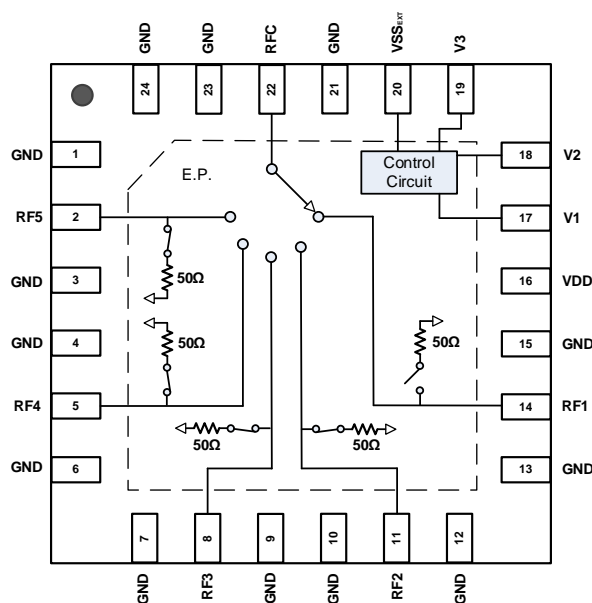
RFX IIP3 vs. Temperature and Voltage



EVKIT Trace and Connector Loss vs. Temperature



PIN DIAGRAM



PIN DESCRIPTION

| Pin | Name | Function |
|--|--------------------|--|
| 1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24 | GND | Ground these pins as close to the device as possible. |
| 2 | RF5 | RF5 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 5 | RF4 | RF4 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 8 | RF3 | RF3 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 11 | RF2 | RF2 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 14 | RF1 | RF1 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 16 | VDD | Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin. |
| 17 | V1 | Control pin to set switch state. See Table 1. |
| 18 | V2 | Control pin to set switch state. See Table 1. |
| 19 | V3 | Control pin to set switch state. See Table 1. |
| 20 | VSS _{EXT} | External VSS negative voltage control. Connect to ground to enable on chip negative voltage generator. To bypass and disable on chip generator connect this pin to an external VSS. |
| 22 | RFC | RF Common Port. Matched to 50 ohms when one of the 5 RF ports is selected. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 25 | — EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |

APPLICATIONS INFORMATION

Default Start-up

There are no internal pull-up or pull-down resistors on the Control pins.

Logic Control

Control pins V1, V2, and V3 are used to set the state of the SP5T switch (see Table 1).

External Vss

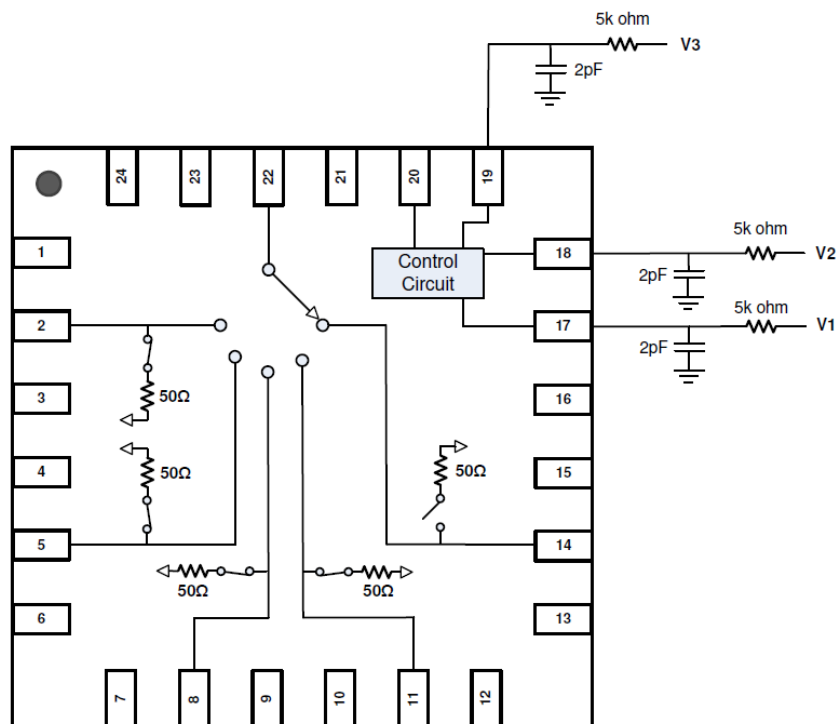
The F2915 is designed with an on-chip negative voltage generator. This on-chip generator is enabled by connecting pin 20 of the device to ground. To disable the on-chip generator apply a negative voltage to pin 20 (VSSEXT) of the device within the range stated in the Recommended Operating Conditions Table.

Power Supplies

A common VDD power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than $1 \text{ V} / 20 \mu\text{s}$. In addition, all control pins should remain at $0 \text{ V} (+/-0.3 \text{ V})$ while the supply voltage ramps or while it returns to zero.

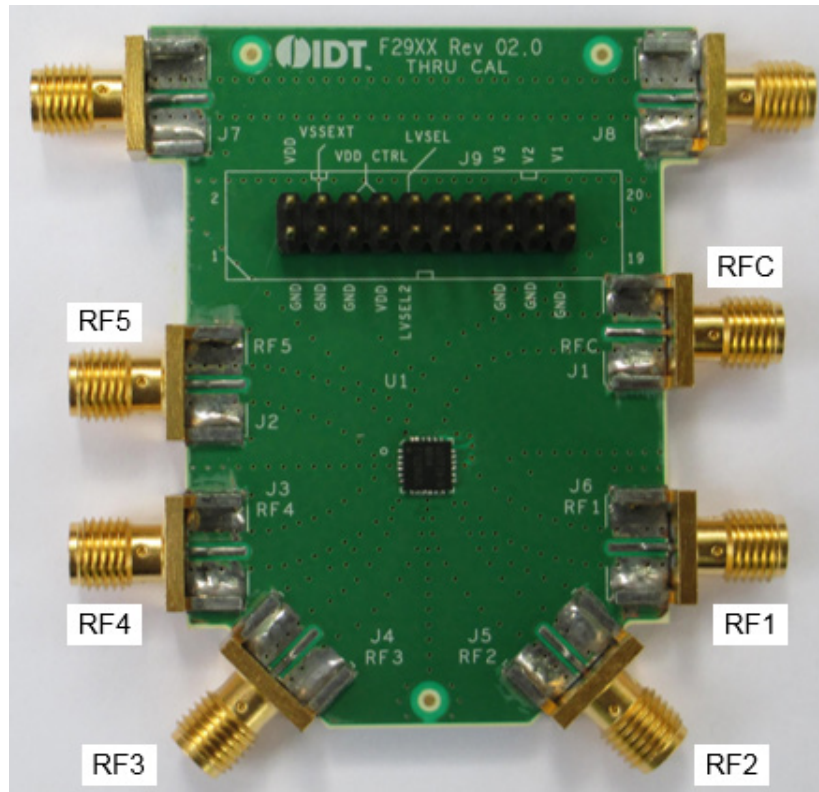
Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 17, 18, and 19 as shown below.

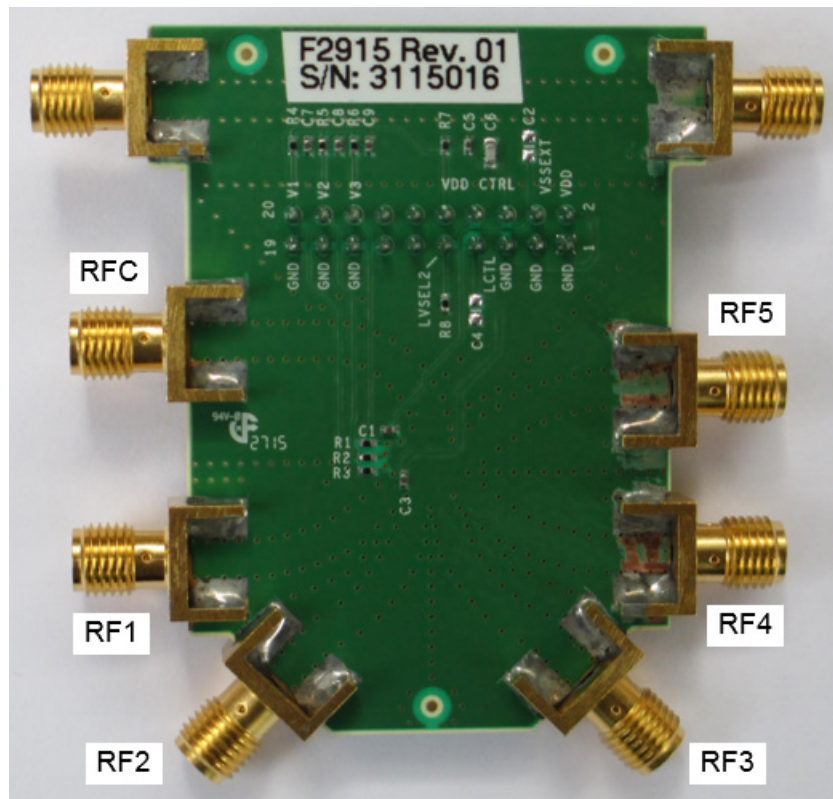


EVKIT PICTURES

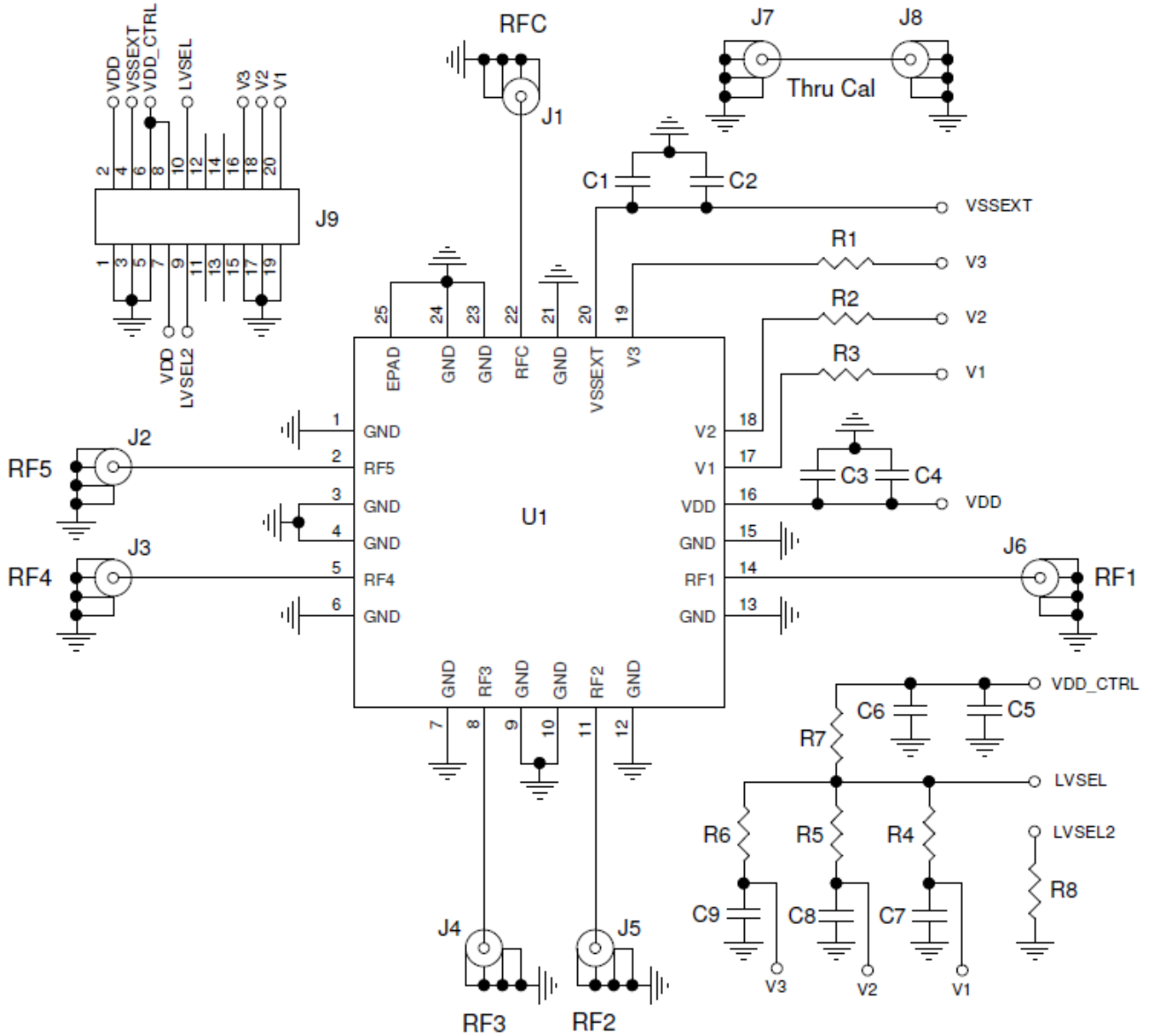
Top View



Bottom View



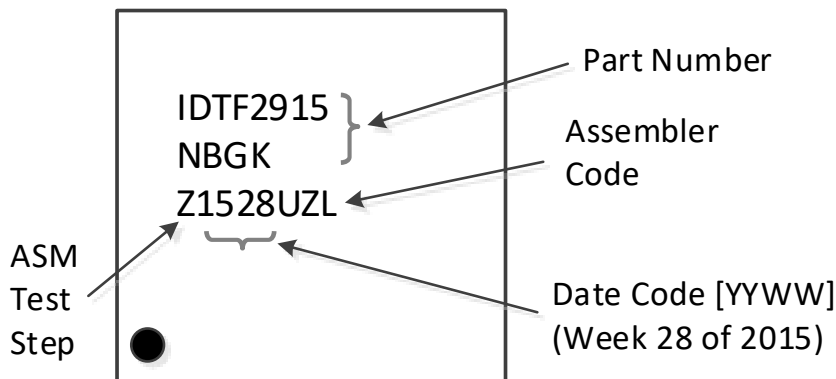
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM

| Part Reference | QTY | DESCRIPTION | Mfr. Part # | Mfr. |
|------------------------|-----|--|----------------------|-----------------|
| C1, C3, C5, C7, C8, C9 | 6 | 100 pF ±5%, 50V, COG Ceramic Capacitor (0402) | GRM1555C1H101J | Murata |
| C2 | 0 | Not Installed (0603) | | |
| C4 | 0 | Not Installed (0603) | | |
| C6 | 1 | 1000 pF ±5%, 50V, COG Ceramic Capacitor (0603) | GRM1885C1H102J | Murata |
| R1, R2, R3 | 3 | 0 Ω ±1%, 1/10W, Resistor (0402) | ERJ-2GE0R00X | Panasonic |
| R4, R5, R6 | 3 | 100 kΩ ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1003X | Panasonic |
| R7 | 1 | 15 kΩ ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1502X | Panasonic |
| R8 | 1 | 22 kΩ ±1%, 1/10W, Resistor (0402) | ERJ-2RKF2202X | Panasonic |
| J1-J8 | 8 | Edge Launch SMA (0.375 inch pitch ground tabs) | 142-0701-851 | Emerson Johnson |
| J9 | 1 | CONN HEADER VERT DBL 10 X 2 POS GOLD | 67997-120HLF | FCI |
| U1 | 1 | SP5T Switch 4 mm x 4 mm QFN24-EP | F2915NBGK | Renesas (IDT) |
| | 1 | Printed Circuit Board | F29XX EVKIT Rev 02.0 | Renesas (IDT) |

TOP MARKINGS



PACKAGE OUTLINE DRAWINGS

The [package outline drawings](#) are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

EVKIT OPERATION

External Supply Setup

Set up a VDD power supply in the voltage range of 2.7 V to 5.5 V and disable the power supply output.

If using the on-chip negative voltage generator install a 2-pin shunt to short pins 3 and 4 of J9.

If an external negative voltage supply is to be used set its voltage within the range of -3.6 V to -3.2 V and disable it. Also, be sure there are no jumper connections on pins 3 and 4 of J9.

Logic Control Setup

Using the EVKIT to manually set the control logic:

On connector J9 connect a 2-pin shunt from pin 7 (VDD) to pin 8 (VDD_CTRL). This connection provides the VDD voltage supply to the Eval Board logic control pull up network.

On connector J9 connect a 2-pin shunt from pin 9 (LVSEL2) to pin 10 (LVSEL). This connection enables R7 (15 k Ω) and R8 (22 k Ω) to form a voltage divider to set the proper logic control levels to support the full voltage range of VDD. Note that when using the on-board R7 / R8 voltage divider the current draw from the VDD supply will be higher by approximately $VDD / 37 \text{ k}\Omega$.

Connector J9 has 3 logic input pins: V1 (pin 20), V2 (pin 18), and V3 (pin 16). See Table 1 for Logic Truth Table. With the pullup network enabled (as noted above), when these pins are left open a logic high will be provided through pull up resistors R4, R5, and R6. To set a logic low to V1, V2, and V3 connect 2-pin shunts from pin 16 to pin 15, pin 18 to pin 17 and pin 20 to pin 19 respectively.

Using external control logic:

Pins 6, 7, 8, 9, and 10 of J9 should have no connection. External logic controls can be applied to J9 pins 16 (V3), 18 (V2) and 20 (V1). See Table 1 for Logic Truth Table.

Turn-on Procedure

Setup the supplies and Eval Board as noted in the **External Supply Setup** and **Logic Control Setup** sections above.

Connect the preset disabled VDD power supply to pin 2 (VDD) and pin 1 (GND) of J9.

If the external negative voltage source is to be used, connect the disabled supply to pin 4 (VSSEXT) and pin 3 (GND) of J9. If using on-chip negative supply be sure the 2-pin shunt is installed connecting pin 3 to pin 4.

Enable the VDD supply then enable the VSSEXT supply (if used).

Set the desired logic setting using V1, V2, and V3 to achieve the desired Table 1 setting. Note that external control logic should not be applied without VDD being applied first.

Turn-off Procedure

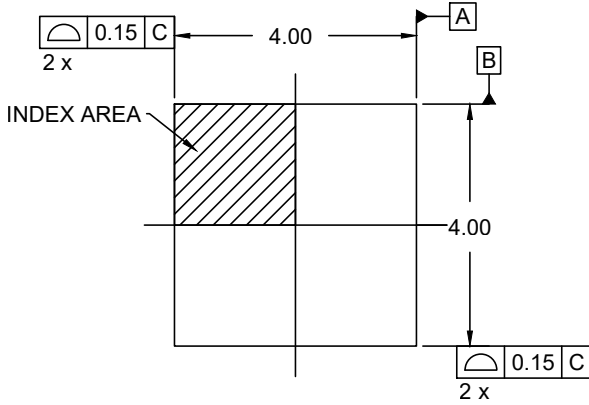
If using external control logic V1, V2, V3 must be set to a logic low.

Disable any external VSSEXT supply.

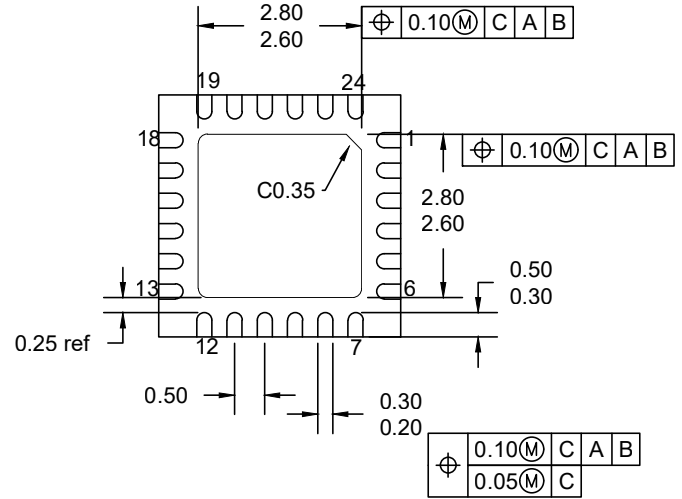
Disable the VDD supply.

REVISION HISTORY

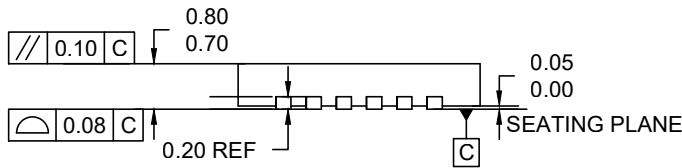
| Date | Description of Change |
|-------------------|---|
| October 26, 2021 | <ul style="list-style-type: none"> • Added RF performance data at 105°C • Completed other minor changes |
| June 22, 2020 | Rebranded the document and completed minor changes throughout; no technical updates were made |
| May 5, 2016 | Added new Guaranteed by Design parameters to specification table. |
| February 22, 2016 | Added min/max limits. Increased frequency range. Updated ESD values. |
| December 11, 2015 | Initial Release |



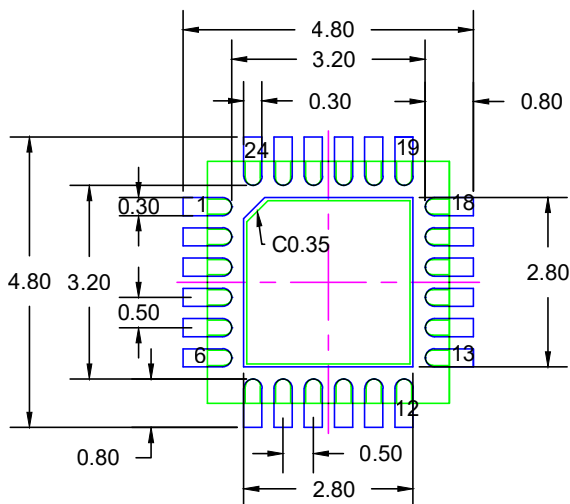
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatibles.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

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(Disclaimer Rev.1.0 Mar 2020)

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