National Semiconductor

July 25, 2006
Rev - 2.1/CS
RoHS Compliant

Evaluation Board User's Guide

ADC121S625 12-Bit, 50 kSPS to 200 kSPS, Differential Input, Micro-Power Sampling A/D Converter

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1.0 Introduction

The ADC121S625EVAL/RoHS Design Kit (consisting of the ADC121S625B Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of the National Semiconductor ADC121S625 12-bit Analog-to-Digital Converter, which can operate at speeds up to 200 kSPS.

The evaluation board can be used in either of two modes. In the Stand-Alone or Manual mode, suitable test equipment, such as a logic analyzer, can be used with the board to evaluate the ADC121S625's performance.

In the Computer or Automatic mode, data capture and evaluation is simplified by connecting this board to National Semiconductor's Data Capture Board (order number WAVEVSN BRD 4.0) with a ribbon cable (order number WV4ADCIFCABLE), which is connected to a personal computer through a USB port and running WaveVision4 software. The WaveVision4 program can be downloaded from the web at http://www.national.com/adc.

The WaveVision4 software operates under Microsoft Windows. The signal at the Analog Input is digitized, captured, and displayed on a PC monitor in the time and frequency domain.

The software will perform an FFT on the captured data upon command. This FFT plot shows dynamic performance in the form of SNR, SINAD, THD, SFDR and ENOB. A histogram of the captured data is also available.

The differential signal at analog inputs J2 or J3 is digitized by U1, the ADC121S625.

The ADC121S625 uses an external oscillator that is provided on this board by Y2 or J6.

2.0 Board Assembly

The ADC121S625B evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement and to *Figure 2* for the Evaluation Board schematic.

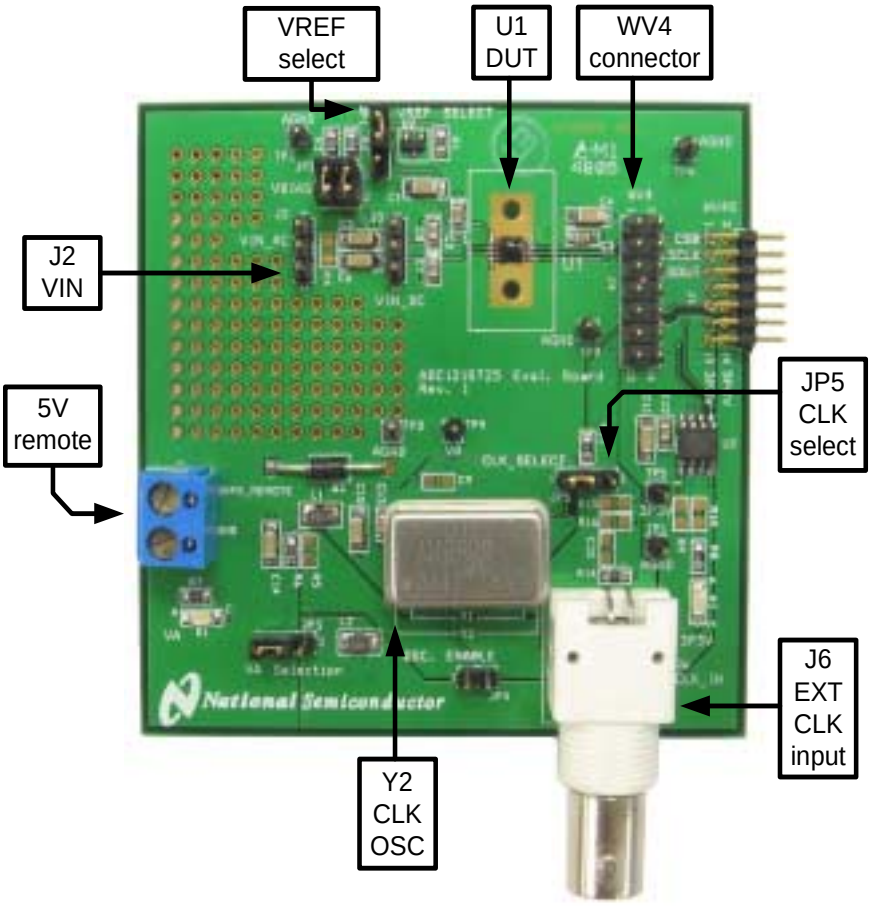

Figure 1 Component and Test Point Locations

3.0 Quick Start

The ADC121S625B evaluation board may be used in the Stand-Alone mode to capture data with a logic analyzer or third party equipment, or it may be used in the Computer Mode with a WaveVision4 Data Capture (WV4) Board. In both cases, the data may be analyzed with the WaveVision4 software.

3.1 Stand Alone Mode

Refer to *Figure 1* for locations of test points and major components.

1. Install an appropriate crystal oscillator into socket Y2 and short pins 1 & 2 of JP5 (See *Table 1*). Alternatively, connect a signal generator with TTL logic levels to BNC connector J6 and short pins 2 & 3 of JP5. In either case, short pins 4 & 10 of J4 to provide the clock signal to the ADC121S625. If using an external source, remove the oscillator from Y2. If using an oscillator at Y2, remove the signal source from J6. The presence of a second clock source could add noise to the conversion process.
2. Connect a clean analog (non-switching) +5V power source to Power Connector J5.
3. Short pins 1 & 2 of JP3 and turn on the power supply.
4. Dynamic differential signal sources centered around ground should be connected across pins 1 & 3 of J2. Pin 2 of J2 is ground. If the source has a 50Ω output impedance, install a 51 ohm resistor at R4. Otherwise, the signal level will be twice as large as expected. To accurately evaluate the performance of the ADC121S625, the source must be better than 90dB THD.
5. Short pins 1 & 2 and pins 3 & 4 of JP2 to provide the bias voltage of VREF for the input to the ADC when driving the ADC from J2.
6. Differential DC sources or dynamic differential signal sources centered at a DC bias point should be connected across pins 1 & 3 of J3. Pin 2 of J3 is ground.
7. Remove the shorts across pins 1 & 2 and pins 3 & 4 of JP2 when driving the ADC input from J3.
8. Select the 2.5V shunt voltage reference as VREF by shorting pins 2 & 3 of JP1 or select VA as VREF by shorting pins 1 & 2 of JP1. If it is desirable to provide an external reference voltage, the jumper must be removed from JP1 and pin 2 may be driven directly.
9. The digital inputs and outputs are available for probing at J4.

3.2 Computer Mode

Refer to *Figure 1* for locations of test points and major components.

1. Run the WaveVision4 program. Version 4.2 or higher is required to interface the WV4 board with the ADC121S625B evaluation board. While the program is loading, continue below.
2. Install an appropriate crystal oscillator into socket Y2 and short pins 1 & 2 of JP5 (See *Table 1*). Alternatively, connect a signal generator with TTL logic levels to BNC connector J6 and short pins 2 & 3 of JP5.
3. Connect a USB cable between the WaveVision4 Data Capture Board and the PC running the WaveVision4 program.
4. Connect a ribbon cable (order number WV4ADCIFCABLE) between J4 of the ADC121S625B evaluation board and J3 of the WV4 board.
5. Connect a clean analog (non-switching) +5V power source to Power Connector J5.
6. Short pins 1 & 2 of JP3 and turn on the power supply. *See Section 4.5 for detailed Power Supply Information*
7. Connect a separate analog +5V power source to power connector J1 on the WV4 board and turn on the power.
8. Connect a jumper cable between TP10 (+3.3V) of the WV4 board and TP5 (3P3V) of the ADC121S625B board.
9. Perform steps 4 & 5 or 6 & 7 of section 3.1 to drive the analog inputs.
10. Perform step 8 of section 3.1 to select the reference voltage.
11. Refer to section 5.0 on Software Operation and Settings.

4.0 Functional Description

Table 1 describes the function of the various jumpers on the ADC121S625B evaluation board. The Evaluation Board schematic is shown in *Figure 2*.

Jumper	Pins 1 & 2	Pins 2 & 3
JP1	Select VA as the VREF	Select 2.5V reg. as the VREF
JP2	Short pins 1 & 2 and pins 3 & 4 to bias input pins at VREF	
JP3	Select 5P0V_REMOTE from J5	Select 5P0V from J1 (WV4S)
JP4	Enable OSC (not required)	
JP5	Select on-board clock OSC Y2	Select clock OSC at BNC J6

Table 1 Jumper Functions

4.1 The Signal Input

The input signal to be digitized should be applied across pins 1 & 3 of J2 or J3.

For input signals centered around ground, J2 should be utilized. Pin 2 of J2 is ground. Resistor R4 is a terminating resistor for the input source. Since all sources do not have the same output impedance, R4 is not stuffed. However, it is recommended that it is stuffed by the end user with the appropriate value that matches the source.

The DC biasing for inputs applied to J2 is supplied through JP2. Short pins 1 & 2 and 3 & 4 of JP2 to properly bias the input to VREF.

If it is desired to digitize a differential DC voltage or a dynamic signal that is already properly biased for the ADC121S625, apply the signal to be digitized across pins 1 & 3 of J3. Pin 2 of J3 is ground. When applying the input at J3, all shorts on JP2 need to be removed.

Dynamic input signals should be applied through a bandpass filter to eliminate the noise and harmonics commonly associated with signal sources. To accurately evaluate the performance of the ADC121S625, the source must be better than 90dB THD

4.2 ADC Reference Circuitry

This evaluation board includes the option of selecting a fixed 2.5V shunt voltage reference or VA as the reference voltage. Select the 2.5V reference as VREF by shorting pins 2 & 3 of JP1 or select VA as VREF by shorting pins 1 & 2 of JP1. If it is desirable to provide an external reference voltage, the jumper must be removed from JP1 and pin 2 may be driven directly.

If it is desirable to change the LM4040DIM3-2.5 to an LM4040 with a different voltage, carefully remove it and adjust the value of R3 to limit the current through the LM4040.

4.3 ADC Clock Circuit

The crystal-based oscillator provided on the evaluation board is selected by shorting pins 1 & 2 of JP5. It is best to remove any external signal generator from J6 when using this oscillator to reduce any unnecessary noise.

This board will also accept a clock signal from an external source by connecting that source to BNC J6 and shorting pins 2 & 3 of JP5. The input applied at J6 is 50 ohm terminated by R14. The external clock signal must meet TTL input requirements. It is best to remove the oscillator at Y2 when using an external clock source to reduce any unnecessary noise.

Regardless of the clock source selected by JP5, the clock signal is designed to be routed off the ADC121S625B evaluation board to National's WV4 board. This assumes a "computer mode" operation of the evaluation board. For applications utilizing the evaluation board in manual mode, short pins 4 & 10 of J4 with a short jumper wire to provide the clock signal to the ADC121S625.

4.4 Digital Data Output

The serial data output from this board may be monitored at J1 or J4.

4.5 Power Supply Connections

When operating in "computer mode" with the WV4 Board, voltage 5P0V for VA and 3P3V for U3 must be supplied to the ADC121S625B evaluation board. For best performance from the ADC121S625, the 5P0V voltage for VA should be supplied by a separate power supply to J5. The 3P3V voltage may be pulled off the WV4 Board with a jumper wire at TP10 (WV4) and applied to TP5.

When operating in "manual mode", only voltage 5P0V needs to be applied to J5.

The 5P0V voltage needs to be set between +4.5V and +5.5V and a shorting jumper must be placed across pins 1 & 2 of JP3.

5.0 Software Operation and Settings

The WaveVision4 software is included with the WV4 board and the latest version can be downloaded for free from National's web site at http://www.national.com/adc. To install this software, follow the procedure in the WaveVision4 Board User's Guide. Once the software is installed, run it and set it up as follows:

1. Connect the WV4 board to the host computer with a USB cable.
2. From the WaveVision main menu, go to Settings, then Board Settings and do the following:

   Select the following from the WaveVision4 main menu:
   - WaveVision 4.0 (USB)
   - # of Samples: 2K to 32K, as desired
3. Apply power as specified in Section 4.5, click on the **"Test"** button and await the firmware to download.
4. Click on the **"Accept"** button.
5. After the steps outlined in Section 3.2 are completed, click on 'Acquire' then 'Samples' from the Main Menu (you can also press the *F1* shortcut key). If a dialog box opens, select 'Discard' or press the *Escape* key to start collecting new updated samples.

A plot of the selected number of samples will be displayed. Make sure there is no clipping of data samples. The samples may be further analyzed by clicking on the magnifying glass icon, then clicking and dragging across a specific area of the plot for better data inspection. See the WaveVision4 Board User's Guide for details.

To view an FFT of the data captured, click on the 'FFT' tab. This plot may be zoomed in on like the data plot. A display of dynamic performance parameters in the form of SINAD, SNR, THD, SFDR and ENOB will be displayed at the top right hand corner of the FFT plot.

Acquired data may be saved to a file. Plots may also be exported as graphics. See the Data Capture Board User's Guide for details.

6.0 Hardware Schematic

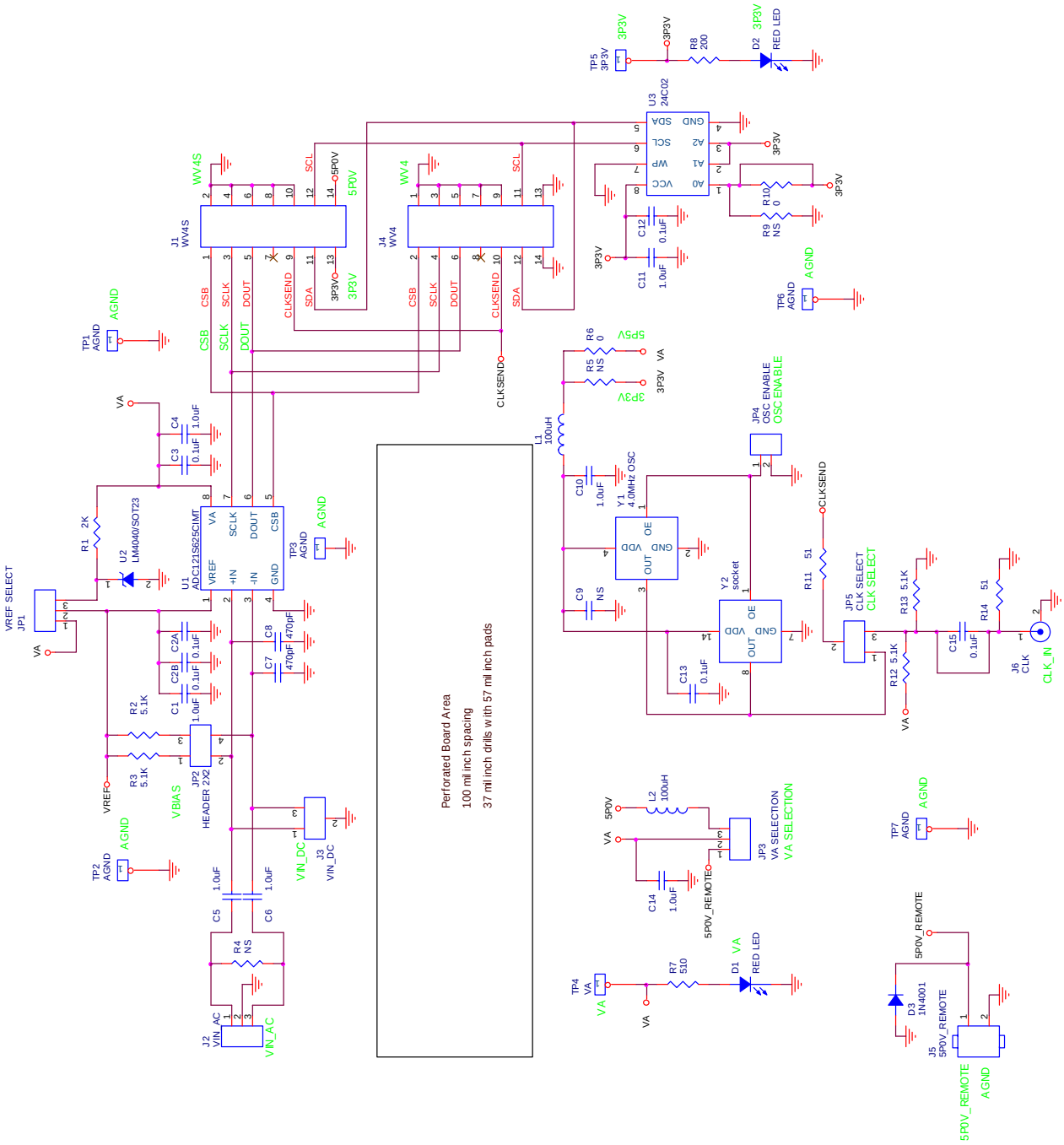

Figure 2 ADC121S625B Evaluation Board Schematic

7.0 Evaluation Board Specifications

Board Size:	3.0" x 3.0" (7.6 cm x 7.6 cm)	
Power Requirements	Min: +4.5V, 100mA	Max: +5.5V, 100 mA
Clock Frequency Range:	800 kHz to 4.0 MHz	
Analog Input	0V to 2VREF	

8.0 ADC121S625B Evaluation Board Bill of Materials

Item	Qty	Reference	PCB Footprint	Source	Source Part #	Value
1	7	C1,C4,C5,C6,C10,C11,C14	sm/c_1206	Digikey	445-1423-2-ND	1.0uF
2	4	C2,C3,C12,C13	sm/c_0805	Digikey	PCC1840TR-ND	0.1uF
3	2	C8,C7	sm/c_0805	Digikey	399-1142-1-ND	470pF
4	2	C15,C9	sm/c_0805			NS
5	2	D2,D1	sm/led_21	Digikey	516-1440-1-ND	RED LED
6	1	D3	DAX2/DO41	Digikey	1N4003-TPMSTR-ND	IN4003
7	1	JP1	header	Digikey	S1011E-36-ND	VREF SELECT
8	1	JP2	header	Digikey	S2041E-30-ND	HEADER 2X2
9	1	JP3	header	Digikey	S1011E-36-ND	VA SELECTION
10	1	JP4	header	Digikey	S1011E-36-ND	OSC ENABLE
11	1	JP5	header	Digikey	S1011E-36-ND	CLK SELECT
12	1	J1	rt angle header	Digikey	S5803-21-ND	WV4S
13	1	J2	header	Digikey	S1011E-36-ND	VIN_AC
14	1	J3	header	Digikey	S1011E-36-ND	VIN_DC
15	1	J4	header	Digikey	S2041E-30-ND	WV4
16	1	J5	term_block	Digikey	ED1609-ND	5P0V_REMOTE
17	1	J6	BNC	Digikey	ARF1177-ND	CLK
18	2	L1,L2	sm/l_1210	Digikey	445-15435-1-ND	100uH
19	1	R1	sm/r_0805		P2.0KATR-ND	2K
20	2	R3,R2	sm/r_0805		311-5.10KCRTR-ND	5.1K
21	6	R4,R5,R9,R10,R15,R16	sm/r_0805			NS
22	1	R6	sm/r_0805		RHM0.0ATR-ND	0
23	1	R7	sm/r_0805		RHM510CTR-ND	510
24	1	R8	sm/r_0805		P200CTR-ND	200
25	2	R14,R11	sm/r_0805		P51ACT-ND	51
26	5	TP1,TP2,TP3,TP6,TP7	header	Digikey	S1011E-36-ND	AGND
27	1	TP4	header	Digikey	S1011E-36-ND	VA
28	1	TP5	header	Digikey	S1011E-36-ND	3P3V
29	1	U1	MSOP8	National	ADC121S625CIMT	ADC121S625
30	1	U2	sm/SOT23	Digikey	LM4040DIM3-2.5TR	2.5V REF
31	1	U3	EEPROM	Digikey	AT24C02BN-10SU-1.8-ND	24C02
32	1	Y2B	OSC	Allied	EC1145-4.000M	4.0MHz OSC
33	1	Y2B	OSC_socket	Digikey	A462-ND	SOCKET
34	1	PCB	Eval Board rev 1	Adv Cir	121S725_r1	ADC121S725
35	5	2-pin jumpers	Jumper	Digikey	S9001-ND	SHUNT
36	4	Rubber Feet		Digikey	SJ5003-0-ND	BUMP

9.0 Test Points, Connectors, and Jumpers

Test Points on the ADC121S625B Evaluation Board

TP1: AGND	Ground. Located at the bottom right area of the board.
TP2: AGND	Ground. Located at the center of the board.
TP3: AGND	Ground. Located at the top left area of the board.
TP4: VA	VA test point. Located at the center of the board.
TP5: 3P3V	3.3V test point. Located at the middle right area of the board.
TP6: AGND	Ground. Located at the top right corner of the board.
TP7: AGND	Ground. Located in the middle right area of the board.

Connectors on the ADC121S625B Evaluation Board

J1: WV4S	14 pin dual row right angle male header: Connects to WV4S board.
J2: VIN_AC	Three pin male header: Differential AC input.
J3: VIN_DC	Three pin male header: Differential DC input.
J4: WV4	14 pin dual row male header: Connects to WV4 board.
J5: 5P0V_REMOTE	Terminal Block: Power connector for 5P0V.
J6: CLK_IN	BNC Connector: External clock input.

Selection Jumpers on the ADC121S625B Evaluation Board (Refer to Table 1 in Section 4.0 for configuration details)

JP1: VREF SELECT	Selects reference source for VREF.
JP2: VBIAS	Provides DC bias for analog inputs.
JP3: VA Selection	Selects source of voltage for VA.
JP4: OSC ENABLE	Not required for OSC provided with evaluation board.
JP5: CLK_SELECT	Selects clock source (on-board oscillator or external source).

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Concernant les EVMs avec antennes détachables

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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