Dual Channel 4A, 42V, Synchronous Step-Down Silent Switcher 2 with 6.2µA Quiescent Current

FEATURES

- Silent Switcher®2 Architecture:
  - Ultralow EMI on Any PCB
  - Eliminates PCB Layout Sensitivity
  - Internal Bypass Capacitors Reduce Radiated EMI
  - Optional Spread Spectrum Modulation
- 4A DC from Each Channel Simultaneously
- Up to 6A on Either Channel
- Ultralow Quiescent Current Burst Mode® Operation:
  - 6.2µA I_Q Regulating $12V_{IN}$ to $5V_{OUT1}$ and $3.3V_{OUT2}$
  - Output Ripple <$10mV_{P-P}$
- Optional External VC Pin: Fast Transient Response and Current Sharing (Extra 50µA I_Q/Channel)
- Forced Continuous Mode
- High Efficiency at High Frequency
- 94.6% Efficiency at 2A, $5V_{OUT}$ from $12V_{IN}$ at 2MHz
- 93.3% Efficiency at 4A, $5V_{OUT}$ from $12V_{IN}$ at 2MHz
- Fast Minimum Switch-On Time: 40ns
- Wide Input Voltage Range: 3.0V to 42V
- Adjustable and Synchronizable: 300kHz to 3MHz
- Small 4mm × 6mm 32-Pin LQFN Package

APPLICATIONS

- General Purpose Step-Down
- Automotive and Industrial Supplies

DESCRIPTION

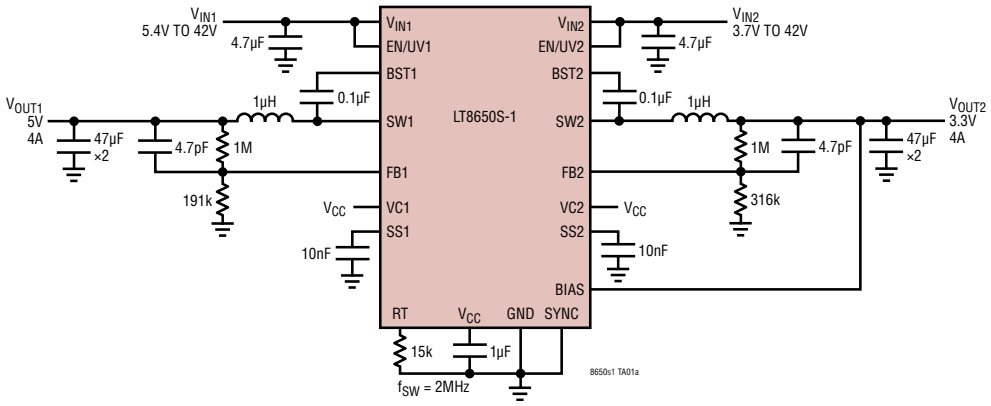
The LT®8650S-1 is a dual step-down regulator that delivers up to 4A of continuous current from both channels and supports loads up to 6A from each channel. The LT8650S-1 features the second generation Silent Switcher architecture to minimize EMI emissions while delivering high efficiency at high switching frequencies. This includes integration of bypass capacitors to optimize high frequency current loops and make it easy to achieve advertised EMI performance by eliminating layout sensitivity.

The LT8650S-1 is the H-grade version of the LT8650S. The internal capacitors are X8R type to achieve the 150°C rating. This requires the use of an external boost capacitor between the BST and SW nodes.

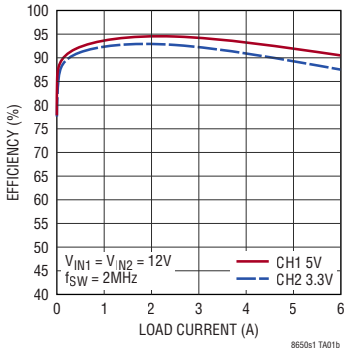
Burst Mode operation features a 6.2µA quiescent current resulting in high efficiency at low output currents, forced continuous mode allows fixed switching frequency operation over the entire output load range, and spread spectrum operation can further reduce EMI emissions. External VC pins allow optimal loop compensation for fast transient response. The VC pins can also be used for current sharing and the CLKOUT pin enables synchronizing two LT8650S-1 chips to generate a 4-phase, 16A supply.

TYPICAL APPLICATION

5V/4A, 3.3V/4A 2MHz Step-Down Converter



Efficiency



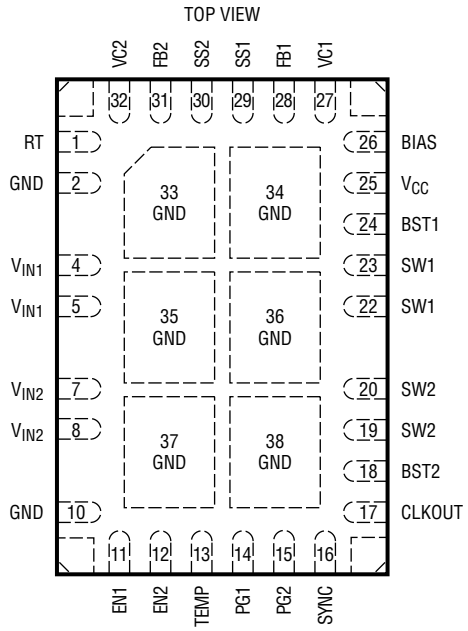
Rev 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2}, EN/UV1, EN/UV2, PG1, PG2.....42V
BIAS.....30V
FB1, FB2, SS1, SS2 .....4V
VC1, VC2.....3.5V
SYNC. 6V
Operating Junction Temperature Range (Note 2)
LT8650SH-1.....–40 to 150°C
Storage Temperature Range .....–65 to 150°C
Maximum Reflow (Package Body)
Temperature.....260°C

PIN CONFIGURATION



LQFN PACKAGE
32-LEAD (6mm × 4mm × 0.94mm

T_{JMAX} = 150°C, θ_{JA} = 23°C/W
EXPOSED PAD (PINS 33, 34, 35, 36, 37, 38) ARE GND, MUST BE SOLDERED TO PCB)

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE** TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LT8650SHV-1#PBF	Au (RoHS)	650SV1	e4	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 150°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Parts ending with PBF are RoHS and WEEE compliant.
- Recommended PCB Assembly and Manufacturing Procedures
- Package and Tray Drawings

**The LT8650S-1 package has the same dimensions as a standard 6mm × 4mm QFN package

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		2.6	3	V
V_{IN1} Quiescent Current in Shutdown	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 0V, V_{SYNC} = 0V	 ●		1.7	4 8	µA µA
V_{IN1} + V_{CC} Quiescent Current in Sleep with Internal Compensation	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 2V, V_{FB1} = V_{FB2} >0.8V, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V	 ●		3.7	8 16	µA µA
V_{IN1} + V_{CC} Quiescent Current in Sleep with External Compensation	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 2V, V_{FB1} = V_{FB2} >0.8V, V_{VC1} = V_{VC2} = Float, V_{SYNC} = 0V	 ●		90	120 140	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1} + V_{CC} Quiescent Current when Active	$V_{EN/UV1}$ = $V_{EN/UV2}$ = 2V, V_{FB1} = V_{FB2} >0.8V, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 3.4V	●		5	7	mA
V_{IN} Current in Regulation	V_{IN} = 12V, V_{OUT} = 3.3V, Output Load = 100µA, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V V_{IN} = 12V, V_{OUT} = 3.3V, Output Load = 1mA, V_{VC1} = V_{VC2} = V_{CC}, V_{SYNC} = 0V			45 350	75 550	µA µA
Feedback Reference Voltage		 ●	0.794 0.790	0.800 0.800	0.806 0.810	V V
Feedback Voltage Line Regulation	V_{IN} = 4.0V to 36V			0.004	0.02	%/V
Feedback Pin Input Current	V_{FB} = 0.8V		–20		20	nA
Minimum On-Time	I_{LOAD} = 3A, SYNC = 3.4V	●		40	60	ns
Oscillator Frequency	R_T = 133k R_T = 35.7k R_T = 15k	● ● ●	270 0.95 1.85	300 1.0 2.00	330 1.05 2.15	kHz MHz MHz
Top Power NMOS Current Limit		●	10	12	14	A
Bottom Power NMOS Current Limit			6.5	8.5	10.5	A
SW Leakage Current	V_{IN} = 42V, V_{SW} = 0V,42V		–2		2	µA
EN/UV Pin Threshold	EN/UV Falling	●	0.7	0.74	0.78	V
EN/UV Pin Hysteresis				30		mV
EN/UV Pin Current	V_{EN}/UV = 2V		–20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Falling	●	5.5	7.5	9	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Rising	●	–9.5	–7.5	–6	%
PG Hysteresis				0.3		%
PG Leakage	V_{PG} = 12V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		600	1200	Ohm
SYNC Threshold	SYNC DC and Clock Low Level Voltage SYNC Clock High Level Voltage SYNC DC High Level Voltage		0.4		 1.5 2.8	V V V
SYNC Pin Current	V_{SYNC} = 6V			120		µA
SS Source Current		●	1.0	2.0	3.0	µA
SS Pull-Down Resistance	Fault Condition, SS = 0.1V			200		Ω
Error Amplifier Transconductance	V_C = 1.25V			0.9		mS
VC Source Current	V_{FB} = 0.6V, V_{VC} = 1.25V			170		µA
VC Sink Current	V_{FB} = 1.0V, V_{VC} = 1.25V			170		µA
VC Pin to Switch Current Gain				9.6		A/V
TEMP Output Voltage	I_{TEMP} = 0µA, Temperature = 25°C I_{TEMP} = 0µA, Temperature = 125°C		190 1100	250 1200	310 1300	mV mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

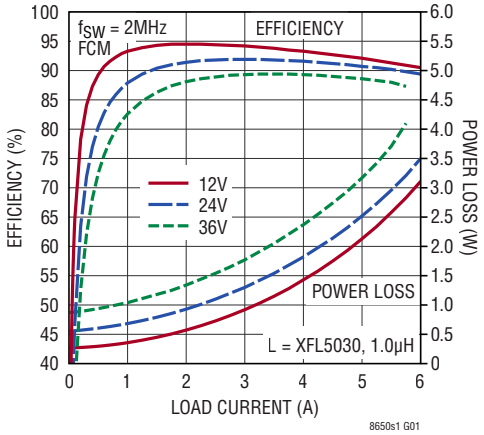
Note 2: The LT8650S-1 is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$ where θ_{JA} (in °C/W) is the package thermal impedance.

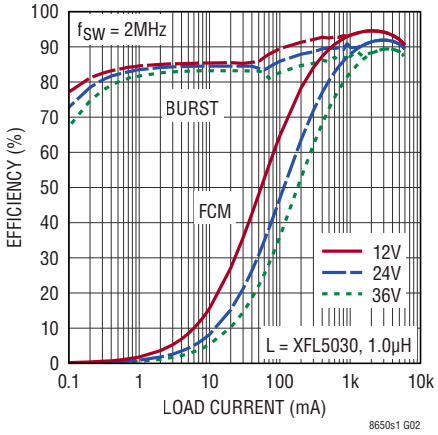
Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

TYPICAL PERFORMANCE CHARACTERISTICS

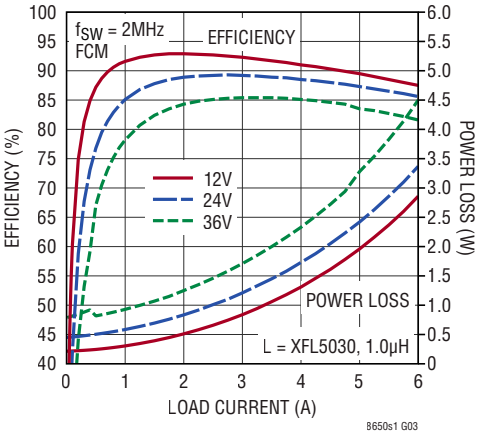
5V_{OUT} Efficiency



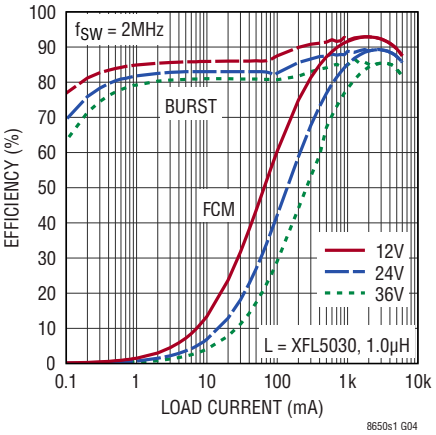
5V_{OUT} Efficiency



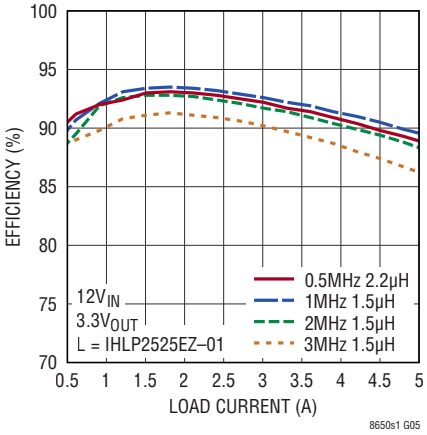
3.3V_{OUT} Efficiency



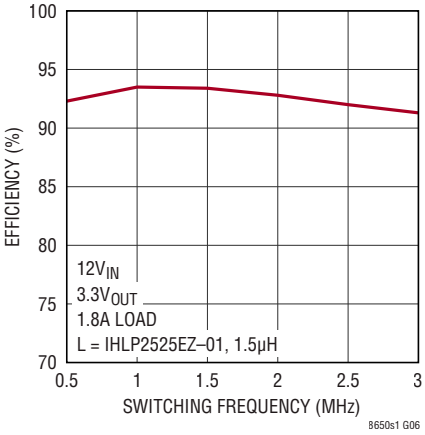
3.3V_{OUT} Efficiency



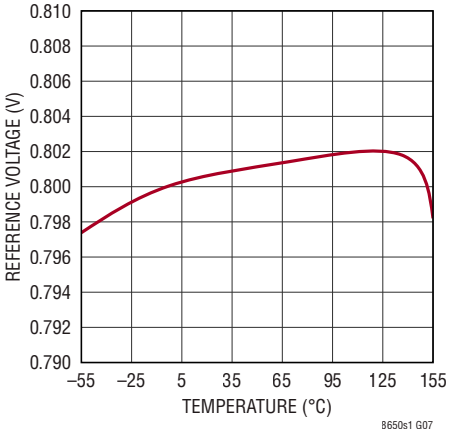
Efficiency at Different f_{SW}



Efficiency vs f_{SW}

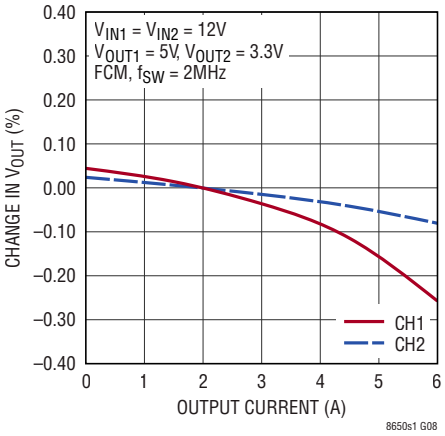


Reference Voltage

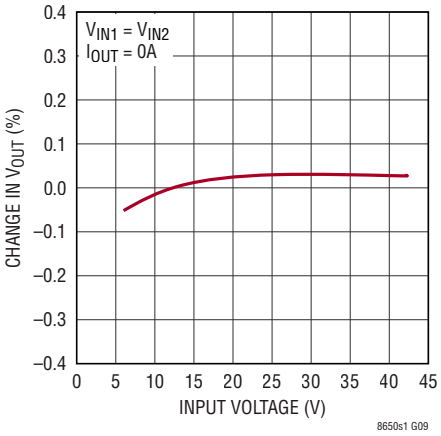


TYPICAL PERFORMANCE CHARACTERISTICS

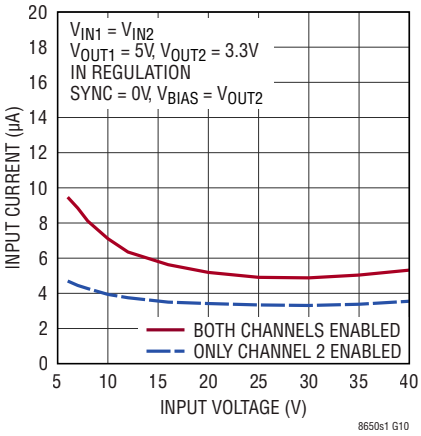
Load Regulation



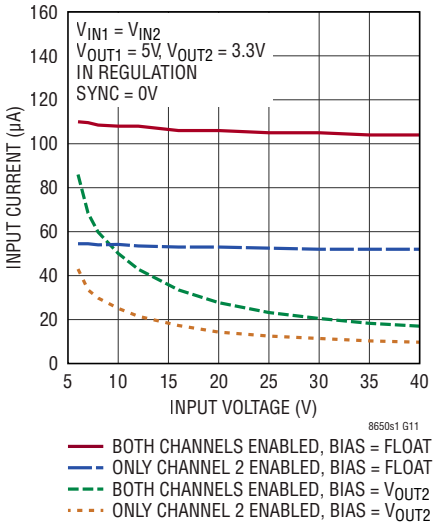
Line Regulation



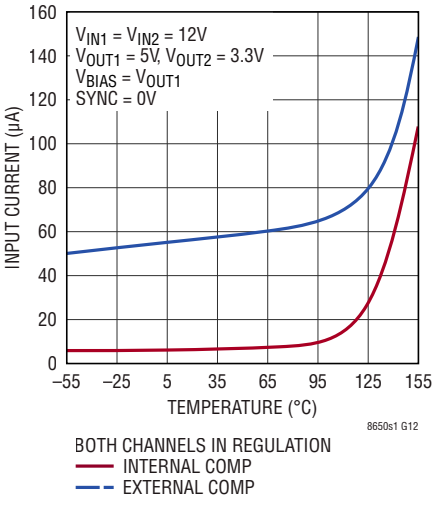
No Load Supply Current with Internal Compensation



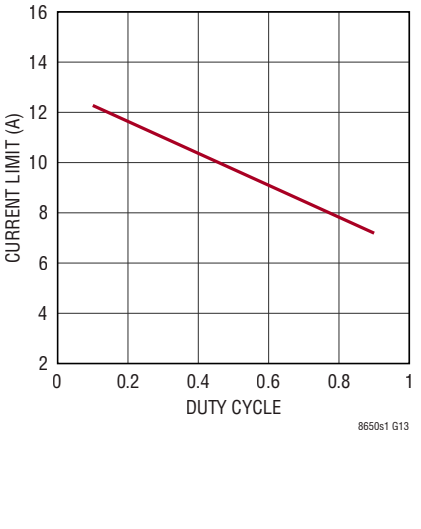
No Load Supply Current with External Compensation



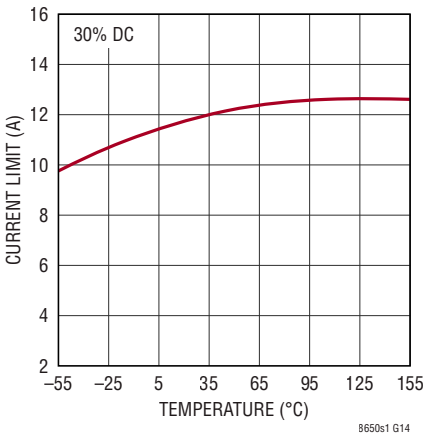
No Load Supply Current



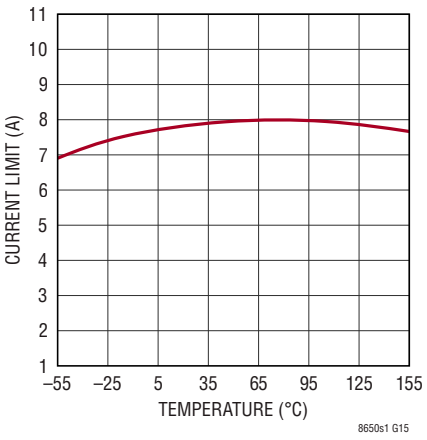
Top FET Current Limit



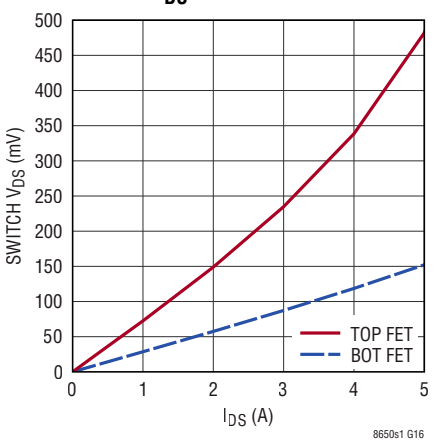
Top FET Current Limit



Bottom FET Current Limit

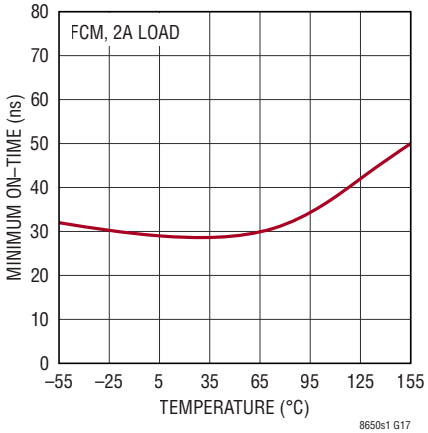


Switch V_{DS}

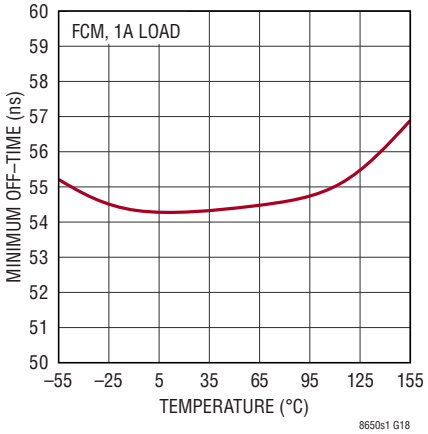


TYPICAL PERFORMANCE CHARACTERISTICS

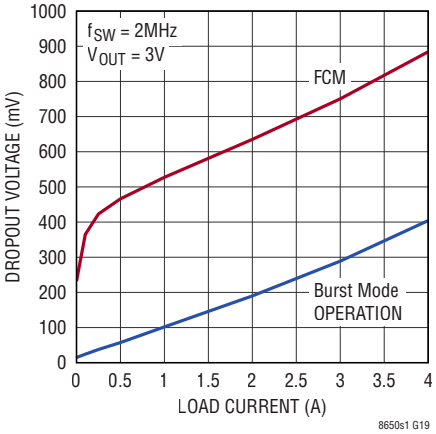
Minimum On-Time



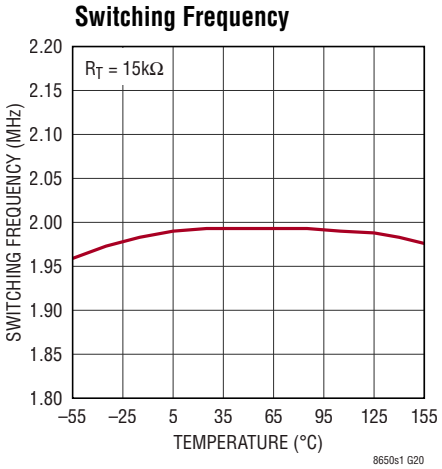
Minimum Off-Time



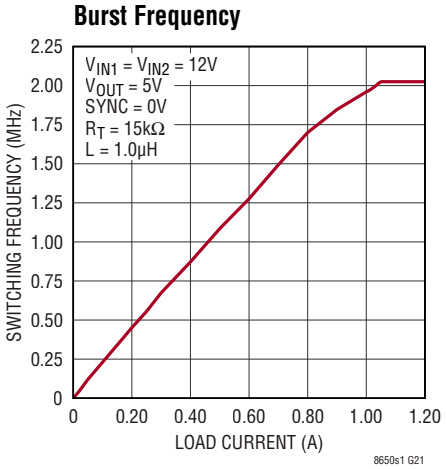
Dropout Voltage



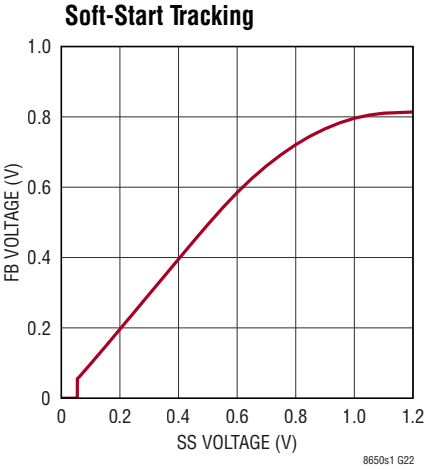
Switching Frequency



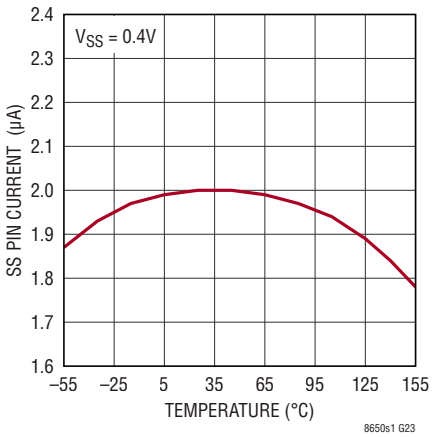
Burst Frequency



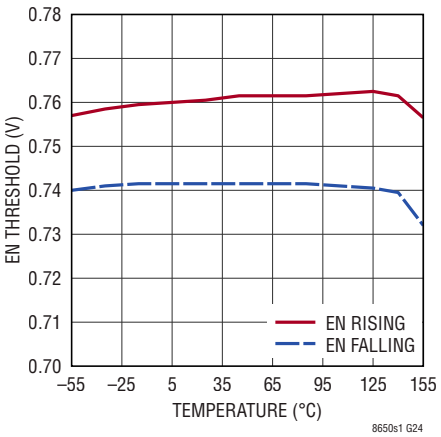
Soft-Start Tracking



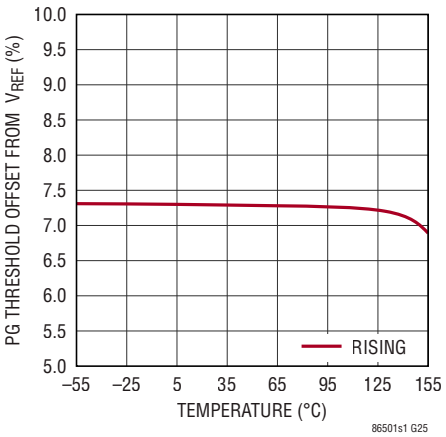
Soft-Start Current



EN Pin Thresholds

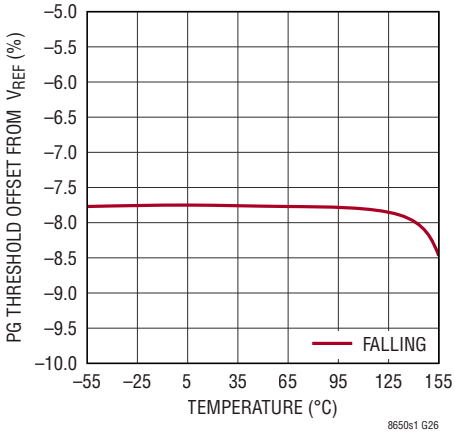


PG High Threshold

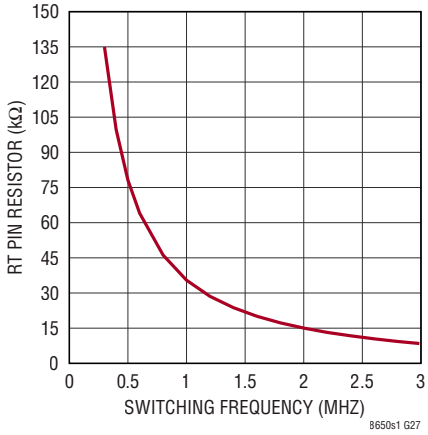


TYPICAL PERFORMANCE CHARACTERISTICS

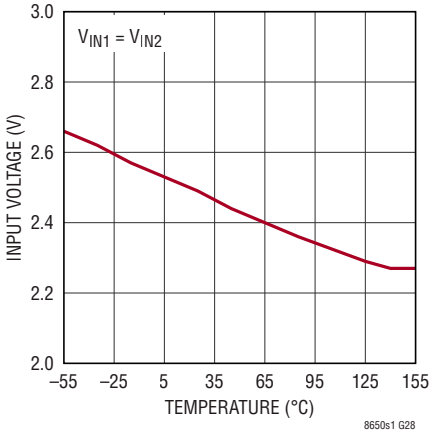
PG Low Threshold



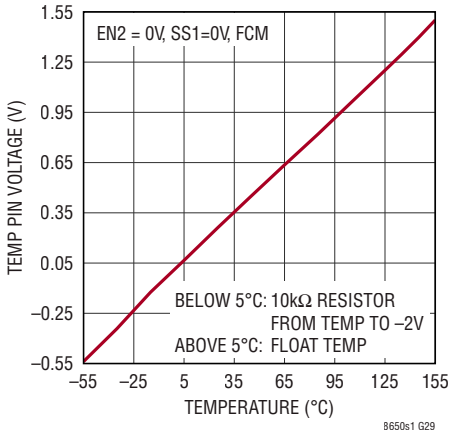
RT Programmed Switching Frequency



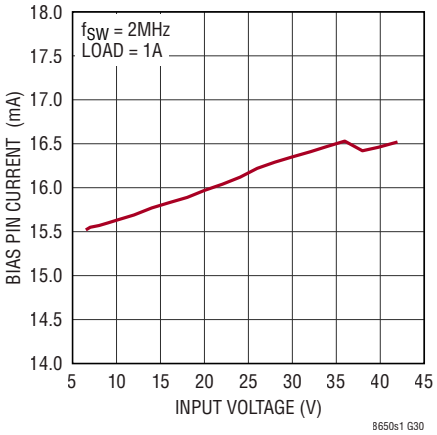
Minimum Input Voltage



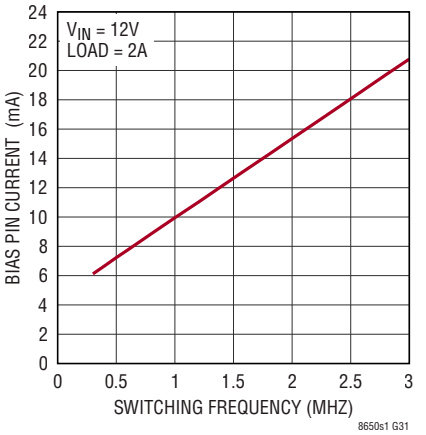
Temperature Monitor Pin



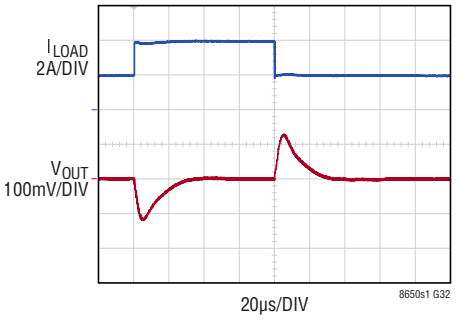
Bias Pin Current per Channel



Bias Pin Current per Channel

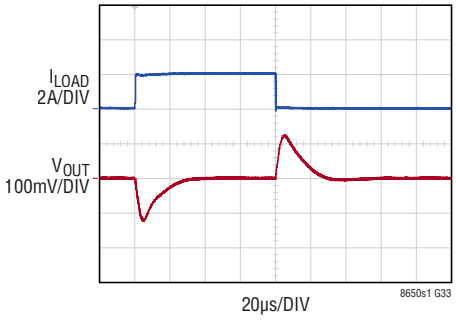


Transient Response Internal Compensation



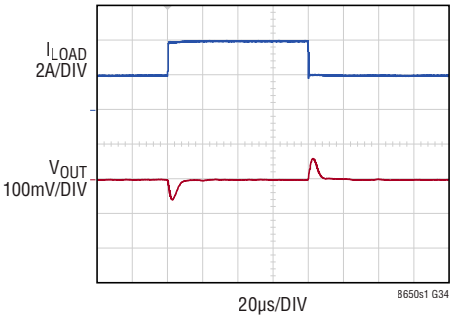
2A TO 4A TRANSIENT
$3.3V_{OUT}$
C_{OUT} = 47µF ×2
FCM, f_{SW} = 2MHz

Transient Response Internal Compensation



40mA TO 2A TRANSIENT
$3.3V_{OUT}$
C_{OUT} = 47µF ×2
FCM, f_{SW} = 2MHz

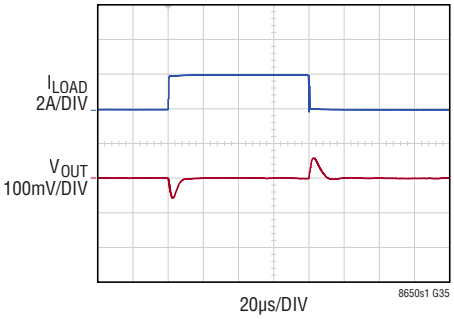
Transient Response External Compensation



2A TO 4A TRANSIENT
$3.3V_{OUT}$
C_{OUT} = 47µF ×2
FCM, f_{SW} = 2MHz
C_C = 220pF, R_C = 14kΩ

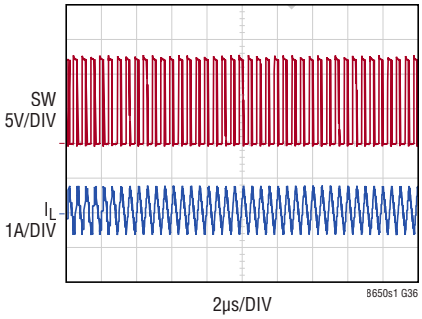
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response External Compensation



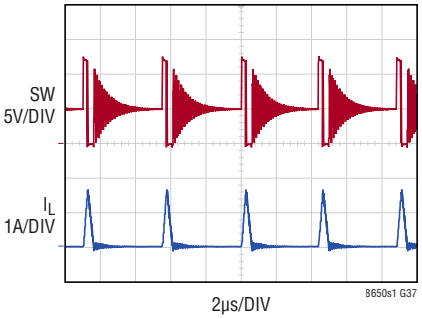
40mA TO 2A TRANSIENT
$3.3V_{OUT}$
C_{OUT} = 47µF ×2
FCM, f_{SW} = 2MHz
C_C = 220pF, R_C = 14kΩ

Forced Continuous Mode (FCM)



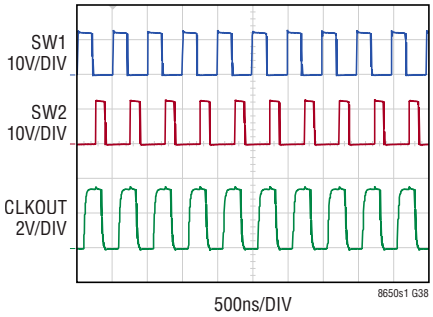
$12V_{IN}$ TO $5V_{OUT}$ AT 100mA
SYNC = FLOAT

Burst Mode Operation



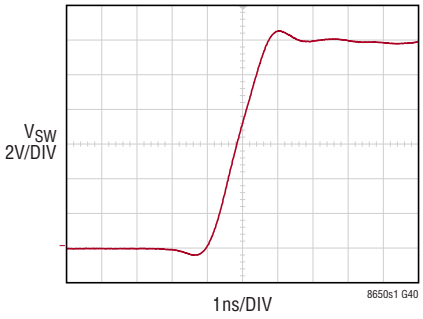
$12V_{IN}$ TO $5V_{OUT}$ AT 100mA
SYNC = 0V

CH1, CH2, and CLKOUT

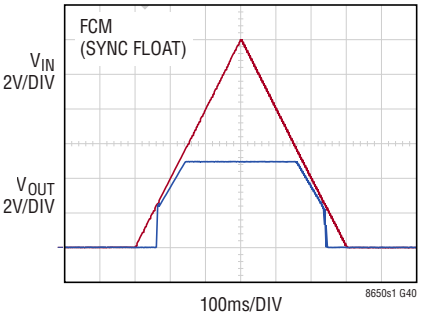


V_{IN} = 12V
CH1 = $5V_{OUT}$
CH2 = $3.3V_{OUT}$
SYNC = FLOAT

Switch Rising Edge

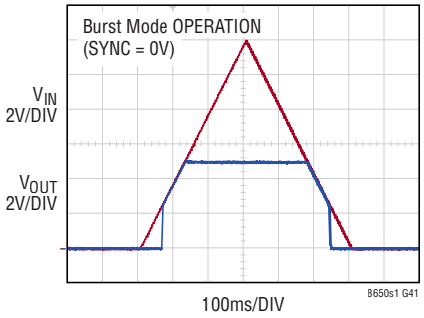


Start-Up Dropout Performance



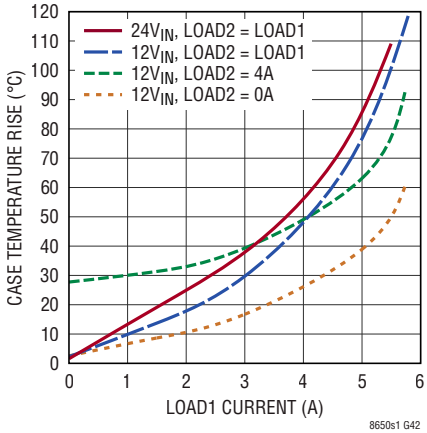
5Ω LOAD
(1A IN REGULATION)

Start-Up Dropout Performance



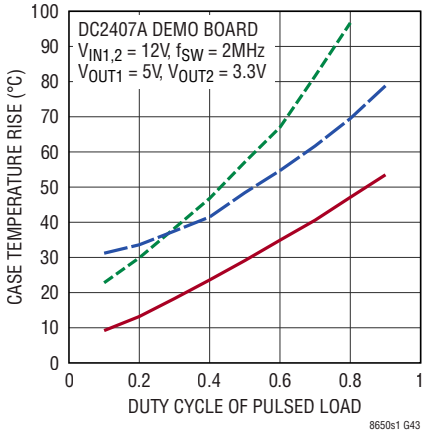
5Ω LOAD
(1A IN REGULATION)

Case Temperature Rise



DC2407A DEMO BOARD
V_{OUT1} = 5V, V_{OUT2} = 3.3V, f_{SW} = 2MHz

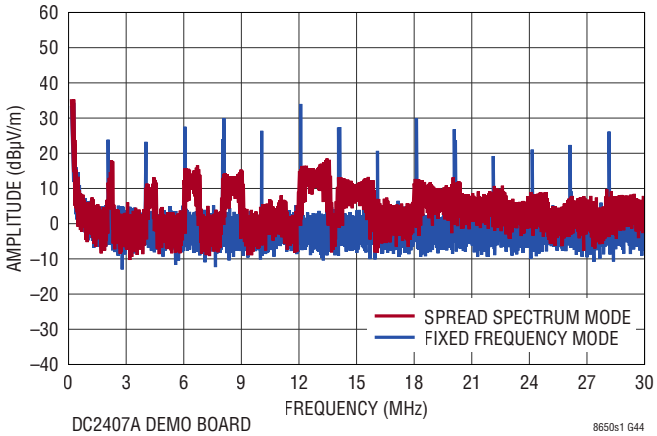
Case Temperature Rise



CH1 = 0.5A STANDBY, 6A PULSED; CH2 = 0A DC
CH1 = 0.5A STANDBY, 6A PULSED; CH2 = 4A DC
CH1 = CH2 = 2A STANDBY, 6A PULSED

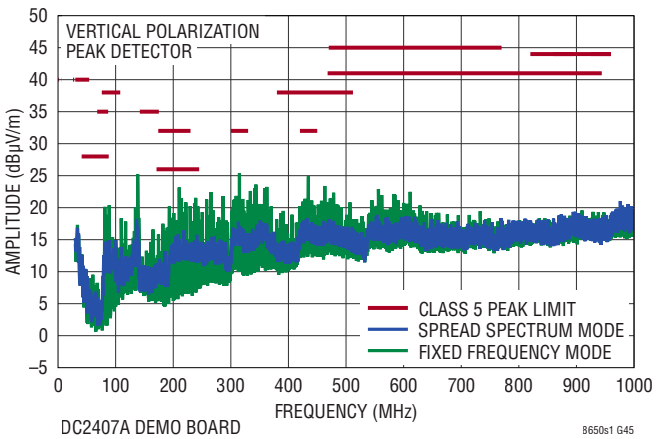
TYPICAL PERFORMANCE CHARACTERISTICS

Conducted EMI Performance



DC2407A DEMO BOARD
(WITH EMI FILTER INSTALLED)
12V INPUT TO 5V OUTPUT1 AT 4A AND 3.3V OUTPUT2 AT 4A, f_{SW} = 2MHz

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



DC2407A DEMO BOARD
(WITH EMI FILTER INSTALLED)
12V INPUT TO 5V OUTPUT1 AT 4A AND 3.3V OUTPUT2 AT 4A, f_{SW} = 2MHz

PIN FUNCTIONS

RT (Pin 1): A resistor is tied between RT and ground to set the switching frequency.

V_{IN1} (Pin 4, 5): The V_{IN1} pin supplies current to the LT8650S-1 internal circuitry and to the internal top side power switch of channel 1. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN1} pin, and the negative capacitor terminal as close as possible to the GND pins.

V_{IN2} (Pin 7, 8): The V_{IN2} pin supplies current to the internal top side power switch of channel 2. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN2} pin, and the negative capacitor terminal as close as possible to the GND pins. This input is capable of operating from a different supply than V_{IN1}. V_{IN1} must be present to run channel 2.

EN/UV1 (Pin 11): Channel 1 of the LT8650S-1 is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 0.77V going up and 0.74V going down. Tie to V_{IN1} if the shutdown feature is not used. An external resistor divider from V_{IN1} can be used to program a V_{IN} threshold below which channel 1 of the LT8650S-1 will shut down. Do not float this pin.

EN/UV2 (Pin 12): Channel 2 of the LT8650S-1 is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 0.77V going up and 0.74V going down. Tie to V_{IN2} if shutdown feature is not used. An external resistor divider from V_{IN2} can be used to program a V_{IN} threshold below which channel 2 of the LT8650S-1 will shut down. Do not float this pin.

TEMP (Pin 13): Temperature Output Pin. This pin outputs a voltage proportional to junction temperature. The pin is 250mV for 25°C and has a slope of 9.5mV/°C. The output of this pin is not valid during light output loads on both channels while in Burst Mode operation. Put the LT8650S-1 in forced continuous mode for the TEMP output to be valid across the entire output load range. See the Applications Information section for more information.

PG1 (Pin 14): The PG1 pin is the open-drain output of an internal comparator. PG1 remains low until the FB1 pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. PG1 is pulled low during V_{IN1} UVLO, V_{CC} UVLO, Thermal Shutdown, or when both EN/UV pins are low.

PG2 (Pin 15): The PG2 pin is the open-drain output of an internal comparator. PG2 remains low until the FB2 pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. PG2 is pulled low during V_{IN1} UVLO, V_{CC} UVLO, Thermal Shutdown, or when both EN/UV pins are low.

SYNC (Pin 16): External Clock Synchronization Input. Ground this pin for low ripple Burst Mode operation at low output loads. Apply a DC voltage of 2.8V to 4V or tie to V_{CC} for forced continuous mode with spread spectrum modulation. Float the SYNC pin for forced continuous mode without spread spectrum modulation. When in forced continuous mode, the I_Q will increase to several hundred µA. Apply a clock source to the SYNC pin for synchronization to an external frequency. The LT8650S-1 will be in forced continuous mode when an external frequency is applied.

CLKOUT (Pin 17): In forced continuous mode, the CLKOUT pin provides a 50% duty cycle square wave 90 degrees out of phase with channel 1. This allows synchronization with other regulators with up to four phases. When an external clock is applied to the SYNC pin, the CLKOUT pin will output a waveform with the same phase, duty cycle, and frequency as the SYNC waveform. In burst mode, the CLKOUT pin will be low. Float this pin if the CLKOUT function is not used.

BST2 (Pin 18): This pin is used to provide a drive voltage, higher than the input voltage, to the top side power switch of channel 2. Place a 0.1µF boost capacitor as close as possible to the IC.

SW2 (Pin 19, 20): The SW2 pin is the output of the channel 2 internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance.

SW1 (Pin 22, 23): The SW1 pin is the output of the channel 1 internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance.

PIN FUNCTIONS

BST1 (Pin 24): This pin is used to provide a drive voltage, higher than the input voltage, to the top side power switch of channel 1. Place a 0.1µF boost capacitor as close as possible to the IC.

V_{CC} (Pin 25): Internal Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. V_{CC} current will be supplied from BIAS if V_{BIAS} > 3.1V, otherwise current will be drawn from V_{IN1}. Voltage on V_{CC} will vary between 2.8V and 3.3V when V_{BIAS} is between 3.0V and 3.5V. Decouple this pin to ground with at least a 1µF low ESR ceramic capacitor. Do not load the V_{CC} pin with external circuitry.

BIAS (Pin 26): The internal regulator will draw current from BIAS instead of V_{IN1} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V and above this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT} use a 1µF local bypass capacitor on this pin.

VC1 (Pin 27): Channel 1 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to V_{CC} to use the default internal compensation. If internal compensation is used, the burst mode quiescent current is only 2.5µA for channel 1. If external compensation is used, the burst mode quiescent current is increased to about 50µA for channel 1.

FB1 (Pin 28): The LT8650S-1 regulates the FB1 pin to 800mV. Connect the feedback resistor divider tap to this pin.

SS1 (Pin 29): Channel 1 Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during startup. A SS1 voltage below 0.8V forces the LT8650S-1 to regulate the FB1 pin to equal the SS1 pin voltage. When SS1 is above 0.8V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from V_{CC} on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the soft-start feature is not being used.

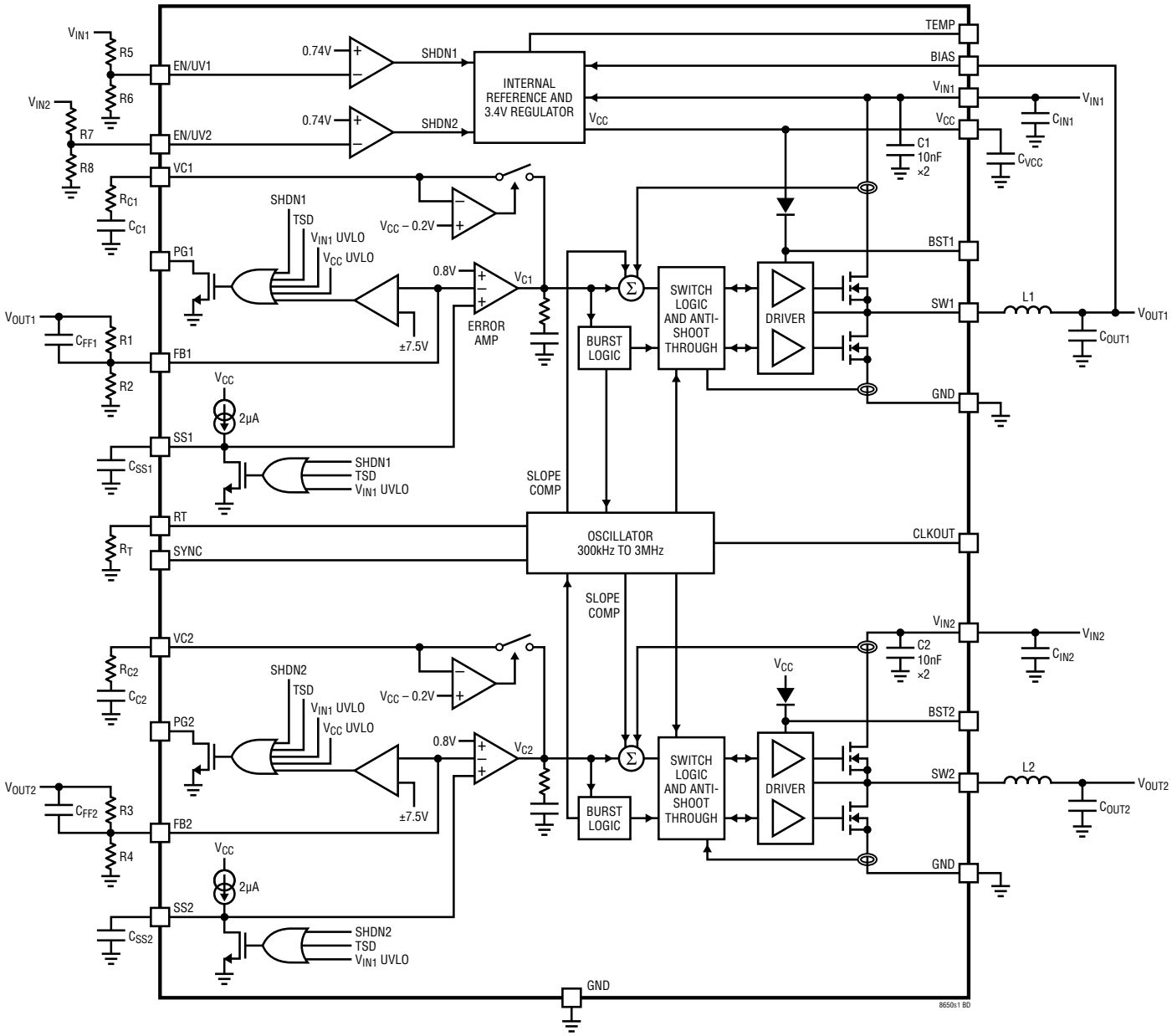
SS2 (Pin 30): Channel 2 Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during startup. A SS2 voltage below 0.8V forces the LT8650S-1 to regulate the FB2 pin to equal the SS2 pin voltage. When SS2 is above 0.8V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from V_{CC} on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the soft-start feature is not being used.

FB2 (Pin 31): The LT8650S-1 regulates the FB2 pin to 800mV. Connect the feedback resistor divider tap to this pin.

VC2 (Pin 32): Channel 2 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to V_{CC} to use the default internal compensation. If internal compensation is used, the burst mode quiescent current is only 2.5µA for channel 2. If external compensation is used, the burst mode quiescent current is increased to about 50µA for channel 2.

GND (Pin 2, 10, Exposed Pad Pins 33–38): LT8650S-1 System Ground. Connect these pins to the system ground and the board ground plane. Place the negative terminal of the input capacitors as close to the GND pins as possible. The exposed pad must be soldered to the PCB in order to lower the thermal resistance.

BLOCK DIAGRAM



OPERATION

Foreword

The LT8650S-1 is a dual monolithic step down regulator. The two channels are the same in terms of current capability and power switch size. The following sections describe the operation of channel 1 and common circuits. They will highlight channel 2 differences and interactions only when relevant. To simplify the application, both V_{IN1} and V_{IN2} are assumed to be connected to the same input supply. However, note that V_{IN1} must be greater than 3V for either channel to operate.

Operation

The LT8650S-1 is a dual monolithic, constant frequency, peak current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the VC node. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 0.8V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero when not in forced continuous mode (FCM). If overload conditions result in more than the bottom NMOS current limit flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The S in LT8650S-1 refers to the second generation Silent Switcher technology. This technology allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI performance. This includes the integration of ceramic capacitors into the package for V_{IN1} and V_{IN2} (C1 to C2 in the Block Diagram). These caps keep all the fast AC current loops small, which improves EMI performance.

If either EN/UV pin is low, the corresponding channel is shut down. If both EN/UV pins are low, the LT8650S-1 is fully shut down and draws 1.7µA from the input supply. When the EN/UV pins are above 0.74V, corresponding switching regulators will become active. 3.7µA is supplied by V_{IN1} to common bias circuits for both channels.

Each channel can independently enter Burst Mode operation to optimize efficiency at light load. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the channel's contribution to input supply current. In a typical application, 6.2µA will be consumed from input supply when regulating both channels with no load. Ground the SYNC pin for Burst Mode operation, float it for forced continuous mode (FCM) or apply a DC voltage from 2.8V to 4V to use FCM with spread spectrum modulation (SSM). If a clock is applied to the SYNC pin both channels will synchronize to the external clock frequency and operate in FCM. While in FCM the oscillator operates continuously and rising SW transitions are aligned to the clock. During light loads, the inductor current is allowed to go negative to maintain the programmed switching frequency. Minimum current limits for both power switches are enforced to prevent large negative inductor current from flowing back to the input. SSM dithers the switching frequency from the programmed value set by the RT pin up to 20% higher than the programmed value to spread out the switching energy in the frequency domain. The CLKOUT pin has no output in Burst Mode, but outputs a square wave 90 degrees phase shifted from channel 1 when in FCM. If a clock is applied to the SYNC pin, the CLKOUT pin has the same phase and duty cycle as the external clock.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.3V or above. Otherwise, the internal circuitry will draw current exclusively from V_{IN1}. The BIAS pin should be connected to the lowest V_{OUT} programmed at 3.3V or above.

The VC pin allows the loop compensation of the switching regulator to be optimized based on the programmed switching frequency. Internal compensation can be se-

OPERATION

lected by connecting the VC pin to V_{CC}, which simplifies the application circuit. External compensation improves the transient response at the expense of about 50µA more quiescent current per channel.

Comparators monitoring the FB pin voltage will pull the corresponding PG pin low if the output voltage varies more than ±7.5% (typical) from the regulation voltage or if a fault condition is present.

The voltage present at the TEMP pin is proportional to the average die temperature of the LT8650S-1. The TEMP pin will be 250mV for a die temperature of 25°C and will have a slope of 9.5mV/°C

Tracking soft-start is implemented by providing constant current via the SS pin to an external soft-start capacitor to generate a voltage ramp. FB voltage is regulated to the voltage at the SS pin until it exceeds 0.8V; FB is then regulated to the reference 0.8V. When the SS pin is below 40mV, the corresponding switching regulator will stop switching. The SS capacitor is reset during shutdown, V_{IN1} undervoltage, or thermal shutdown.

Both channels are designed for output currents up to 6A, but thermal considerations practically limit the output currents to 4A of continuous current from each channel simultaneously. Channel 1 has a minimum V_{IN1} requirement of 3V, channel 2 can operate with no minimum V_{IN2} provided the minimum V_{IN1} has been satisfied.

APPLICATIONS INFORMATION

Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8650S-1 operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. 3.7µA is supplied by V_{IN1} to common bias circuits. In Burst Mode operation the LT8650S-1 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode both channels consume a combined 6.2µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8650S-1 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 6.2µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

While in Burst Mode operation the current limit of the top switch is approximately 1.2A resulting in output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 1. The output load at which the LT8650S-1 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

For some applications it is desirable to select forced continuous mode (FCM) to maintain full switching frequency down to zero output load. See Forced Continuous Mode section.

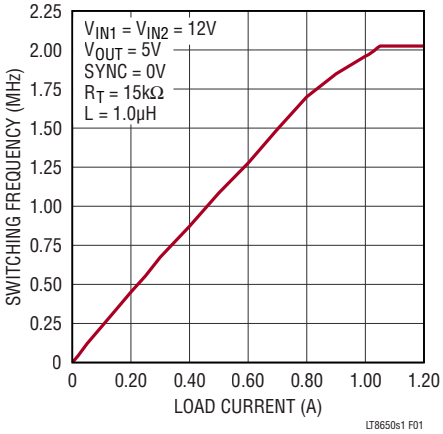


Figure 1. Burst Frequency

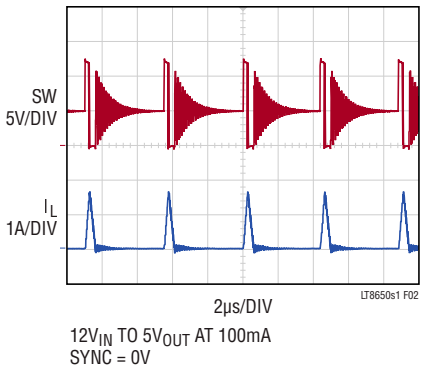


Figure 2. Burst Mode Operation

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin (R1-2 for channel 1, R3-4 for channel 2). Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT1}}{0.8V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

APPLICATIONS INFORMATION

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter, which is approximately:

$$I_Q = 3.7\mu A + \left(\frac{V_{OUT1}}{R1+R2}\right)\left(\frac{V_{OUT1}}{V_{IN1}}\right)\left(\frac{1}{n}\right)$$

where 3.7µA is the quiescent current of channel 1 and common circuitries, the second term is the current in the feedback divider reflected to the input of channel 1 operating at its light load efficiency n. For a 3.3V application with R1 = 1M and R2 = 316k, the feedback divider draws 2.5µA. With V_{IN} = 12V and n = 80%, this adds 0.9µA to the 3.7µA quiescent current resulting in 4.6µA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN}; this is plotted in the Typical Performance Characteristics section.

A similar calculation can be done to determine the input current contribution from the channel 2 feedback resistors. For a 5V application with R3 = 1M, R4 = 191k, V_{IN} = 12V, and h = 80%, this adds 2.2µA to the input current resulting in a total of 6.8µA with both channels on.

For a typical FB resistor of 1M, a 4.7pF to 10pF phase-lead capacitor should be connected from V_{OUT} to FB.

Setting the Switching Frequency

The LT8650S-1 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 3MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T value for a desired switching frequency.

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{41.7}{f_{SW}} - 5.8$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

The two channels of the LT8650S-1 operate 180° out of phase to avoid aligned switching edge noise and reduce input current ripple.

Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	137
0.4	100
0.5	78.7
0.6	63.4
0.8	46.4
1.0	35.7
1.2	28.7
1.4	23.7
1.6	20
1.8	17.4
2.0	15
2.2	13
2.5	11
3.0	8.06

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.12V, respectively at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time of 60ns (see the Electrical Characteristics). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio. Choose the switching frequency based on which channel has the lower frequency constraint.

APPLICATIONS INFORMATION

For transient operation, V_{IN} may go as high as the absolute maximum rating of 42V regardless of the R_T value, however the LT8650S-1 will reduce switching frequency on each channel independently as necessary to maintain control of inductor current to assure safe operation.

In Burst Mode, the LT8650S-1 is capable of a maximum duty cycle of greater than 99%, and the V_{IN} to V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the channel that enters dropout skips switch cycles, resulting in a lower switching frequency. In forced continuous mode, the LT8650S-1 will not skip cycles to achieve a higher duty cycle. The part will maintain the programmed switching frequency and the dropout voltage will be larger due to the smaller maximum duty cycle.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)}$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.12V, respectively at maximum load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Note there is no minimum V_{IN2} voltage requirement as it does not supply the internal common bias circuits, making the channel 2 uniquely capable of operating from very low input voltages as long as V_{IN1} has a supply of 3V or greater.

Inductor Selection and Maximum Output Current

The LT8650S-1 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8650S-1 safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L1,2 = \frac{V_{OUT1,2} + V_{SW(BOT)}}{2f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.12V) and L is the inductor value in µH. To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L$$

where ΔI_L is the inductor ripple current as calculated in Equation 1 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 1A output should use an inductor with an RMS rating of greater than 1A and an I_{SAT} of greater than 1.3A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement must be greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.04Ω, and the core material should be intended for high frequency applications.

The LT8650S-1 limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is at least 10A at low duty cycles and decreases linearly to 7A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (1)$$

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where f_{SW} is the switching frequency of the LT8650S-1, and L is the value of the inductor. Therefore, the maximum output current that the LT8650S-1 will deliver depends on the switch current limit, the inductor value, and the input and output voltages.

Each channel has a secondary bottom switch current limit. After the top switch has turned off, the bottom switch carries the inductor current. If for any reason the inductor current is too high, the bottom switch will remain on, delaying the top switch turning on until the inductor current returns to a safe level. This level is specified as the Bottom NMOS Current Limit, and is independent of duty cycle. Maximum output current in the application circuit is limited to this valley current plus one half of the inductor ripple current.

In most cases current limit is enforced by the top switch. The bottom switch limit controls the inductor current when the minimum on-time condition is violated (high input voltage, high frequency or saturated inductor).

The bottom switch current limit is designed to be equal to the peak current limit to avoid any contribution to maximum rated current of the LT8650S-1.

For more information about maximum output current and discontinuous operation, see the Analog Devices Application Note 44.

Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. See Application Note 19.

Table 2. Inductor Manufacturers

VENDOR	URL
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Toko	www.toko.com
Würth Elektronik	www.we-online.com
Vishay	www.vishay.com

Input Capacitor

Bypass the input of the LT8650S-1 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8650S-1 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8650S-1 and to force this very high frequency switching current into a tight local loop, minimizing EMI. Typically a 0.1µF capacitor in a small 0402 case size is placed as close as possible to the LT8650S-1 and a larger bulk ceramic is added for more capacitance (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8650S-1. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8650S-1 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8650S-1's voltage rating. This situation is easily avoided (see the Analog Devices Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8650S-1 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8650S-1's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feed forward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient

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performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8650S-1 due to their piezoelectric nature. When in Burst Mode operation, the LT8650S-1's switching frequency depends on the load current, and at very light loads the LT8650S-1 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8650S-1 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 3. Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
Taiyo Yuden	www.t-yuden.com
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com

Enable Pin

The LT8650S-1 is in shutdown when both EN/UV pins are low and active when either pin is high. The rising threshold of the EN/UV comparator is 0.74V, with 30mV of hysteresis. The EN/UV pins can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8650S-1 to operate only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R5 and R6 (R7 and R8 for channel 2) such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R5}{R6} + 1\right) \bullet 0.74V$$

where the corresponding channel will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8650S-1. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

V_{CC} Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN1} that powers the drivers and the internal bias circuitry. For this reason, V_{IN1} must be present and valid to use either channel. The V_{CC} can supply enough current for the LT8650S-1's circuitry and must be bypassed to ground with a 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically the BIAS pin can be tied to the lowest output or external supply above 3.1V. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3V, the internal LDO will consume current from V_{IN1}.

Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN1} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the V_{CC} pin.

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Frequency Compensation

The LT8650S-1 has VC pins which can be used to optimize the loop compensation of each channel. If the VC pins are shorted to V_{CC}, then internal compensation is used. This simplifies the circuit design and minimizes the quiescent current, but since the internal compensation has to be stable across the 300kHz to 3MHz range of switching frequencies, the internal compensation will not be optimal, especially at high switching frequencies. If the best transient response is desired, an external compensation network can be connected to the VC pin, which usually consists of a series resistor and capacitor (see R_C and C_C in the Block Diagram).

Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in the data sheet that is similar to your application and tune the compensation network to optimize the performance. LTspice® simulations can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature.

Figure 3 shows an equivalent circuit for the LT8650S-1 control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switches, and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the VC pin.

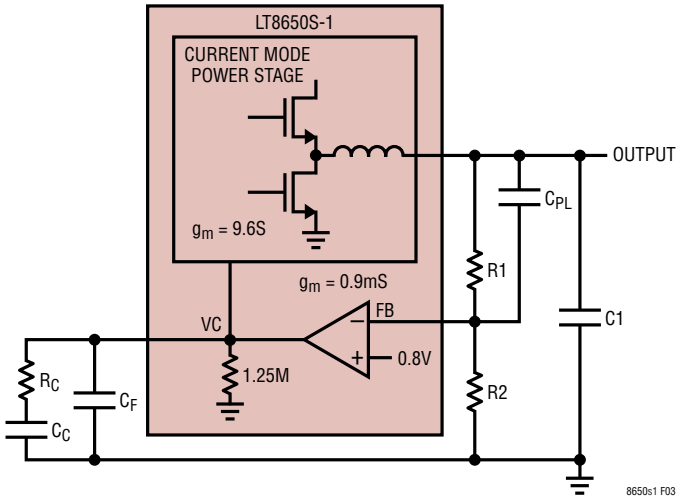
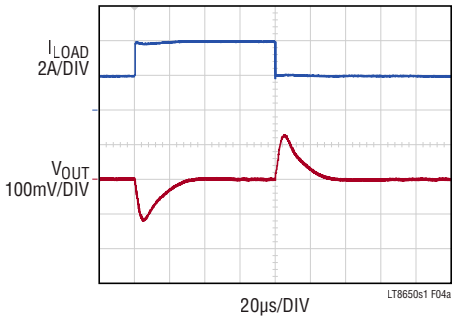


Figure 3. Model for Loop Response

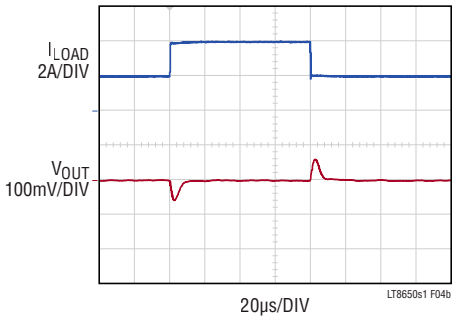
Note that the output capacitor integrates this current and that the capacitor on the VC pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. A zero is required and comes from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider can be used to improve the transient response and is required to cancel the parasitic pole caused by the feedback node to ground capacitance.

Figure 4a shows the transient response for the front page application which uses internal compensation. Figure 4b shows the improved transient response of the same application when a 14kΩ R_C and 220pF C_C compensation network is used. Use of an external compensation network increases the quiescent current by about 50µA per channel.



2A TO 4A TRANSIENT
$3.3V_{OUT}$
C_{OUT} = 47µF ×2
FCM, f_{SW} = 2MHz

a)



2A TO 4A TRANSIENT
$3.3V_{OUT}$
C_{OUT} = 47µF ×2
FCM, f_{SW} = 2MHz
C_C = 220pF, R_C = 14kΩ

b)

Figure 4 Transient Response

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Output Voltage Tracking and Soft-Start

The LT8650S-1 allows the user to program its output voltage ramp rate with the SS pin. An internal 2µA current pulls up the SS pin to V_{CC}. Putting an external capacitor on SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the SS pin voltage. For output tracking applications, SS can be externally driven by another voltage source. From 0V to 0.04V, the SS pin will stop the corresponding channel from switching, thus allowing the SS pin to be used as a shutdown pin. From 0.04V to 0.8V, the SS voltage will override the internal 0.8V reference input to the error amplifier, thus regulating the FB pin voltage to that of SS pin (Figure 5). When SS is above 0.8V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The SS pin may be left floating if the function is not needed. Note that in both Burst Mode and forced continuous mode (FCM) the LT8650S-1 will not discharge the output to regulate to a lower SS voltage. This is achieved by disabling FCM when the SS voltage is below 2V.

In Burst Mode operation (SYNC low), an active pull-down circuit is connected to the SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the corresponding EN/UV pin below 0.74V, V_{IN1} voltage falling too low, or thermal shutdown.

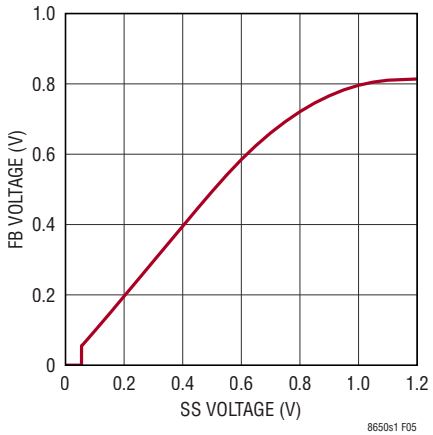

Figure 5. SS Pin Tracking

Output Power Good

When the LT8650S-1's output voltage is within the ±7.5% window of the regulation point, which is a FB voltage in the range of 0.74V to 0.86V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 0.3% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: corresponding EN/UV pin below 0.74V, V_{CC} voltage falling too low, V_{IN1} under voltage, or thermal shutdown.

Sequencing

Startup sequencing and tracking can be configured in several ways with the LT8650S-1. One channel can be required to be valid before enabling the other channel to sequence their startup order. This can be done by connecting the PG pin of the first channel to either the EN/UV pin or SS pin of the second channel. The SS pin of the first channel can also be connected to the EN/UV pin of the second channel (see Figure 6).

The channels can also be started at the same time where the output voltages can track in a ratiometric fashion (see Figure 6).

Paralleling

To increase the possible output current the two channels can be connected in parallel to the same output. To do this the VC, SS, and FB pins of each channel are connected together, while each channel's SW node is connected to the common output through its own inductor. External compensation network must be used when paralleling outputs. Figure 7 shows an application where the two channels of one LT8650S-1 regulator are combined to get one output capable of 8A DC with 12A peak transients.

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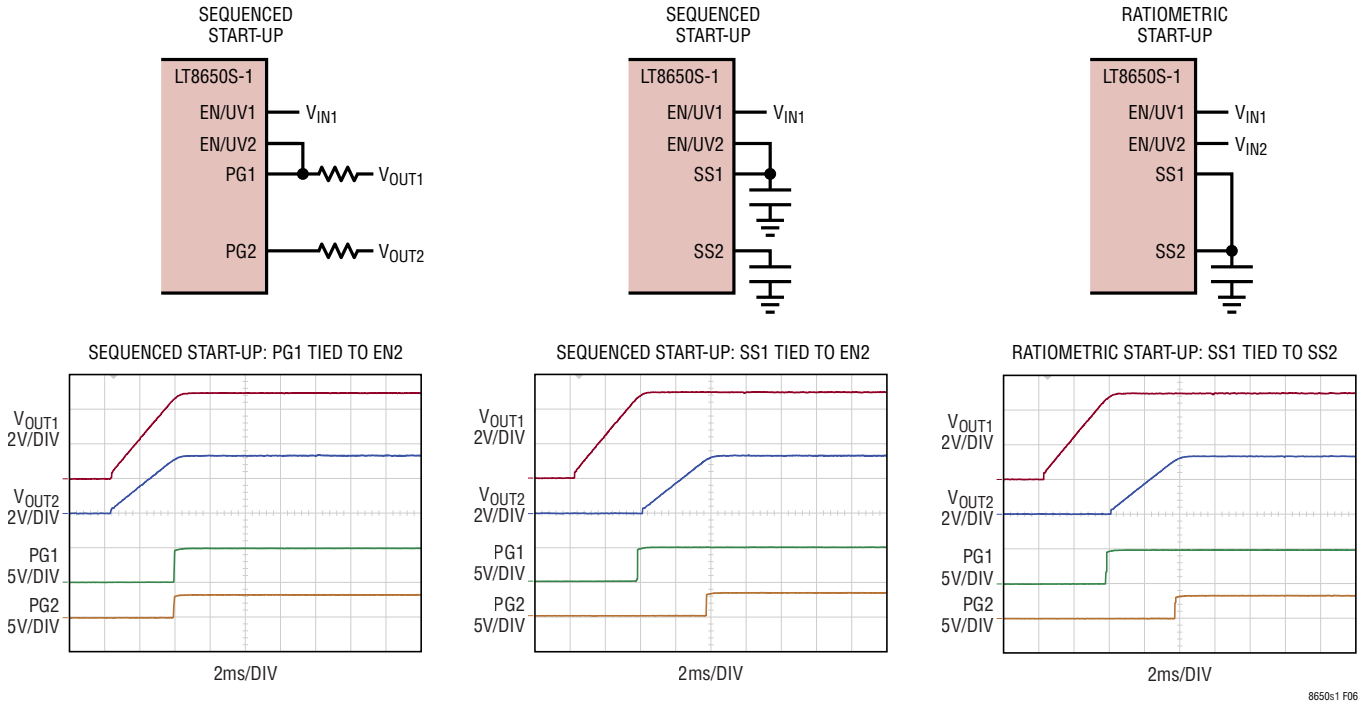

Figure 6. Sequencing and Start-Up Configurations

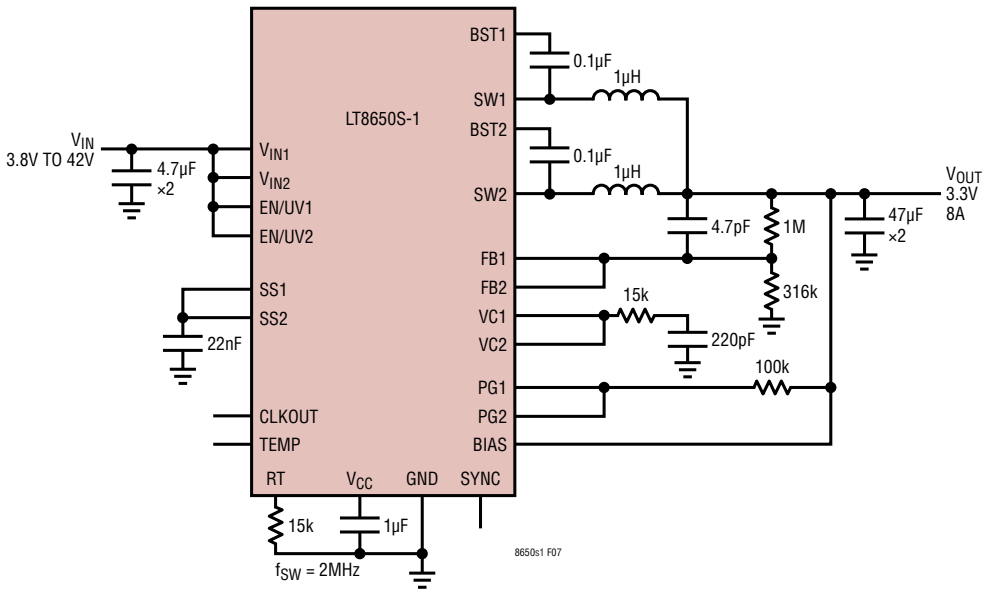

Figure 7 Two-Phase Application

APPLICATIONS INFORMATION

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic low output). To select forced continuous mode (FCM), float the SYNC pin. To select FCM with spread spectrum modulation (SSM), tie the SYNC pin above 2.8V (SYNC can be tied to V_{CC}). To synchronize the LT8650S-1 oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V). When synchronized to an external clock the LT8650S-1 will use FCM.

Channel 1 will synchronize its positive switch edge transitions to the positive edge of the SYNC signal, and channel 2 will synchronize to the negative edge of the SYNC signal.

The LT8650S-1 may be synchronized over a 300kHz to 3MHz range. The R_T resistor should be chosen to set the LT8650S-1 switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for nominal 500kHz.

The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by R_T, then the slope compensation will be sufficient for all synchronization frequencies.

A synchronizing signal that incorporates spread spectrum may reduce EMI. The duty cycle of the SYNC signal can be used to set the relative phasing of the two channels for minimizing input ripple.

Forced Continuous Mode

Forced continuous mode (FCM) is activated by either floating the SYNC pin, tying the SYNC pin to V_{CC}, applying a DC voltage above 2.8V to the SYNC pin, or applying an external clock to the SYNC pin.

While in FCM discontinuous mode operation is disabled and the inductor current is allowed to go negative so that the regulator can switch at the programmed frequency all the way down to zero output current. This has the advantage of maintaining the programmed switching frequency across the entire load range so that the switch harmonics and EMI are consistent and predictable. The disadvantage of FCM is that the light load efficiency will be low compared to Burst Mode operation.

At low input voltages when the part enters dropout, the programmed switching frequency will be maintained and off time skipping will not be allowed. This keeps the switching frequency controlled, but the dropout voltage will be higher than in burst mode, due to maximum duty cycle constraints.

The negative inductor current is limited to a maximum of about –2.5A, so the LT8650S-1 can only sink a maximum of about –1.3A. This prevents boosting an excessive amount of current back from the output to the input. FCM is disabled if the input voltage is greater than 37V to prevent overvoltaging the LT8650S-1 if the input capacitor is charged when sinking current from the output. Additional safety features include disabling FCM when the SS pin voltage is below 1.8V to prevent discharging the output when starting up into a pre-biased output, and a bottom FET current limit to prevent over charging the output if the minimum on time is violated.

Spread Spectrum Modulation

Spread spectrum modulation (SSM) is activated by tying the SYNC pin to V_{CC} or applying a DC voltage from 2.8V to 4V to the SYNC pin. SSM reduces the EMI emissions by modulating the switching frequency between the value programmed by RT to approximately 20% higher than that value. The switching frequency is modulated linearly up and then linearly down at a 5kHz rate. This is an analog function, so each switching period will be different than the previous one. For example, when the LT8650S-1 is programmed to 2MHz and the SSM feature is enabled, the switching frequency will vary from 2MHz to 2.4MHz at a 5kHz rate. When in SSM, the part will also operate in forced continuous mode.

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Clock Output

The CLKOUT pin outputs a clock which can be used to synchronous other regulators to the LT8650S-1. In Burst Mode (SYNC pin low), the CLKOUT pin is grounded. In forced continuous mode (SYNC pin float or DC high), the CLKOUT pin outputs a 50% duty cycle clock where the CLKOUT rising edge is approximately 90 degrees phase shifted relative to channel 1. If this CLKOUT waveform is applied to the SYNC pin of another LT8650S-1 regulator, then four-phase operation can be achieved. If an external clock is applied to the SYNC pin of the LT8650S-1, then the CLKOUT pin will output a waveform with the same phasing and duty cycle as the SYNC pin clock. The low and high levels of the CLKOUT pin are ground and V_{CC}, respectively. The drive strength of the CLKOUT pin is several hundred ohms, so the CLKOUT waveform has rise and fall times of several tens of ns. The edge rates will be slower if the CLKOUT trace has extra capacitance.

Temperature Monitor Function

The TEMP pin will output a voltage proportional to die temperature. The TEMP pin typically outputs 250mV for 25°C and has a slope of 9.5mV/°C. Without the aid of an external circuitry, the TEMP pin output is valid from 20°C to 150°C (200mV to 1.5V). Do not load the TEMP pin with more than 100µA. To extend the TEMP pin output below 20°C, connect a resistor from the TEMP pin to a negative voltage.

As a safeguard, the LT8650S-1 has an additional thermal shutdown set at a typical value of 165°C. If the thermal shutdown is exceeded, both channels of the LT8650S-1 will be shutdown until the thermal overload event expires.

It should be noted that the TEMP pin voltage represents the steady-state, average die temperature and should not be used to guarantee that maximum junction temperatures are not exceeded. Instantaneous power along with thermal gradients and time constants may cause portions of the die to exceed maximum ratings. Be sure to calculate die temperature rise for steady state (>1 Min) as well as impulse conditions.

Shorted and Reversed Input Protection

The LT8650S-1 will tolerate a shorted output. The bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels. Fault condition of one channel will not affect the operation of the other channel, unless the part goes into thermal shutdown.

There is another situation to consider in systems where the output will be held high when the input to the LT8650S-1 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is ORed with channel 1's output. If the V_{IN1} pin is allowed to float and either EN/UV pin is held high (either by a logic signal or because it is tied to V_{IN1}), then the LT8650S-1's internal circuitry will pull its quiescent current through its SW1 pin. This is acceptable if the system can tolerate current draw in this state. If both EN/UV pins are grounded the SW1 pin current will drop to near 1.7µA. However, if the V_{IN1} pin is grounded while channel 1 output is held high, regardless of EN/UV1, parasitic body diodes inside the LT8650S-1 can pull current from the output through the SW1 pin and the V_{IN1} pin, damaging the IC.

V_{IN2} is not connected to the shared internal supply and will not draw any current if left floating. If both V_{IN1} and V_{IN2} are floating, regardless of EN/UV pins states, no load will be present at the output of channel 2. However, if the V_{IN2} pin is grounded while channel 2 output is held high, parasitic body diodes inside the LT8650S-1 can pull current from the output through the SW2 pin and the V_{IN2} pin, damaging the IC.

Figure 8 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8650S-1 to run only when the input voltage is present and that protects against a shorted or reversed input.

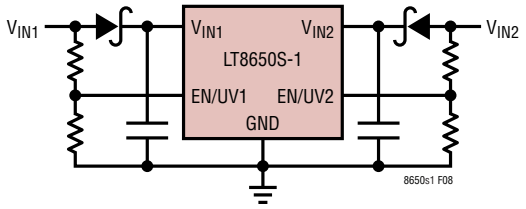


Figure 8. Reverse V_{IN} Protection for Two Independent Input Voltages

APPLICATIONS INFORMATION

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 9 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8650S-1's V_{IN} pins, GND pins, and the input capacitors. The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} and GND pins. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad acts as a heat sink and is connected electrically to ground. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8650S-1 to additional ground planes within the circuit board and on the bottom side. See Figure 9 for example PCB layout.

High Temperature Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8650S-1. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8650S-1. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8650S-1 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8650S-1 power dissipation by the thermal resistance from junction to ambient.

The internal thermal shutdown protection of LT8650S-1 will stop switching and indicate a fault condition if junction temperature exceeds 165°C. The fault condition will clear and switching resume when the temperature drops back below 160°C.

Temperature rise of the LT8650S-1 is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. Figure 10 shows examples case temperature vs V_{IN}, switching frequency, and load.

The LT8650S-1's internal power switches are capable of safely delivering up to 6A of peak output current. However, due to thermal limits, the package can only handle 6A loads for short periods of time. Figure 11 shows an example of how case temperature rise changes with the duty cycle of a 1kHz pulsed 6A load.

APPLICATIONS INFORMATION

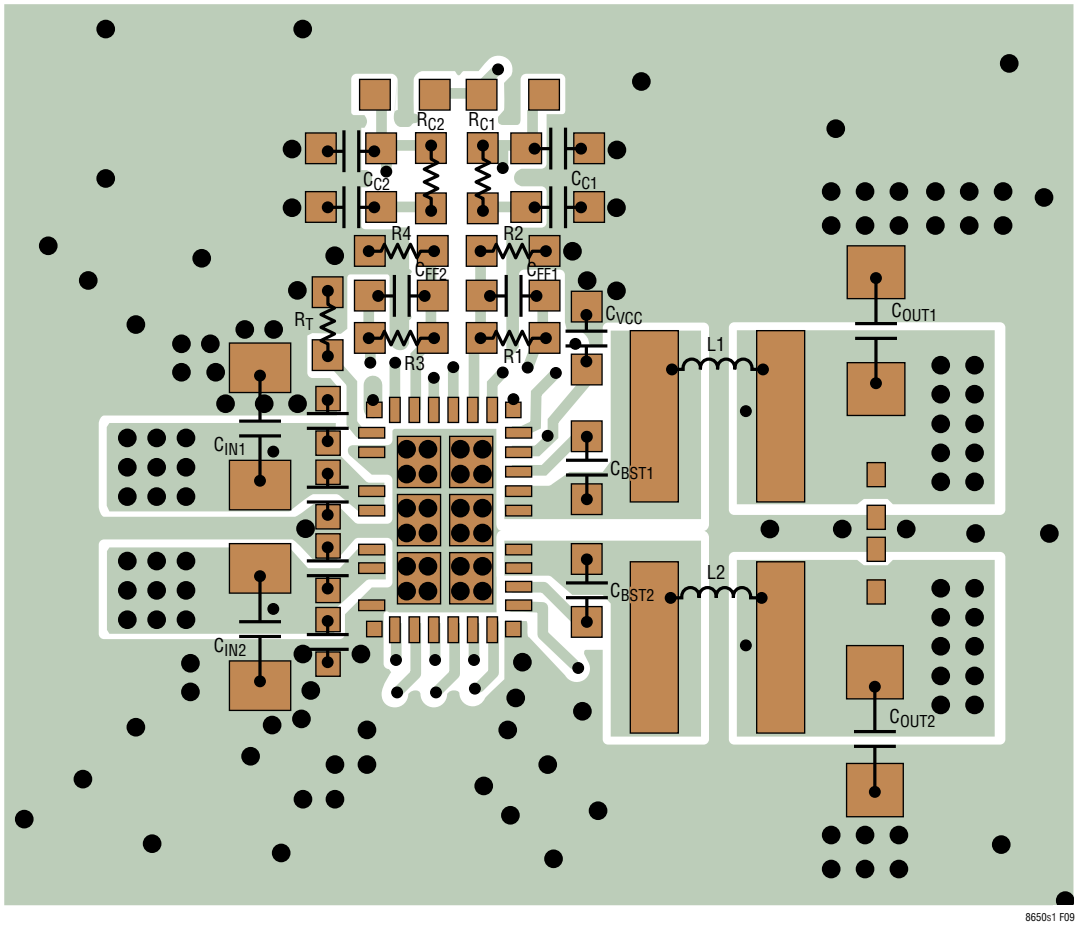


Figure 9. Recommended Layout

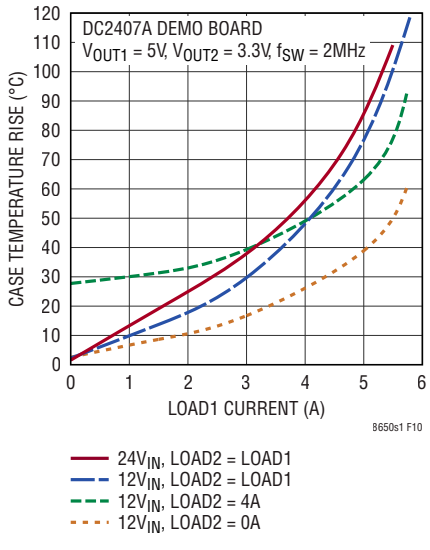


Figure 10. Case Temperature Rise

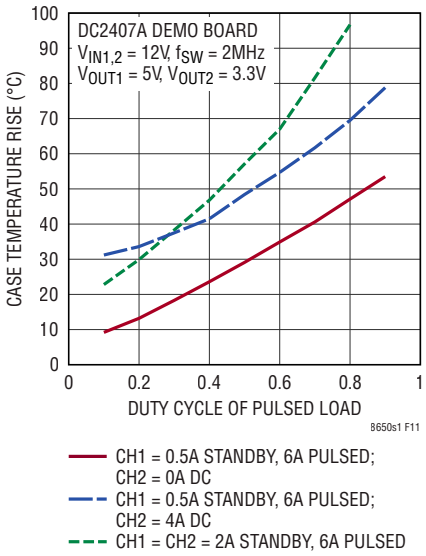
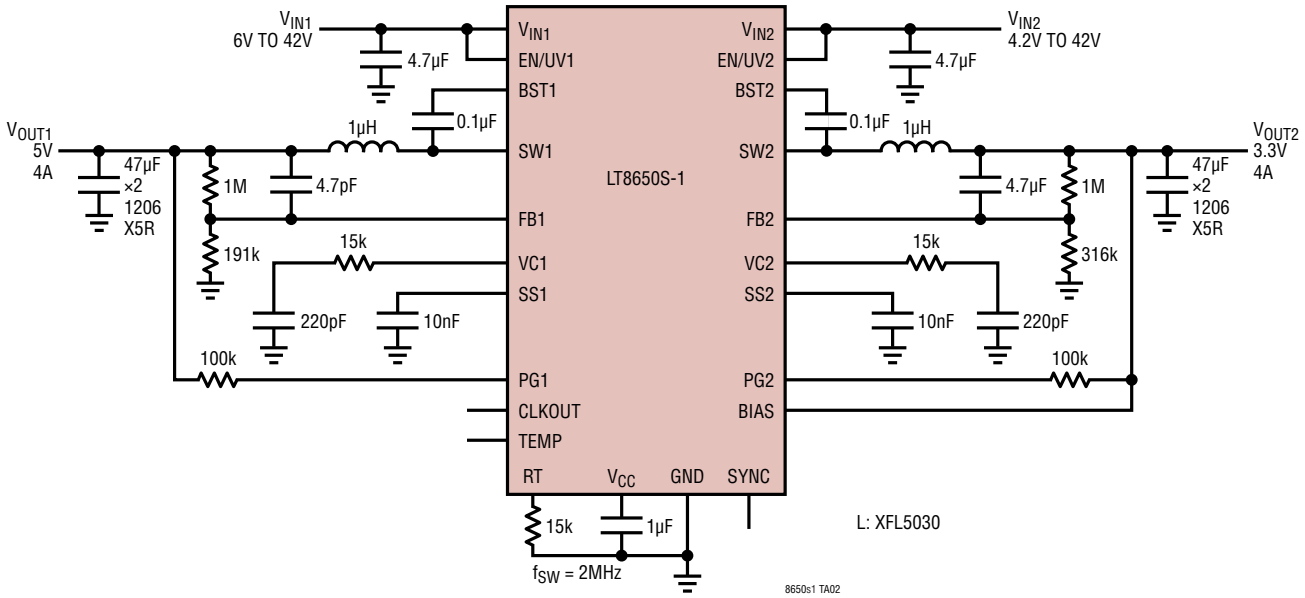


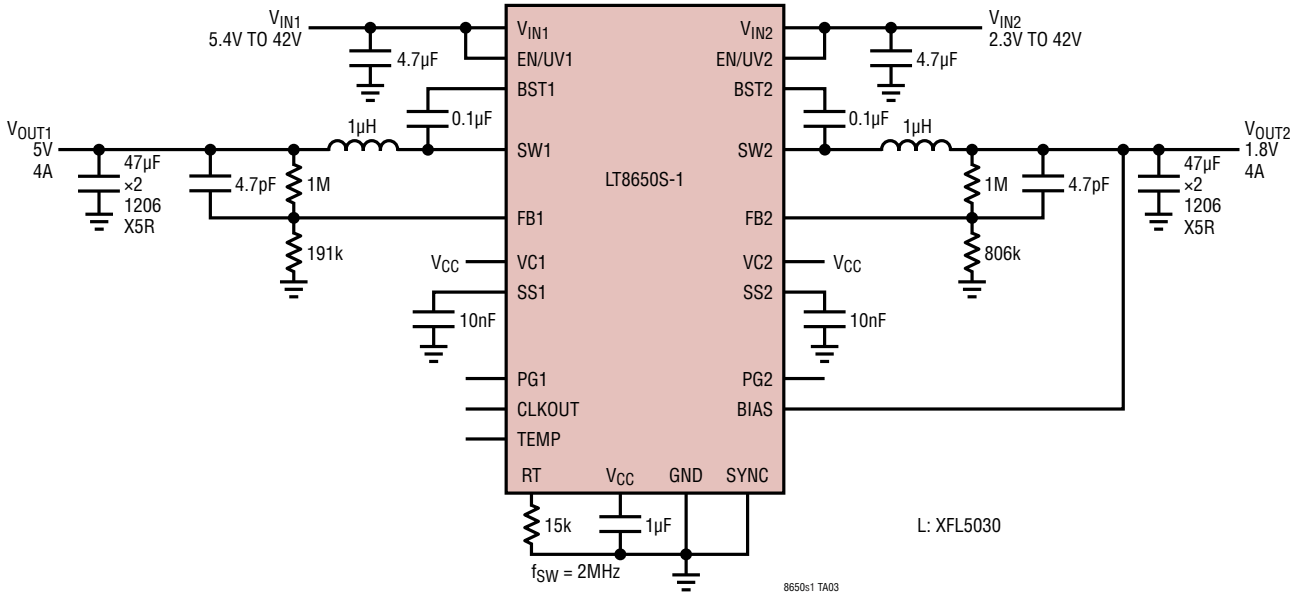
Figure 11. Case Temperature Rise vs 6A Pulsed Load

TYPICAL APPLICATIONS

5V, 3.3V, 2MHz Step-Down Converter with FCM and External Compensation

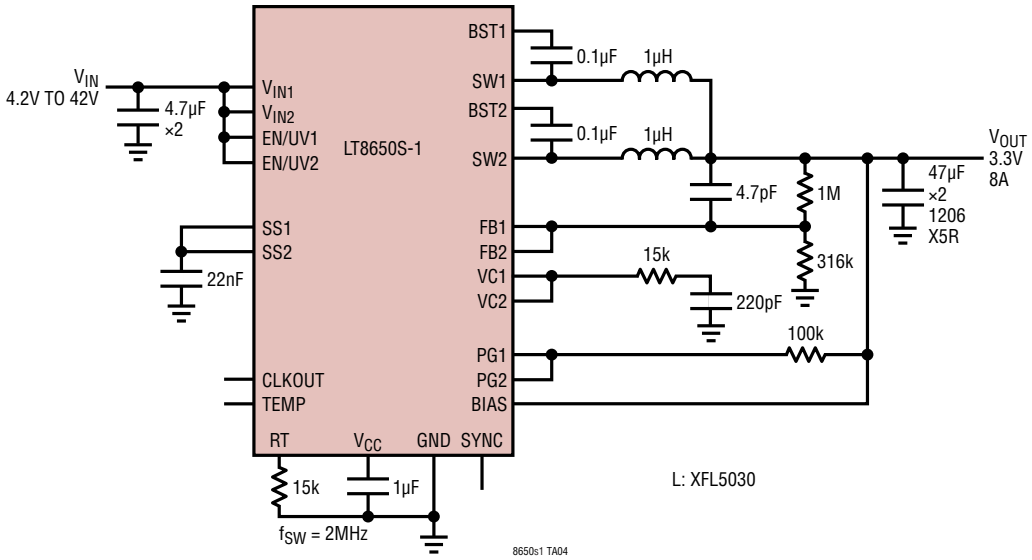


5V, 1.8V, 2MHz Step-Down Converter with Burst Mode and Internal Compensation

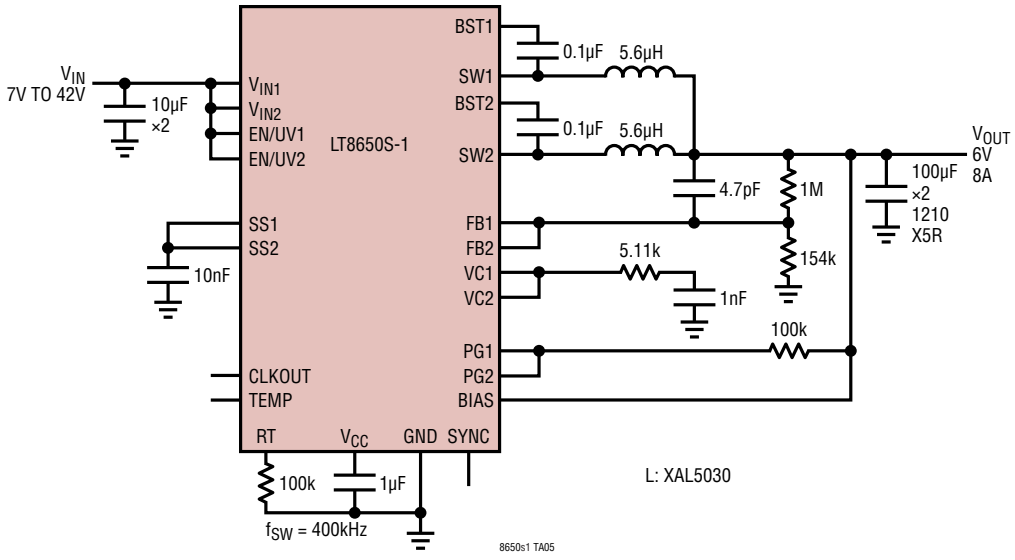


TYPICAL APPLICATIONS

Two Phase, 3.3V, 8A, 2MHz Step-Down Converter

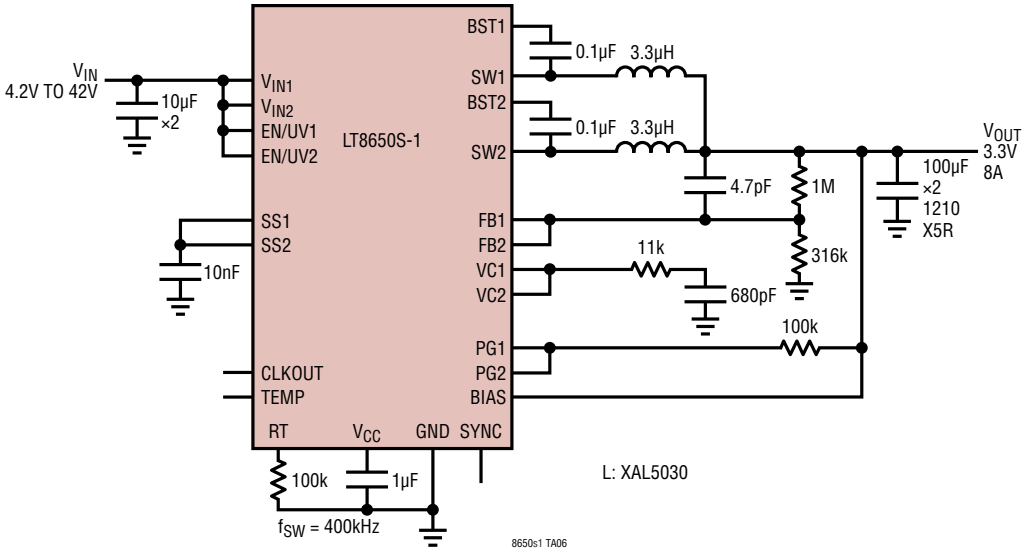


Two Phase, 6V, 8A,400kHz Step-Down Converter



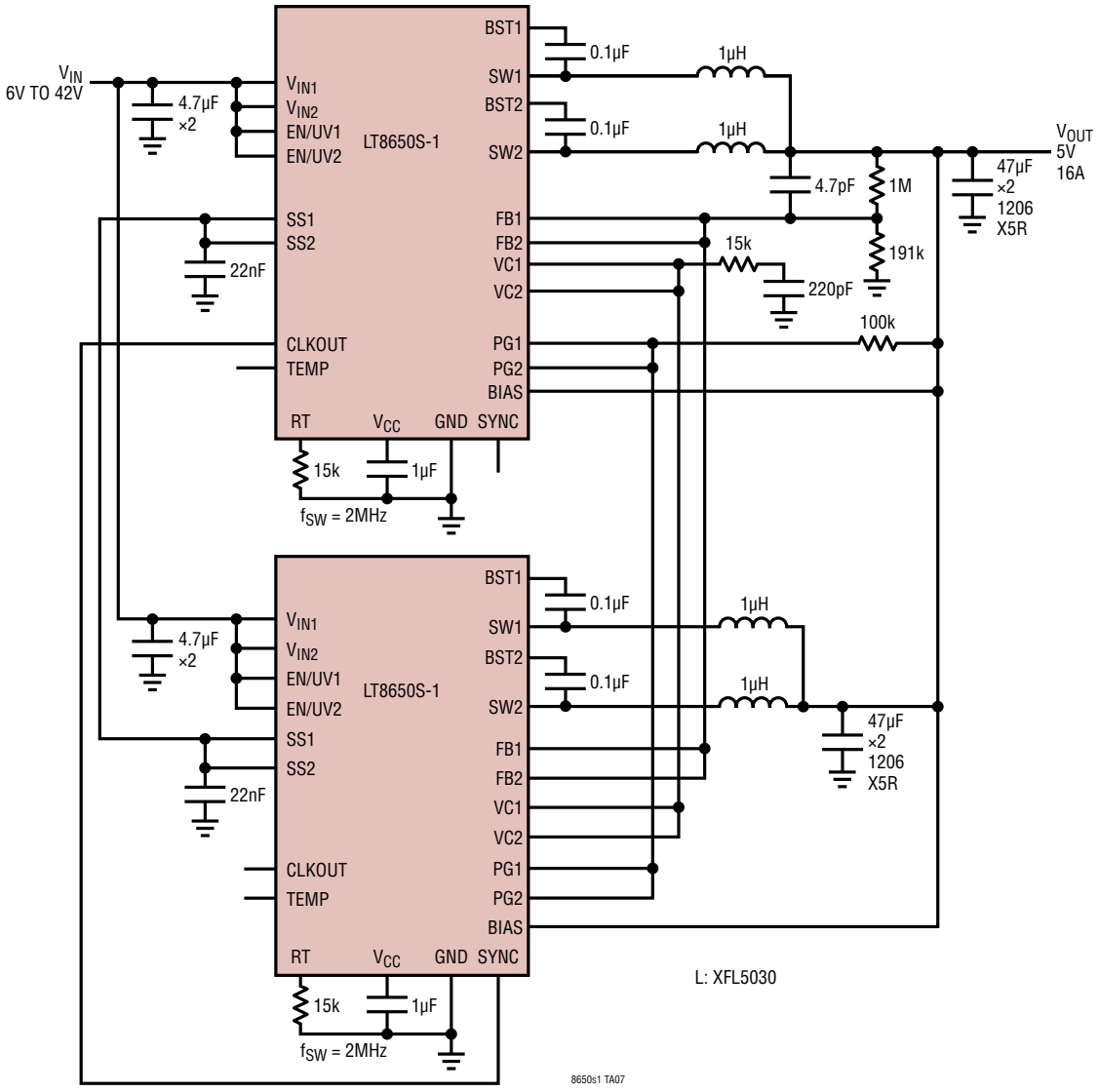
TYPICAL APPLICATIONS

Two Phase, 3.3V, 8A, 400kHz Step-Down Converter



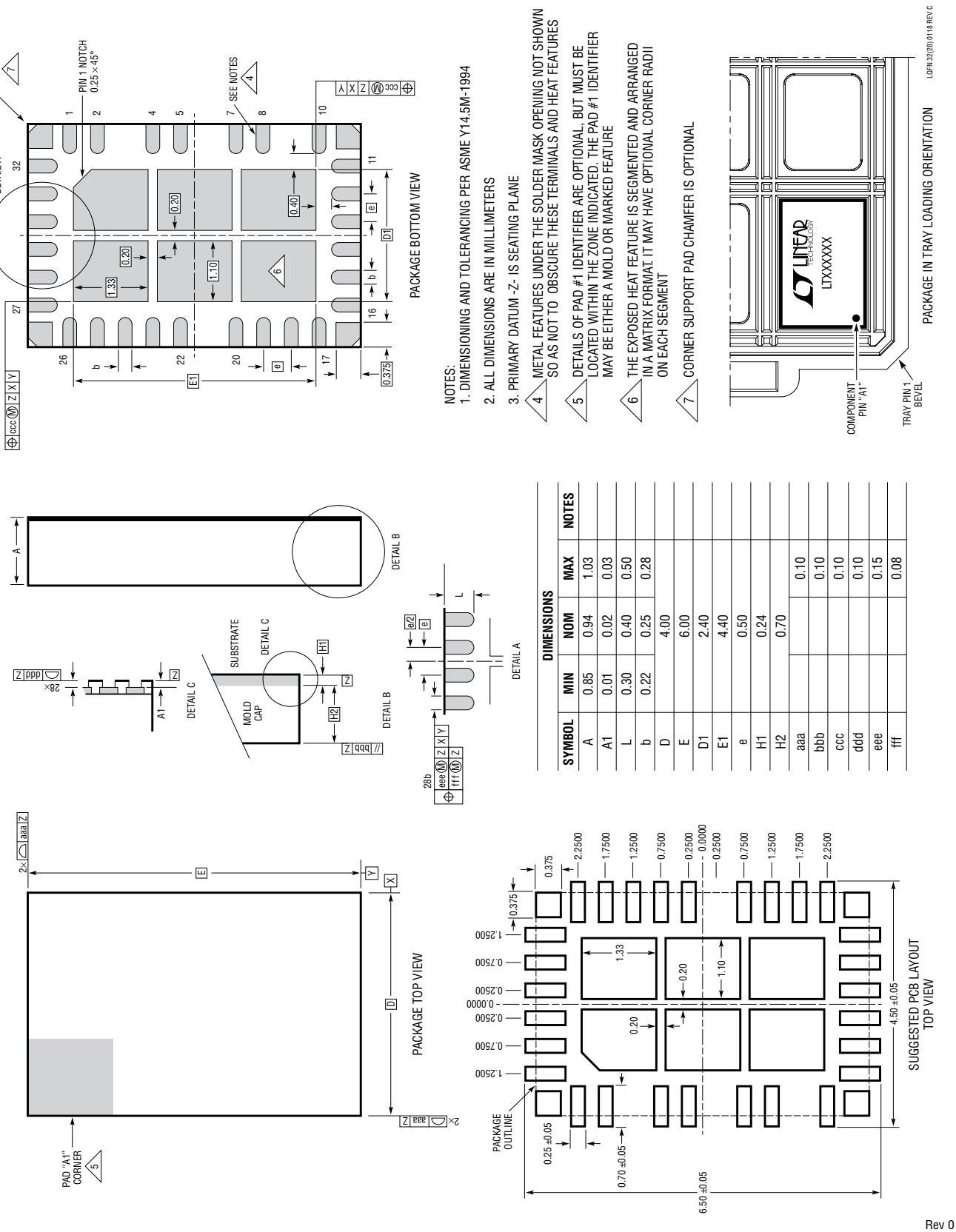
TYPICAL APPLICATIONS

Four Phase, 5V, 16A, 2MHz Step-Down Converter



PACKAGE DESCRIPTION

LQFN Package
32(28)-Lead (6mm × 4mm × 0.94mm)
(Reference LTC DWG # 05-08-1665 Rev C)

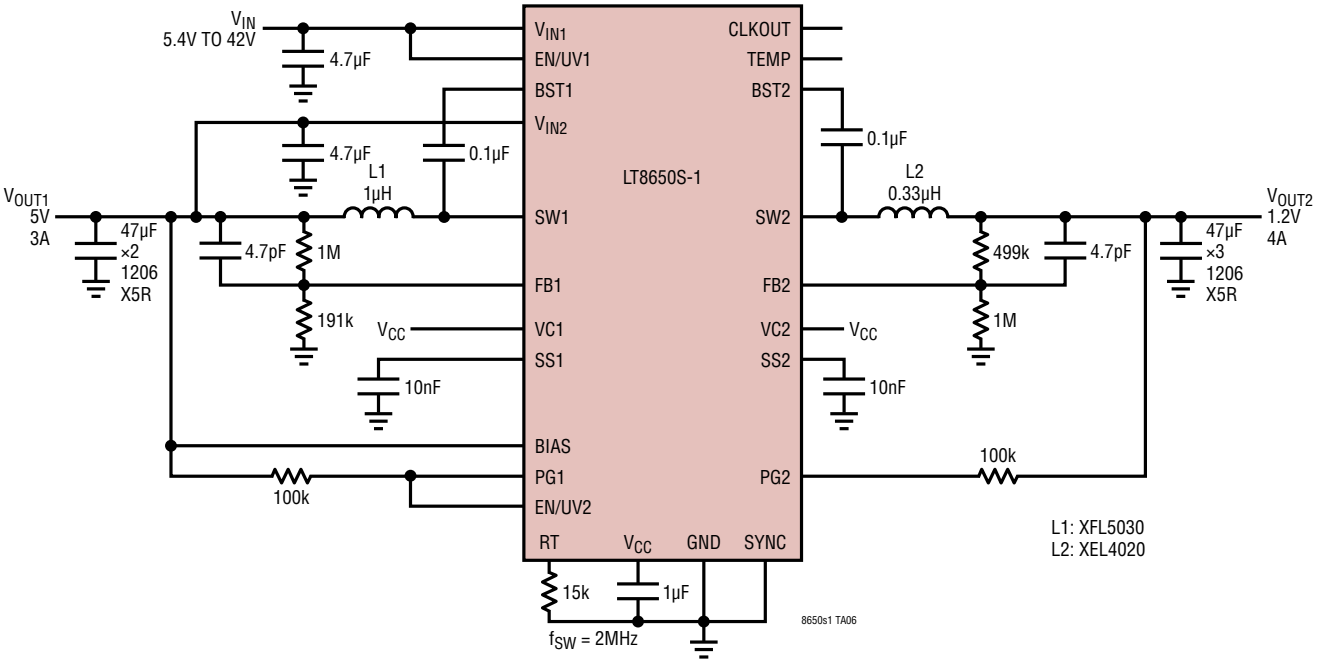


DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.94	1.03	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		6.00		
D1		2.40		
E1		4.40		
e		0.50		
H1		0.24		
H2		0.70		
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

Rev 0

TYPICAL APPLICATION

5V, 1.2V, 2MHz Two Stage Step-Down Converter with Output Sequencing



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8650S	42V, Dual 4A, 94% Efficiency, 3MHz Synchronous Silent Switcher 2 DC/DC Converter with I_Q = 6.2µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.2µA, 4x6 QFN-32 Package
LT8640S	42V, 5A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 4x4 QFN-24 Package
LT8609S	42V, 2A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, 3x3 QFN-16 Package
LT8645S	65V, 7A, 95% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 65V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, 4x6 QFN-32 Package
LT8609/ LT8609A	42V, 2A, 94% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-10E Package
LT8616	42V, Dual 2.5A + 1.5A 95% Efficiency, 3MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 6.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.5µA, I_{SD} < 1µA, TSSOP-28E, 3x6 QFN-28 Packages
LT8610A/ LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package
LT8610AC	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E Package
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 3.0µA, I_{SD} < 1µA, 3x6 QFN-28 Package
LT8602	42V, Quad Output (2.5A+1.5A+1.5A+1.5A) 95% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 25µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 25µA, I_{SD} < 1µA, 6x6 QFN-40 Package