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NTE4569B
Integrated Circuit
CMOS, Programmable Divide–By–"N"
Dual 4–Bit BCD/Binary Counter

Description:

The NTE4569B is a programmable divide–by–N dual 4–bit binary or BCD down counter in a 16–Lead DIP type package constructed with MOS P–channel and N–channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with a 4569B phase comparator/counter in frequency synthesizers, phase–locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

Features:

- 9.5Mhz Typical Counting Rate at 10V for Any Division Ratio Greater Than 1
- Speed–Up Circuitry for Zero Detection and Preset Enable
- Each 4–Bit Counter Can Divide Independently in BCD or Binary Mode
- Quiescent Current = 5.0nA/Package (Typ) at 5Vdc

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–0.88	–	–2.4	–	mAdc
(V_{OL} = 0.4Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	50	–	0.005	50	–	150	µAdc
(Per Package)		10	–	100	–	0.010	100	–	300	µAdc
		15	–	200	–	0.015	200	–	600	µAdc
Total Supply Current	I_T	5.0	I_T = (0.58µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on All Outputs, All Buffers Switching Note 3, Note 5)		10	I_T = (1.20µA/kHz) f + I_{DD}							µAdc
		15	I_T = (1.95µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both “1” and “0” = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	$t_{TLH,}$	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Turn−On Delay Time PE_{out}	t_{PLH}	5.0	–	420	700	ns
		10	–	175	300	ns
		15	–	125	250	ns
Q Output		5.0	–	675	1200	ns
		10	–	285	500	ns
		15	–	200	400	ns
Turn−Off Delay Time PE_{out}	t_{PHL}	5.0	–	380	600	ns
		10	–	150	300	ns
		15	–	100	200	ns
Q Output		5.0	–	530	1000	ns
		10	–	225	400	ns
		15	–	155	300	ns
Circuit Pulse Width	t_{WH}	5.0	300	100	–	ns
		10	150	45	–	ns
		15	115	30	–	ns
Clock Pulse Frequency (Note 4)	f_{cl}	5.0	–	3.5	2.1	MHz
		10	–	9.5	5.7	MHz
		15	–	13.0	7.8	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			µs
		10				µs
		15				µs

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. This implies that zero detection and preset enable is done while the clock is running at the specified frequency.

Operating Characteristics:

The NTE4569B includes a high speed Johnson counter followed by a BCD/binary 4−bit synchronous counter. The use of an encoder allows the Johnson counter to be programmed (i.e. preset) in BCD or binary code through inputs D_{PA2}, D_{PA3}, and D_{PA4}.

The BCD/binary counter can be programmed through inputs D_{PA1}, D_{PA2}, D_{PA3}, and D_{PA4}. For each counter a divide ratio of 10 (BCD count) or 16 (binary count) can be chosen independently by inputs CTL_A and CTL_B respectively. When one of those inputs is set to high, the divide ratio of the corresponding counter is 10 (BCD); when it i set low, the division ratio is 16 (binary).

A Cascade Feedback input (Pin7), a Q output (Pin15) and a Preset Enable output (Pin1) made it possible to cascade a 4568B, NTE4522B and NTE4526B with this device. CF, Q an PE_{out} of NTE4569B must be respectively connected to “0”, C and PE of the following counter.

Operating Characteristics (Cont'd):

When NTE4569B is used alone, CF must be connected to V_{DD}. One pulse will appear on output PE_{out} every N clock periods (N being the value programmed on the D_P inputs). Both counters included in NTE4569B and eventually all the counters which are cascaded, should normally be preset at the programmed values during the clock period where they all reach the count zero. For best speed performance, preset is started as soon as count 1 is detected. As a consequence, it is not possible to program a frequency division ratio of one. However, it is possible to program a division ratio of 11 (i.e. D_{PA1} . . . D_{PA4} = 1,0,0,0 and D_{PB1} . . . D_{PB4} = 1,0,0,0), or a division ratio of 101 if another counter is cascaded with the NTE4569B.

This high speed configuration makes it possible to guarantee a maximum clock pulse frequency of 5.7Mhz for a 10V V_{DD} supply for any division ratio greater than one. Due to the presence of the early zero detection, the circuit must be used in the two least significant digit positions.

Because all the circuitry i static, there is no minimum frequency specification for the Clock Input, C (Pin9).

Pin Connection Diagram