

# TVS Diodes

Transient Voltage Suppressor Diodes

## ESD18VU1B-02LRH

ESD / Transient Protection Diode for Near Field Communication (NFC)

ESD18VU1B-02LRH

## Data Sheet

Revision 1.4, 2013-08-07  
Final

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**Revision History: Revision 1.3, 2013-06-26**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.4, 2013-08-07</b>	
7 - 10	Figure 5) - Figure 9) updated

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Last Trademarks Update 2010-06-09

# 1 ESD / Transient Protection Diode for Near Field Communication (NFC)

## 1.1 Features

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD):  $\pm 15$  kV air discharge,  $\pm 12$  kV contact discharge
  - IEC61000-4-5 (surge):  $\pm 2$  A ( $t_p = 8 / 20 \mu s$ )
- AC working voltage up to  $\pm 18.5$  V ( $V_{TRIG \min} = 20$  V)
- Ultra-low capacitance:  $C_L = 0.3$  pF (typical)
- Small leadless plastic package, size 0402
- Pb-free (RoHS compliant) and halogen free package



## 1.2 Application Examples

- ESD Protection of RF signal lines in Near Field Communication (NFC) applications

## 1.3 Product Description

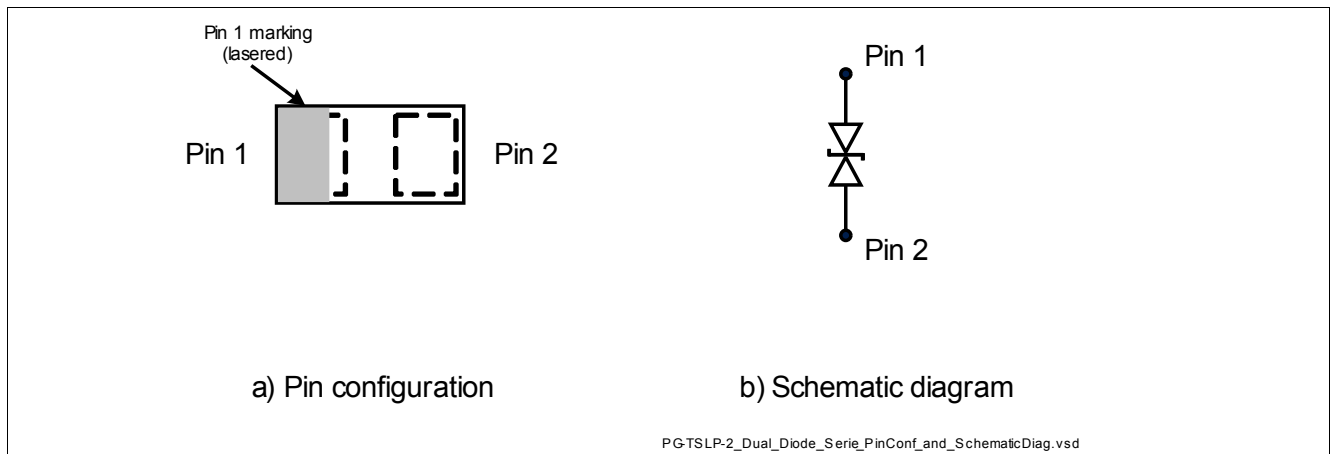


Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD18VU1B-02LRH	TSLP-2-17	1 line, bi-directional	X

## 2 Characteristics

**Table 2** Maximum Rating at  $T_A = 25\text{ °C}$ , unless otherwise specified

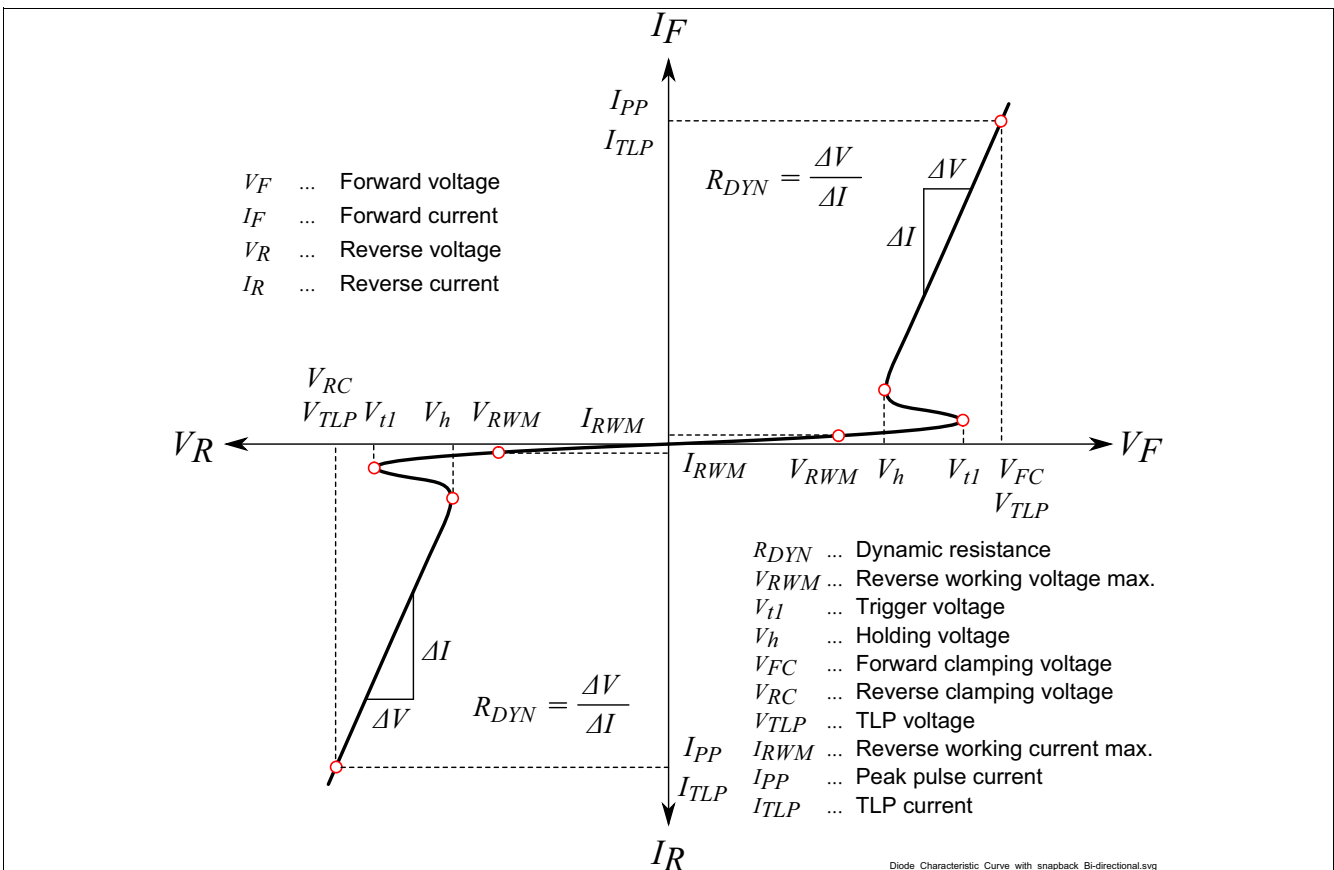
Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD air discharge <sup>1)</sup>	$V_{ESD}$	–	–	±15	kV
ESD contact discharge <sup>1)</sup>	$V_{ESD}$	–	–	±12	kV
Peak pulse current ( $t_p = 8 / 20\ \mu\text{s}$ ) <sup>2)</sup>	$I_{PP}$	–	–	±2	A
Operating temperature	$T_{OP}$	-40	–	85	°C
Storage temperature	$T_{stg}$	-55	–	150	°C

1)  $V_{ESD}$  according to IEC61000-4-2

2)  $I_{PP}$  according to IEC61000-4-5

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

### 2.1 Electrical Characteristics at $T_A = 25\text{ °C}$ , unless otherwise specified



**Figure 2** Definitions of electrical characteristics

**Characteristics**
**Table 3 AC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
AC working voltage	$V_{RWM}$	–	–	18.5	V	Both directions
AC trigger voltage	$V_{TRIG}$	20	–	–	V	Both directions
AC reverse current	$I_R$	–	–	30	nA	$V_R = 18.5\text{ V}$ Both directions
		–	–	1	mA	$V_R = 20\text{ V}$ Both directions

**Table 4 RF Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance <sup>1)</sup>	$C_L$	0.15	0.3	0.6	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
		0.15	0.3	0.6	pF	$V_R = 0\text{ V}, f = 1\text{ GHz}$
Serie inductance	$L_S$	–	0.4	–	nH	

1) Total capacitance I/O to *GND*

**Table 5 ESD Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>1)</sup>	$V_{CL}$	–	28	–	V	$I_{TLP} = 16\text{ A},$ $t_p = 100\text{ ns}$
		–	34	–		$I_{TLP} = 25\text{ A},$ $t_p = 100\text{ ns}$
Clamping voltage <sup>2)</sup>	$V_{CL}$	–	17	–	V	$I_{PP} = 1\text{ A},$ $t_p = 8 / 20\text{ }\mu\text{s}$
Dynamic resistance <sup>1)</sup>	$R_{DYN}$	–	0.6	–	$\Omega$	

1) Please refer to Application Note AN210 [1]. TLP parameter:  $Z_0 = 50\text{ }\Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristics between  $I_{TLP1} = 5\text{ A}$  and  $I_{TLP2} = 30\text{ A}$

2)  $I_{PP}$  according to IEC61000-4-5

2.2 Typical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

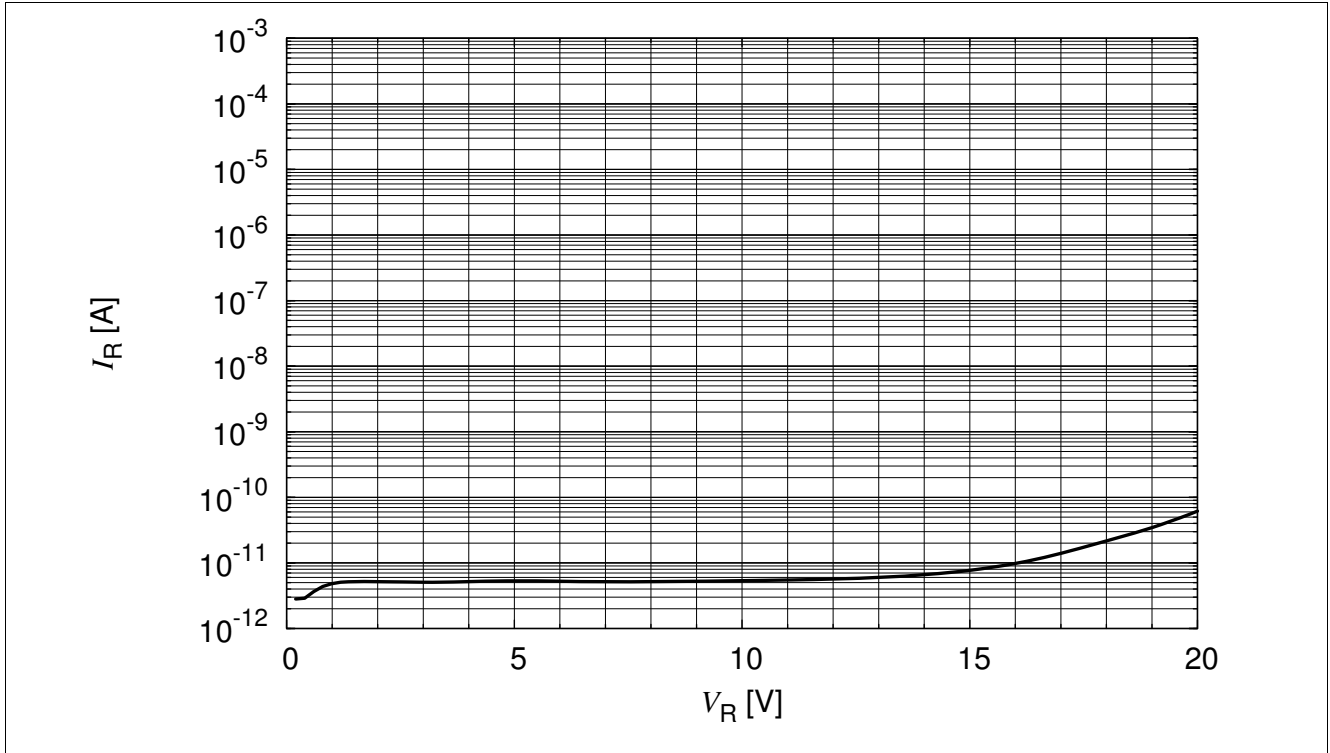


Figure 3 Reverse current:  $I_R = f(V_R)$

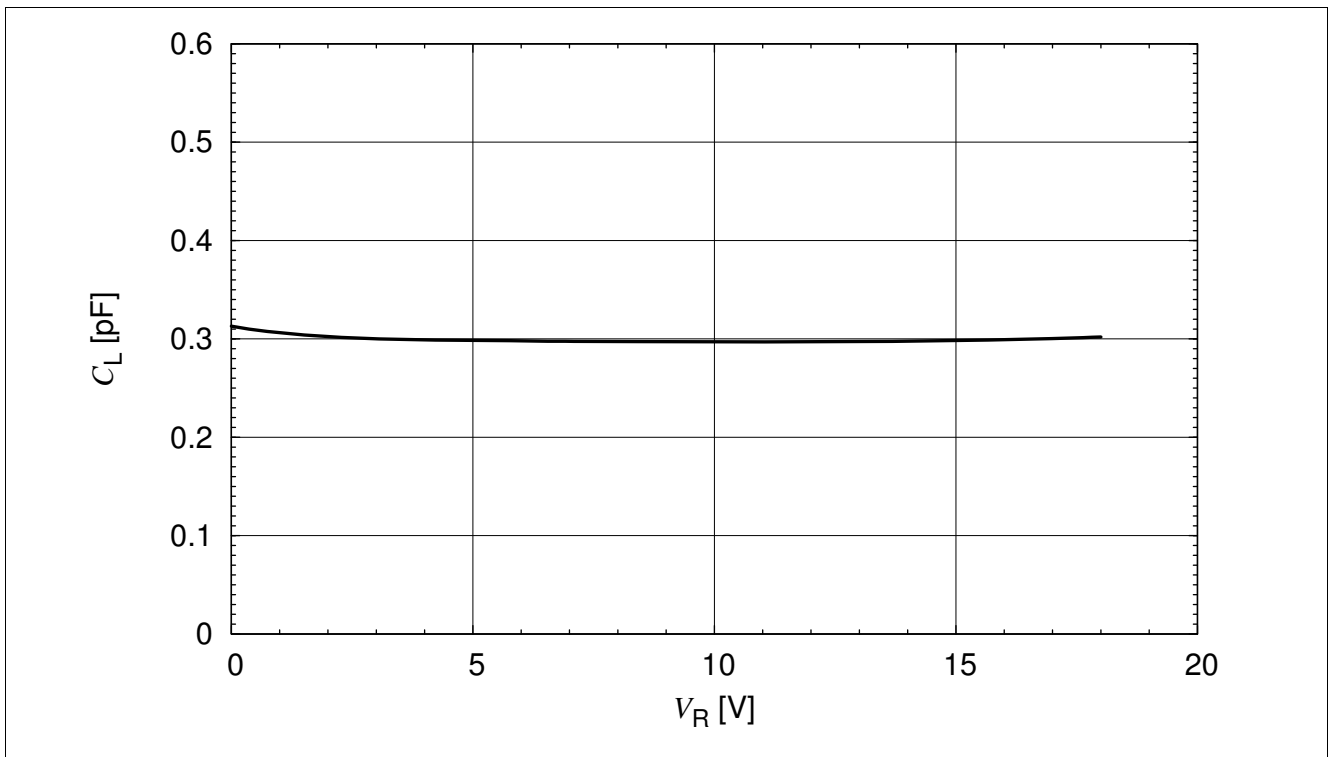
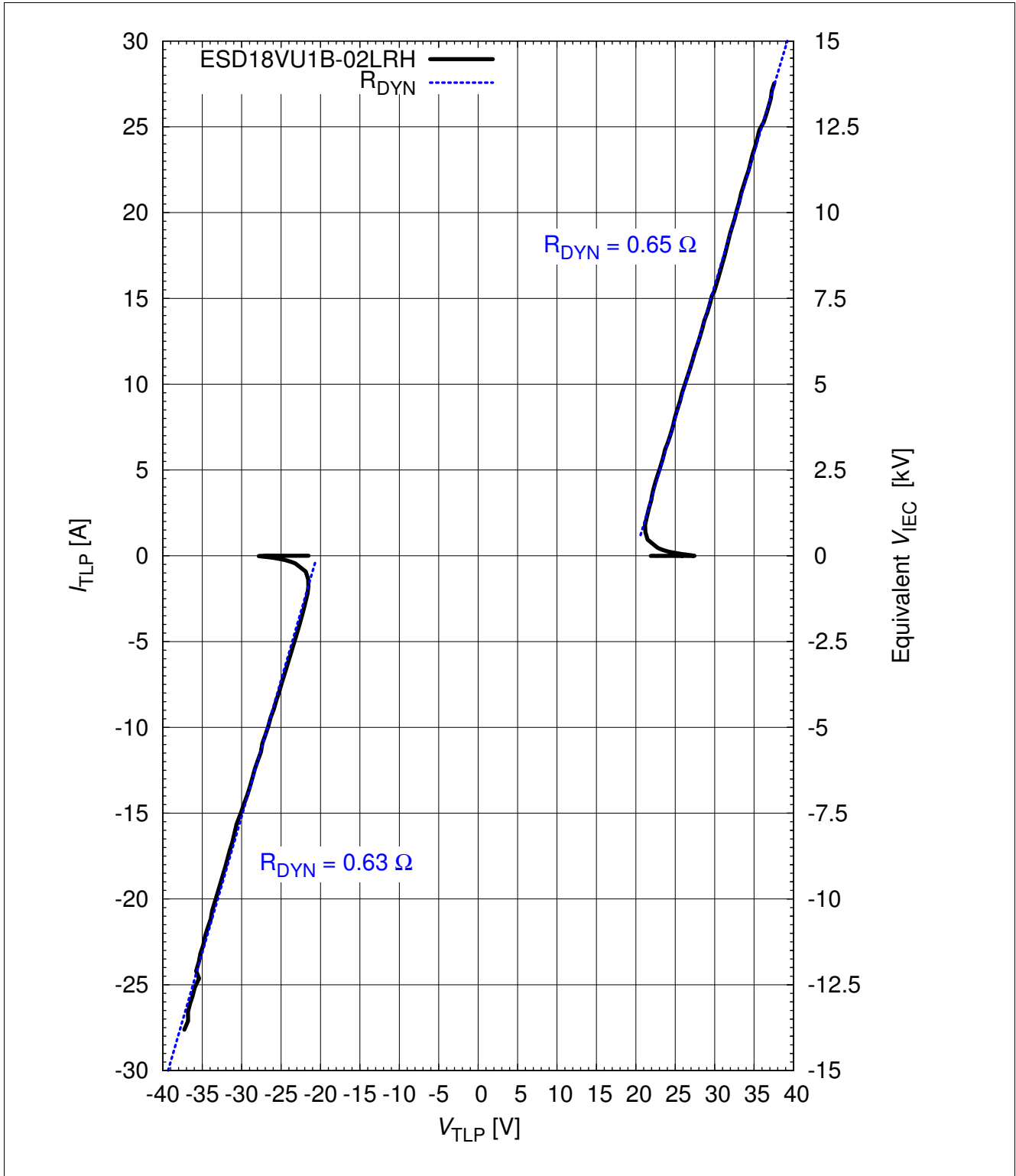


Figure 4 Line capacitance:  $C_L = f(V_R), f = 1\text{ MHz}$



**Figure 5** Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$  according ANSI/ESD STM5.5.1- Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 0.6 \text{ ns}$ ,  $I_{TLP}$  and  $V_{TLP}$  averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ , extraction of dynamic resistance using squares fit to ELP characteristic between  $I_{TLP1} = 5 \text{ A}$  and  $I_{TLP2} = 30 \text{ A}$ . Please refer to Application Note AN210 [1]



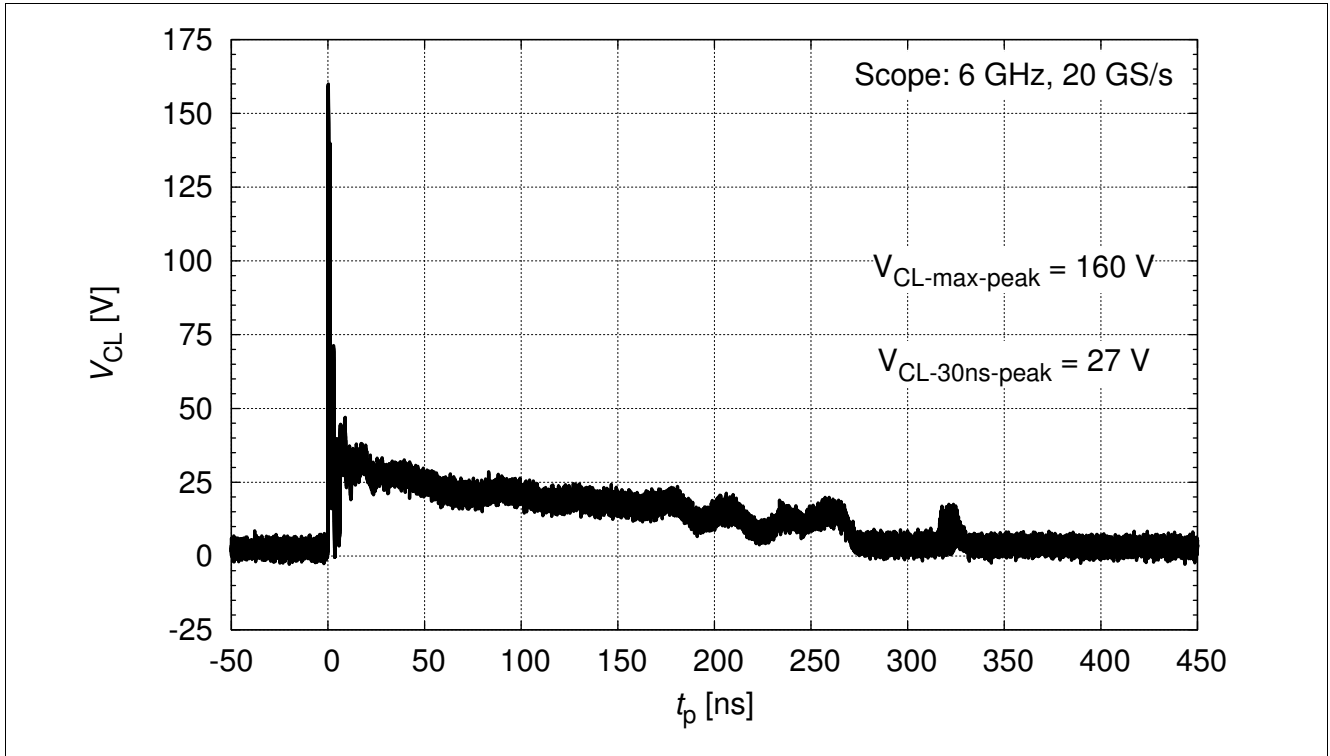


Figure 6 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV positiv pulse from pin 1 to pin 2

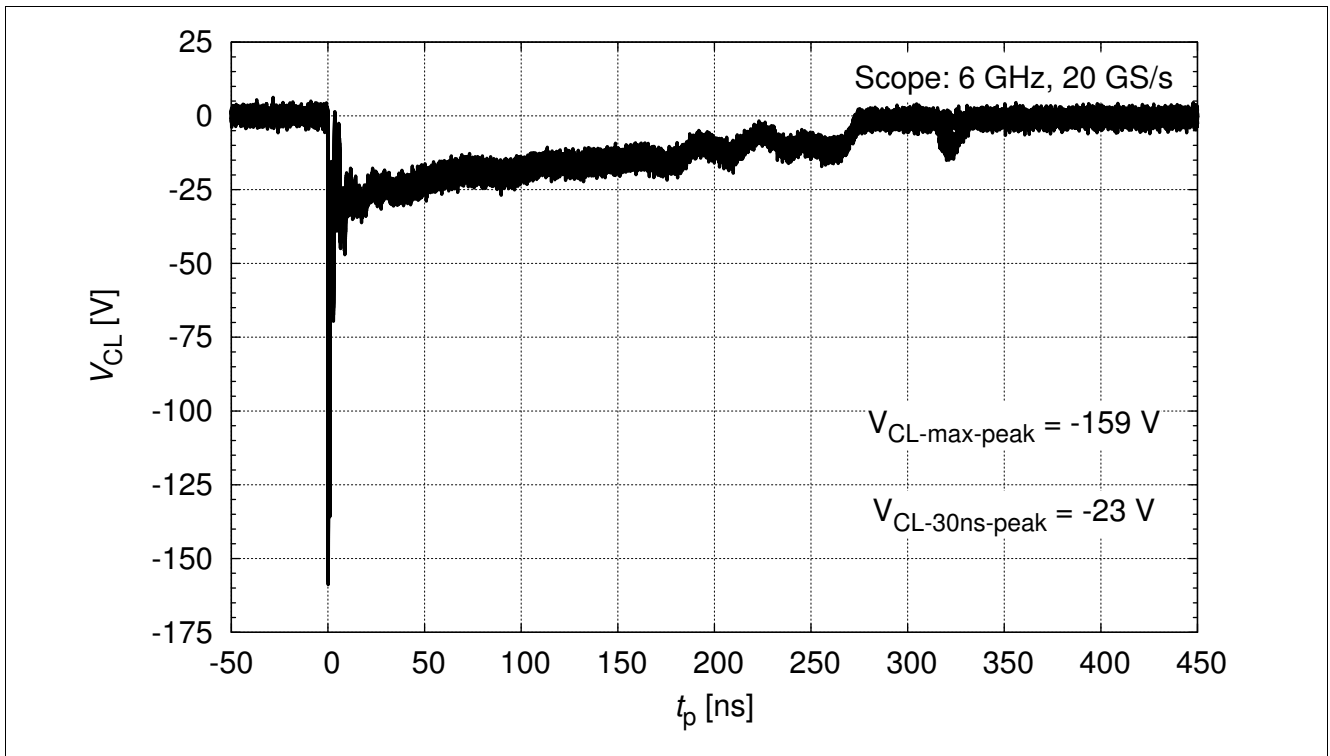


Figure 7 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV negativ pulse from pin 1 to pin 2

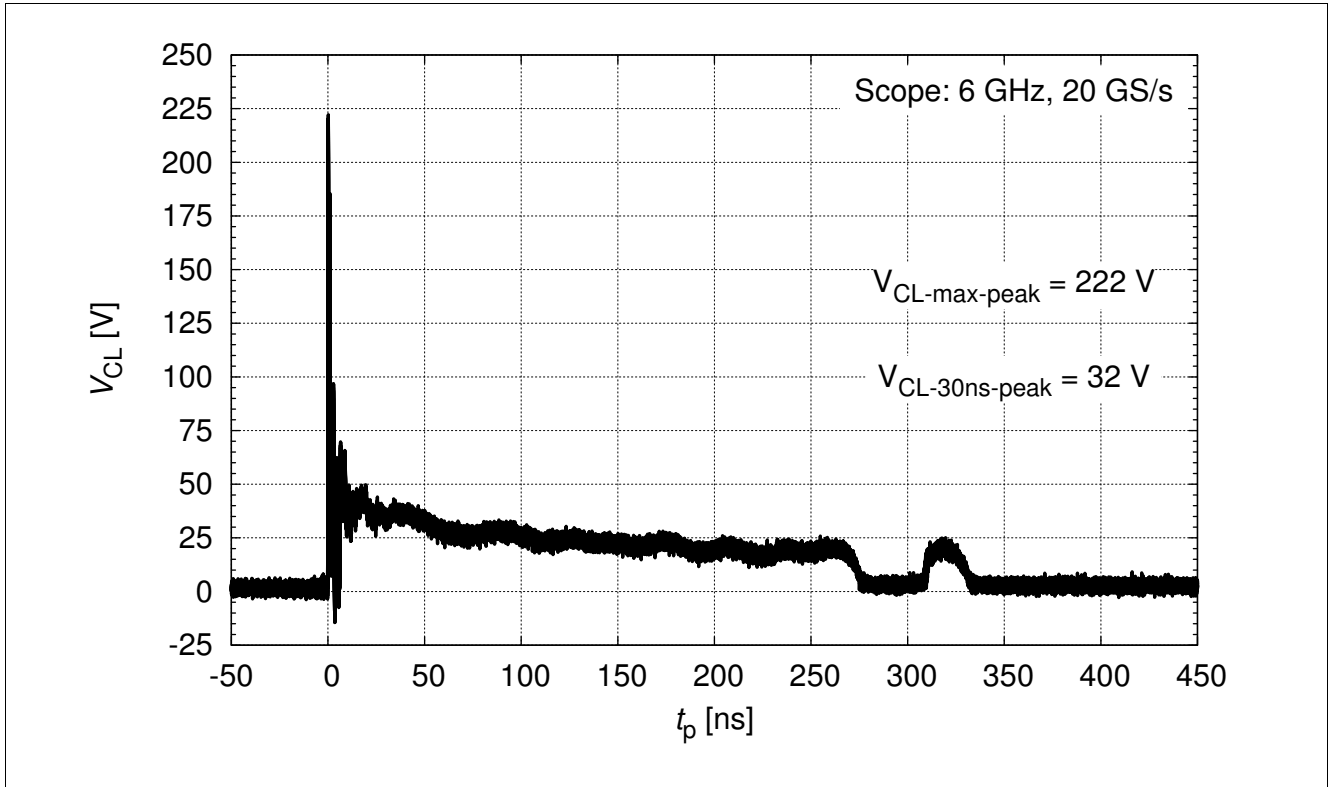


Figure 8 IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV positiv pulse from pin 1 to pin 2

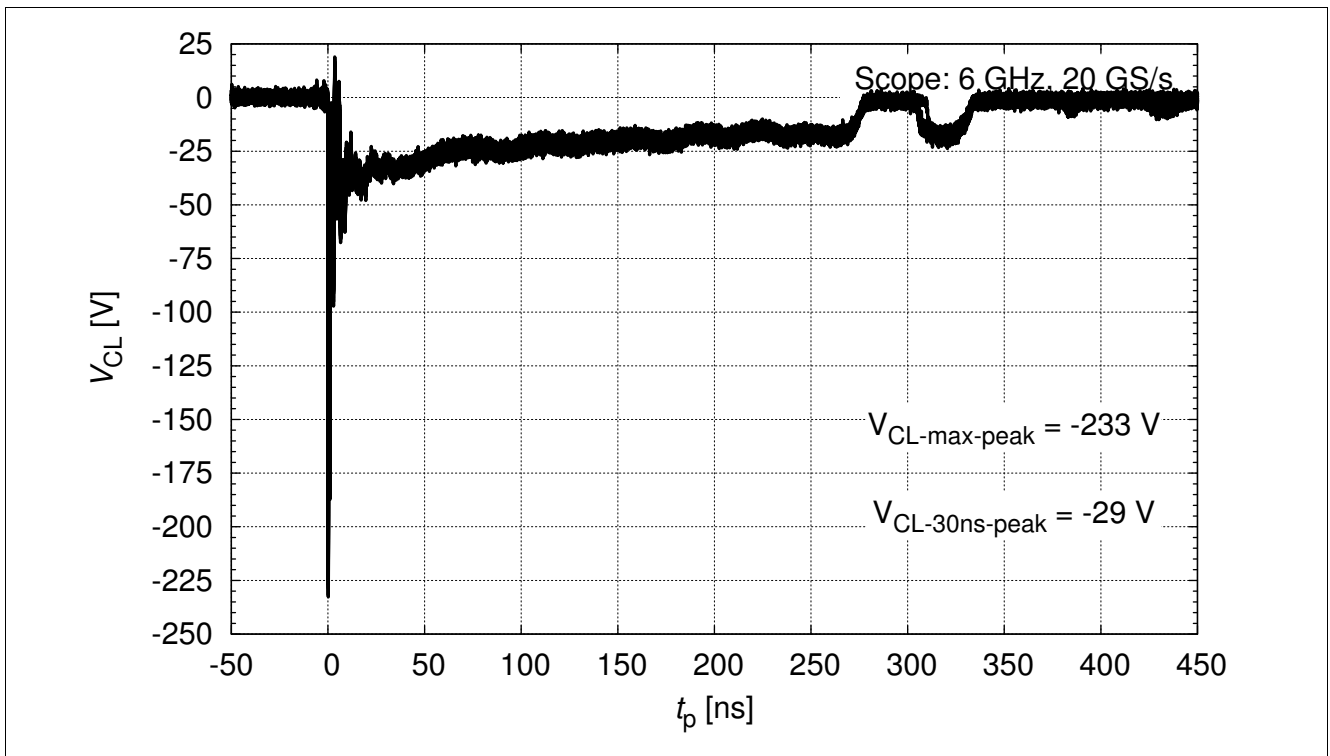


Figure 9 IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV negativ pulse from pin 1 to pin 2

### 3 Application Information

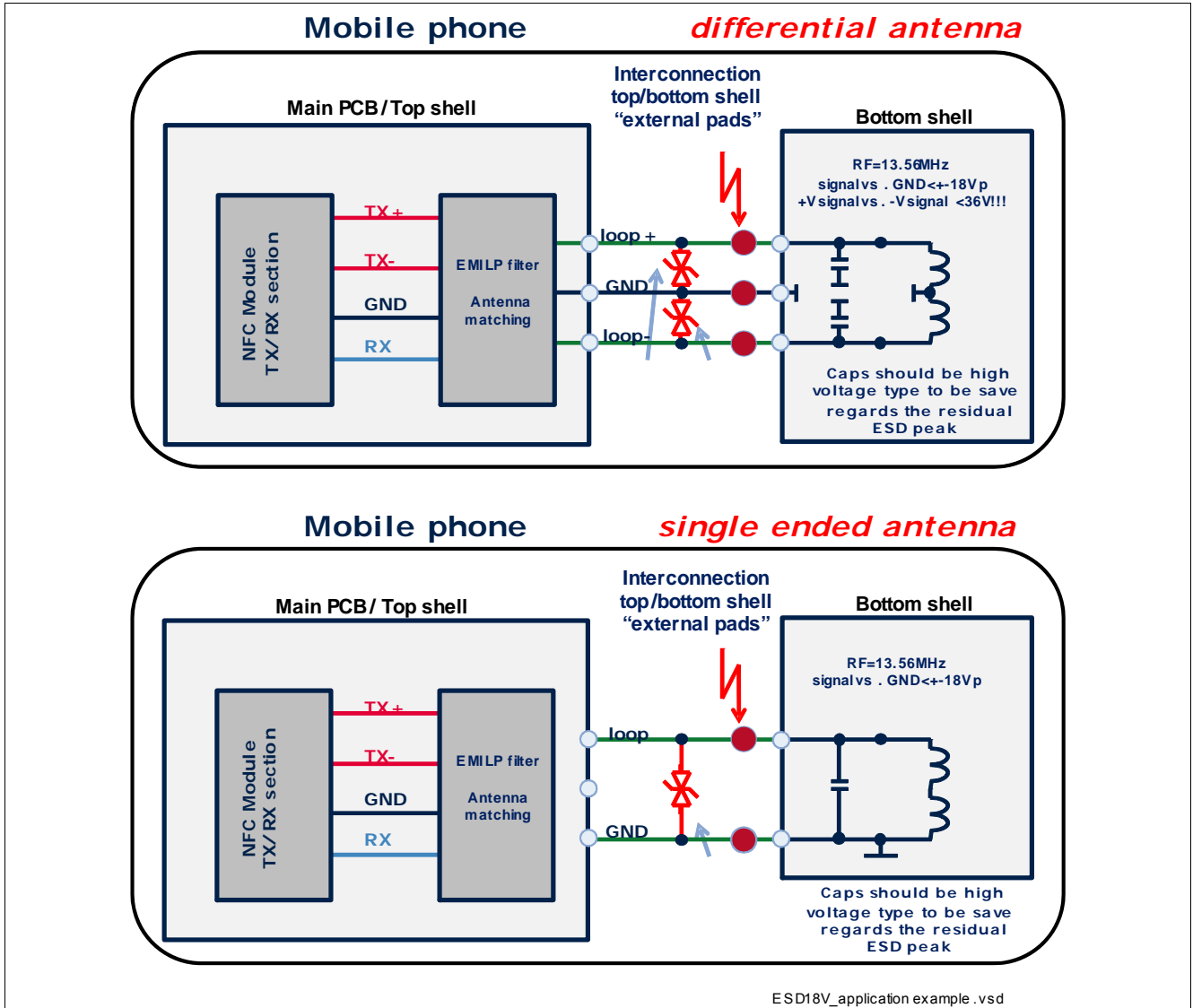


Figure 10 Bi-directional ESD / Transient protection for NFC Frontend [3]

#### 4 Ordering Information Scheme (Examples)

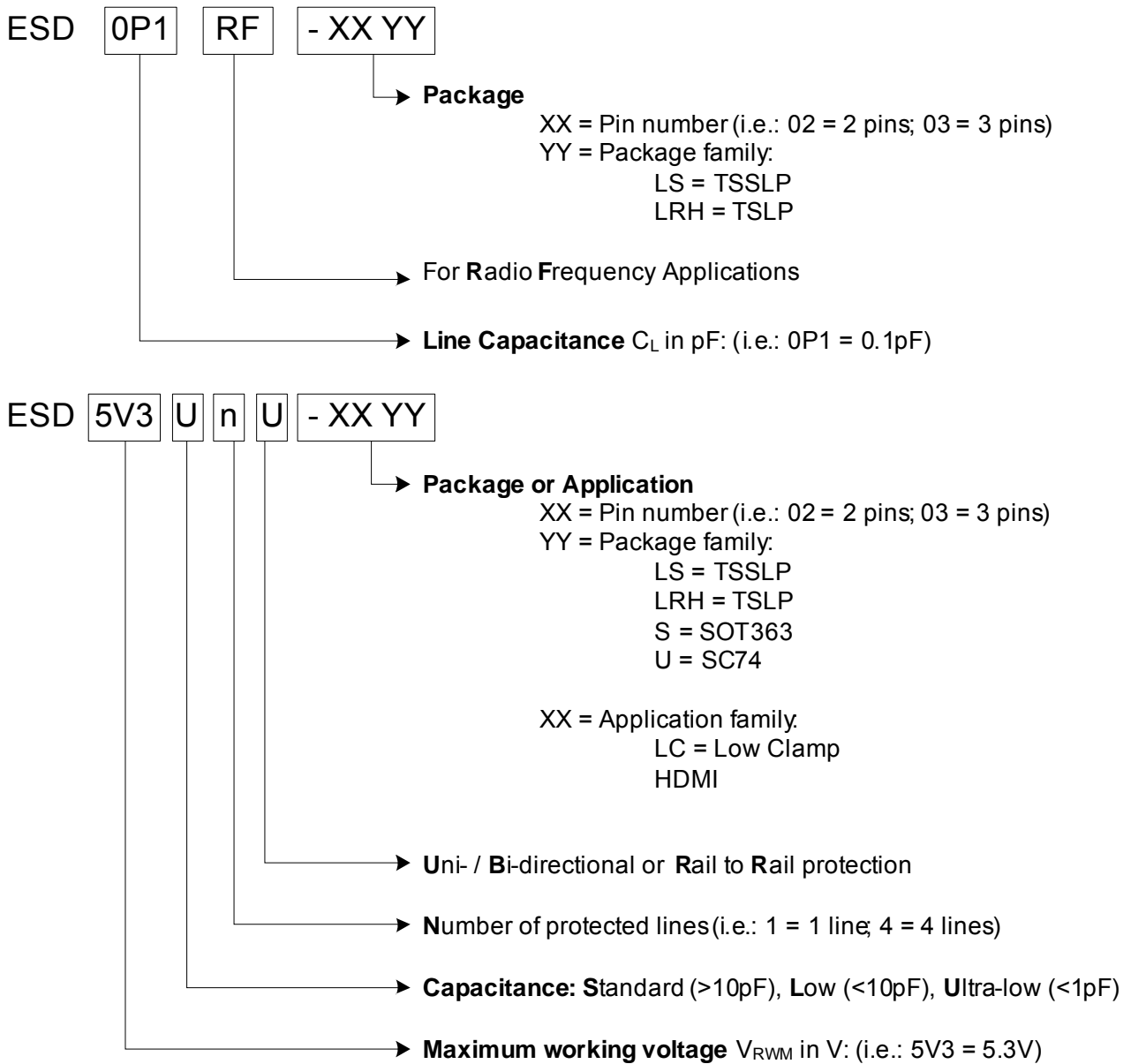


Figure 11 Ordering information scheme

## 5 Package Information

### 5.1 PG-TSLP-2-17 [2]

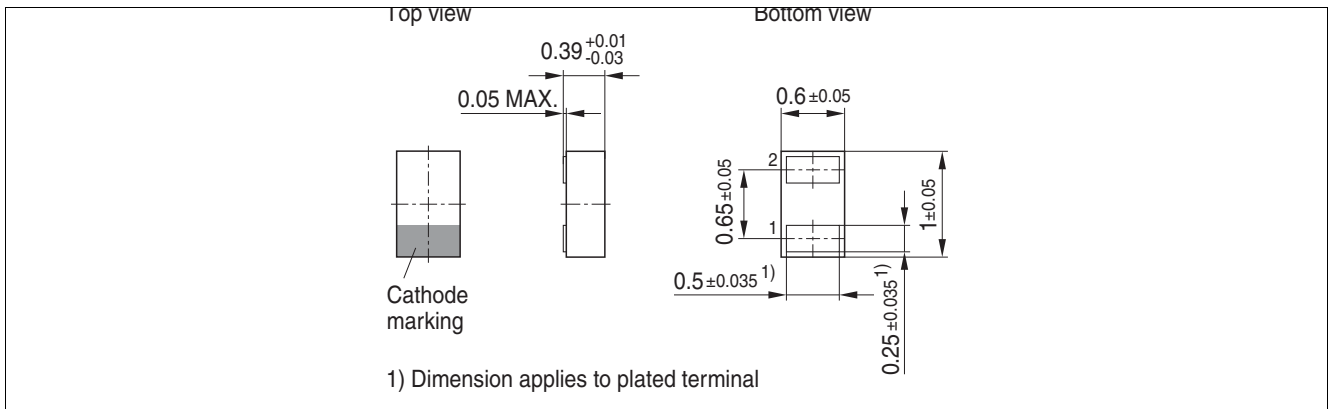


Figure 12 PG-TSLP-2-17: Package overview

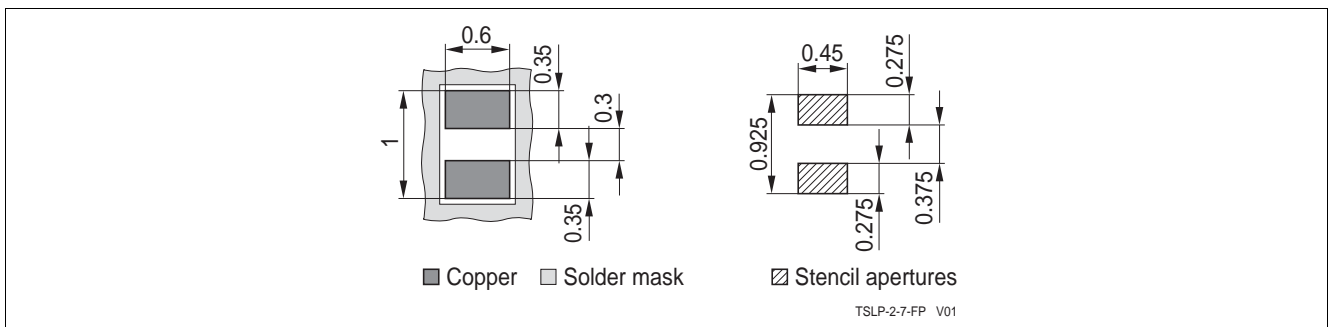


Figure 13 PG-TSLP-2-17: Footprint

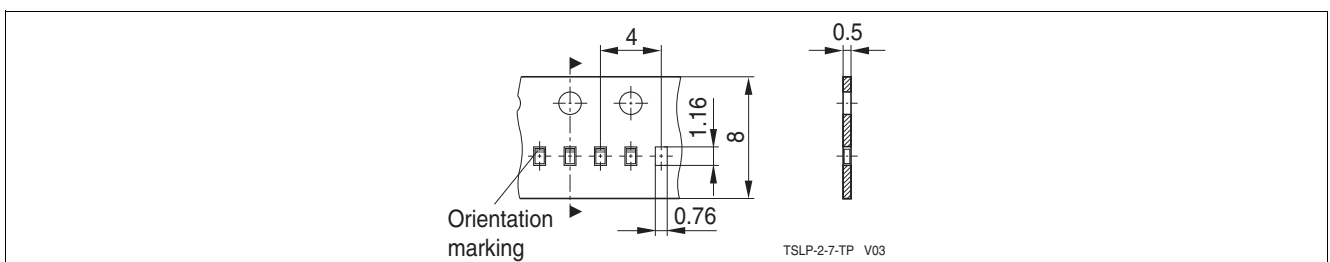


Figure 14 PG-TSLP-2-17: Packing

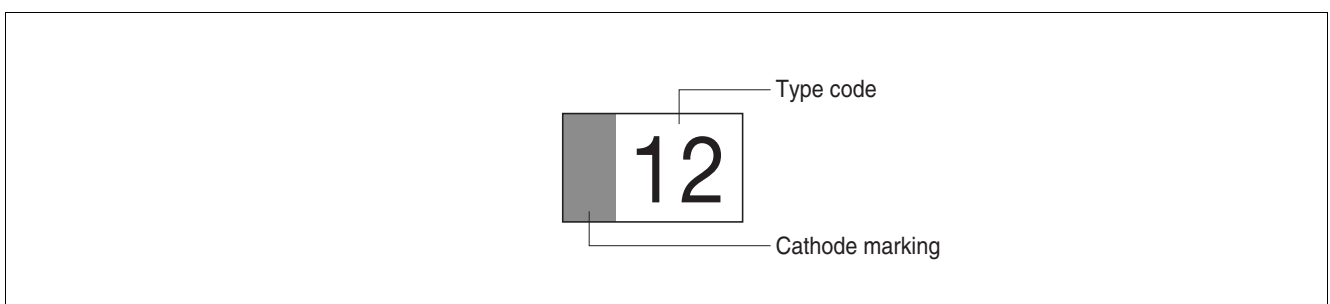


Figure 15 PG-TSLP-2-17: Marking (example)

**References**

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages
- [3] Infineon AG - **Application Note AN244**: Tailored ESD Protection for the NFC Frontend

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