MGA-444940-02

4.4 - 4.9 GHz 10W High Efficiency High Power Amplifier Data Sheet and Application Note

MicroWave Technology

FEATURES

- GaN Based High Power Amplifier
- 20% Efficiency at 33 dBm Linear Output Power
- 40 dBm P-$_{3dB}$
- 33 dBm Linear Pout @ 2.5% EVM (802.11 64QAM)
- 12 dB Gain
- Fully Matched Input and Output for Easy Cascase
- +28V Bias Voltage
- RoHS Compliant Surface Mount Package
- MTTF > 100 years @ 85C Ambient Temperature

APPLICATIONS

- Telemetry
- Avionics
- Private Microwave Network Systems
- Military Wireless Communications

DESCRIPTION

The MGA-444940-02 is a power amplifier with the State-of-the-Art linear power-added-efficiency between 4.4 GHz and 4.9 GHz frequency band. Based on advanced robust GaN device technology, the power-added-efficiency of this power amplifier is over 20% at 2W linear burst power with 2.5% EVM and ACPR better than -38 dBc. The modulation test pattern is 802.16x 64QAM. The high efficiency linear power amplifier also has excellent reliability. Ideal applications include the driver and the output power stage of the telemetry, avionics, private microwave network systems, and military wireless communications.

TYPICAL RF PERFORMANCE:

Vds=28V, Vgs=-3.0V, Idq=100mA, Ta=25C, Z0=50ohm

PARAMETER	UNITS	TYPICAL DATA
Frequency Range	MHz	4400-4900
Gain (Typ / Min)	dB	12 / 10
Gain Flatness (Typ / Max)	+/-dB	1.0 / 1.5
Input Return Loss	dB	8
Output Return Loss	dB	10
Output P3dB	dBm	40
Pout @ 2.5% EVM	dBm	33
Operating Current Range	mA	100-400
Thermal Resistance	ºC/W	7

ABSOLUTE MAXIMUM RATINGS:

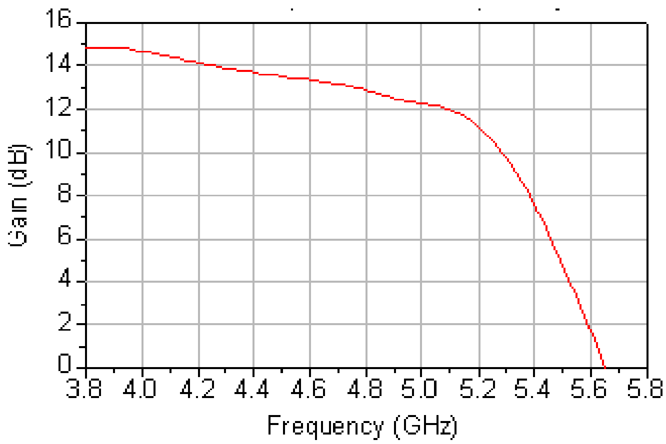
Ta=25C *

SYMBOL	PARAMETERS	UNITS	MAX
Vds	Drain to Source Voltage	V	50
Vgs	Gate to Source Voltage	V	10
Id	Drain Current	mA	1000
Ig	Gate Current	mA	10
Pdiss	DC Pow er Dissipation	W	50
Pin max	RF Input Pow er	dBm	+33
Tch	Channel Temperature	ºC	175
Tstg	Storage Temperature	ºC	-55 to 150

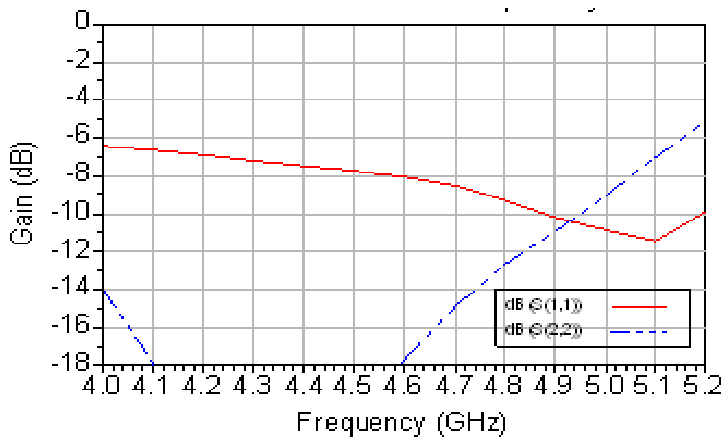
Exceeding any on of these limits may cause permanent damage.

TYPICAL RF PERFORMANCE: *Vds=28V, Vgs=-3.0V, Idq=100mA, Ta=25C, Z0=50ohm*

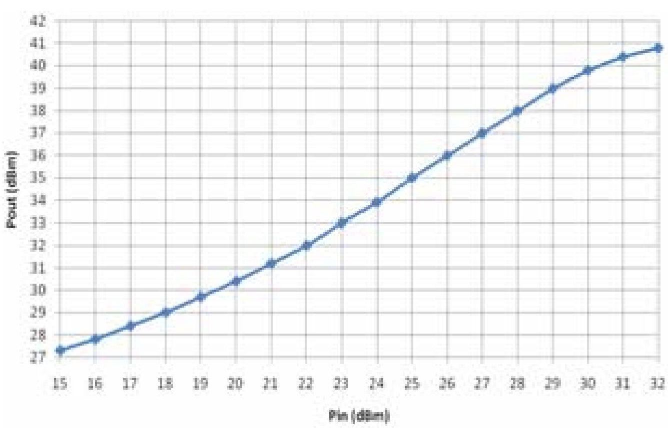
Gain Response vs. Frequency



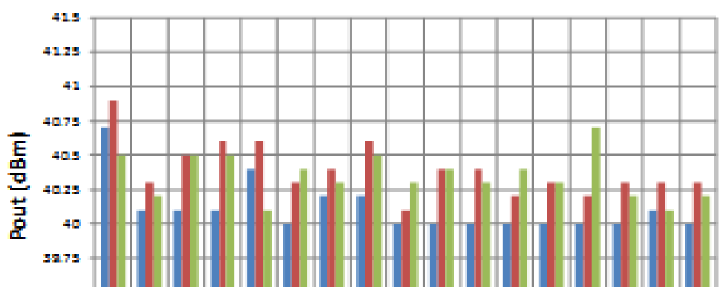
Return Loss vs. Frequency



Pout vs. Pin Fo=4.5GHz Vdd=28 Vdc Idq=121 mA

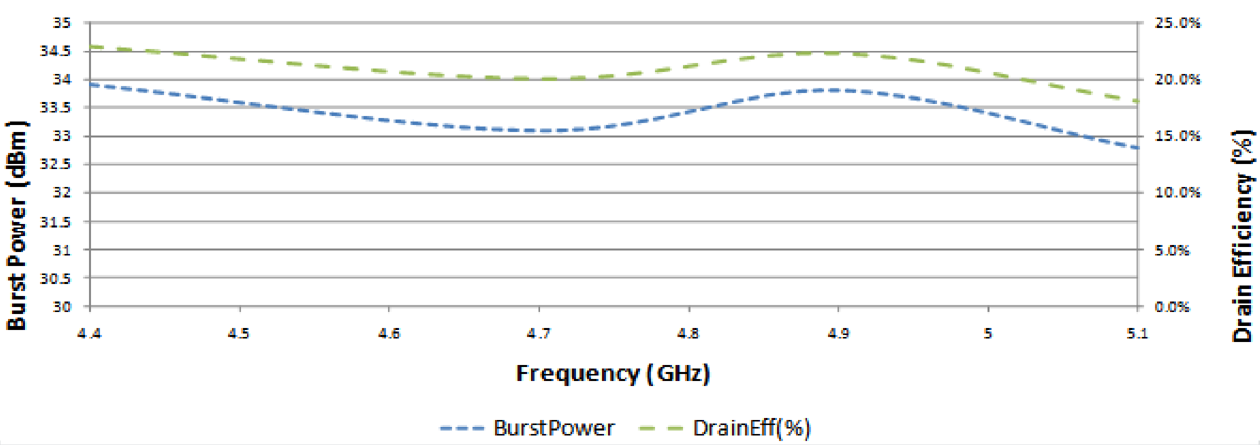


Pout @ LSG=9dB vs. Frequency vs. Sample



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
4.4 GHz	40.7	40.1	40.1	40.1	40.4	40	40.2	40.2	40	40	40	40	40	40	40	40.1	40
4.7 GHz	40.9	40.3	40.5	40.6	40.6	40.3	40.4	40.6	40.1	40.4	40.4	40.2	40.3	40.2	40.3	40.3	40.3
5.1 GHz	40.5	40.2	40.5	40.5	40.1	40.4	40.3	40.5	40.3	40.4	40.3	40.4	40.3	40.7	40.2	40.1	40.2

Burst Power @ 2.5% EVM, Drain Efficiency vs. Frequency



APPLICATION NOTE

The evaluation board material, shown in Figure 1, is Rogers 4003 material, 20 mil thick, and 2 oz copper weight and is used to evaluate the MGA444924-02 hardware. The 10 watt device in the '02' package has a limited temperature range of approximately 85°C. An earless flange or flange package is offered with better Tjc and can be used at much higher temperatures. Please consult the factory for your specific application. Through holes with a diameter of 20 mils are placed uniformly over the center pad for thermal relief and RF ground.

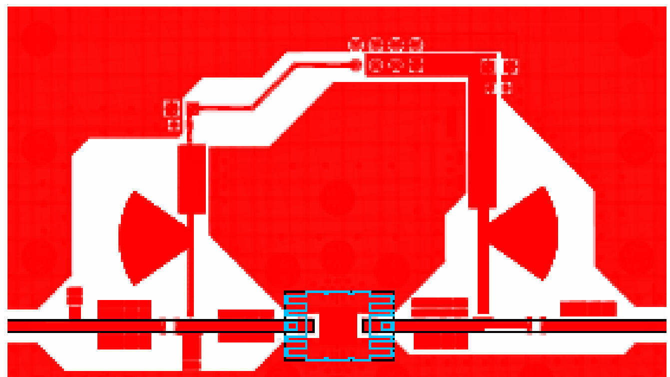


FIGURE 1 Evaluation Board

It is recommended that via holes be placed near the DC bias connector to maintain ground continuity between the top layer and bottom ground planes. Mounting holes near the unit will help secure the board to the chassis, minimize ground current loops and improve thermal conductivity in the absence of sweat soldering the board to the chassis. Biasing with quarter-wave stubs at the gate and drain are shown in Figure 1. The impedance of the quarter wave structures is cyclical with frequency. A RF short is observed at frequencies that are even multiples of quarter-wavelength and open impedance is observed at frequencies that are odd multiples of a quarter-wavelength. A 56 ohm resistor is added in series to the gate bias. The effective impedance is increased which reduces the risk of oscillations. The 56 ohm resistor is not shown in Figure 1. Through holes underneath the package is required to connect the top and bottom grounds and to improve thermal conductivity. The through holes can be back filled with conductive epoxy for best thermal performance. The MGA444940-02 has a noise figure less than 3.0 dB. A plot of noise figure versus frequency at Idq is shown in Figure 2. At small signal levels the amplifier operates at Idq. As the output power is increased the amplifier drive current will increase. A plot of Pout versus Pin shown in Figure 3 is plotted from 25 dBm to 40 dBm. The drain current Idd increases from 0.10 to 0.89 A. The RF drive level is increased incrementally and stopped when the gate leakage current of 10 mA is reached. The temperature performance for Pout vs Pin has a slope of -0.019 dB/!. A plot of Pout vs Pin at 4.7 GHz over a temperature range from 0 to 85! is shown in Figure 4.

The Burst power and ACPR data are shown in Figure 5. These measurements are recorded at EVM=2.5% across the frequency range at 4.4, 4.7, 4.9 and 5.1 GHz. A WPS44492202 amplifier is used as the drive stage and has a residual EVM error of less than 0.8%. The modulation is 802.16x and each frame cycle has a 10 msec duration and runs continuously. Equalization is enabled when measuring EVM performance. The MGA amplifier bias condition is Vdd=28V and the gate voltage is adjusted for an Idq=100 mA. A diagram of test setup is shown in Figure 7 and includes the frame information about the test pattern. As the output power is backed off from the peak performance, the amplifier changes its DC/RF operation from Class 'A' to Class 'A/B'. An example of this dynamic DC/RF operation can be obverse in EVM versus Burst Power performance shown in Figure 6. The EVM is optimal at 33 dBm but not at 25 dBm in which the output power is backed off and the amplifier's operating current to reduced 150 mA. At this bias condition the amplifier is back-off near pinch off.

Applications that require gating the amplifier for TDD applications can be supported using a constant current source with a command switch to disable current loop and turnoff the amplifier as shown in Figure 9. A 1% precision resistor R8 0.2 ohm is used to convert the current to voltage. Applying KVL principal around Q2 and Q3, the current through Q2 and the load current is 30 times defined by resistor network R4 over R8. As the load current is equalized, the gate voltage to the gate of the GaN is adjusted until the voltage at Q3 base and voltage at Q2 collector is balanced. A MOSFET M2 is used to enable and disable the loop. The loop bandwidth has been intentionally truncated to minimize the loop dynamics from attacking the envelope. This allows the bias current to increase as the Pout increases; this is shown in Figure 8.

APPLICATION NOTE CONTINUED

FIGURE 2
Noise Figure vs. Frequency

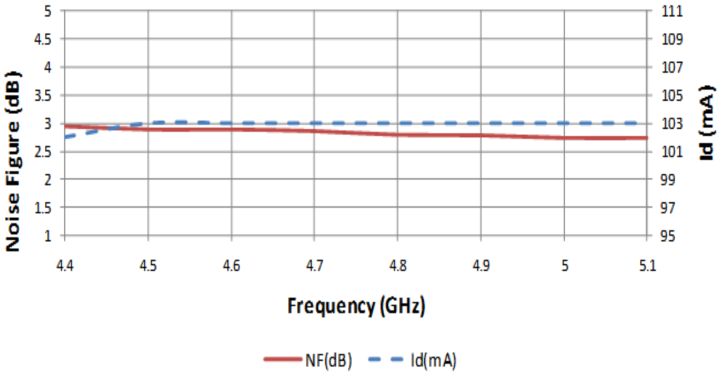


FIGURE 3
Supply Current vs. Pout (CW)

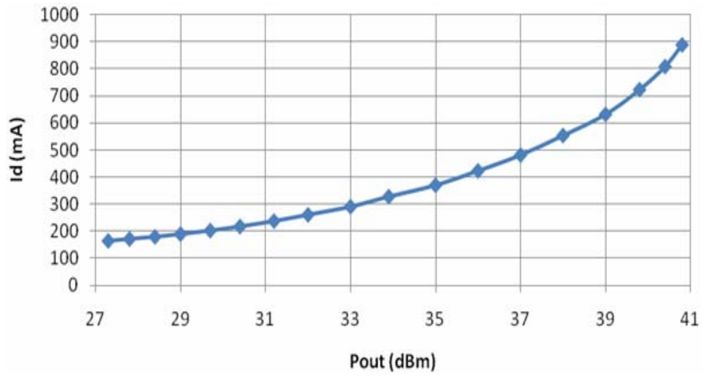


FIGURE 4
Pout vs. Pin over Temperature

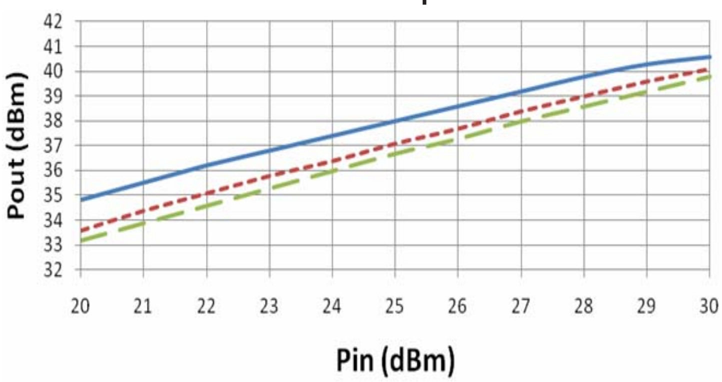


FIGURE 5
Burst Power and ACPR vs. Frequency

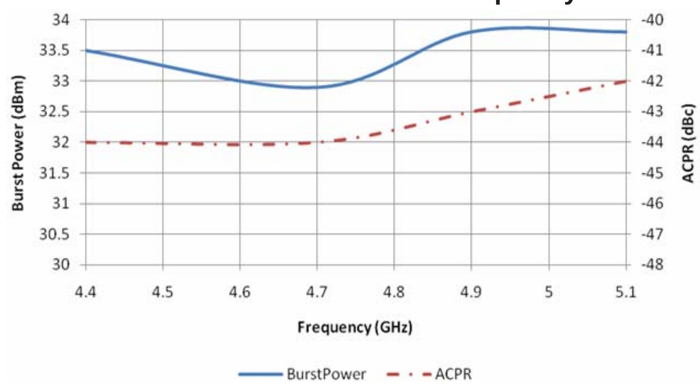
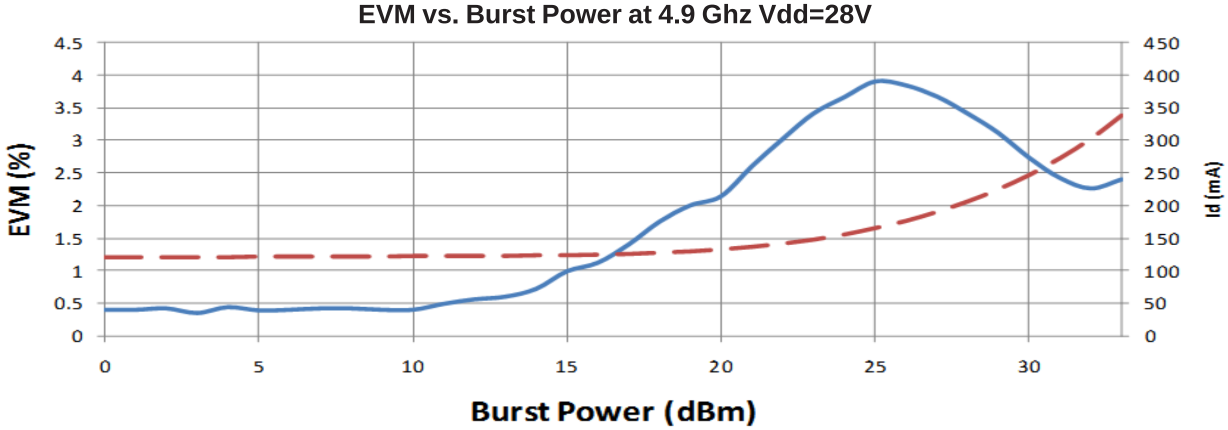


FIGURE 6
EVM vs. Burst Power at 4.9 Ghz Vdd=28V



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APPLICATION NOTE CONTINUED

FIGURE 7
Burst Power and ACPR Test Setup

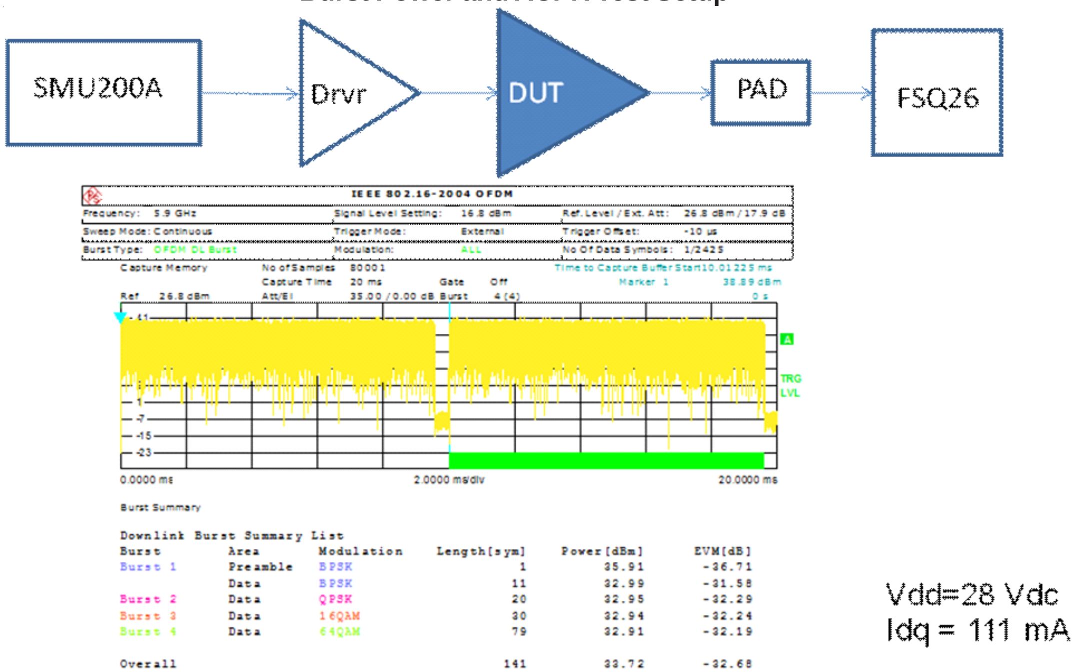
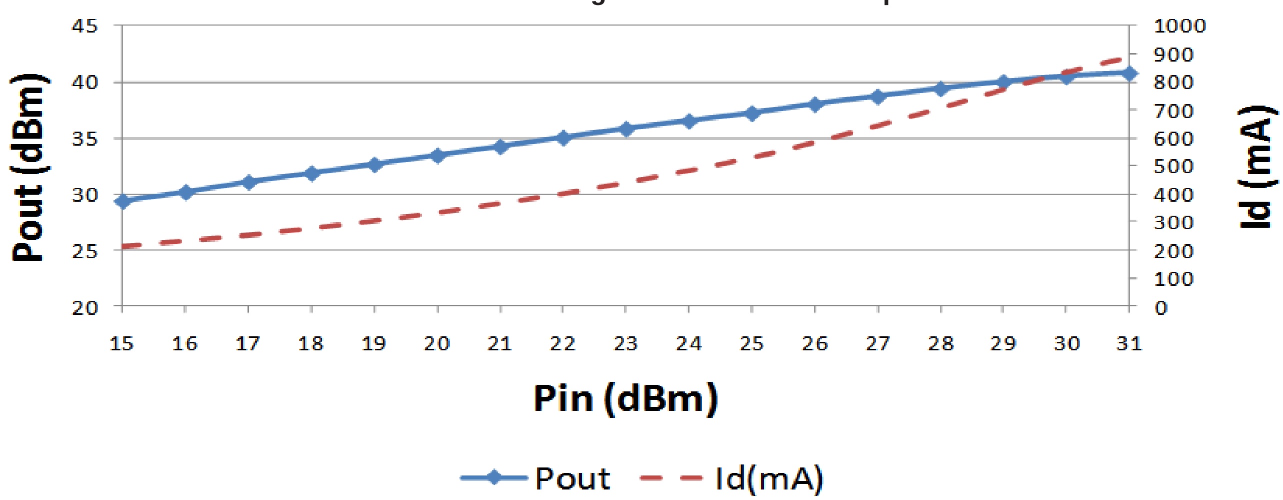
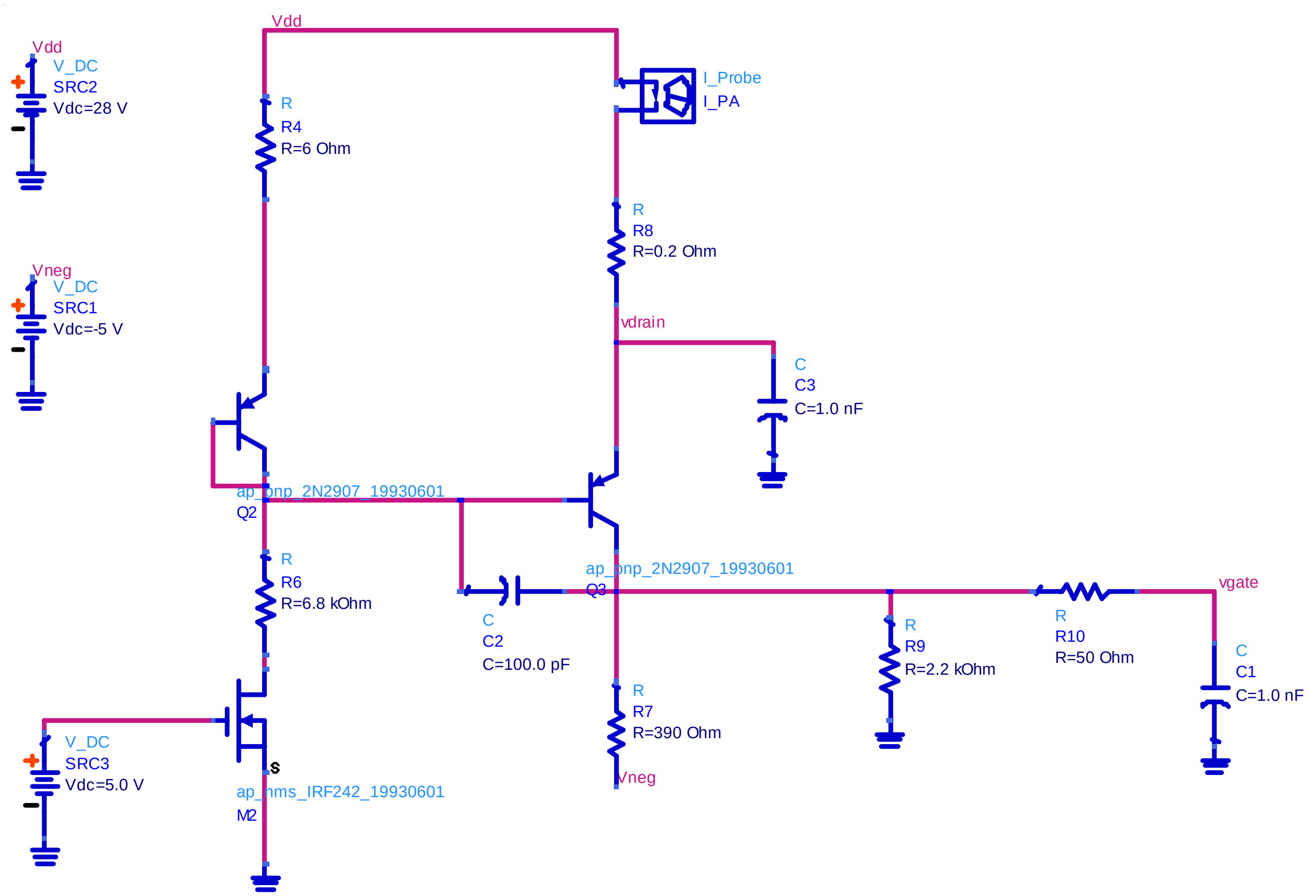


FIGURE 8
Pout vs. Pin Using Constant Current Loop



APPLICATION NOTE CONTINUED

FIGURE 9
Schematic of Constant Current Loop



TYPICAL SCATTERING PARAMETERS:

Vds=28V, Vgs=-3.0V, Idq=100mA, Ta=25C, Z0=50ohm

freq	magS11	AngS11	magS21	AngS21	magS12	AngS12	magS22	AngS22
4.000 GHz	0.476	-95.278	5.425	179.684	0.053	107.480	0.199	127.699
4.100 GHz	0.466	-114.659	5.255	165.042	0.052	91.188	0.128	122.925
4.200 GHz	0.452	-132.649	5.093	150.587	0.052	76.650	0.067	117.810
4.300 GHz	0.436	-150.169	4.957	136.380	0.052	62.494	0.015	90.628
4.400 GHz	0.422	-167.491	4.833	122.148	0.051	48.205	0.036	-58.814
4.500 GHz	0.410	175.635	4.738	107.515	0.052	34.343	0.084	-68.182
4.600 GHz	0.395	159.112	4.650	92.460	0.052	19.121	0.131	-77.156
4.700 GHz	0.375	144.029	4.545	76.604	0.052	3.774	0.181	-86.306
4.800 GHz	0.343	132.073	4.411	59.842	0.052	-13.017	0.232	-97.645
4.900 GHz	0.308	126.214	4.218	43.001	0.051	-29.577	0.285	-109.164
5.000 GHz	0.286	124.757	4.097	25.305	0.051	-46.874	0.352	-119.753
5.100 GHz	0.269	132.149	3.973	4.531	0.050	-68.273	0.447	-132.674
5.200 GHz	0.321	145.665	3.620	-19.383	0.046	-92.078	0.553	-148.263

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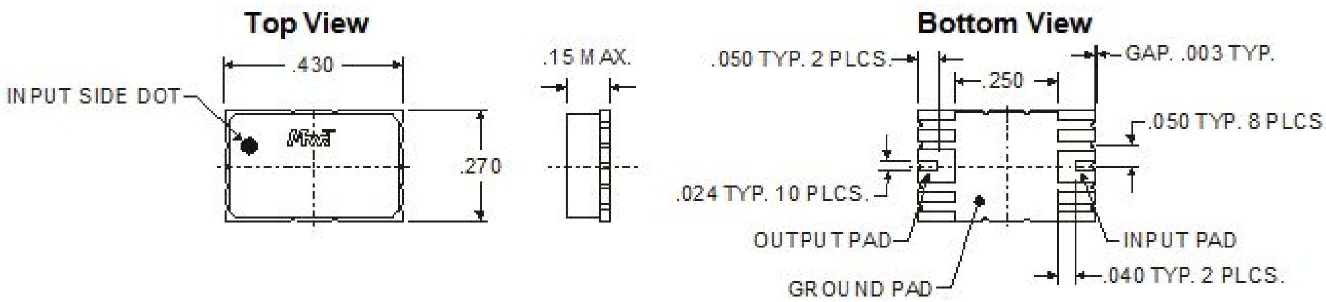
OUTLINE DRAWING



All dimensions are in inches

Pin Designation (Top View)			
Pin 1 (DOT Top Left)	GND	Pin 10	GND
Pin 2	GND	Pin 9	GND
Pin 3	RF In/Vg	Pin 8	RF Out/Vdd
Pin 4	GND	Pin 7	GND
Pin 5	GND	Pin 6	GND

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