PCA9957

24-channel SPI serial bus 32 mA/5.5 V constant current LED driver

Rev. 2.1 — 22 October 2021 **Product data sheet**

1 General description

The PCA9957 is a daisy-chain SPI-compatible 4-wire serial bus controlled 24-channel constant current LED driver optimized for dimming and blinking 32 mA Red/Green/Blue/Amber (RGBA) LEDs.

Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 100 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to once every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCA9957 operates with a supply voltage range of 2.7 V to 5.5 V and the constant current sink LED outputs allow up to 5 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 125 μA to 31.875 mA with REXT = 2 kΩ.

Gradation control for all current sources is achieved via the 4-wire serial bus interface and allows user to ramp current automatically without MCU intervention. 8-bit DACs are available to adjust brightness levels for each LED current source. There are six selectable gradation control groups and each group has four independent registers to control ramp-up and ramp-down rate, step time, hold ON/OFF time and final hold ON output current. Two gradation operation modes are available for each group: single shot mode (output pattern once) and continuous mode (output pattern repeat). Each channel can be set to either gradation mode or normal mode and assigned to any one of these six gradation control groups.

This device has built-in open, short load and overtemperature detection circuitry. The error information from the corresponding register can be read via the 4-wire serial bus. Additionally, a thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCA9957 device is designed to use 4-wire read/write serial bus with higher data clock frequency (up to 10 MHz).

The active LOW output enable input pin ($\overline{\text{OE}}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

2 Features and benefits

- 24 LED drivers. Each output programmable at:
  - Off
  - On
  - 8 bits programmable LED brightness
  - 8 bits programmable group dimming/blinking mixed with individual LED brightness
  - Programmable LED output delay to reduce EMI and surge currents
- Gradation control for all channels
  - Each channel can be assigned to one of six gradation control groups
  - Programmable gradation time and rate for ramp-up and/or ramp-down operations
  - Programmable step time (6-bit) from 0.5 ms (minimum) to 512 ms (maximum)
  - Programmable hold-on time after ramp-up and hold-off time after ramp-down (3-bit) from 0 s to 6 s
  - Programmable final ramp-up and hold-on current
  - Programmable brightness current output adjustment, either linear or exponential curve
- 24 constant current output channels can sink up to 32 mA, and tolerate up to 5.5 V when OFF
- Output current adjusted through an external resistor (REXT input)
- Output current accuracy
  - ±6.5 % absolute accuracy with 30 mA output current
  - Maximum ±4 % channel to channel variation
  - Maximum ±6 % device to device variation
- Open/short load/overtemperature detection mode to detect individual LED errors
- 4-wire serial bus interface with 10 MHz data clock rate
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness fully ON using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- No glitch on LEDn outputs on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 2.7 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- -40 °C to +85 °C operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds per JESD22:
  - 2 kV Human-Body Model (A114-A)
  - 1 kV Charged-Device Model (C101)
- Package offered: HVQFN40

3 Applications

- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices
- Fade-in and fade-out for breathlight control

4 Ordering information

Table 1. Ordering information

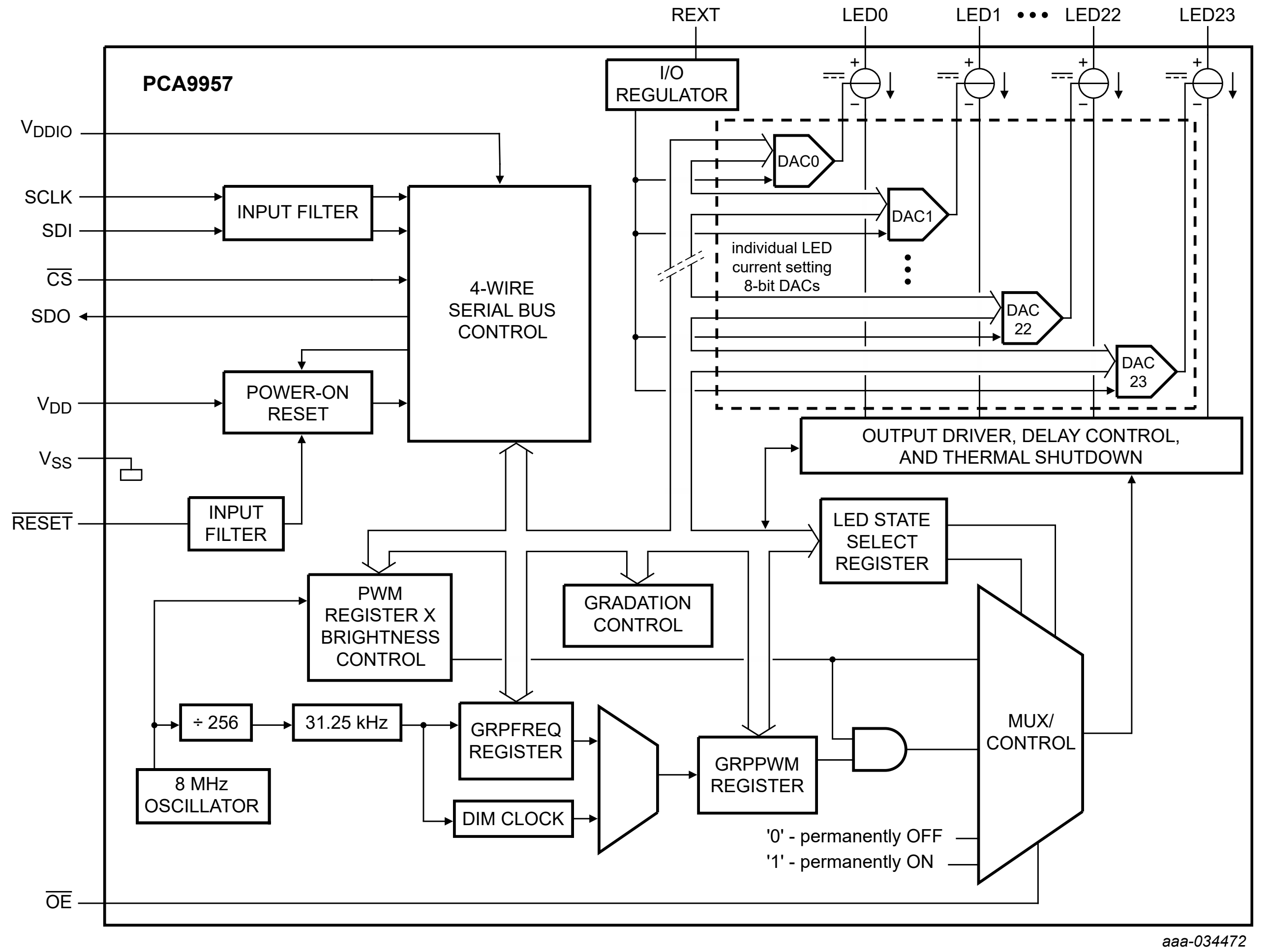
Type number	Topside mark	Package		
		Name	Description	Version
PCA9957HN	P9957	HVQFN40	Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 5 x 5 x 0.85 mm	SOT1369-5

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9957HN	PCA9957HNMP	HVQFN40	Reel 13" Q2/T3 DP	6000	T_{amb} = -40 °C to +85 °C

5 Block diagram


REXT
LED0
LED1
LED22
LED23
PCA9957
I/O REGULATOR
VDDIO
SCLK
SDI
CS
SDO
INPUT FILTER
4-WIRE SERIAL BUS CONTROL
DAC0
DAC1
individual LED current setting 8-bit DACs
DAC 22
DAC 23
VDD
POWER-ON RESET
VSS
RESET
INPUT FILTER
OUTPUT DRIVER, DELAY CONTROL, AND THERMAL SHUTDOWN
LED STATE SELECT REGISTER
PWM REGISTER X BRIGHTNESS CONTROL
GRADATION CONTROL
MUX/ CONTROL
÷ 256
31.25 kHz
GRPFREQ REGISTER
GRPPWM REGISTER
8 MHz OSCILLATOR
DIM CLOCK
'0' - permanently OFF
'1' - permanently ON
OE
aaa-034472

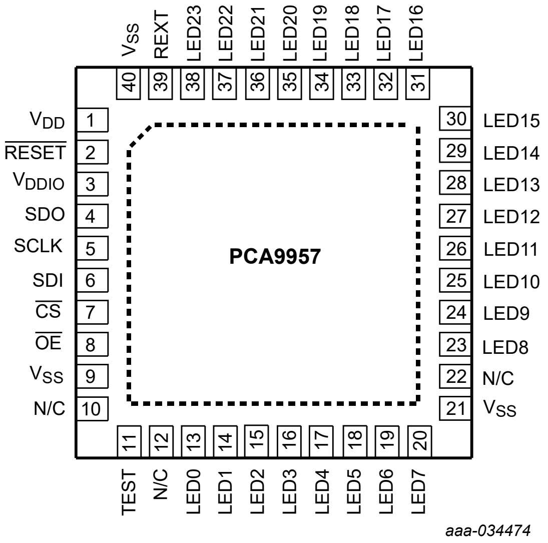
Dim repetition rate = 122 Hz

Blink repetition rate = 15 Hz to every 16.8 seconds

Figure 1. Block diagram of PCA9957

6 Pinning information

6.1 Pinning


VSS
REXT
LED23
LED22
LED21
LED20
LED19
LED18
LED17
LED16
40 39 38 37 36 35 34 33 32 31
VDD 1
RESET 2
VDDIO 3
SDO 4
SCLK 5
SDI 6
CS 7
OE 8
VSS 9
N/C 10
30 LED15
29 LED14
28 LED13
27 LED12
26 LED11
25 LED10
24 LED9
23 LED8
22 N/C
21 VSS
PCA9957
11 12 13 14 15 16 17 18 19 20
TEST
N/C
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
aaa-034474

1. Thermal pad; connected to V_{SS}.

Figure 2. Pin configuration for HVQFN40

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
REXT	39	I	current set resistor input; resistor to ground
SDO	4	O	serial data output
$\overline{CS}$	7	I	active LOW chip select - when held HIGH the SDO pin is held LOW
$\overline{OE}$	8	I	active LOW output enable for LEDs
LED0	13	O	LED driver 0
LED1	14	O	LED driver 1
LED2	15	O	LED driver 2
LED3	16	O	LED driver 3
LED4	17	O	LED driver 4
LED5	18	O	LED driver 5
LED6	19	O	LED driver 6
LED7	20	O	LED driver 7
LED8	23	O	LED driver 8
LED9	24	O	LED driver 9
LED10	25	O	LED driver 10
LED11	26	O	LED driver 11

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
LED12	27	O	LED driver 12
LED13	28	O	LED driver 13
LED14	29	O	LED driver 14
LED15	30	O	LED driver 15
LED16	31	O	LED driver 16
LED17	32	O	LED driver 17
LED18	33	O	LED driver 18
LED19	34	O	LED driver 19
LED20	35	O	LED driver 20
LED21	36	O	LED driver 21
LED22	37	O	LED driver 22
LED23	38	O	LED driver 23
$\overline{\text{RESET}}$	2	I	active LOW reset input with external 10 kΩ pull-up resistor
SCLK	5	I	serial clock line
SDI	6	I	serial data input
V_{SS}	9, 21, 40 [1]	ground	supply ground
V_{DDIO}	3	power supply	supply rail of SPI interface
V_{DD}	1	power supply	supply voltage
N/C	10, 12, 22	N/A	no connection
TEST	11	factory test	internal pull down - connect to GND or leave floating

[1] HVQFN40 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7 Functional description

Refer to Figure 1.

7.1 Register address and data

Following a chip select ($\overline{\text{CS}}$) asserted condition (from HIGH to LOW), the data transfers are (16 × n) bits wide (where ‘n’ is the number of slaves in the chain) with MSB transferred first. The first 7 bits are the address of the register to be accessed. The eighth bit indicates the types of access — read (= 1) or write (= 0). The second group of 8 bits consists of data as shown in Figure 3.

See Section 8 for more detail.

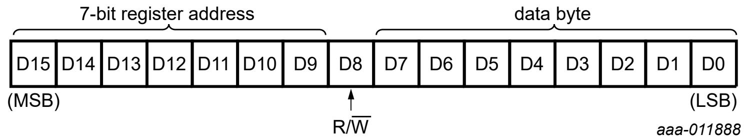


Figure 3. Register address and data format for each slave

7.2 Register definitions

Table 4. Register summary - default values

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	0	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	0	0	0	0	0	0	EFLAG0	read only	output error flag 0
03h	0	0	0	0	0	0	0	0	EFLAG1	read only	output error flag 1
04h	0	0	0	0	0	0	0	0	EFLAG2	read only	output error flag 2
05h	0	0	0	0	0	0	0	0	EFLAG3	read only	output error flag 3
06h	0	0	0	0	0	0	0	0	EFLAG4	read only	output error flag 4
07h	0	0	0	0	0	0	0	0	EFLAG5	read only	output error flag 5
08h	1	0	1	0	1	0	1	0	LEDOUT0	read/write	LED output state 0
09h	1	0	1	0	1	0	1	0	LEDOUT1	read/write	LED output state 1
0Ah	1	0	1	0	1	0	1	0	LEDOUT2	read/write	LED output state 2
0Bh	1	0	1	0	1	0	1	0	LEDOUT3	read/write	LED output state 3
0Ch	1	0	1	0	1	0	1	0	LEDOUT4	read/write	LED output state 4
0Dh	1	0	1	0	1	0	1	0	LEDOUT5	read/write	LED output state 5
0Eh	1	1	1	1	1	1	1	1	GRPPWM	read/write	group duty cycle control
0Fh	0	0	0	0	0	0	0	0	GRPFREQ	read/write	group frequency
10h	0	0	0	0	0	0	0	0	PWM0	read/write	brightness control LED0
11h	0	0	0	0	0	0	0	0	PWM1	read/write	brightness control LED1
12h	0	0	0	0	0	0	0	0	PWM2	read/write	brightness control LED2
13h	0	0	0	0	0	0	0	0	PWM3	read/write	brightness control LED3
14h	0	0	0	0	0	0	0	0	PWM4	read/write	brightness control LED4
15h	0	0	0	0	0	0	0	0	PWM5	read/write	brightness control LED5
16h	0	0	0	0	0	0	0	0	PWM6	read/write	brightness control LED6
17h	0	0	0	0	0	0	0	0	PWM7	read/write	brightness control LED7
18h	0	0	0	0	0	0	0	0	PWM8	read/write	brightness control LED8
19h	0	0	0	0	0	0	0	0	PWM9	read/write	brightness control LED9
1Ah	0	0	0	0	0	0	0	0	PWM10	read/write	brightness control LED10
1Bh	0	0	0	0	0	0	0	0	PWM11	read/write	brightness control LED11
1Ch	0	0	0	0	0	0	0	0	PWM12	read/write	brightness control LED12

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
1Dh	0	0	0	0	0	0	0	0	PWM13	read/write	brightness control LED13
1Eh	0	0	0	0	0	0	0	0	PWM14	read/write	brightness control LED14
1Fh	0	0	0	0	0	0	0	0	PWM15	read/write	brightness control LED15
20h	0	0	0	0	0	0	0	0	PWM16	read/write	brightness control LED16
21h	0	0	0	0	0	0	0	0	PWM17	read/write	brightness control LED17
22h	0	0	0	0	0	0	0	0	PWM18	read/write	brightness control LED18
23h	0	0	0	0	0	0	0	0	PWM19	read/write	brightness control LED19
24h	0	0	0	0	0	0	0	0	PWM20	read/write	brightness control LED20
25h	0	0	0	0	0	0	0	0	PWM21	read/write	brightness control LED21
26h	0	0	0	0	0	0	0	0	PWM22	read/write	brightness control LED22
27h	0	0	0	0	0	0	0	0	PWM23	read/write	brightness control LED23
28h	0	0	0	0	0	0	0	0	IREF0	read/write	output gain control register 0
29h	0	0	0	0	0	0	0	0	IREF1	read/write	output gain control register 1
2Ah	0	0	0	0	0	0	0	0	IREF2	read/write	output gain control register 2
2Bh	0	0	0	0	0	0	0	0	IREF3	read/write	output gain control register 3
2Ch	0	0	0	0	0	0	0	0	IREF4	read/write	output gain control register 4
2Dh	0	0	0	0	0	0	0	0	IREF5	read/write	output gain control register 5
2Eh	0	0	0	0	0	0	0	0	IREF6	read/write	output gain control register 6
2Fh	0	0	0	0	0	0	0	0	IREF7	read/write	output gain control register 7
30h	0	0	0	0	0	0	0	0	IREF8	read/write	output gain control register 8
31h	0	0	0	0	0	0	0	0	IREF9	read/write	output gain control register 9
32h	0	0	0	0	0	0	0	0	IREF10	read/write	output gain control register 10
33h	0	0	0	0	0	0	0	0	IREF11	read/write	output gain control register 11
34h	0	0	0	0	0	0	0	0	IREF12	read/write	output gain control register 12
35h	0	0	0	0	0	0	0	0	IREF13	read/write	output gain control register 13
36h	0	0	0	0	0	0	0	0	IREF14	read/write	output gain control register 14
37h	0	0	0	0	0	0	0	0	IREF15	read/write	output gain control register 15
38h	0	0	0	0	0	0	0	0	IREF16	read/write	output gain control register 16
39h	0	0	0	0	0	0	0	0	IREF17	read/write	output gain control register 17
3Ah	0	0	0	0	0	0	0	0	IREF18	read/write	output gain control register 18
3Bh	0	0	0	0	0	0	0	0	IREF19	read/write	output gain control register 19
3Ch	0	0	0	0	0	0	0	0	IREF20	read/write	output gain control register 20
3Dh	0	0	0	0	0	0	0	0	IREF21	read/write	output gain control register 21
3Eh	0	0	0	0	0	0	0	0	IREF22	read/write	output gain control register 22
3Fh	0	0	0	0	0	0	0	0	IREF23	read/write	output gain control register 23

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
40h	0	0	0	0	0	0	0	0	RAMP_RATE_GRP0	read/write	ramp enable and rate control for group 0
41h	0	0	0	0	0	0	0	0	STEP_TIME_GRP0	read/write	step time control for group 0
42h	0	0	0	0	0	0	0	0	HOLD_CNTL_GRP0	read/write	hold ON/OFF time control for group 0
43h	0	0	0	0	0	0	0	0	IREF_GRP0	read/write	output gain control for group 0
44h	0	0	0	0	0	0	0	0	RAMP_RATE_GRP1	read/write	ramp enable and rate control for group 1
45h	0	0	0	0	0	0	0	0	STEP_TIME_GRP1	read/write	step time control for group 1
46h	0	0	0	0	0	0	0	0	HOLD_CNTL_GRP1	read/write	hold ON/OFF time control for group 1
47h	0	0	0	0	0	0	0	0	IREF_GRP1	read/write	output gain control for group 1
48h	0	0	0	0	0	0	0	0	RAMP_RATE_GRP2	read/write	ramp enable and rate control for group 2
49h	0	0	0	0	0	0	0	0	STEP_TIME_GRP2	read/write	step time control for group 2
4Ah	0	0	0	0	0	0	0	0	HOLD_CNTL_GRP2	read/write	hold ON/OFF time control for group 2
4Bh	0	0	0	0	0	0	0	0	IREF_GRP2	read/write	output gain control for group 2
4Ch	0	0	0	0	0	0	0	0	RAMP_RATE_GRP3	read/write	ramp enable and rate control for group 3
4Dh	0	0	0	0	0	0	0	0	STEP_TIME_GRP3	read/write	step time control for group 3
4Eh	0	0	0	0	0	0	0	0	HOLD_CNTL_GRP3	read/write	hold ON/OFF time control for group 3
4Fh	0	0	0	0	0	0	0	0	IREF_GRP3	read/write	output gain control for group 3
50h	0	0	0	0	0	0	0	0	RAMP_RATE_GRP4	read/write	ramp enable and rate control for group 4
51h	0	0	0	0	0	0	0	0	STEP_TIME_GRP4	read/write	step time control for group 4
52h	0	0	0	0	0	0	0	0	HOLD_CNTL_GRP4	read/write	hold ON/OFF time control for group 4
53h	0	0	0	0	0	0	0	0	IREF_GRP4	read/write	output gain control for group 4
54h	0	0	0	0	0	0	0	0	RAMP_RATE_GRP5	read/write	ramp enable and rate control for group 5
55h	0	0	0	0	0	0	0	0	STEP_TIME_GRP5	read/write	step time control for group 5
56h	0	0	0	0	0	0	0	0	HOLD_CNTL_GRP5	read/write	hold ON/OFF time control for group 5
57h	0	0	0	0	0	0	0	0	IREF_GRP5	read/write	output gain control for group 5
58h	0	0	0	0	0	0	0	0	GRAD_MODE_SEL0	read/write	gradation mode select register for channel 7 to channel 0
59h	0	0	0	0	0	0	0	0	GRAD_MODE_SEL1	read/write	gradation mode select register for channel 15 to channel 8

Table 4. Register summary - default values*...continued*

Register # (hex)	D7	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
5Ah	0	0	0	0	0	0	0	0	GRAD_MODE_SEL2	read/write	gradation mode select register for channel 23 to channel 16
5Bh	0	0	0	0	0	0	0	0	GRAD_GRP_SEL0	read/write	gradation group select for channel 1 to channel 0
5Ch	0	0	0	0	0	0	0	0	GRAD_GRP_SEL1	read/write	gradation group select for channel 3 to channel 2
5Dh	0	0	0	1	0	0	0	1	GRAD_GRP_SEL2	read/write	gradation group select for channel 5 to channel 4
5Eh	0	0	0	1	0	0	0	1	GRAD_GRP_SEL3	read/write	gradation group select for channel 7 to channel 6
5Fh	0	0	1	0	0	0	1	0	GRAD_GRP_SEL4	read/write	gradation group select for channel 9 to channel 8
60h	0	0	1	0	0	0	1	0	GRAD_GRP_SEL5	read/write	gradation group select for channel 11 to channel 10
61h	0	0	1	1	0	0	1	1	GRAD_GRP_SEL6	read/write	gradation group select for channel 13 to channel 12
62h	0	0	1	1	0	0	1	1	GRAD_GRP_SEL7	read/write	gradation group select for channel 15 to channel 14
63h	0	1	0	0	0	1	0	0	GRAD_GRP_SEL8	read/write	gradation group select for channel 17 to channel 16
64h	0	1	0	0	0	1	0	0	GRAD_GRP_SEL9	read/write	gradation group select for channel 19 to channel 18
65h	0	1	0	1	0	1	0	1	GRAD_GRP_SEL10	read/write	gradation group select for channel 21 to channel 20
66h	0	1	0	1	0	1	0	1	GRAD_GRP_SEL11	read/write	gradation group select for channel 23 to channel 22
67h	0	0	0	0	0	0	0	0	GRAD_CNTL0	read/write	gradation control register for group 3 to group 0
68h	0	0	0	0	0	0	0	0	GRAD_CNTL1	read/write	gradation control register for group 5 to group 4
69h	0	0	0	0	1	0	0	0	OFFSET	read/write	Offset/delay on LEDn outputs
6Ah	0	0	0	0	0	0	0	0	PWMALL	write only	brightness control for all LEDn
6Bh	0	0	0	0	0	0	0	0	IREFALL	write only	output gain control for all registers IREF0 to IREF23
6Ch									reserved[1]	read only	not used
to	:	:	:	:	:	:	:	:			
7Fh											

[1] Reserved registers should not be written to - default is 0

7.2.1 MODE1 — Mode register 1

Table 5. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	R/W	0*	reserved
5	-	R/W	0*	reserved
4	SLEEP	R/W	0*	Normal mode[1].
			1	Low-power mode. Oscillator off[2][3].
3	-	R/W	0*	reserved
2	-	R/W	0*	reserved
1	-	R/W	0*	reserved
0	-	R/W	0*	reserved

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2] No blinking, dimming or gradation control is possible when the oscillator is off.

[3] The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

7.2.2 MODE2 — Mode register 2

Table 6. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	OVERTEMP	read only	0*	O.K.
			1	overtemperature condition
6	ERROR	read only	0*	no error at LED outputs
			1	any open or short-circuit detected in error flag registers (EFLAGn)
5	DMBLNK	R/W	0*	group control = dimming
			1	group control = blinking
4	CLRERR	write only	0*	self clear after write ‘1’
			1	Write ‘1’ to clear all error status bits in EFLAGn register and ERROR (bit 6). The EFLAGn and ERROR bit will set to ‘1’ if open or short-circuit is detected again.
3	AUTO_ SWITCHOFF_ DIS	R/W	0*	Disable the channel for which open or short error is detected and enable it again when write 1 to CLRERR, clears all error status bits in EFLAGn registers and ERROR bit
			1	The channel won’t be turned off when open/short detected
2	EXP_EN	R/W	0*	linear adjustment for gradation control
			1	exponential adjustment for gradation control

Table 6. MODE2 - Mode register 2 (address 01h) bit description*...continued*

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
1	-	read only	0*	reserved
0	-	read only	1*	reserved

Brightness adjustment for gradation control is either linear or exponential by setting the EXP_EN bit as shown in Figure 4. When EXP_EN = 0, linear adjustment scale is used. When EXP_EN = 1, exponential scale is used.

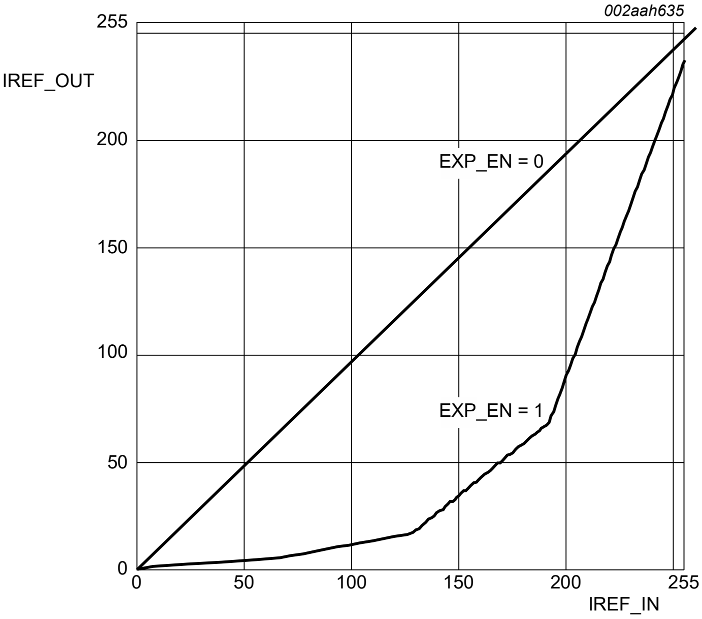


Figure 4. Linear and exponential adjustment curves

7.2.3 LEDOUT0 to LEDOUT5, LED driver output state

Table 7. LEDOUT0 to LEDOUT5 - LED driver output state registers (address 08h to 0Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	LEDOUT0	7:6	LDR3	R/W	10*	LED3 output state control
		5:4	LDR2	R/W	10*	LED2 output state control
		3:2	LDR1	R/W	10*	LED1 output state control
		1:0	LDR0	R/W	10*	LED0 output state control
09h	LEDOUT1	7:6	LDR7	R/W	10*	LED7 output state control
		5:4	LDR6	R/W	10*	LED6 output state control
		3:2	LDR5	R/W	10*	LED5 output state control
		1:0	LDR4	R/W	10*	LED4 output state control
0Ah	LEDOUT2	7:6	LDR11	R/W	10*	LED11 output state control

Table 7. LEDOUT0 to LEDOUT5 - LED driver output state registers (address 08h to 0Dh) bit description*...continued*

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
		5:4	LDR10	R/W	10*	LED10 output state control
		3:2	LDR9	R/W	10*	LED9 output state control
		1:0	LDR8	R/W	10*	LED8 output state control
0Bh	LEDOUT3	7:6	LDR15	R/W	10*	LED15 output state control
		5:4	LDR14	R/W	10*	LED14 output state control
		3:2	LDR13	R/W	10*	LED13 output state control
		1:0	LDR12	R/W	10*	LED12 output state control
0Ch	LEDOUT4	7:6	LDR19	R/W	10*	LED19 output state control
		5:4	LDR18	R/W	10*	LED18 output state control
		3:2	LDR17	R/W	10*	LED17 output state control
		1:0	LDR16	R/W	10*	LED16 output state control
0Dh	LEDOUT5	7:6	LDR23	R/W	10*	LED23 output state control
		5:4	LDR22	R/W	10*	LED22 output state control
		3:2	LDR21	R/W	10*	LED21 output state control
		1:0	LDR20	R/W	10*	LED20 output state control

LDRx = 00

LED driver x is off (x = 0 to 23).

LDRx = 01

LED driver x is fully on (individual brightness and group dimming/blinking not controlled). The $\overline{\text{OE}}$ pin can be used as external dimming/blinking control in this state.

LDRx = 10

LED driver x individual brightness can be controlled through its PWMx register (default power-up state) or PWMALL register for all LEDn outputs.

LDRx = 11

LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

Remark: Setting the device in low power mode while being on group dimming/blinking mode (LDRx = 11) may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

7.2.4 GRPPWM, group duty cycle control

Table 8. GRPPWM - Group brightness control register (address 0Eh) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
0Eh	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 24 outputs is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$dutycycle = \frac{GDC[7:0]}{256} \quad (1)$$

7.2.5 GRPFREQ, group frequency

Table 9. GRPFREQ - Group frequency register (address 0Fh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Fh	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a ‘Don’t care’ when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$globalblinkingperiod = \frac{GFRQ[7:0]+1}{15.26}\ (s) \quad (2)$$

7.2.6 PWM0 to PWM23, individual brightness control

Table 10. PWM0 to PWM23 - PWM registers 0 to 23 (address 10h to 27h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
10h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
11h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
12h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle

Table 10. PWM0 to PWM23 - PWM registers 0 to 23 (address 10h to 27h) bit description*...continued*

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
13h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
14h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
15h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
16h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
17h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle
18h	PWM8	7:0	IDC8[7:0]	R/W	0000 0000*	PWM8 Individual Duty Cycle
19h	PWM9	7:0	IDC9[7:0]	R/W	0000 0000*	PWM9 Individual Duty Cycle
1Ah	PWM10	7:0	IDC10[7:0]	R/W	0000 0000*	PWM10 Individual Duty Cycle
1Bh	PWM11	7:0	IDC11[7:0]	R/W	0000 0000*	PWM11 Individual Duty Cycle
1Ch	PWM12	7:0	IDC12[7:0]	R/W	0000 0000*	PWM12 Individual Duty Cycle
1Dh	PWM13	7:0	IDC13[7:0]	R/W	0000 0000*	PWM13 Individual Duty Cycle
1Eh	PWM14	7:0	IDC14[7:0]	R/W	0000 0000*	PWM14 Individual Duty Cycle
1Fh	PWM15	7:0	IDC15[7:0]	R/W	0000 0000*	PWM15 Individual Duty Cycle
20h	PWM16	7:0	IDC8[7:0]	R/W	0000 0000*	PWM16 Individual Duty Cycle
21h	PWM17	7:0	IDC9[7:0]	R/W	0000 0000*	PWM17 Individual Duty Cycle
22h	PWM18	7:0	IDC10[7:0]	R/W	0000 0000*	PWM18 Individual Duty Cycle
23h	PWM19	7:0	IDC11[7:0]	R/W	0000 0000*	PWM19 Individual Duty Cycle
24h	PWM20	7:0	IDC12[7:0]	R/W	0000 0000*	PWM20 Individual Duty Cycle
25h	PWM21	7:0	IDC13[7:0]	R/W	0000 0000*	PWM21 Individual Duty Cycle
26h	PWM22	7:0	IDC14[7:0]	R/W	0000 0000*	PWM22 Individual Duty Cycle
27h	PWM23	7:0	IDC15[7:0]	R/W	0000 0000*	PWM23 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FEh (99.2 % duty cycle = LED output at maximum brightness) and FFh (100 % duty cycle = LED output completed ON). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$dutycycle = \frac{IDCx[7:0]}{256} \quad (3)$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM will not have effective brightness control of LEDs due to edge rate control of LED output pins.

7.2.7 IREF0 to IREF23, LED output current value registers

These registers reflect the gain settings for output current for LED0 to LED23.

Table 11. IREF0 to IREF23 - LED output gain control registers (address 28h to 3Fh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
28h	IREF0	7:0	R/W	00h*	LED0 output current setting
29h	IREF1	7:0	R/W	00h*	LED1 output current setting
2Ah	IREF2	7:0	R/W	00h*	LED2 output current setting
2Bh	IREF3	7:0	R/W	00h*	LED3 output current setting
2Ch	IREF4	7:0	R/W	00h*	LED4 output current setting
2Dh	IREF5	7:0	R/W	00h*	LED5 output current setting
2Eh	IREF6	7:0	R/W	00h*	LED6 output current setting
2Fh	IREF7	7:0	R/W	00h*	LED7 output current setting
30h	IREF8	7:0	R/W	00h*	LED8 output current setting
31h	IREF9	7:0	R/W	00h*	LED9 output current setting
32h	IREF10	7:0	R/W	00h*	LED10 output current setting
33h	IREF11	7:0	R/W	00h*	LED11 output current setting
34h	IREF12	7:0	R/W	00h*	LED12 output current setting
35h	IREF13	7:0	R/W	00h*	LED13 output current setting
36h	IREF14	7:0	R/W	00h*	LED14 output current setting
37h	IREF15	7:0	R/W	00h*	LED15 output current setting
38h	IREF16	7:0	R/W	00h*	LED16 output current setting
39h	IREF17	7:0	R/W	00h*	LED17 output current setting
3Ah	IREF18	7:0	R/W	00h*	LED18 output current setting
3Bh	IREF19	7:0	R/W	00h*	LED19 output current setting
3Ch	IREF20	7:0	R/W	00h*	LED20 output current setting
3Dh	IREF21	7:0	R/W	00h*	LED21 output current setting
3Eh	IREF22	7:0	R/W	00h*	LED22 output current setting
3Fh	IREF23	7:0	R/W	00h*	LED23 output current setting

7.2.8 Gradation control

Gradation control is designed to use six independent groups of registers to program the full cycle of the gradation timing to implement on each selected channel. Each group has four registers to define the ramp rate, step time, hold ON/OFF time, and final hold ON current, as shown in Figure 5.

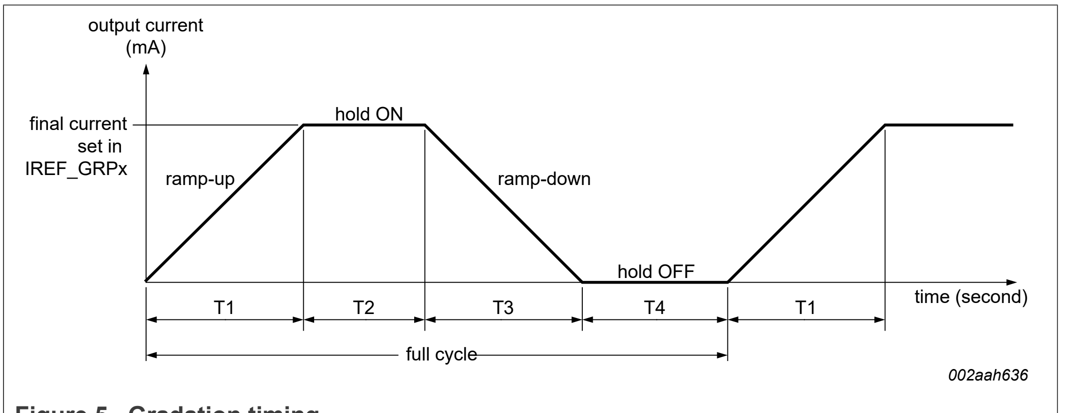


Figure 5. Gradation timing

- The ‘final’ and ‘hold ON’ current is defined in IREF_GRPx register value × (125 μA if REXT = 2 kΩ).
- Ramp rate value and enable/disable ramp operation is defined in RAMP_RATE_GRPx register.
- Total number of ramp steps (or level changes) is calculated as ‘IREF_GRPx value’ ÷ ‘ramp rate value in RAMP_RATE_GRPx’. Rounds a number up to the next integer if the total number is not an integer.
- Time for each step is calculated as ‘cycle time’ × ‘multiple factor’ bits in STEP_TIME_GRPx register. Minimum time for one step is 0.5 ms (0.5 ms × 1) and maximum time is 512 ms (8 ms × 64).
- The ramp-up or ramp-down time (T1 or T3) is calculated as ‘(total steps + 1)’ × ‘step time’.
- Hold ON or OFF time (T2 or T4) is defined in HOLD_CNTL_GRPx register in the range of 0/0.25/0.5/0.75/1/2/4/6 seconds.
- Gradation start or stop with single shot mode (one full cycle only) or continuous mode (repeat full cycle) is defined in the GRAD_CNTL register for all groups.
- Each channel can be assigned to one of these six groups in the GRAD_GRP_SELx register.
- Each channel can set either normal mode or gradation mode operation in the GRAD_MODE_SELx register.

To enable the gradation operation, the following steps are required:

1. Program all gradation control registers except the gradation start bit in GRAD_CNTL register.
2. Program either LDRx = 01 (LED fully ON mode) only, or LDRx = 10 or 11 (PWM control mode) with individual brightness control PWMx register for duty cycle.
3. Program output current value IREFx register to non-zero, which enables LED output.
4. Set the gradation start bit in GRAD_CNTL register for enabling gradation operation.

7.2.8.1 RAMP_RATE_GRP0 to RAMP_RATE_GRP5, ramp rate control registers

Table 12. RAMP_RATE_GRP[0:3] - Ramp enable and rate control registers (address 40h, 44h, 48h, 4Ch, 50h, 54h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
40h 44h 48h 4Ch 50h 54h	RAMP_RATE_GRP0 RAMP_RATE_GRP1 RAMP_RATE_GRP2 RAMP_RATE_GRP3 RAMP_RATE_GRP4 RAMP_RATE_GRP5	7	R/W	0*	Ramp-up disable
				1	Ramp-up enable
		6	R/W	0*	Ramp-down disable
				1	Ramp-down enable
		5:0	R/W	0x00*	Ramp rate value per step is defined from 1 (00h) to 64 (3Fh)[1][2]

[1] Total number of ramp steps is defined as ‘IREF_GRP[7:0]’ ÷ ‘ramp_rate[5:0]’. (Round up to next integer if it is not an integer number.)

[2] Per step current increment or decrement is calculated by the (ramp_rate × I_{ref}), where the I_{ref} reference current is 125 μA (REXT = 2 kΩ).

7.2.8.2 STEP_TIME_GRP0 to STEP_TIME_GRP5, step time control registers

Table 13. STEP_TIME_GRP[0:3] - Step time control registers (address 41h, 45h, 49h, 4Dh, 51h, 55h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
41h 45h 49h 4Dh 51h 55h	STEP_TIME_GRP0 STEP_TIME_GRP1 STEP_TIME_GRP2 STEP_TIME_GRP3 STEP_TIME_GRP4 STEP_TIME_GRP5	7	read only	0*	reserved
		6	R/W	0*	Cycle time is set to 0.5 ms
				1	Cycle time is set to 8 ms
		5:0	R/W	0x00*	Multiple factor per step, the multiple factor is defined from 1 (00h) to 64 (3Fh)[1]

[1] Step time = cycle time (0.5 ms or 8 ms) × multiple factor (1 ~ 64); minimum step time is 0.5 ms and maximum step time is 512 ms.

7.2.8.3 HOLD_CNTL_GRP0 to HOLD_CNTL_GRP5, hold ON and OFF control registers

Table 14. HOLD_CNTL_GRP[0:3] - Hold ON and OFF enable and time control registers (address 42h, 46h, 4Ah, 4Eh, 52h, 56h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
42h 46h 4Ah 4Eh 52h 56h	HOLD_CNTL_GRP0 HOLD_CNTL_GRP1 HOLD_CNTL_GRP2 HOLD_CNTL_GRP3 HOLD_CNTL_GRP4 HOLD_CNTL_GRP5	7	R/W	0*	Hold ON disable
				1	Hold ON enable
		6	R/W	0*	Hold OFF disable
				1	Hold OFF enable
		5:3	R/W	000*	Hold ON time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s
		2:0	R/W	000*	Hold OFF time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s

[1] Hold ON or OFF minimum time is 0 s and maximum time is 6 s.

7.2.8.4 IREF_GRP0 to IREF_GRP5, output gain control

Table 15. IREF_GRP[0:3] - Final and hold ON output gain setting registers (address 43h, 47h, 4Bh, 4Fh, 53h, 57h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
43h 47h 4Bh 4Fh 53h 57h	IREF_GRP0 IREF_GRP1 IREF_GRP2 IREF_GRP3 IREF_GRP4 IREF_GRP5	7:0	R/W	00h*	Final ramp-up and hold ON output current gain setting[1]

[1] Output current = I_{ref} × IREF_GRPx[7:0], where I_{ref} is reference current. I_{ref} = 125 μA if REXT = 2 kΩ,

7.2.8.5 GRAD_MODE_SEL0 to GRAD_MODE_SEL2, Gradation mode select registers

Table 16. GRAD_MODE_SEL[0:1] - Gradation mode select register for channel 23 to channel 0 (address 58h, 59h, 5Ah) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1][2]
58h	GRAD_MODE_SEL0	7:0	R/W	00*	Normal operation mode for channel 7 to channel 0
				FFh	Gradation operation mode for channel 7 to channel 0
59h	GRAD_MODE_SEL1	7:0	R/W	00*	Normal operation mode for channel 15 to channel 8
				FFh	Gradation operation mode for channel 15 to channel 8
5Ah	GRAD_MODE_SEL2	7:0	R/W	00*	Normal operation mode for channel 23 to channel 16
				FFh	Gradation operation mode for channel 23 to channel 16

[1] Each bit represents one channel that can set either 0 for normal mode (use IREFx to set individual LED output current), or 1 for gradation mode (use IREF_GRPx to set group LEDs output current.).

[2] In gradation mode, it only affects the source of the IREF current level and does not affect the PWMx operation or LEDOUTx registers' function. It is possible to use the gradation feature, individual PWMx and group PWM simultaneously.

7.2.8.6 GRAD_GRP_SEL0 to GRAD_GRP_SEL11, Gradation group select registers

Table 17. GRAD_GRP_SEL[0:3] - Gradation group select register for channel 23 to channel 0 (address 5Bh, 5Ch, 5Dh, 5Eh, 5Fh, 60h, 61h, 62h, 63h, 64h, 65h, 66h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1]
5Bh	GRAD_GRP_SEL0	7	R/W	0*	Reserved
		6:4	R/W	000*	Gradation group select for LED1 output
		3	R/W	0*	Reserved
		2:0	R/W	000*	Gradation group select for LED0 output
5Ch	GRAD_GRP_SEL1	7	R/W	0*	Reserved
		6:4	R/W	000*	Gradation group select for LED3 output
		3	R/W	0*	Reserved
		2:0	R/W	000*	Gradation group select for LED2 output
5Dh	GRAD_GRP_SEL2	7	R/W	0*	Reserved
		6:4	R/W	001*	Gradation group select for LED5 output
		3	R/W	0*	Reserved
		2:0	R/W	001*	Gradation group select for LED4 output
5Eh	GRAD_GRP_SEL3	7	R/W	0*	Reserved
		6:4	R/W	001*	Gradation group select for LED7 output
		3	R/W	0*	Reserved

Table 17. GRAD_GRP_SEL[0:3] - Gradation group select register for channel 23 to channel 0 (address 5Bh, 5Ch, 5Dh, 5Eh, 5Fh, 60h, 61h, 62h, 63h, 64h, 65h, 66h) bit description*...continued*

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1]
		2:0	R/W	001*	Gradation group select for LED6 output
5Fh	GRAD_GRP_SEL4	7	R/W	0*	Reserved
		6:4	R/W	010*	Gradation group select for LED9 output
		3	R/W	0*	Reserved
		2:0	R/W	010*	Gradation group select for LED8 output
60h	GRAD_GRP_SEL5	7	R/W	0*	Reserved
		6:4	R/W	010*	Gradation group select for LED11 output
		3	R/W	0*	Reserved
		2:0	R/W	010*	Gradation group select for LED10 output
61h	GRAD_GRP_SEL6	7	R/W	0*	Reserved
		6:4	R/W	011*	Gradation group select for LED13 output
		3	R/W	0*	Reserved
		2:0	R/W	011*	Gradation group select for LED12 output
62h	GRAD_GRP_SEL7	7	R/W	0*	Reserved
		6:4	R/W	011*	Gradation group select for LED15 output
		3	R/W	0*	Reserved
		2:0	R/W	011*	Gradation group select for LED14 output
63h	GRAD_GRP_SEL8	7	R/W	0*	Reserved
		6:4	R/W	100*	Gradation group select for LED17 output
		3	R/W	0*	Reserved
		2:0	R/W	100*	Gradation group select for LED16 output
64h	GRAD_GRP_SEL9	7	R/W	0*	Reserved
		6:4	R/W	100*	Gradation group select for LED19 output
		3	R/W	0*	Reserved
		2:0	R/W	100*	Gradation group select for LED18 output
65h	GRAD_GRP_SEL10	7	R/W	0*	Reserved
		6:4	R/W	101*	Gradation group select for LED21 output
		3	R/W	0*	Reserved
		2:0	R/W	101*	Gradation group select for LED20 output
66h	GRAD_GRP_SEL11	7	R/W	0*	Reserved
		6:4	R/W	101*	Gradation group select for LED23 output
		3	R/W	0*	Reserved
		2:0	R/W	101*	Gradation group select for LED22 output

[1] LED[3:0] outputs default assigned to group 0; LED[7:4] outputs default assigned to group 1; LED[11:8] outputs default assigned to group 2; LED[15:12] outputs default assigned to group 3;

LED[19:16] outputs default assigned to group 4; LED[23:20] outputs default assigned to group 5.

7.2.8.7 GRAD_CNTL, Gradation control register

Table 18. GRAD_CNTL[0:1] - Gradation control register for group 5 to group 0 (address 67h, 68h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
67h	GRAD_CNTL0	7	R/W	0*	Gradation stop or done for group 3[1]
				1	Gradation start for group 3[2]
		6	R/W	0*	Single shot operation for group 3
				1	Continuous operation for group 3
		5	R/W	0*	Gradation stop or done for group 2[1]
				1	Gradation start for group 2[2]
		4	R/W	0*	Single shot operation for group 2
				1	Continuous operation for group 2
		3	R/W	0*	Gradation stop or done for group 1[1]
				1	Gradation start for group 1[2]
		2	R/W	0*	Single shot operation for group 1
				1	Continuous operation for group 1
		1	R/W	0*	Gradation stop or done for group 0[1]
				1	Gradation start for group 0[2]
		0	R/W	0*	Single shot operation for group 0
				1	Continuous operation for group 0
68h	GRAD_CNTL1	7	R/W	0*	Gradation stop or done for group 5[1]
				1	Gradation start for group 5[2]
		6	R/W	0*	Single shot operation for group 5
				1	Continuous operation for group 5
		5	R/W	0*	Gradation stop or done for group 4[1]
				1	Gradation start for group 4[2]
		4	R/W	0*	Single shot operation for group 4
				1	Continuous operation for group 4
		3:0	R	0*	Reserved

[1] When the gradation operation is forced to stop, the output current stops immediately and is frozen at the last output level.

[2] This bit will be self-cleared when single mode is completed, and writing 0 to this bit will force to stop the gradation operation when single mode is not completed or continuous mode is running.

7.2.8.8 Ramp control — equation and calculation example

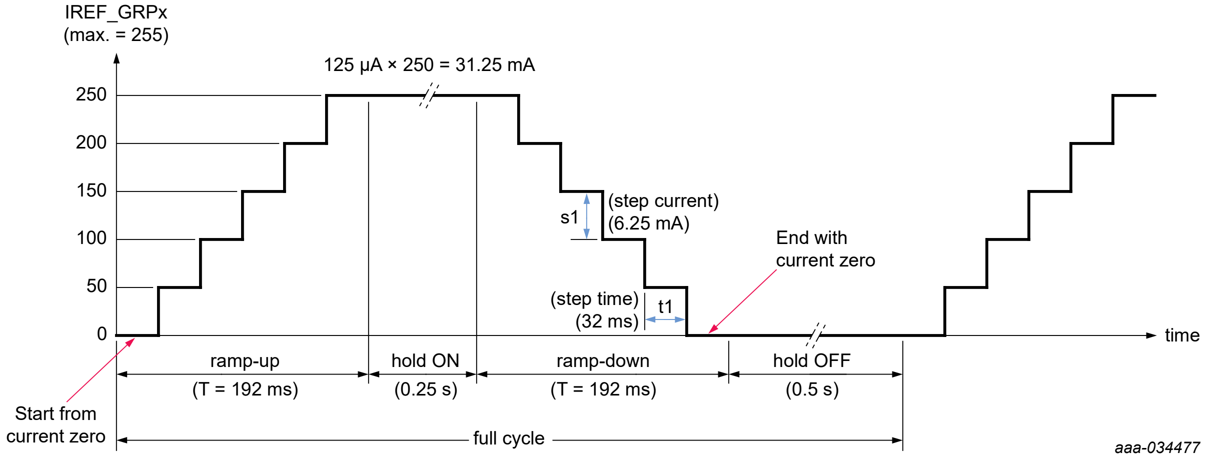


Figure 6. Ramp calculation example 1

- t1 (step time) = cycle time × multiple factor, where:
  - Cycle time = 0.5 ms (fast ramp) or 8 ms (slow ramp) in STEP_TIME_GRPx[6]
  - Multiple factor = 6-bit, from 1 (00h) to 64 (3Fh) counts in STEP_TIME_GRPx[5:0]
- s1 (step current) = ramp_rate × I_{ref}, where:
  - ramp_rate = 6-bit, from 1 (00h) to 64 (3Fh) counts in RAMP_RATE_GRPx[5:0]
  - I_{ref} = reference current of 125 µA if REXT = 2 kΩ
- S (total steps) = (IREF_GRPx / ramp_rate), where:
  - IREF_GRPx = output current gain setting, 8-bit, up to 255 counts
  - ramp_rate = 6-bit, up to 64 counts in RAMP_RATE_GRPx[5:0]
  - If it is not an integer, then round up to next integer number.
- T (ramp time) = (S (total steps) + 1) × t1 (step time)
  - Ramp-up time starts from zero current and ends at the maximum current
  - Ramp-down time starts from the maximum current and ends at the zero current

Calculation example 1 (Figure 6):

- Assumption:
  - I_{ref} = 125 µA if REXT = 2 kΩ
  - Output hold ON current = 125 µA × 250 = 31.25 mA (IREF_GRPx[7:0] = FAh)
  - Cycle time = 0.5 ms (STEP_TIME_GRPx[6] = 0)
  - Multiple factor = 64 (STEP_TIME_GRPx[5:0] = 3Fh)
  - Ramp rate = 50 (RAMP_RATE_GRPx[5:0] = 31h)
  - Hold ON = 0.25 s (HOLD_CNTL_GRPx[5:3] = 001)
  - Hold OFF = 0.5 s (HOLD_CNTL_GRPx[2:0] = 010)
- t1 (step time) = cycle time (0.5 ms) × multiple (64) = 32 ms
- Step current = ramp_rate × I_{ref} = 50 × 125 µA = 6.25 mA
- S (total steps) = (IREF_GRPx ÷ ramp_rate) = (250 ÷ 50) = 5 steps
- T (ramp time) = (S + 1) × t1 = 6 × 32 ms = 192 ms

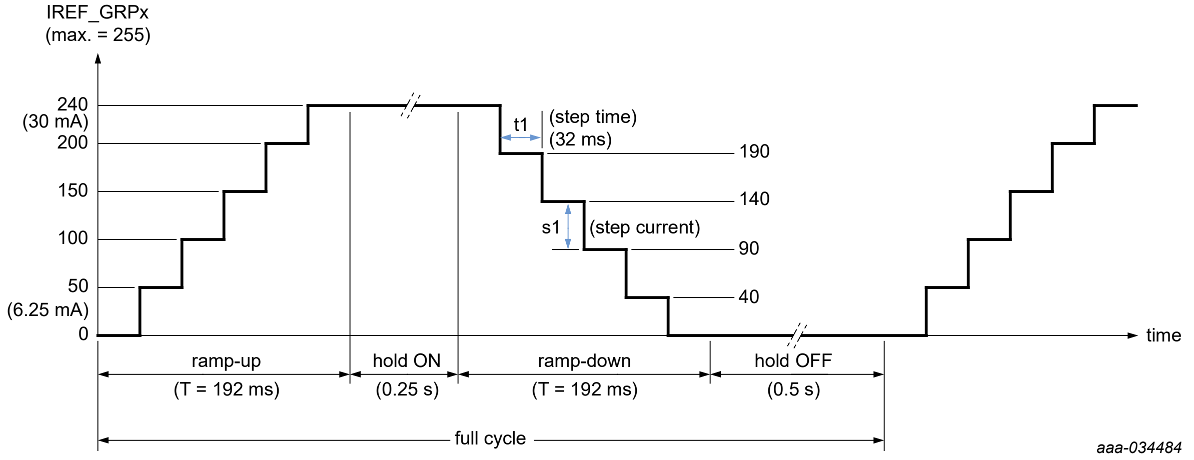
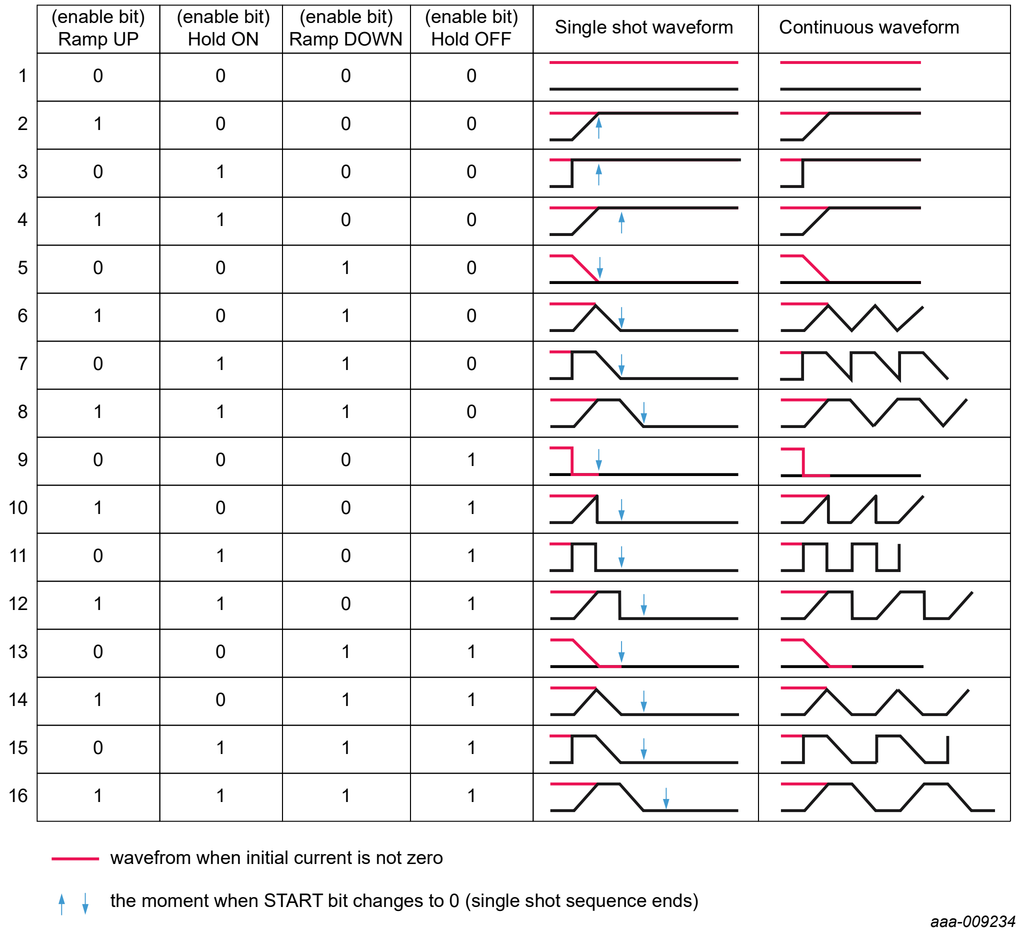


Figure 7. Ramp calculation example 2

Calculation example 2:

- Assumption:
  - I_{ref} = 125 μA if REXT = 2 kΩ
  - Output hold ON current = 125 μA × 240 = 30 mA (IREF_GRPx[7:0] = F0h)
  - Cycle time = 0.5 ms (STEP_TIME_GRPx[6] = 0)
  - Multiple factor = 64 (STEP_TIME_GRPx[5:0] = 3Fh)
  - Ramp rate = 50 (RAMP_RATE_GRPx[5:0] = 31h)
  - Hold ON = 0.25 s (HOLD_CNTL_GRPx[5:3] = 001)
  - Hold OFF = 0.5 s (HOLD_CNTL_GRPx[2:0] = 010)
- t1 (step time) = cycle time (0.5 ms) × multiple (64) = 32 ms
- Step current = ramp_rate × I_{ref} = 50 × 125 μA = 6.25 mA (except the last one)
- S (total steps) = IREF_GRPx ÷ ramp_rate = 240 ÷ 50 = 4.8 steps (round up to next integer) = 5 steps
- T (ramp time) = (S + 1) × t1 = 6 × 32 ms = 192 ms



	(enable bit) Ramp UP	(enable bit) Hold ON	(enable bit) Ramp DOWN	(enable bit) Hold OFF
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

— wavefrom when initial current is not zero

↑ ↓ the moment when START bit changes to 0 (single shot sequence ends)

aaa-009234

Figure 8. Gradation output waveform in single shot or continuous mode

7.2.9 OFFSET — LEDn output delay offset register

Table 19. OFFSET - LEDn output delay offset register (address 69h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
69h	OFFSET	7:4	read only	0000*	not used
		3:0	R/W	1000*	LEDn output delay offset factor (0000 - 1011)

The PCA9957 can be programmed to have turn-on delay between LED outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

This turn-on delay also applies to $\overline{OE}$ pin when becomes low.

The order in which the LED outputs are enabled will always be the same (channel 0 will enable first and channel 23 will enable last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows, and the valid number is 0000 – 1011. The number greater than 1011 (such as 1100 - 1111) will have the same turn-on delay as 1011 setting (1.375 μS), and read back value will be changed to 1011:

0000 = no delay between outputs (all on, all off at the same time)
0001 = delay of 1 clock cycle (125 ns) between successive outputs
0010 = delay of 2 clock cycles (250 ns) between successive outputs
0011 = delay of 3 clock cycles (375 ns) between successive outputs
:
1011 = delay of 11 clock cycles (1.375 μs) between successive outputs
:
1111 = delay of 11 clock cycles (1.375 μs) between successive outputs

Example: If the value in the OFFSET register is 1000, the corresponding delay = 8 × 125 ns = 1 μs delay between successive outputs.

channel 0 turns on at time 0 μs
channel 1 turns on at time 1 μs
channel 2 turns on at time 2 μs
channel 3 turns on at time 3 μs
channel 4 turns on at time 4 μs
channel 5 turns on at time 5 μs
channel 6 turns on at time 6 μs
channel 7 turns on at time 7 μs
channel 8 turns on at time 8 μs
channel 9 turns on at time 9 μs
channel 10 turns on at time 10 μs
channel 11 turns on at time 11 μs
channel 12 turns on at time 12 μs
channel 13 turns on at time 13 μs
channel 14 turns on at time 14 μs
channel 15 turns on at time 15 μs
channel 16 turns on at time 16 μs
channel 17 turns on at time 17 μs
channel 18 turns on at time 18 μs
channel 19 turns on at time 19 μs
channel 20 turns on at time 20 μs
channel 21 turns on at time 21 μs
channel 22 turns on at time 22 μs
channel 23 turns on at time 23 μs

7.2.10 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register will be used for PWM duty cycle for all the LEDn outputs and will be reflected in PWM0 through PWM23 registers.

Table 20. PWMALL - brightness control for all LEDn outputs register (address 6Ah) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
6Ah	PWMALL	7:0	write only	0000 0000*	duty cycle for all LEDn outputs

Remark: Write to any of the PWM0 to PWM23 registers will overwrite the value in corresponding PWMn register programmed by PWMALL.

7.2.11 IREFALL register: output current value for all LED outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LED outputs will be set to a current corresponding to this register value.

Writes to IREF0 to IREF23 will overwrite the output current settings.

Table 21. IREFALL - Output gain control for all LED outputs (address 6Bh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
6Bh	IREFALL	7:0	write only	00h*	Current gain setting for all LED outputs.

7.2.12 LED driver constant current outputs

In LED display applications, PCA9957 provides nearly no current variations, the absolute accuracy is less than ± 6.5 %.

7.2.12.1 Adjusting output current

The PCA9957 scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_O) at each output port. The maximum output current for the outputs can be set using R_{ext}. In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF23. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

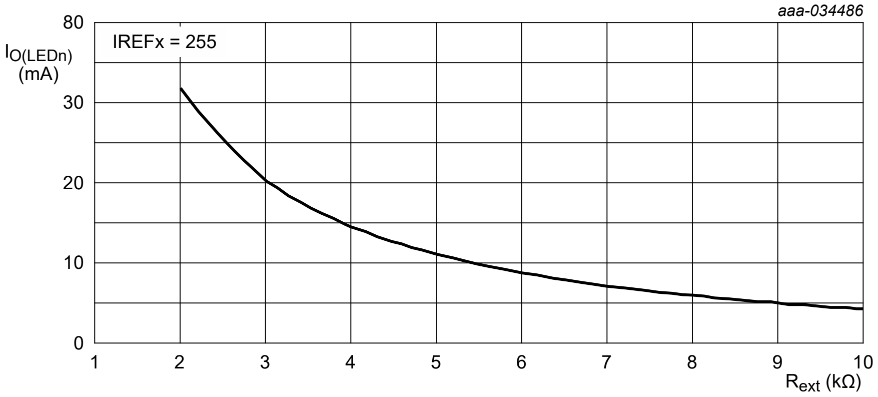
Equation 4 and Equation 5 can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O\_LED\_MIN = \frac{1000mV}{R_{ext}} \times \frac{1}{4} \left(\text{minimum constant current}\right) \quad (4)$$

$$I_O\_LED\_MAX = \left(255 \times I_O\_LED\_MIN\right) = \left(\frac{1000mV}{R_{ext}} \times \frac{255}{4}\right) \quad (5)$$

For a given IREFx setting:

$$I_O\_LED = IREFx \times \frac{1000mV}{R_{ext}} \times \frac{1}{4}$$



$I_{O(LEDn)}$ (mA) = IREFx × (1 / 4) / R_{ext} (kΩ)

maximum $I_{O(LEDn)}$ (mA) = 255 × (1 / 4) / R_{ext} (kΩ)

Remark: Default IREFx at power-up = 0.

Figure 9. Maximum I_{LED} versus R_{ext}

Example 1: If R_{ext} = 2 kΩ, I_O_LED_MIN = 125.0 μA, I_O_LED_MAX = 31.875 mA (as shown in Figure 10).

So each channel can be programmed with its individual IREFx in 256 steps and in 125 μA increments to a maximum output current of 31.875 mA independently.

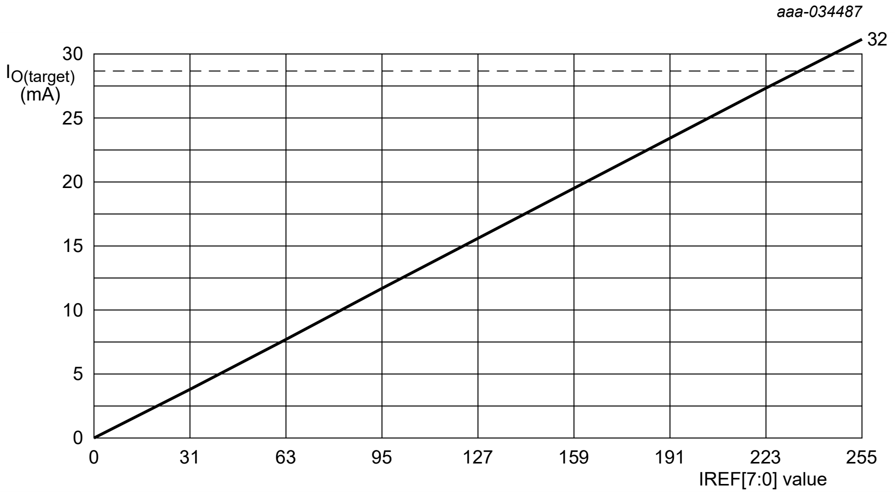


Figure 10. $I_{O(target)}$ versus IREFx value with R_{ext} = 2 kΩ

7.2.13 LED error detection

The PCA9957 is capable of detecting an LED open or a short condition at its open-drain LED outputs. Users will recognize these faults by reading the status of a pair of error bits (ERRx) in error flag registers (EFLAGn) for each channel. Both LDRx value in LEDOUTx registers and IREFx value must be set to ‘00’ for those unused LED output channels. If the output is selected to be fully on, individual dim, or individual and group dim, that channel will be tested.

The user can poll the ERROR status bit (bit 6 in MODE2 register) to check if there is a fault condition in any of the 24 channels. The EFLAGn registers can then be read to determine which channels are at fault and the type of fault in those channels.

The error status reported by the EFLAGn register is real time information, when AUTO_SWITCHOFF_DIS = 1, it will get self cleared once the error is fixed or write ‘1’ to CLRERR bit (bit 4 in MODE2 register), when AUTO_SWITCHOFF_DIS = 0, PCA9957 will stop detection once error occurs, the EFLAGn register will keep the last error status until write ‘1’ to CLRERR bit or get reset.

Remark: When LED outputs programmed with LDRx = 10 or 11 in LEDOUT[3:0] registers, checks for open and short-circuit will not occur if the PWM value in PWM0 to PWM23 registers is less than 8 or 255 (100 % duty cycle).

Table 22. EFLAG0 to EFLAG5 - Error flag registers (address 02h to 07h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	EFLAG0	7:6	ERR3	R only	00*	Error status for LED3 output
		5:4	ERR2	R only	00*	Error status for LED2 output
		3:2	ERR1	R only	00*	Error status for LED1 output
		1:0	ERR0	R only	00*	Error status for LED0 output
03h	EFLAG1	7:6	ERR7	R only	00*	Error status for LED7 output
		5:4	ERR6	R only	00*	Error status for LED6 output
		3:2	ERR5	R only	00*	Error status for LED5 output
		1:0	ERR4	R only	00*	Error status for LED4 output
04h	EFLAG2	7:6	ERR11	R only	00*	Error status for LED11 output
		5:4	ERR10	R only	00*	Error status for LED10 output
		3:2	ERR9	R only	00*	Error status for LED9 output
		1:0	ERR8	R only	00*	Error status for LED8 output
05h	EFLAG3	7:6	ERR15	R only	00*	Error status for LED15 output
		5:4	ERR14	R only	00*	Error status for LED14 output
		3:2	ERR13	R only	00*	Error status for LED13 output
		1:0	ERR12	R only	00*	Error status for LED12 output
06h	EFLAG4	7:6	ERR19	R only	00*	Error status for LED19 output
		5:4	ERR18	R only	00*	Error status for LED18 output
		3:2	ERR17	R only	00*	Error status for LED17 output
		1:0	ERR16	R only	00*	Error status for LED16 output
07h	EFLAG5	7:6	ERR23	R only	00*	Error status for LED23 output
		5:4	ERR22	R only	00*	Error status for LED22 output
		3:2	ERR21	R only	00*	Error status for LED21 output
		1:0	ERR20	R only	00*	Error status for LED20 output

Table 23. ERRx bit description

LED error detection status	ERRx		Description
	Bit 1	Bit 0	
No error	0	0	In normal operation and no error
Short-circuit	0	1	Detected LED short-circuit condition
Open-circuit	1	0	Detected LED open-circuit condition
DNE (Do Not Exist)	1	1	This condition does not exist

7.2.13.1 Open-circuit detection principle

The PCA9957 LED open-circuit detection compares the effective current level I_O with the open load detection threshold current $I_{th(det)}$. If I_O is below the threshold $I_{th(det)}$, the PCA9957 detects an open load condition. This error status can be read out as an error flag through the EFLAGn registers. For open-circuit error detection of an output channel, that channel must be ON.

Table 24. Open-circuit detection

State of output port	Condition of output current	Error status code	Description
OFF	$I_O = 0$ mA	0	detection not possible
ON	$I_O < I_{th(det)}$[1]	1	open-circuit
	$I_O \geq I_{th(det)}$[1]	this channel open error status bit is 0	normal

[1] $I_{th(det)} = 0.5 \times I_{O(target)}$ (typical). This threshold may be different for each I/O and only depends on IREFx and R_{ext}.

7.2.13.2 Short-circuit detection principle

The LED short-circuit detection compares the effective output voltage level (V_O) with the shorted-load detection threshold voltages $V_{th(trig)}$. If V_O is above the $V_{th(trig)}$ threshold, the PCA9957 detects a shorted-load condition. If V_O is below the $V_{th(trig)}$ threshold, no error is detected and error bit is set to ‘0’. This error status can be read out as an error flag through the EFLAGn registers. For short-circuit error detection of an output channel, that channel must be ON.

Table 25. Short-circuit detection

State of output port	Condition of output voltage	Error status code	Description
OFF	-	0	detection not possible
ON	$V_O \geq V_{th(trig)}$[1]	1	short-circuit
	$V_O < V_{th(trig)}$[1]	this channel short error status bit is 0	normal

[1] $V_{th} \cong 1.96$ V.

Remark: The error status distinguishes between an LED short condition and an LED open condition. Upon detecting an LED short or open, the corresponding LED outputs should be turned OFF to prevent heat dissipation for a short in the chip. Although an open event will not be harmful, the outputs should be turned OFF for both occasions to repair the LED string.

7.2.14 Overtemperature protection

If the PCA9957 chip temperature exceeds its limit ($T_{th(otp)}$ (rising) maximum, see Table 28), all output channels will be disabled until the temperature drops below its limit minus a small hysteresis ($T_{th(otp)}$ (hysteresis) maximum, see Table 28). When an overtemperature situation is encountered, the OVERTEMP flag (bit 7) is set in the MODE2 register. Once the die temperature reduces below the $T_{th(otp)}$ rising - $T_{th(otp)}$ hysteresis, the chip will return to the same condition it was prior to the overtemperature event and the OVERTEMP flag will be cleared.

7.3 Active LOW output enable input

The active LOW output enable ($\overline{\text{OE}}$) pin on PCA9957 allows to enable or disable all the LED outputs at the same time.

- When a LOW level is applied to $\overline{\text{OE}}$ pin, all the LED outputs are enabled, LEDn output delay applies to this sequence.
- When a HIGH level is applied to $\overline{\text{OE}}$ pin, all the LED outputs are high-impedance.

The $\overline{\text{OE}}$ pin can be used as a synchronization signal to switch on/off several PCA9957 devices at the same time when LED drive output state is set fully ON (LDRx = 01 in LEDOUTx register) in these devices. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{\text{OE}}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

LEDn output delay controlled by register OFFSET also applies $\overline{\text{OE}}$ control.

Remark: Do not use $\overline{\text{OE}}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use $\overline{\text{OE}}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

7.4 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9957 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9957 registers and serial bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be pulled lower than 1 V and stay LOW for longer than 20 μs. The device will reset itself, and allow 2 ms for the device to fully wake up.

7.5 Hardware reset recovery

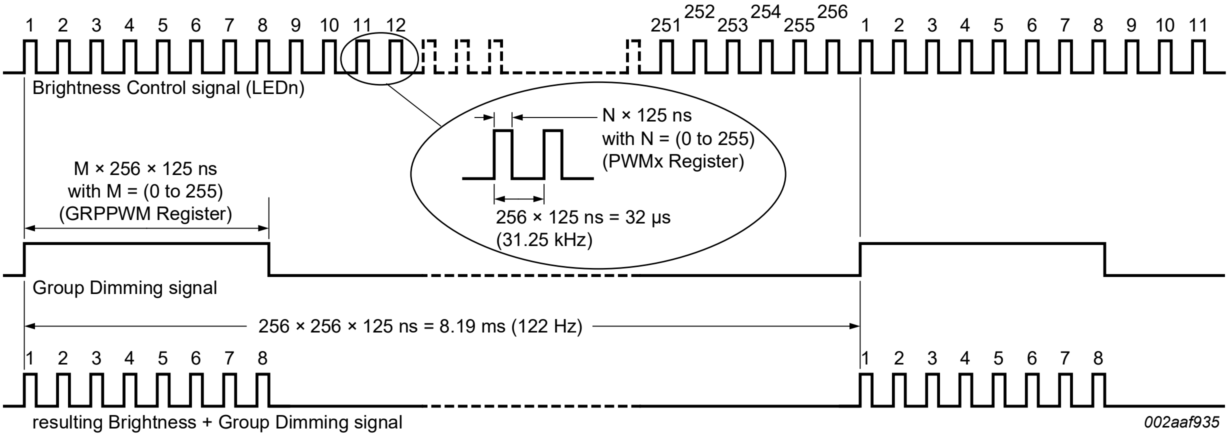
When a reset of PCA9957 is activated using an active LOW input on the $\overline{\text{RESET}}$ pin, a reset pulse width of 2.5 μs minimum is required. The maximum wait time after $\overline{\text{RESET}}$ pin is released is 1.5 ms.

7.6 Individual brightness control with group dimming/blinking

A 31.25 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 24 LED outputs LED0 to LED23).

- A lower 122 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 15 Hz to every 16.8 seconds (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.


1 2 3 4 5 6 7 8 9 10 11 12
251 252 253 254 255 256 1 2 3 4 5 6 7 8 9 10 11
Brightness Control signal (LEDn)
N × 125 ns
with N = (0 to 255)
(PWMx Register)
M × 256 × 125 ns
with M = (0 to 255)
(GRPPWM Register)
256 × 125 ns = 32 µs
(31.25 kHz)
Group Dimming signal
256 × 256 × 125 ns = 8.19 ms (122 Hz)
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8
resulting Brightness + Group Dimming signal
002aaf935

Minimum pulse width for LEDn Brightness Control is 125 ns.

Minimum pulse width for Group Dimming is 32 µs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 1 pulse of the LED Brightness Control signal (pulse width = N × 125 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 8.

Figure 11. Brightness + Group Dimming signals

8 Characteristics of the 4-wire SPI serial-bus interface

The PCA9957 communicates through a daisy-chain SPI-compatible 4-wire serial interface. The interface has three inputs and one output: serial clock (SCLK), active LOW chip select ($\overline{\text{CS}}$), serial data in (SDI) and serial data output (SDO). $\overline{\text{CS}}$ must be LOW to clock data into the device, and SDI must be stable when sampled on the rising edge of SCLK. The PCA9957 ignores all activity on SCLK and SDI except when $\overline{\text{CS}}$ is LOW.

8.1 SPI-compatible 4-wire serial interface signals

$\overline{\text{CS}}$

The active LOW chip select line is used to activate and access the SPI slaves. As long as $\overline{\text{CS}}$ is HIGH, all slaves will not accept the clock signal or data, and output SDO is driven LOW, therefore SPI parallel connection is not supported. Whenever this pin is in a logic LOW state, data can be transferred between the master (controller) and all slaves (targets).

SCLK

Serial clock is provided by SPI master and determines the speed of the data transfer. All receiving and sending data are done synchronously (clocks the internal SPI shift register and the output driver) to this clock.

SDI

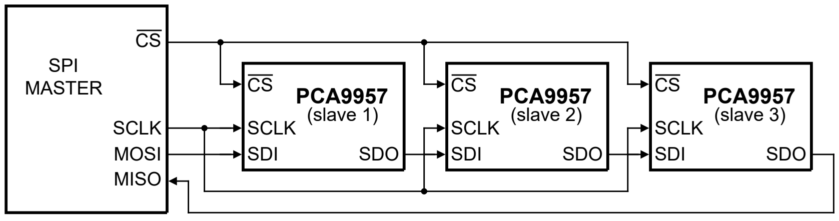
Serial Data In is read on the rising edge of SCLK into the internal 16-bit shift registers. On the rising edge of $\overline{CS}$, the input data is latched into the internal registers of the device. The device ignores all activity on SDI when $\overline{CS}$ is deasserted.

SDO

Serial Data Out is the pin on which the internal 16-bit shift registers data is shifted out serially. SDO is driven LOW until the $\overline{CS}$ pin goes to a logic LOW state. New data appears at the SDO pin following the falling edge of SCLK.

All slave devices can be daisy-chained by connecting the SDO of one device to the SDI of the next device, and driving SCLK and $\overline{CS}$ lines in parallel. Figure 12 depicts how the slaves are connected to the master. All slave devices are accessed at the same time with $\overline{CS}$. An access requires (16 × n) clock cycles, where 'n' is the number of slave devices. As long as $\overline{CS}$ is LOW, the SPI registers are working as simple shift registers and shifting through the SDI data without interpreting the different control and data bits. When $\overline{CS}$ goes back to HIGH, the bits in the SPI registers are interpreted and the SPI logic is activated.

Only the first slave in the chain receives the control and data bits directly from the SPI Master. Every other slave in the network receives its SDI data from the SDO output of the preceding slave in the chain, and the SDO of the last slave is then connected to the data input (MISO) of SPI Master. Each slave has 16-bit shift registers shifted in from SDI and shifted out to SDO, along with the SCLK clock. The whole chain acts as a 48-bit (n × 16-bit, where 'n' is number of slaves) big shift register.

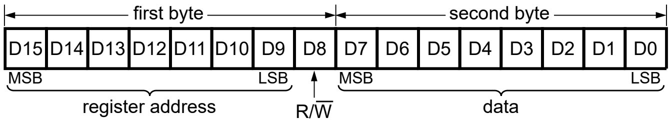


aaa-034488

Figure 12. System level connection

8.2 Data format

As shown in Figure 13, the data transfers are 16-bit × n bits wide (where 'n' is the number of slaves) with MSB transferred first. The first 7 bits, D[15:9], form the address of the register to be accessed, the eighth bit (D8) indicates the types of access, either read (= 1) or write (= 0), and the last 8 bits, D[7:0], consist of data. Register read and write sequences (described in the following sections) always begin from the bus idle condition. The bus idle condition refers to $\overline{CS}$ being HIGH and SCLK being in a LOW state.



aaa-011890

Figure 13. Data format

8.3 Write access sequence

The registers are written using the following write sequence (from a bus idle condition) when the system has three slaves daisy-chained together:

1. All the slave devices in chain will be involved in a write or read operation. Every slave device in the chain is a portion of one big shift register.
2. Drive $\overline{CS}$ LOW. This enables the internal 16-bit shift register.
3. Shift 16 × n bits of data (where 'n' is the number of slaves) into the first slave device in a MSB-first fashion. Data is shifted on the rising edge of SCLK and must be stable during the rising edge of SCLK.
4. The 8th bit of the data for every 16 bits (each device) must be a '0', indicating it is a write transfer.
5. After the last bit of data is transferred, drive SCLK LOW and deassert CS (drive it HIGH).
6. When $\overline{CS}$ goes from LOW to HIGH, the data in the shift register is latched into the device registers.

If fewer than 16 bits of data are transferred before deasserting $\overline{CS}$, then the data is ignored and the register will not be updated. The write transfer format is shown in Figure 14.

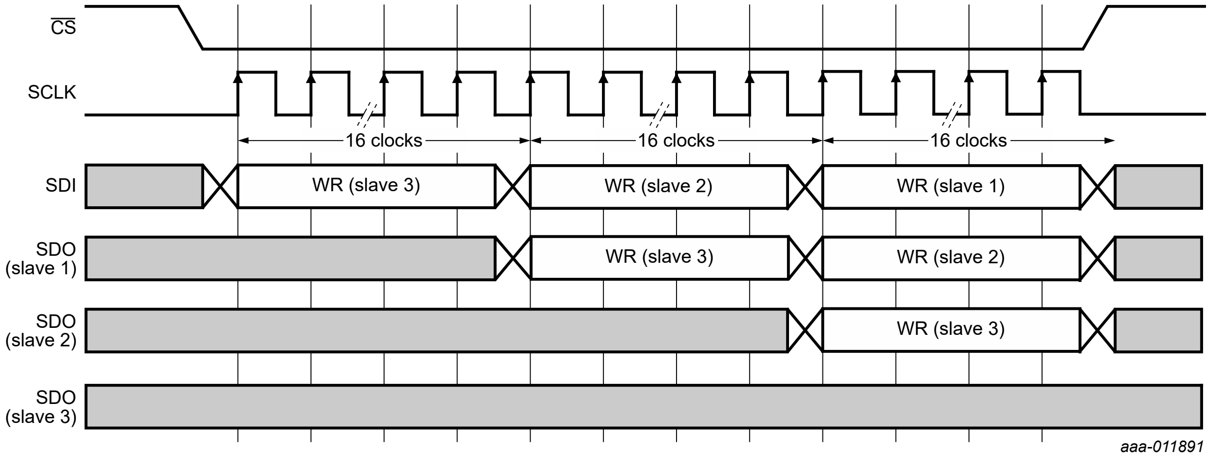


Figure 14. Write access

8.4 Read access sequence

The registers are read using the following read sequence (from a bus idle condition) when the system has three slaves daisy-chained as shown in Figure 15.

1. The master sends the first three 2-byte read instructions with 48 clocks, where the first byte is a 7-bit register address, an eighth bit set to one, followed by dummy data byte (all ones).
2. The Read instruction is decoded when $\overline{CS}$ is deasserted (from LOW to HIGH).
3. The read data is shifted out on SDO when $\overline{CS}$ is asserted again (from HIGH to LOW).
4. The master sends the second three 2-byte 'No Operation' (NOP) operations (all ones) with 48 clocks and reads the requested data on MISO in sequence where the first byte is dummy data (don't care), followed by the read data byte.
5. A read cycle consists of asserting and deasserting of $\overline{CS}$ twice.

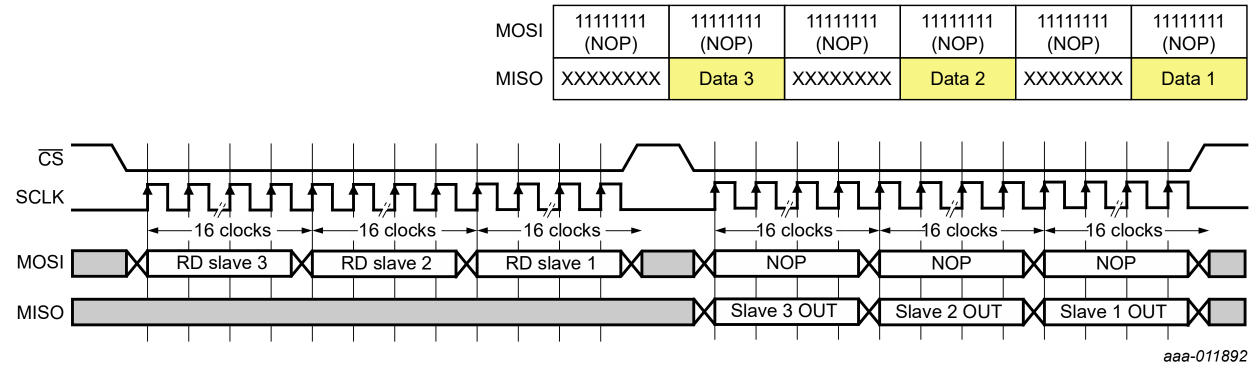

MOSI
11111111 (NOP)
11111111 (NOP)
11111111 (NOP)
11111111 (NOP)
11111111 (NOP)
11111111 (NOP)
MISO
XXXXXXXX
Data 3
XXXXXXXX
Data 2
XXXXXXXX
Data 1
CS
SCLK
16 clocks
16 clocks
16 clocks
16 clocks
16 clocks
16 clocks
MOSI
RD slave 3
RD slave 2
RD slave 1
NOP
NOP
NOP
MISO
Slave 3 OUT
Slave 2 OUT
Slave 1 OUT
aaa-011892

Figure 15. Read access

8.5 Overlapped read and write access sequence

The registers are read and write overlapped using the following sequence (from a bus idle condition) when the system has three slaves daisy-chained as shown in Figure 16.

1. The second phase of the read cycle can be used to send in write data or the next read instruction. This increases the bus utility and hence efficiency.
2. The master sends the first three 2-byte read instructions with 48 clocks, where the first byte is a 7-bit register address, the eighth bit is set to one, followed by dummy data byte (all ones).
3. The read instruction is decoded when $\overline{CS}$ is deasserted (from LOW to HIGH).
4. Start to shift read data out on SDO when $\overline{CS}$ is asserted again (from HIGH to LOW) and start to send in the next read or write instruction on the SDI line.

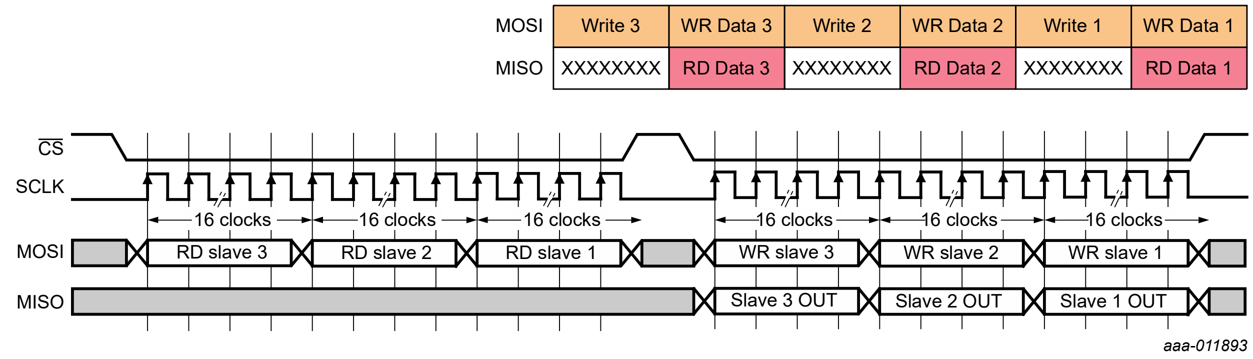
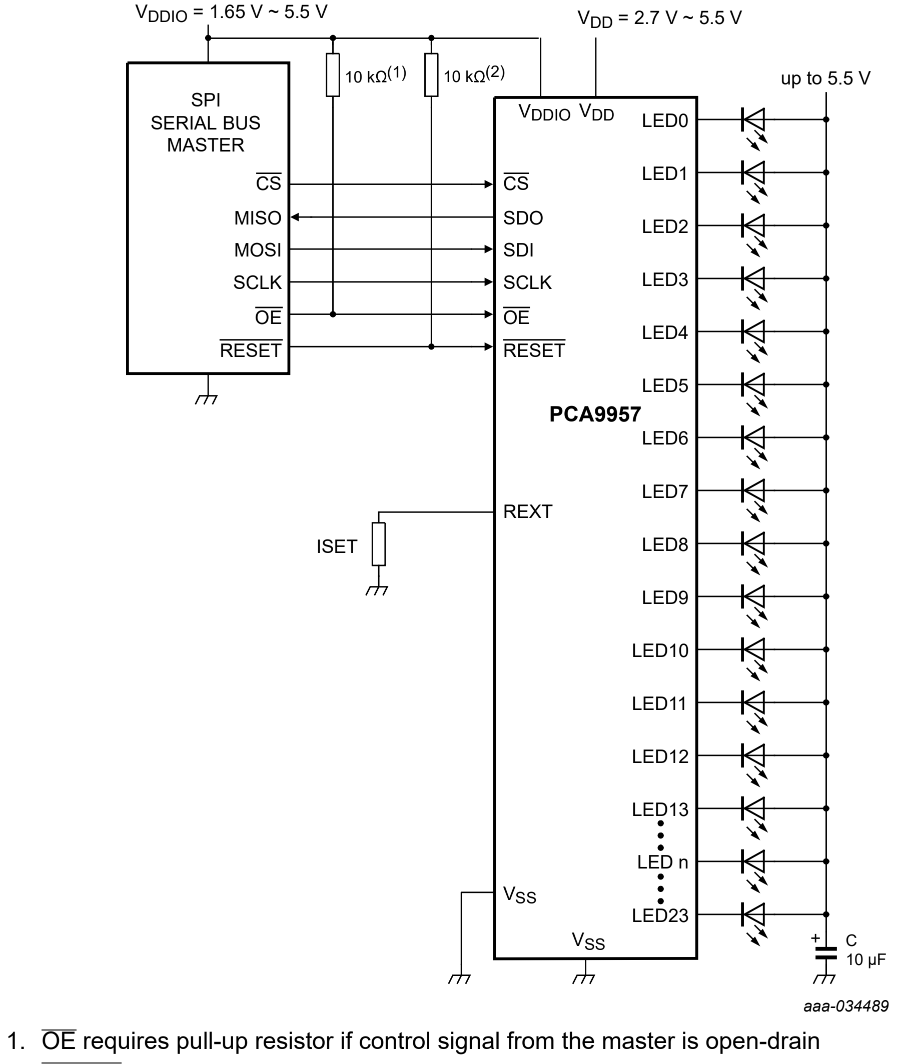

MOSI
Write 3
WR Data 3
Write 2
WR Data 2
Write 1
WR Data 1
MISO
XXXXXXXX
RD Data 3
XXXXXXXX
RD Data 2
XXXXXXXX
RD Data 1
CS
SCLK
16 clocks
16 clocks
16 clocks
16 clocks
16 clocks
16 clocks
MOSI
RD slave 3
RD slave 2
RD slave 1
WR slave 3
WR slave 2
WR slave 1
MISO
Slave 3 OUT
Slave 2 OUT
Slave 1 OUT
aaa-011893

Figure 16. Overlapped read and write access

9 Application design-in information


V_{DDIO} = 1.65 V ~ 5.5 V
V_{DD} = 2.7 V ~ 5.5 V
10 kΩ(1)
10 kΩ(2)
up to 5.5 V
SPI SERIAL BUS MASTER
$\overline{CS}$
MISO
MOSI
SCLK
$\overline{OE}$
$\overline{RESET}$
V_{DDIO} V_{DD}
SDO
SDI
PCA9957
REXT
ISET
V_{SS}
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
LED9
LED10
LED11
LED12
LED13
LED n
LED23
C
10 µF
aaa-034489

1. $\overline{\text{OE}}$ requires pull-up resistor if control signal from the master is open-drain
2. $\overline{\text{RESET}}$ requires a pull-up resistor of <100 kΩ if not used or connected to open-drain output

Figure 17. Typical application

9.1 Thermal considerations

Since the PCA9957 device integrates 24 linear current sources, thermal considerations should be taken into account to prevent overheating, which can cause the device to go into thermal shutdown.

Perhaps the major contributor for device’s overheating is the LED forward voltage mismatch. This is because it can cause significant voltage differences between the LED of the same type (for example, 2 V to 3 V), which ultimately translates into higher power dissipation in the device. The voltage drop across the LED channels of the device is given by the difference between the supply voltage and the LED forward voltage of each LED. Reducing this to a minimum (for example, 0.4 V) helps to keep the power dissipation down. Therefore LEDs binning is recommended to minimize LED voltage forward variation and reduce power dissipation in the device.

In order to ensure that the device will not go into thermal shutdown when operating under certain application conditions, its junction temperature (T_j) should be calculated to ensure that is below the overtemperature threshold limit (130 °C). The T_j of the device depends on the ambient temperature (T_{amb}), device’s total power dissipation (P_{tot}), and thermal resistance.

The device junction temperature can be calculated by using the following equation:

$$T_j = T_{amb} + R_{th(j\text{-}a)} \times P_{tot} \quad (6)$$

where:

T_j = junction temperature
T_{amb} = ambient temperature
$R_{th(j\text{-}a)}$ = junction to ambient thermal resistance
P_{tot} = (device) total power dissipation

An example of this calculation is show below:

Conditions:

T_{amb} = 50 °C
$R_{th(j\text{-}a)}$ = 39 °C/W (per JEDEC 51 standard for multilayer PCB)
I_{LED} = 30 mA / channel
$I_{DD(max)}$ = 20 mA
V_{DD} = 3.3 V
LEDs per channel = 1 LEDs / channel
LED $V_{F(typ)}$ = 3 V per LED
LED V_F mismatch = 0.2 V per LED
$V_{reg(drv)}$ = 0.4 V (This will be present only in the LED string with the highest LED forward voltage.)
V_{sup} = LED $V_{F(typ)}$ + LED V_F mismatch + $V_{reg(drv)}$ = 3 V + 0.2 V + 0.4 V = 3.6 V

P_{tot} calculation:

P_{tot} = IC_power + LED drivers_power;
IC_power = (I_{DD} × V_{DD})
IC_power = (0.02 A × 3.3 V) = 0.066 W
LED drivers_power = [(24 - 1) × (I_{LED}) × (LED V_F mismatch + $V_{reg(drv)}$)] + (I_{LED} × $V_{reg(drv)}$)
LED drivers_power = [23 × 0.03 A × (0.2 V + 0.4 V)] + (0.03 A × 0.4 V)] = 0.426 W
P_{tot} = 0.66 W + 0.426 W = 0.492 W

T_j calculation:

T_j = T_{amb} + $R_{th(j\text{-}a)}$ × P_{tot}
T_j = 50 °C + (30 °C/W × 0.492 W) = 64.76 °C

This confirms that the junction temperature is below the minimum overtemperature threshold of 130 °C, which ensures the device will not go into thermal shutdown under these conditions.

It is important to mention that the value of the thermal resistance junction-to-ambient ($R_{th(j\text{-}a)}$) strongly depends in the PCB design. Therefore, the thermal pad of the device should be attached to a big enough PCB copper area to ensure proper thermal dissipation (similar to JEDEC 51 standard). Several thermal vias in the PCB thermal pad should be used as well to increase the effectiveness of the heat dissipation (for example, 15 thermal vias). The thermal vias should be distributed evenly in the PCB thermal pad.

Finally, it is important to point out that this calculation should be taken as a reference only and therefore evaluations should still be performed under the application environment and conditions to confirm proper system operation.

10 Limiting values

Table 26. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.0	V
V_{DDIO}	supply voltage of interface			-0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin			V_{SS} - 0.5	5.5	V
$V_{drv(LED)}$	LED driver voltage			V_{SS} - 0.5	+6.0	V
$I_{O(LEDn)}$	output current on pin LEDn			-	40	mA
I_{SS}	ground supply current			-	1.0	A
P_{tot}	total power dissipation	T_{amb} = 25 °C		-	3.3	W
		T_{amb} = 85 °C		-	1.3	W
T_{stg}	storage temperature			-65	+150	°C
T_{amb}	ambient temperature	operating for non AEC-Q100		-40	+85	°C
T_j	junction temperature			-40	+125	°C

11 Thermal characteristics

Table 27. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVQFN40	[1]	35.6	°C/W
$R_{th(j-case\ top)}$	thermal resistance between the junction and the case top	HVQFN40		17.9	°C/W
$R_{th(j-case\ bottom)}$	thermal resistance between the junction and the case bottom	HVQFN40		8.5	°C/W
$R_{th(j-board)}$	thermal resistance between the junction and the board	HVQFN40	[1]	27.2	°C/W

[1] Per JEDEC 51 standard for multilayer PCB and Wind Speed (m/s) = 0.

12 Static characteristics

Table 28. Static characteristics

V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
Supply							

Table 28. Static characteristics*...continued*

V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{DD}	supply voltage			2.7	-	5.5	V
V_{DDIO}	supply voltage of SPI interface			1.65	-	5.5	V
I_{DD}	supply current	on pin V_{DD}; operating mode; f_{SCLK} = 10 MHz					
		R_{ext} = 2 kΩ; LED[23:0] = off; IREFx = 00h		-	-	6.2	mA
		R_{ext} = 2 kΩ; LED[23:0] = on; IREFx = FFh		-	-	6.7	mA
I_{DDIO}	supply current	on pin V_{DDIO}; operating mode; f_{SCLK} = 10 MHz; keep writing mode register (01h) with 00h		-	-	650	μA
I_{stb}	standby current	on pin V_{DD}; no load; f_{SCLK} = 0 Hz; MODE1[4] = 1; $V_I = V_{DD}$					
		V_{DD} = 3.3 V		-	170	600	μA
		V_{DD} = 5.5 V		-	170	700	μA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}		-	2	-	V
V_{PDR}	power-down reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[2] [3]	-	1	-	V
Inputs $\overline{\text{CS}}$, SDI, SCLK; output SDO							
V_{IL}	LOW-level input voltage			-0.5	-	+0.3V_{DDIO}	V
V_{IH}	HIGH-level input voltage			0.7V_{DDIO}	-	5.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = -3 mA at SDO		0.8V_{DDIO}	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA at SDO		-	-	0.2V_{DDIO}	V
I_L	leakage current	$V_I = V_{DDIO}$ or V_{SS}		-1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$		-	6	10	pF
Current controlled outputs (LED[23:0])							
$I_{O(LEDn)}$	output current on pin LEDn	V_O = 0.4 V; IREFx = 80h; R_{ext} = 2 kΩ	[3]	15	16	17	mA
		V_O = 0.4 V; IREFx = FFh; R_{ext} = 2 kΩ	[3]	30	32	34	mA
$\Delta I_{O\_Absolute}$	absolute output current variation	V_O = 0.4 V; all channels on; IREFx >= 20h R_{ext} = 2 kΩ; refer to ideal value; guaranteed by design				±6.5	%
		V_O = 0.4 V; all channels on; IREFx < 20h; R_{ext} = 2 kΩ; refer to ideal value; guaranteed by design				±8	%
$\Delta I_{O\_mis\_p2p}$	part to part output current mismatch	all channels on; IREFx = FFh. R_{ext} = 2 kΩ; V_O = 0.4 V; average value of 24 output current of each device, comparing to ideal value	[4]	-	-	±6	%

Table 28. Static characteristics *...continued*

V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$\Delta I_{O\_mis\_c2c}$	channel to channel output current mismatch	all channels on; IREFx = FFh. R_{ext} = 2 kΩ; V_O = 0.4 V; each channel current comparing to average current of 24 channels	[5]	-	-	±4	%
$V_{reg(drv)}$	driver regulation voltage	minimum regulation voltage; IREFx = FFh; R_{ext} = 2 kΩ		0.4		5.5	V
$I_{L(off)}$	off-state leakage current	V_O = 5 V		-	-	1	μA
V_{trip}	trip voltage	short LED protection; Error flag trips during verification test if $V_O \geq V_{trip}$; R_{ext} = 2 kΩ		1.85	1.96	-	V
$\overline{\text{OE}}$ input, $\overline{\text{RESET}}$ input							
V_{IL}	LOW-level input voltage			-0.5	-	+0.3V_{DDIO}	V
V_{IH}	HIGH-level input voltage			0.7V_{DDIO}	-	5.5	V
I_{LI}	input leakage current			-1	-	+1	μA
C_i	input capacitance		[3]	-	3.7	5	pF
Overtemperature protection							
$T_{th(otp)}$	overtemperature protection threshold temperature	rising	[3]	130	-	150	°C
		hysteresis	[3]	15	-	30	°C

[1] Typical limits at V_{DD} = 3.3 V, T_{amb} = 25 °C.

[2] V_{DD} must be lowered to 1 V in order to reset part.

[3] Value not tested in production, but guaranteed by design and characterization.

[4] Part-to-part mismatch is calculated:

$$\Delta\% = \left(\frac{\left(\frac{I_{O(LED0)} + I_{O(LED1)} + \ldots + I_{O(LED22)} + I_{O(LED23)}}{24} - ideal output current \right)}{ideal output current} \right) \times 100$$

where 'ideal output current' = 31.875 mA (R_{ext} = 2 kΩ, IREFx = FFh).

[5] Channel-to-channel mismatch is calculated:

$$\Delta\% = \left(\frac{I_{O(LEDn)} (\text{where n = 0 to 23})}{\left(\frac{I_{O(LED0)} + I_{O(LED1)} + \ldots + I_{O(LED22)} + I_{O(LED23)}}{24} \right)} - 1 \right) \times 100$$

13 Dynamic characteristics

Table 29. Dynamic characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency			0	-	10	MHz
t_{LOW}	LOW period of the SCLK clock			50	-	-	ns
t_{HIGH}	HIGH period of the SCLK clock			50	-	-	ns
t_{DS}	data set-up time			10	-	-	ns
t_{DH}	data hold time			20	-	-	ns
t_{CSS}	chip select asserted to SCLK rise set-up time			10	-	-	ns
t_{CSH}	SCLK fall to chip select deasserted hold time			0	-	-	ns
t_{CS_HI}	minimum chip select deasserted HIGH time			40	-	-	ns

Table 29. Dynamic characteristics[1] ***...continued***

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(SDO)}$	SDO delay time	C_L = 50 pF		-	-	40	ns
$t_{d(LED0)}$	The latency time between $\overline{\text{OE}}$ pin assertion to LED channel 0 output on			-	-	1[2]	μs
$t_{OE(disable)}$	$\overline{\text{OE}}$ pin disable (HIGH) period time			250	-	-	ns
$t_{OE(enable)}$	$\overline{\text{OE}}$ pin enable (LOW) period time			250	-	-	ns

[1] All parameters tested at V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = +25 °C. Specifications over temperature are guaranteed by design.

[2] Guaranteed by design.

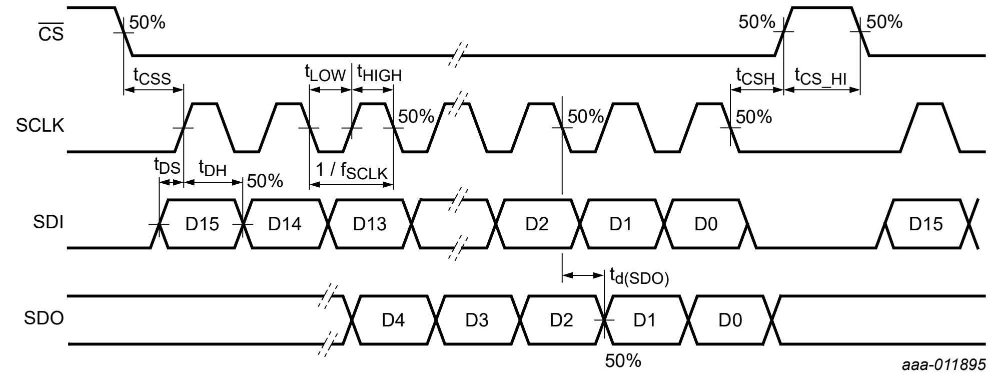

$\overline{\text{CS}}$
50%
50%
50%
t_{CSS}
t_{LOW}
t_{HIGH}
t_{CSH}
t_{CS_HI}
SCLK
50%
50%
50%
t_{DS}
t_{DH}
50%
1 / f_{SCLK}
SDI
D15
D14
D13
D2
D1
D0
D15
$t_{d(SDO)}$
SDO
D4
D3
D2
D1
D0
50%
aaa-011895

Figure 18. Definition of timing

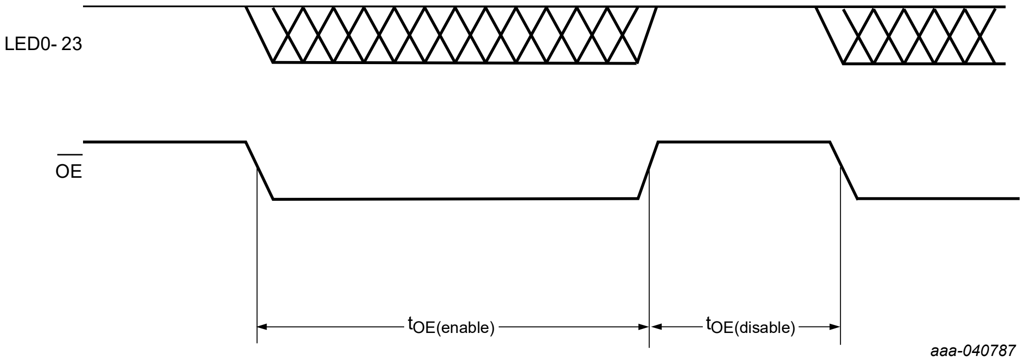
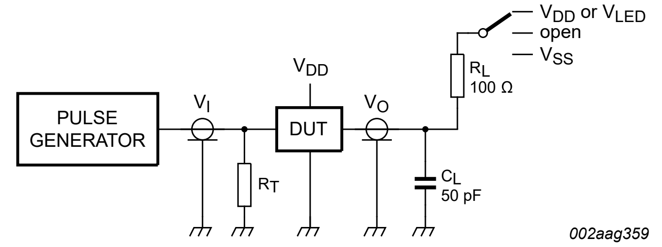

LED0- 23
$\overline{\text{OE}}$
$t_{OE(enable)}$
$t_{OE(disable)}$
aaa-040787

Figure 19. $\overline{\text{OE}}$ pin timing

14 Test information


V_{DD} or V_{LED}
open
V_{SS}
R_L
100 Ω
V_{DD}
PULSE GENERATOR
V_I
DUT
V_O
R_T
C_L
50 pF
002aag359

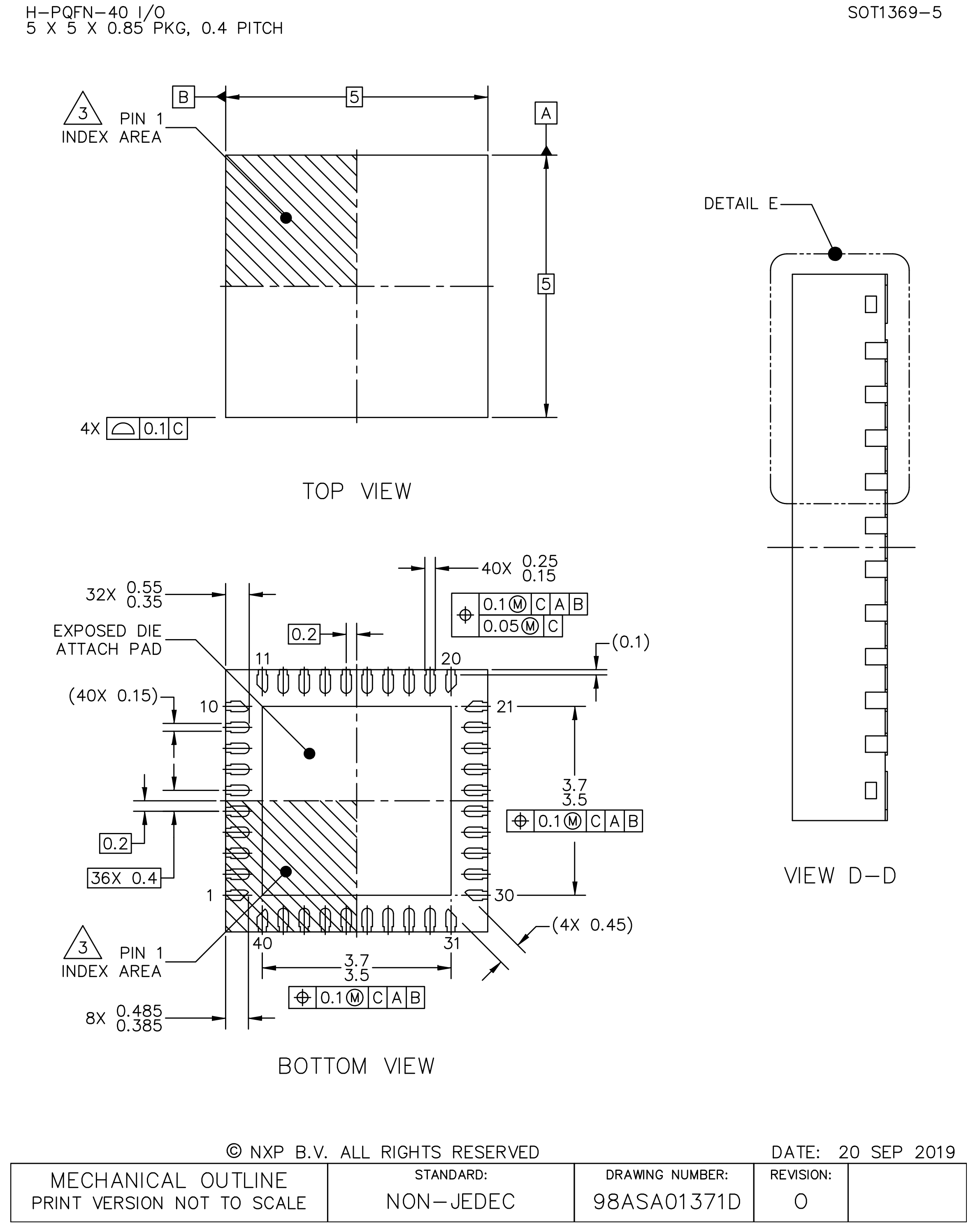
R_L = Load resistor for LEDn.

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Figure 20. Test circuitry for switching times

15 Package outline


H-PQFN-40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH
SOT1369-5
3
PIN 1
INDEX AREA
B
5
A
5
4X ⌓ 0.1 C
TOP VIEW
DETAIL E
VIEW D-D
40X 0.25 0.15
32X 0.55 0.35
0.1 Ⓜ C A B
0.05 Ⓜ C
0.2
EXPOSED DIE
ATTACH PAD
(0.1)
11
20
(40X 0.15)
10
21
3.7
3.5
0.1 Ⓜ C A B
0.2
36X 0.4
1
30
(4X 0.45)
40
31
3
PIN 1
INDEX AREA
3.7
3.5
0.1 Ⓜ C A B
8X 0.485 0.385
BOTTOM VIEW
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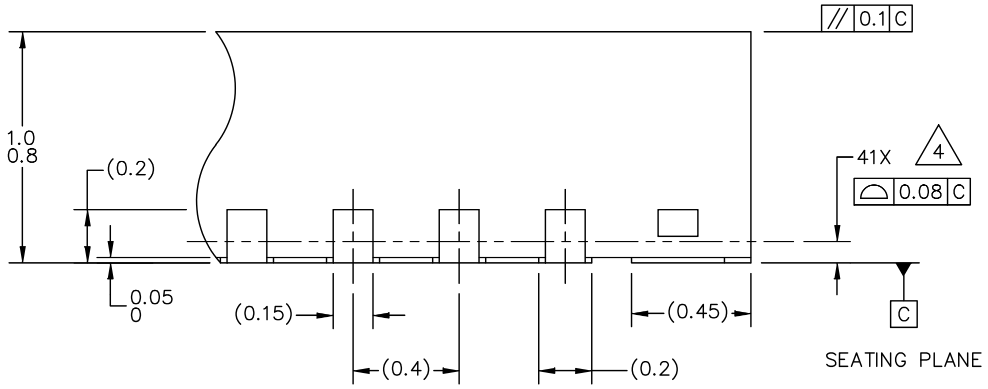
DATE: 20 SEP 2019
MECHANICAL OUTLINE
PRINT VERSION NOT TO SCALE
STANDARD:
NON-JEDEC
DRAWING NUMBER:
98ASA01371D
REVISION:
O

Figure 21. Package outline SOT1369-5 (HVQFN40) (1 of 3)

H-PQFN-40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369-5


// 0.1 C
1.0
0.8
(0.2)
41X
4
0.08 C
0.05
0
(0.15)
(0.45)
(0.4)
(0.2)
C
SEATING PLANE

DETAIL E
VIEW ROTATED 90° CW

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	NON-JEDEC	98ASA01371D	O	

Figure 22. Package outline SOT1369-5 (HVQFN40) (2 of 3)

H–PQFN–40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369–5

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. △ PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. △ COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.15 MM.

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Figure 23. Package outline SOT1369-5 (HVQFN40) (3 of 3)

16 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 30 and Table 31

Table 30. SnPb eutectic process (from J-STD-020D)

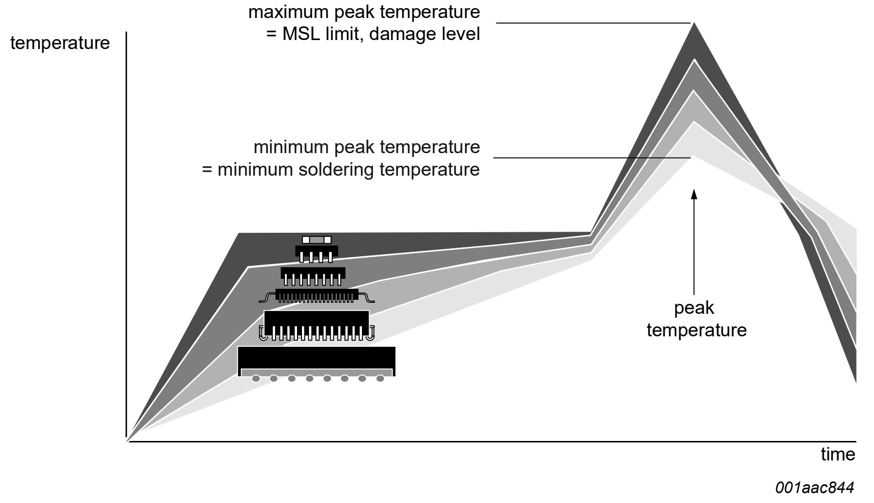
Package thickness (mm)	**Package reflow temperature (°C)**	
	Volume (mm³)	
	< 350	**≥ 350**
< 2.5	235	220
≥ 2.5	220	220

Table 31. Lead-free process (from J-STD-020D)

Package thickness (mm)	**Package reflow temperature (°C)**		
	Volume (mm³)		
	< 350	**350 to 2000**	**> 2000**
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.


temperature
maximum peak temperature
= MSL limit, damage level
minimum peak temperature
= minimum soldering temperature
peak
temperature
time
001aac844

MSL: Moisture Sensitivity Level

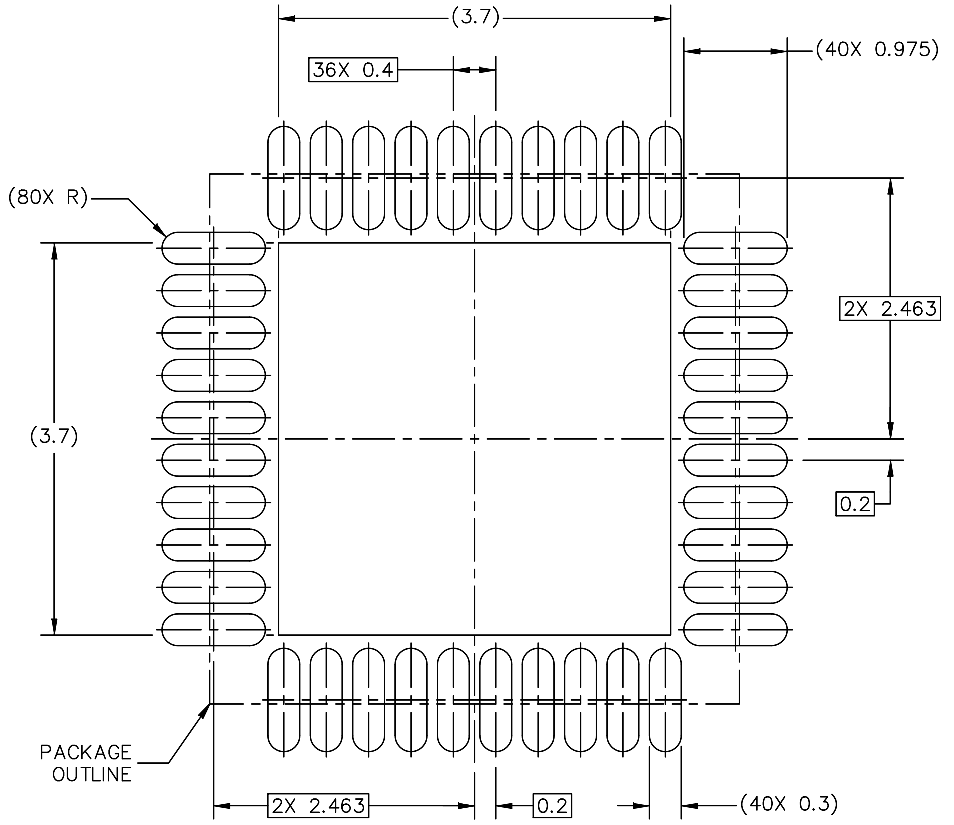
Figure 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

18 Soldering: PCB footprints

H−PQFN−40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369−5



PCB DESIGN GUIDELINES − SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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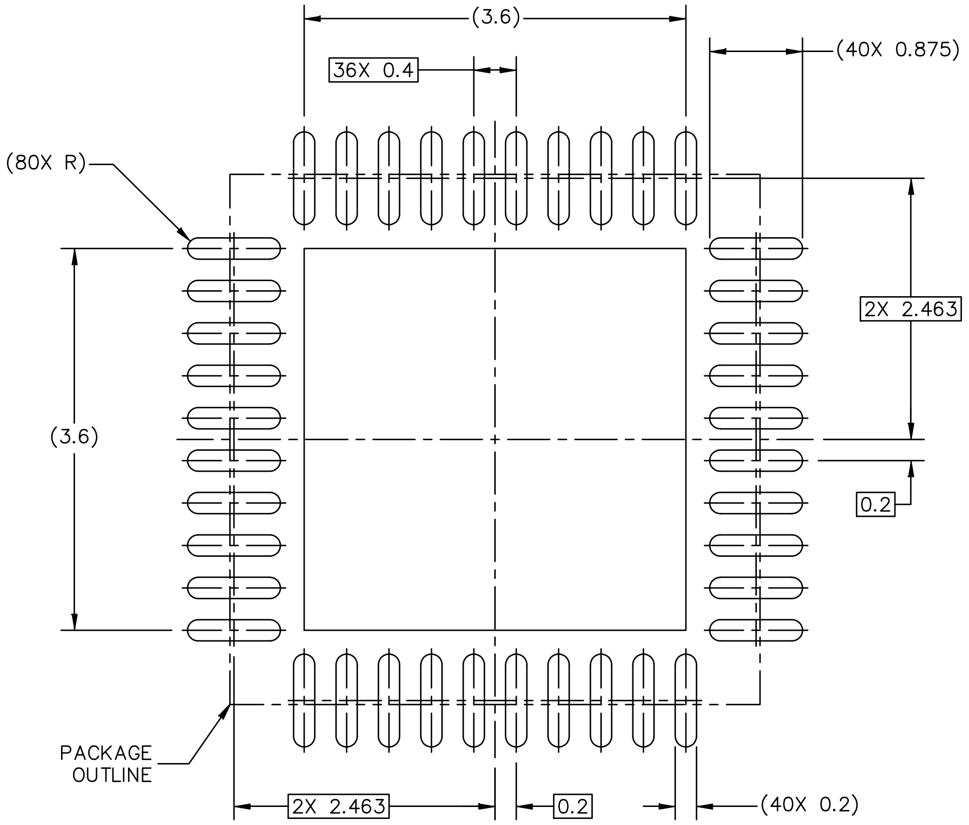
Figure 25. PCB footprint for SOT1369-5 (HVQFN40); solder mask opening pattern

H-PQFN-40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369-5



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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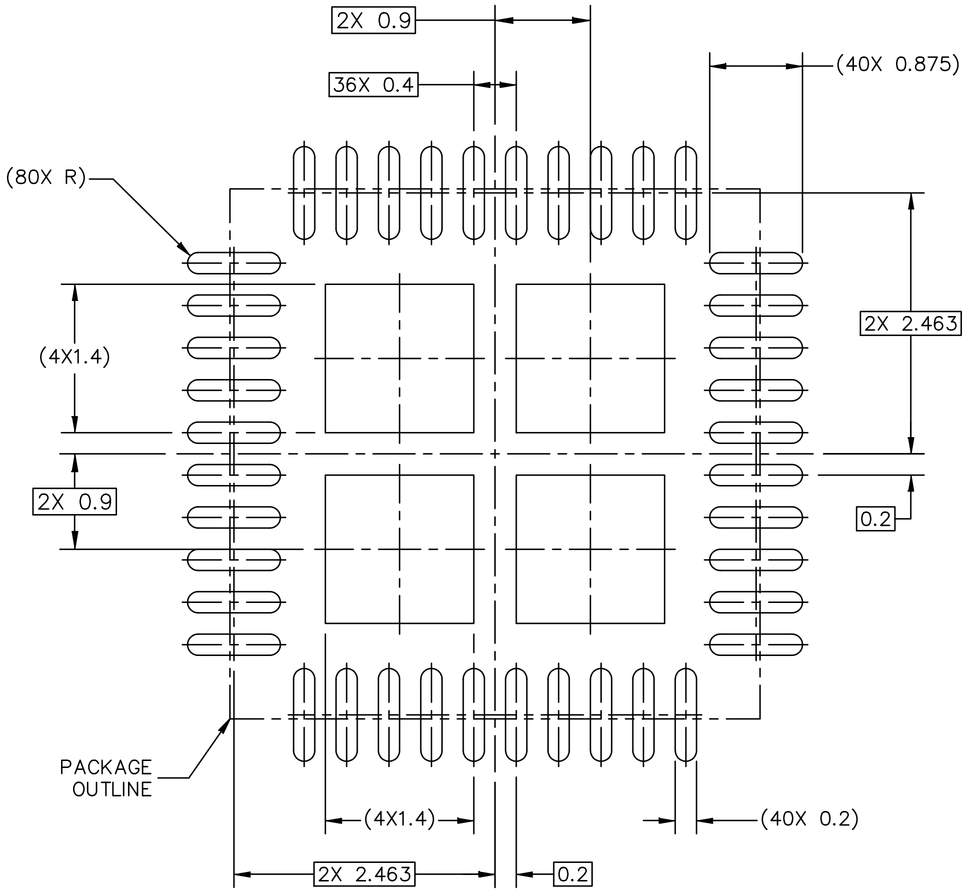
Figure 26. PCB footprint for SOT1369-5 (HVQFN40); I/O pads and solderable area

H-PQFN-40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369-5



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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Figure 27. PCB footprint for SOT1369-5 (HVQFN40); solder paste stencil

19 Abbreviations

Table 32. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DAC	Digital-to-Analog Converter
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
LED	Light Emitting Diode
LSB	Least Significant Bit
MCU	MicroController Unit
MISO	Master In, Slave Out
MOSI	Master Out, Slave In
MSB	Most Significant Bit
NMOS	Negative-channel Metal-Oxide Semiconductor
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus
SPI	Serial Peripheral Interface

20 Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9957 v.2.1	20211022	Product data sheet	202110025I	PCA9957 v.2.0
Modifications:	• Table 3: Updated description for $\overline{CS}$ • Section 8.1: Updated SDO information in sections $\overline{CS}$ and SDO			
PCA9957 v.2.0	20210225	Product data sheet	-	PCA9957 v.1.0
Modifications:	• Added V_{trip} minimum of 1.85 V • Section 7.2.13 "LED error detection": Corrected "if there is a fault condition in any of the 16 channels" to "if there is a fault condition in any of the 24 channels" • Section 7.2.9 "OFFSET — LEDn output delay offset register": Updated register description information for bits 3:0 • Section 13 "Dynamic characteristics": Added $\overline{OE}$ pin enable/disable min time and chart			
PCA9957 v.1.0	20191024	Product data sheet	-	-

21 Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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