

SLG59M1527V

Dual 4.5 A Load Switch

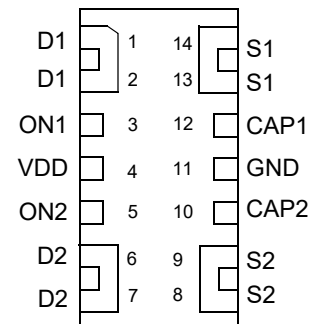
General Description

The SLG59M1527V is designed for load switching application. The part comes with two 4.5 A rated MOSFETs switched on by two ON control pins. Each MOSFETs turn on time is independently adjusted by an external capacitor.

Features

- Two 4.5 A independent MOSFETs
- Two Integrated VGS Charge Pumps
- Two internal discharges per channel for gate and source
- Independent Ramp Control
- Protected by thermal shutdown with current limit
- Pb-Free / RoHS Compliant
- Halogen-Free
 - STDFN-14L, 1 x 3 x 0.55 mm

Pin Configuration

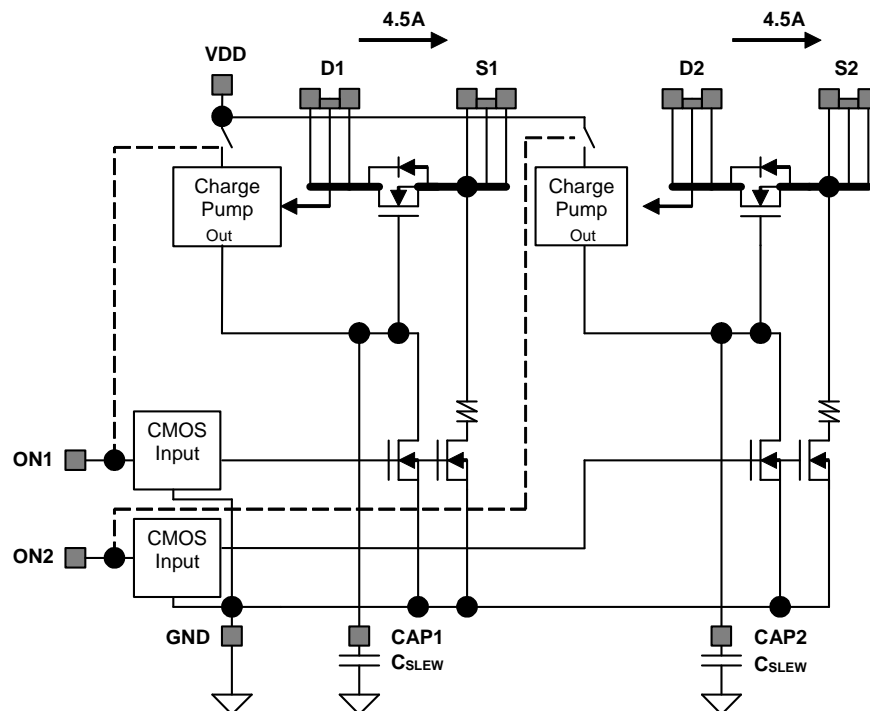


**14-pin STDFN
(Top View)**

Applications

- Ideal for switching ON and OFF S0 +5.0 and 3.3 V power rails with associated support circuitry discharges.
- Ideal for switching ON and OFF power rails 5 V or less.
- Can use either channel up to 4.5 A with combined maximum current of 8.5 A
- Maximum load capacitance of 1000 μ F for each Channel Source terminal.

Block Diagram



Do not probe CAP1 (PIN 12) or CAP2 (PIN 10) with low impedance probe.

SLG59M1527V

Dual 4.5 A Load Switch

Pin Description

Pin #	Pin Name	Type	Pin Description
1, 2	D1	MOSFET	Drain/Input terminal of Power MOSFET Channel 1. Connect a 10 μ F (or larger) low ESR capacitor from this pin to GND. Capacitors used at D1 should be rated at 10 V or higher.
3	ON1	Input	A low-to-high transition on this pin closes the Channel 1 of load switch. ON1 is an asserted-HIGH, level-sensitive CMOS input with $ON_V_{IL} < 0.3$ V and $ON_V_{IH} > 0.85$ V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. While there is an internal pull down circuit to ground (~ 4 M Ω), it is allowed this pin to be open-circuited.
4	VDD	VDD	VDD supplies the power for the operation of the load switch and internal control circuitry where its range is 2.5 V $\leq V_{DD} \leq 5.5$ V. Bypass the VDD pin to GND with a 0.1 μ F (or larger) capacitor.
5	ON2	Input	A low-to-high transition on this pin closes the Channel 2 of load switch. ON2 is an asserted-HIGH, level-sensitive CMOS input with $ON_V_{IL} < 0.3$ V and $ON_V_{IH} > 0.85$ V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. While there is an internal pull down circuit to ground (~ 4 M Ω), it is allowed this pin to be open-circuited.
6, 7	D2	MOSFET	Drain/Input terminal of Power MOSFET Channel 2. Connect a 10 μ F (or larger) low ESR capacitor from this pin to GND. Capacitors used at D2 should be rated at 10 V or higher.
8, 9	S2	MOSFET	Source/Output terminal of Power MOSFET Channel 2. Connect a 10 μ F (or larger) low ESR capacitor from this pin to GND. Capacitors used at S2 should be rated at 10 V or higher.
10	CAP2	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP2 pin to GND, sets the V_{S2} slew rate and overall turn on time of the SLG59M1527V. For best performance, the range for C_{SLEW} values are 1 nF $\leq C_{SLEW} \leq 22$ nF. Capacitors used at the CAP2 pin should be rated at 10V or higher.
11	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.
12	CAP1	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP1 pin to GND, sets the V_{S1} slew rate and overall turn on time of the SLG59M1527V. For best performance, the range for C_{SLEW} values are 1 nF $\leq C_{SLEW} \leq 22$ nF. Capacitors used at the CAP1 pin should be rated at 10V or higher.
13, 14	S1	MOSFET	Source/Output terminal of Power MOSFET Channel 1. Connect a 10 μ F (or larger) low ESR capacitor from this pin to GND. Capacitors used at S1 should be rated at 10 V or higher.

Ordering Information

Part Number	Type	Production Flow
SLG59M1527V	STDFN-14L	Industrial, -40 °C to 85 °C
SLG59M1527VTR	STDFN-14L (Tape and Reel)	Industrial, -40 °C to 85 °C

SLG59M1527V

Dual 4.5 A Load Switch

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply Voltage		--	--	6	V
T _S	Storage Temperature		-65	--	150	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	--	--	V
W _{DIS}	Package Power Dissipation		--	--	1.2	W
I _{DS} _{MAX}	Max Continuous Switch Current				4.5	A
MOSFET I _{DS} _{PK}	Peak Current from Drain to Source	For no more than 10 continuous seconds out of every 100 seconds	--	--	6	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply Voltage		2.5	--	5.5	V
I _{DD}	Power Supply Current	when OFF	--	0.1	1	μA
	Power Supply Current, both channels	when ON, no Load	--	50	75	μA
R _{DS} _{ON[1,2]}	ON Resistance	T _A = 25 °C; I _{DS} = 100 mA	--	14.5	18	mΩ
		T _A = 70 °C; I _{DS} = 100 mA	--	17	22	mΩ
		T _A = 85 °C; I _{DS} = 100 mA	--	18	23	mΩ
		T _A = 85 °C; I _{DS} = 4.5 A	--	19.3	25.1	mΩ
MOSFET I _{DS}	Current from D[1,2] to S[1,2]	Continuous	--	--	4.5	A
V _{D[1,2]}	Load Switch input Voltage		0.9	--	V _{DD}	V
T _{ON} _{Delay}	ON Delay Time	50% ON to V _{S[1,2]} Ramp Start	--	300	500	μs
T _{Total_ON}	Total Turn On Time	50% ON to 90% V _{S[1,2]}	Set by External C _{SLEW} ¹			ms
		Example: C _{SLEW} = 4 nF, V _{DD} = V _{D[1,2]} = 5 V; C _{LOAD} = 10 μF; R _{LOAD} = 20 Ω	--	2.0	--	ms
V _{S(SR)}	V _{S[1,2]} Slew Rate	10% V _S to 90% V _S	Set by External C _{SLEW} ¹			V/ms
		Example: C _{SLEW} = 4 nF, V _{DD} = V _{D[1,2]} = 5 V; C _{LOAD} = 10 μF; R _{LOAD} = 20 Ω	--	3.0	--	V/ms
C _{LOAD}	Output Load Capacitance	C _{LOAD} connected from S[1,2] to GND	--	--	1000	μF
R _{DISCHRG}	Output Discharge Resistance	V _{DD} = 2.5 V to 5.5 V; V _{S[1,2]} = 0.4 V Input bias	100	150	300	Ω
ON_V _{IH}	High Input Voltage on ON pin		0.85	--	V _{DD}	V
ON_V _{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V

SLG59M1527V

Dual 4.5 A Load Switch

Electrical Characteristics (continued)

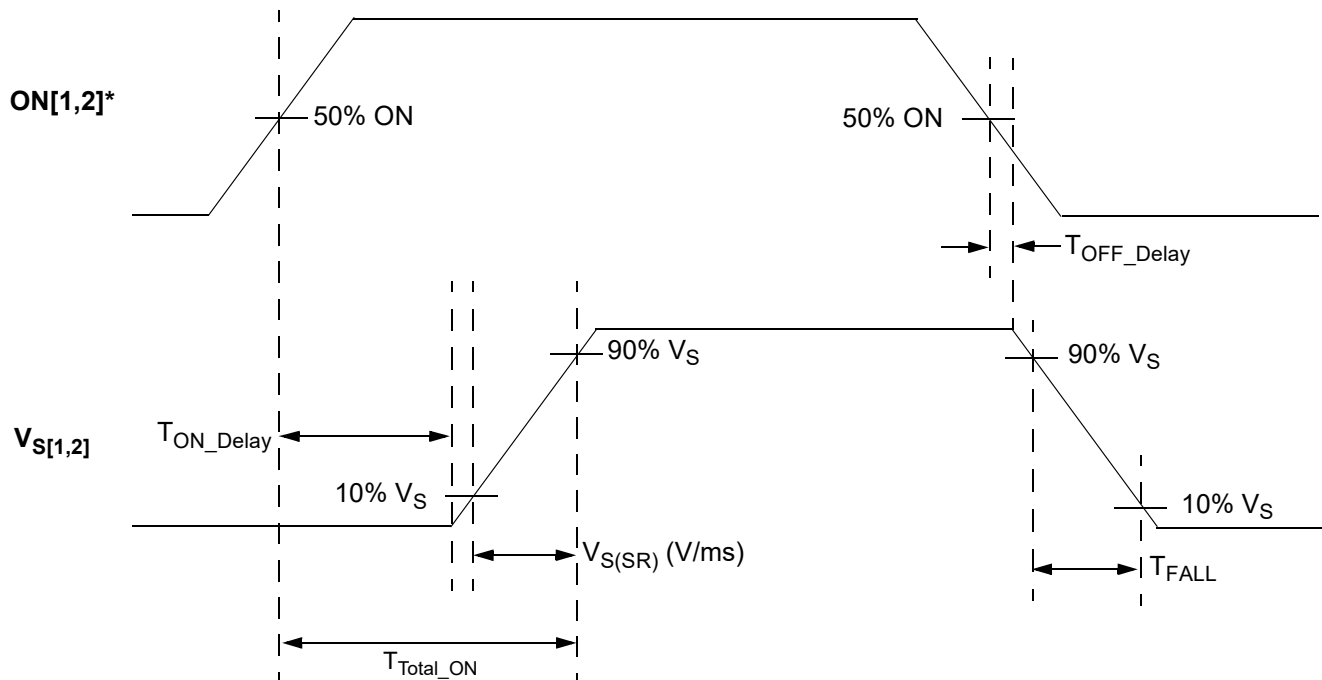
$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values are at $T_A = 25\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{LIMIT}	Active Current Limit, I_{ACL}	MOSFET will automatically limit current when $V_{S[1,2]} > 250\text{ mV}$	--	6.0	--	A
	Short Circuit Current Limit, I_{SCL}	MOSFET will automatically limit current when $V_{S[1,2]} < 250\text{ mV}$	--	0.5	--	A
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	$^{\circ}\text{C}$
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	$^{\circ}\text{C}$
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to $V_{S[1,2]}$ Fall Start; $V_{DD} = V_{D[1,2]} = 5\text{ V}$	--	--	15	μs

Notes:

1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information when available.

T_{ON_Delay} , $V_{S(SR)}$, and T_{Total_ON} Timing Details

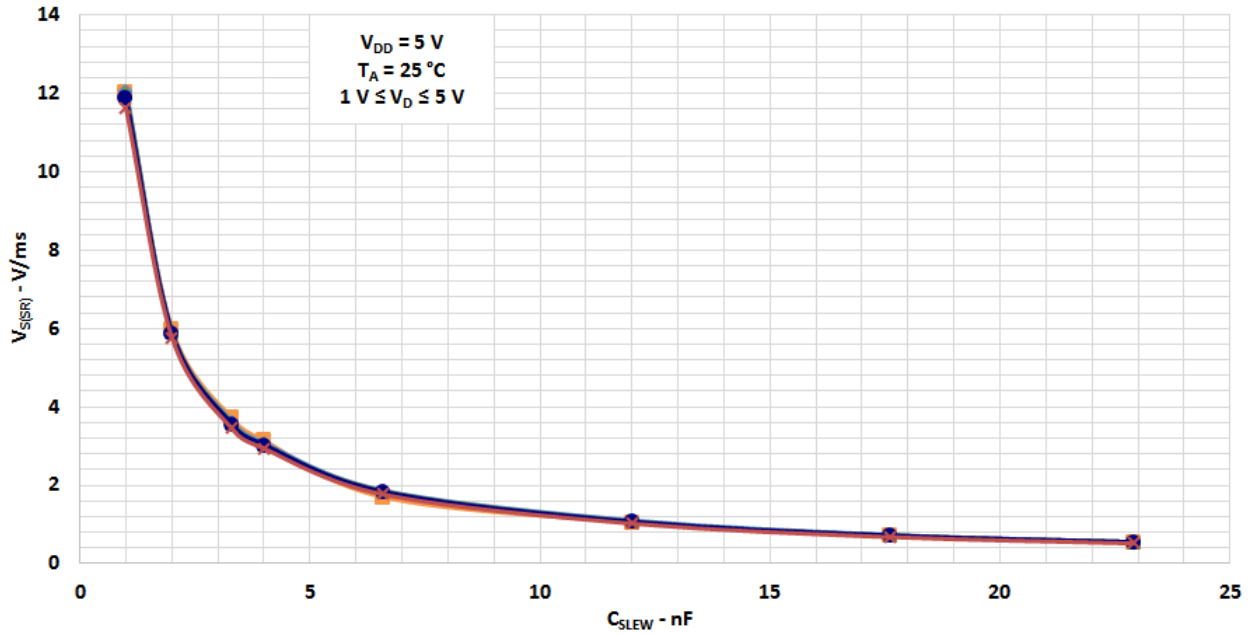


*Rise and Fall Times of the ON Signal are 100 ns

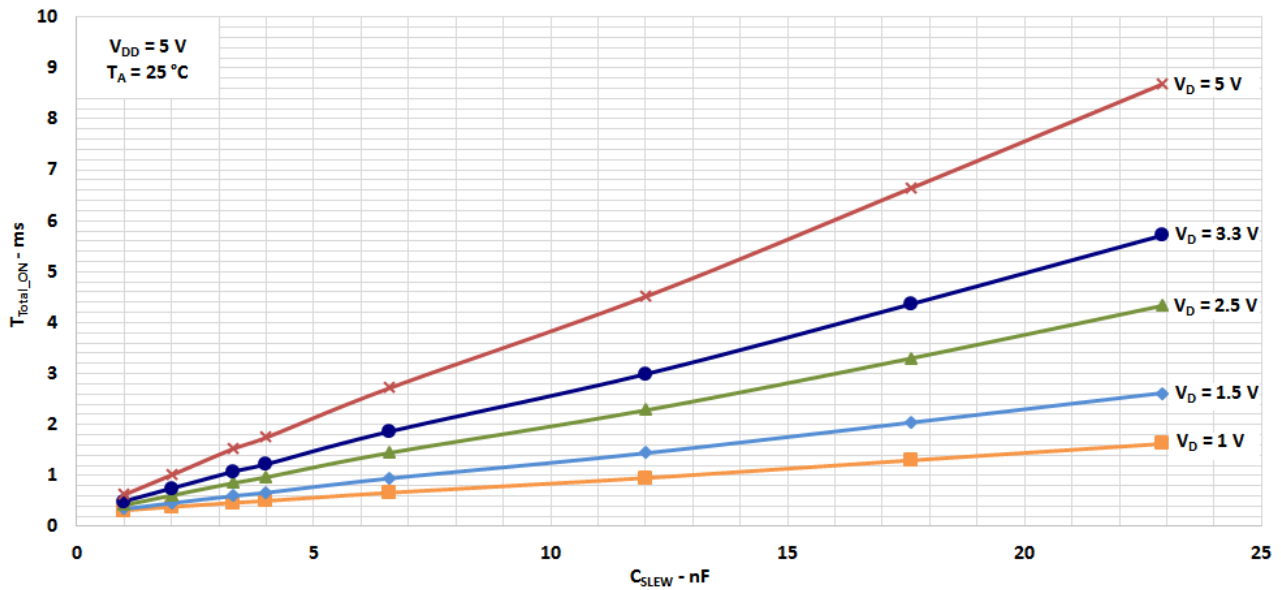
SLG59M1527V

Dual 4.5 A Load Switch

Slew Rate vs. C_{SLEW}



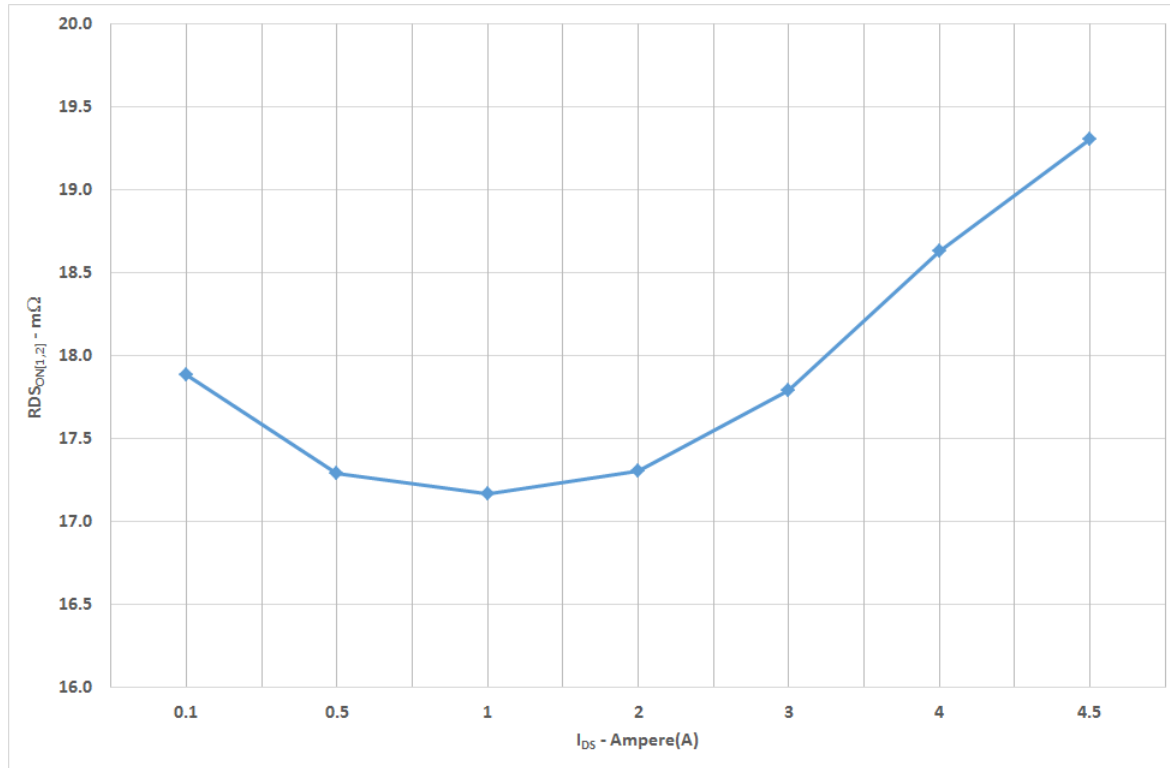
T_{Total_ON} vs. C_{SLEW}



SLG59M1527V

Dual 4.5 A Load Switch

RDS_{ON[1,2]} vs. I_{DS} @ T_A = 85 °C



SLG59M1527V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_{D[1,2]} after V_{DD} exceeds 1 V. Then allow V_{D[1,2]} to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_{D[1,2]} need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 μF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_{D[1,2]} higher than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_{D[1,2]} have reached their steady-state values, the load switch timing parameters may differ from datasheet specifications.

The slew rate of output V_{S[1,2]} follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1527V Current Limiting

The SLG59M1527V has two modes of current limiting, differentiated by the output (Source pin) voltage.

1. Standard Current Limiting Mode (with Thermal Protection)

When V_{S[1,2]} > 250 mV, the output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceeding the Active Current Limit.

SLG59M1527V

Dual 4.5 A Load Switch

However, if an overload condition persists, the die temperature rise due to the increased FET resistance while at maximum current can activate Thermal Protection. If the die temperature exceeds the $THERM_{ON}$ specification, the FET is shut completely OFF, allowing the die to cool. When the die cools to the $THERM_{OFF}$ temperature, the FET is allowed to turn back on. This process may repeat as long as the overload condition is present.

2. Short Circuit Current Limiting Mode (with Thermal Protection)

When $V_{S[1,2]} < 250$ mV (which is the case with a hard short, such as a solder bridge on the power rail), the current is limited to approximately 500 mA. Thermal Protection is also present, but since the Short Circuit Current Limit is much lower than Standard Current Limit, activation may only occur at higher ambient temperatures.

Power Dissipation

The junction temperature of the SLG59M1527V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON} -generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1527V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON1} \times I_{DS1}^2) + (RDS_{ON2} \times I_{DS2}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$RDS_{ON[1,2]}$ = Channel 1 and Channel 2 Power MOSFET ON resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

Power Dissipation (continued)

where:

T_J = Die junction temperature, in Celsius degrees ($^{\circ}C$)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt ($^{\circ}C/W$) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees ($^{\circ}C$)

In nominal operating mode, the SLG59M1527V's power dissipation can also be calculated by taking into account the voltage drop across each switch ($V_{Dx} - V_{Sx}$) and the magnitude of that channel's output current (I_{DSx}):

$$PD_{TOTAL} = [(V_{D1} - V_{S1}) \times I_{DS1}] + [(V_{D2} - V_{S2}) \times I_{DS2}] \text{ or}$$

$$PD_{TOTAL} = [(V_{D1} - (R_{LOAD1} \times I_{DS1})) \times I_{DS1}] + [(V_{D2} - (R_{LOAD2} \times I_{DS2})) \times I_{DS2}]$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$V_{D[1,2]}$ = Channel 1 and Channel 2 Input Voltage, in Volts (V), respectively

$R_{LOAD[1,2]}$ = Channel 1 and Channel 2 Output Load Resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 output current, in Amps (A), respectively

$V_{S[1,2]}$ = Channel 1 and Channel 2 output voltage, or $R_{LOAD[1,2]} \times I_{DS[1,2]}$, respectively

For more information on GreenFET load switch features, please visit our website and see App Note "AN-1068 GreenFET and High Voltage GreenFET Load Switch Basics".

SLG59M1527V

Dual 4.5 A Load Switch

Layout Guidelines:

1. The VDD pin needs a 0.1 μ F (or larger) external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG59M1527V's pin 4.
2. Since the D1, D2, S1 and S2 pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 1](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1527V's D1, D2, S1 and S2 pins;
4. The GND pin should be connected to system analog or power ground plane.
5. 2 oz. copper is recommended for high current operation.

SLG59M1527V Evaluation Board:

A GreenFET Evaluation Board for SLG59M1527V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M1527V here

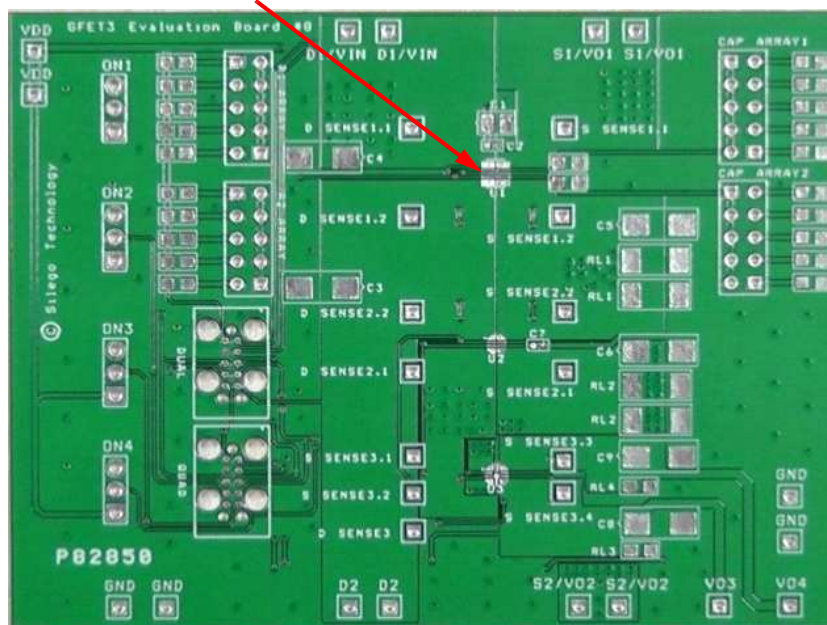


Figure 1. SLG59M1527V Evaluation Board

SLG59M1527V

Dual 4.5 A Load Switch

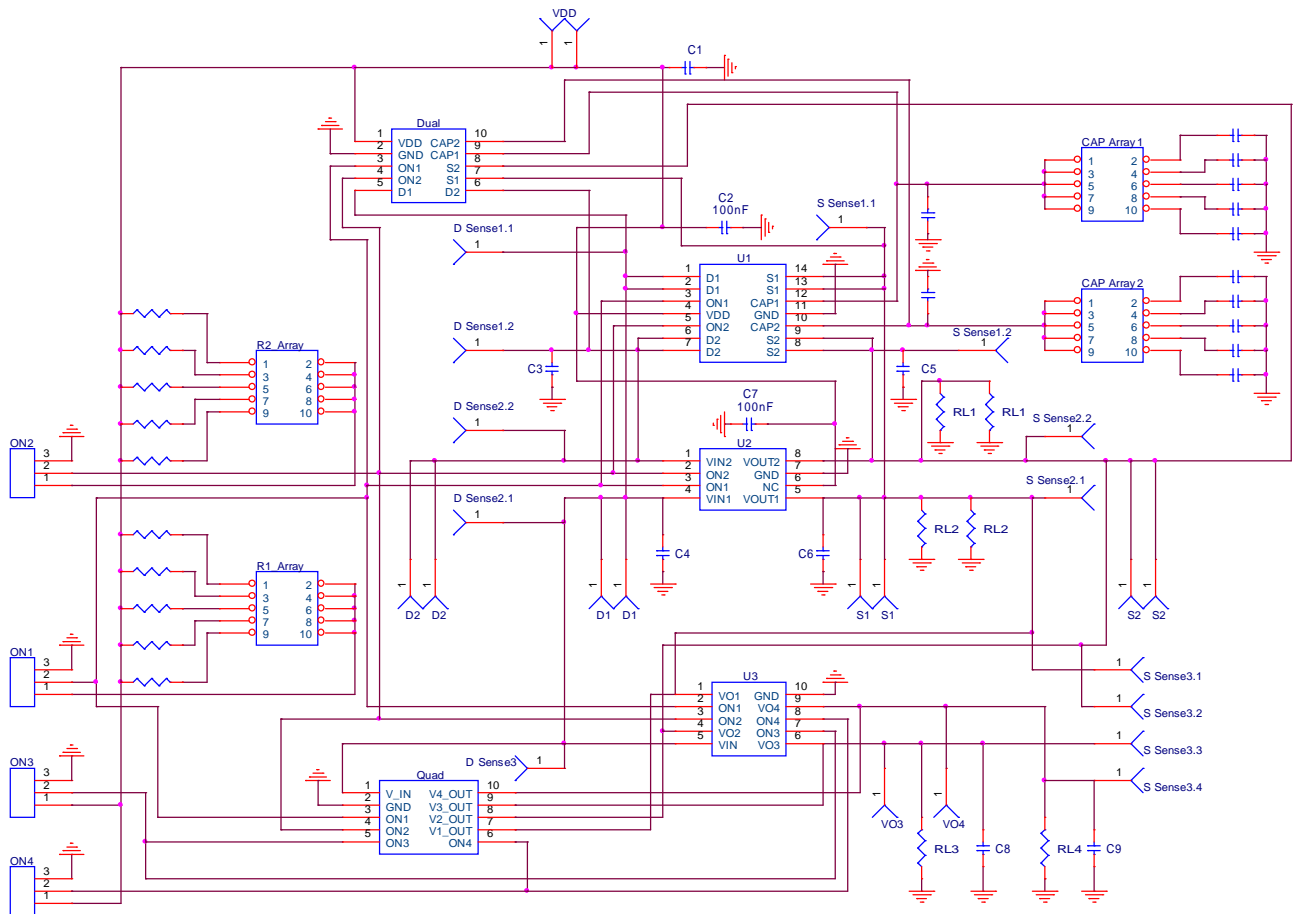


Figure 2. SLG59M1527V Evaluation Board Connection Circuit

SLG59M1527V

Dual 4.5 A Load Switch

Basic Test Setup and Connections

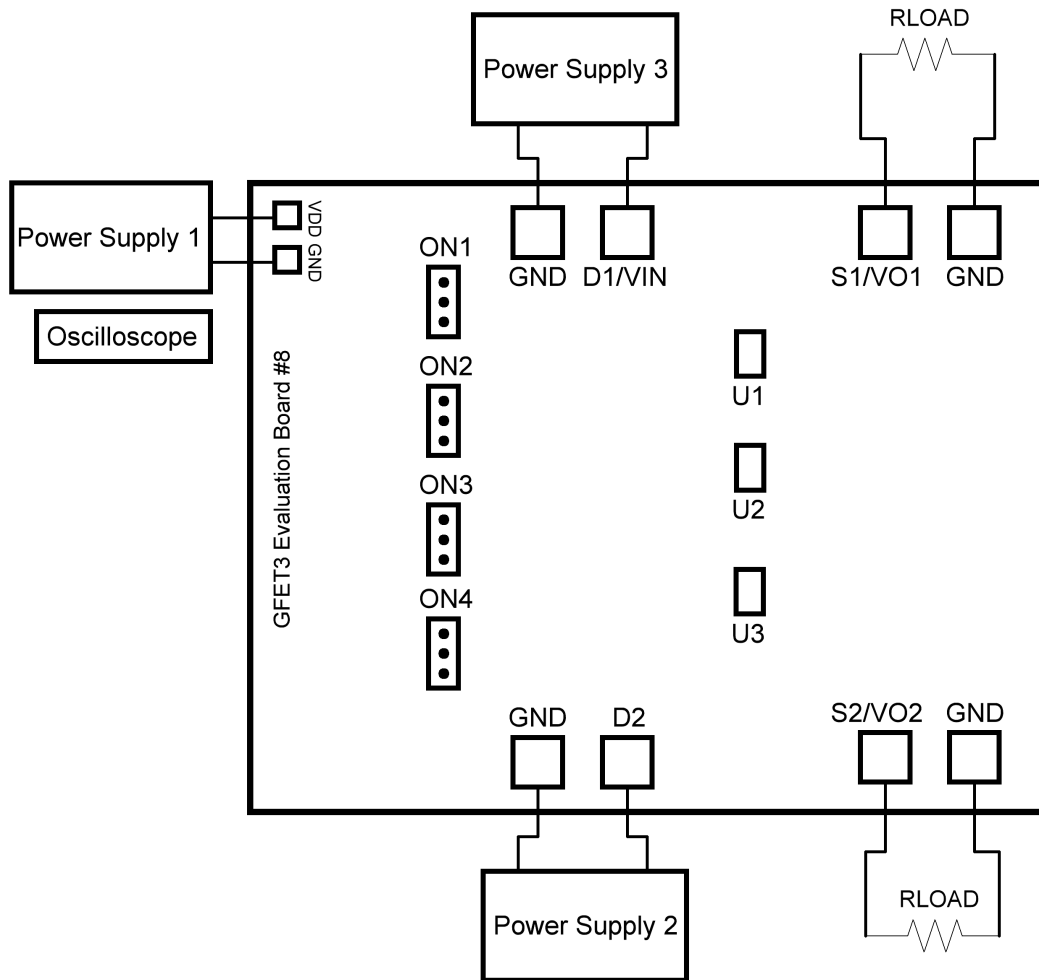


Figure 3. SLG59M1527V Evaluation Board Connection Circuit

EVB Configuration

1. Connect oscilloscope probes to D1/VIN, D2, S1/VO1, S2/VO2, ON1, ON2 etc.;
2. Turn on Power Supply 1 and set desired V_{DD} from 2.5 V...5.5 V range;
3. Turn on Power Supply 2, 3 and set desired $V_{D[1,2]}$ from 0.9 V... V_{DD} range;
4. Toggle the ON[1,2] signal High or Low to observe SLG59M1527V operation.

SLG59M1527V

Dual 4.5 A Load Switch

Package Top Marking System Definition



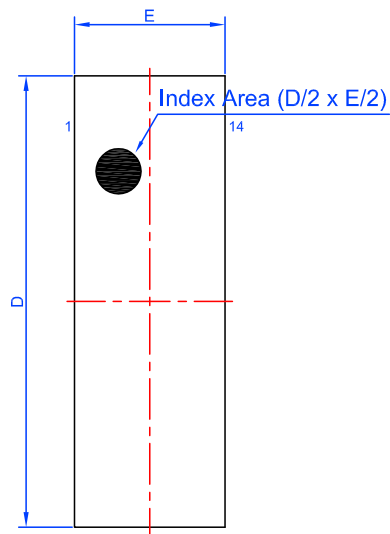
Part Number: SLG59M1527V
Production Part Code: KU

SLG59M1527V

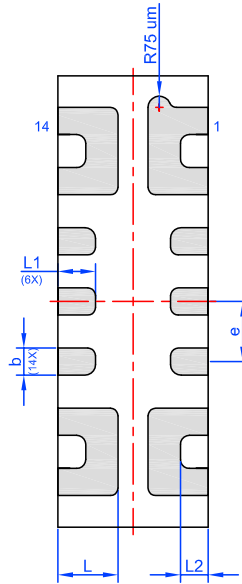
Dual 4.5 A Load Switch

Package Drawing and Dimensions

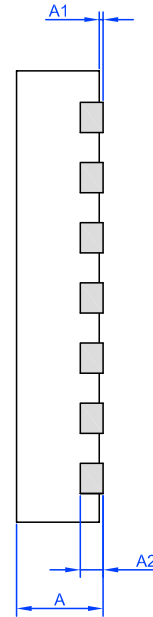
14 Lead STDFN Package 1 mm x 3 mm (Fused Lead)



Top View



BTM View



SIDE View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.20	0.25	0.30
e	0.40 BSC			L2	0.06	0.11	0.16

SLG59M1527V

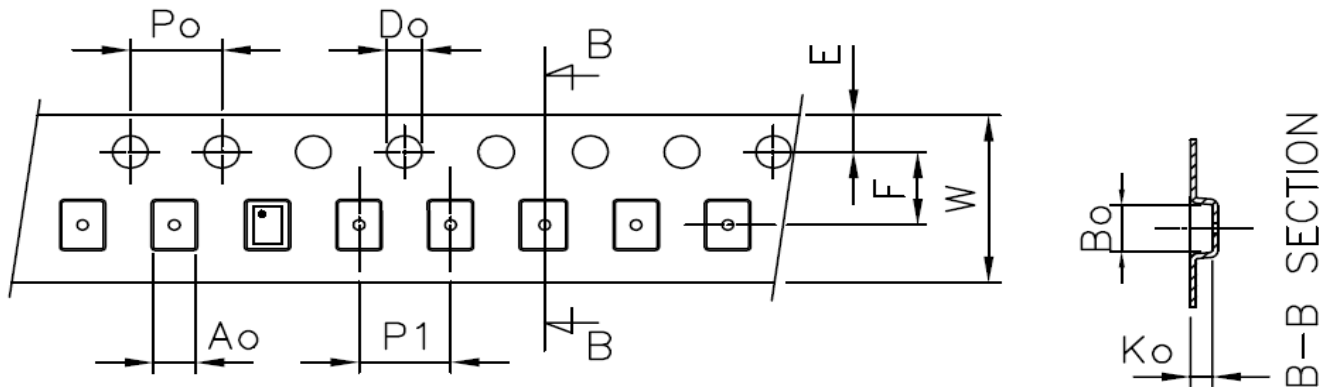
Dual 4.5 A Load Switch

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size	Units per Reel	Max Units per Box	Reel & Hub Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
						Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STDFN 14L	14	1x3x0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 14L	1.15	3.15	0.7	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.65 mm³ (nominal). More information can be found at www.jedec.org.

SLG59M1527V

Dual 4.5 A Load Switch

Revision History

Date	Version	Change
2/3/2022	1.06	Updated Company name and logo Fixed typos
12/10/18	1.05	Updated style and formatting Updated Charts Added Layout Guidelines
3/17/16	1.04	Added RDSon @ 4.5 A Added Application Notes Added RDSon vs IDS chart
12/15/15	1.03	Added Marking Information
4/20/14	1.02	Updated Block Diagram to separate CAP and OUT lines from Charge Pump
10/8/14	1.01	Updated VD Min from 1.0 V to 0.9 V
4/21/14	1.0	Production Release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.