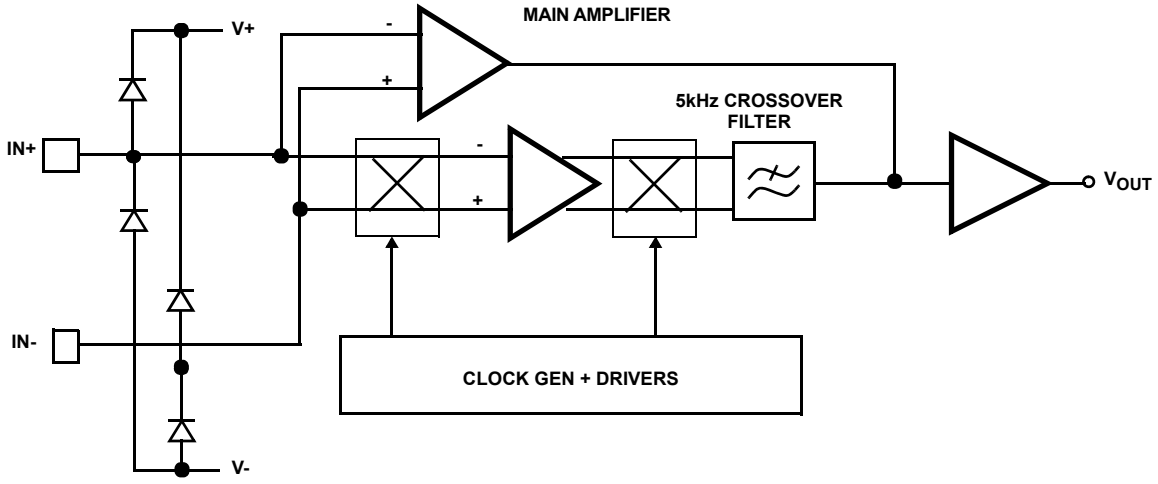
Block Diagram



Ordering Information

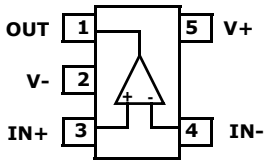
PART NUMBER	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)
ISL28133FHZ-T7 (Note 2)	BCFA (Note 5)	5 Ld SOT-23	P5.064A	Reel, 3k
ISL28133FHZ-T7A (Note 2)				Reel, 250
ISL28133FEZ-T7 (Note 2)	BHA (Note 5)	5 Ld SC70	P5.049	Reel, 3k
ISL28133ISENSEV1Z	Evaluation Board			
ISL28133EVAL1Z	Evaluation Board			
ISL28133CSENSEV1Z	Evaluation Board			

NOTES:

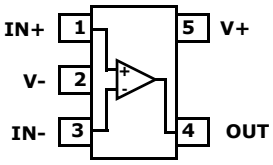
1. See TB347 for details on reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see the device information page for the ISL28133. For more information on MSL please see techbrief TB363.
5. The part marking is located on the bottom of the part.

Pin Configurations

ISL28133
(5 LD SOT-23)
TOP VIEW

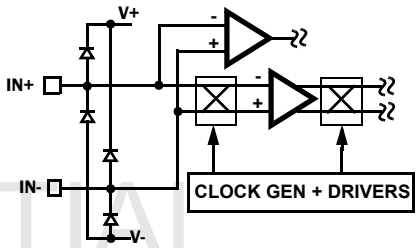
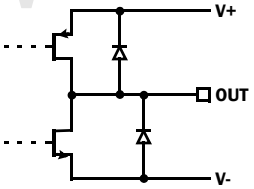


ISL28133
(5 LD SC-70)
TOP VIEW



TOP VIEW

Pin Descriptions

ISL28133 (5 Ld SOT23)	ISL28133 (5 Ld SC-70)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
3	1	IN+	Non-inverting input	 Circuit 1
2	2	V-	Negative supply	
4	3	IN-	Inverting input	(See Circuit 1)
1	4	OUT	Output	 Circuit 2
5	5	V+	Positive supply	

Absolute Maximum Ratings

Max Supply Voltage V+ to V- 6.5V
Max Voltage VIN to GND . . . . . -0.5V to 6.5V
Max Input Differential Voltage 6.5V
Max Input Current 20mA
Max Voltage VOUT to GND (10s) 6.5V
ESD Rating
Human Body Model 3000V
Machine Model 200V
Charged Device Model 1500V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 (Note 6, 7)	225	110
5 Ld SC-70 (Note 6)	206	N/A

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +125°C
Maximum Junction Temperature . . . . . 140°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See TB379 for details.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_+ = 5V, V_- = 0V, VCM = 2.5V, T_A = +25°C, R_L = Open, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-8	±2	8	µV
			-15.5		**15.5**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient			0.02	**0.075**	µV/°C
I_{OS}	Input Offset Current			-60		pA
I_B	Input Bias Current		-300	±30	300	pA
			-600		**600**	pA
Common Mode Input Voltage Range		V+ = 5.0V, V- = GND	-0.1		5.1	V
CMRR	Common Mode Rejection Ratio	VCM = -0.1V to 5.0V	118	125		dB
			115			dB
PSRR	Power Supply Rejection Ratio	Vs = 2V to 5.5V	110	138		dB
			110			dB
V_{OH}	Output Voltage Swing, High	R_L = 10kΩ	**4.965**	4.981		V
V_{OL}	Output Voltage Swing, Low	R_L = 10kΩ		18	**35**	mV
A_{OL}	Open Loop Gain	R_L = 1MΩ		174		dB
V_+	Supply Voltage	(Note 9)	1.8		5.5	V
I_S	Supply Current	R_L = OPEN		18	25	µA
					35	µA
I_{SC+}	Output Source Short Circuit Current	R_L = Short to ground or V+	13	17	26	mA
I_{SC-}	Output Sink Short Circuit Current		-26	-19	-13	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product f = 50kHz	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}		400		kHz
e_N V_{P-P}	Peak-to-Peak Input Noise Voltage	f = 0.01Hz to 10Hz		1.1		μV_{P-P}
e_N	Input Noise Voltage Density	f = 1kHz		65		nV/√(Hz)

Electrical Specifications

V_+ = 5V, V_- = 0V, VCM = 2.5V, T_A = +25°C, R_L = Open, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
i_N	Input Noise Current Density	f = 1kHz		72		fA/√(Hz)
		f = 10Hz		79		fA/√(Hz)
C_{in}	Differential Input Capacitance	f = 1MHz		1.6		pF
	Common Mode Input Capacitance			1.12		pF
TRANSIENT RESPONSE						
SR	Positive Slew Rate	V_{OUT} = 1V to 4V, R_L = 10kΩ		0.2		V/µs
	Negative Slew Rate			0.1		V/µs
t_r, t_f, Small Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = 0.1V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		1.1		µs
	Fall Time, t_f 10% to 90%			1.1		µs
t_r, t_f Large Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = 2V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		8		µs
	Fall Time, t_f 10% to 90%			10		µs
t_s	Settling Time to 0.1%, 2V_{P-P} Step	A_V = +1, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		35		µs

NOTES:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
9. Parts are 100% tested with a minimum operating voltage of 1.8V to a VOS limit of ±15µV.

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open.

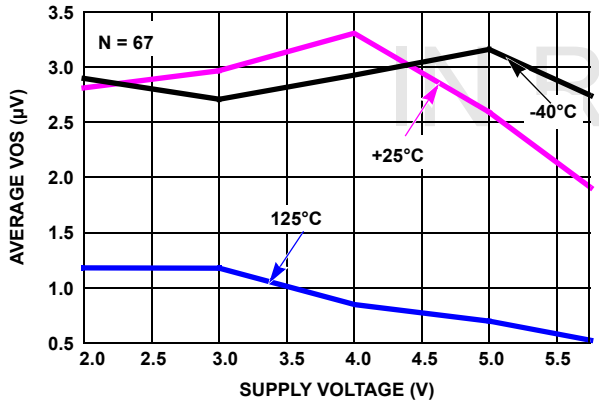


FIGURE 3. AVERAGE INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

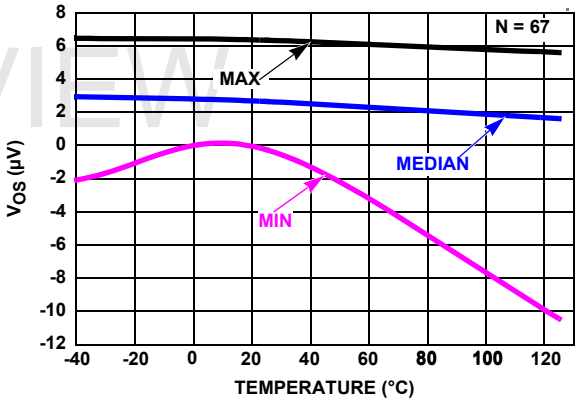


FIGURE 4. V_{OS} vs TEMPERATURE, V_S = ±1.0V, V_{IN} = 0V, R_L = INF

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. **(Continued)**

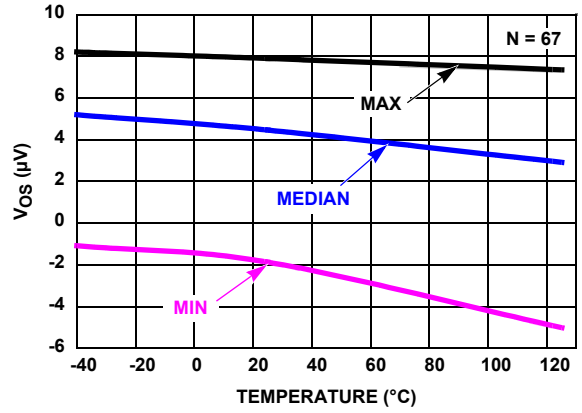


FIGURE 5. V_{OS} vs TEMPERATURE, V_S = ±2.5V, V_{IN} = 0V, R_L = INF

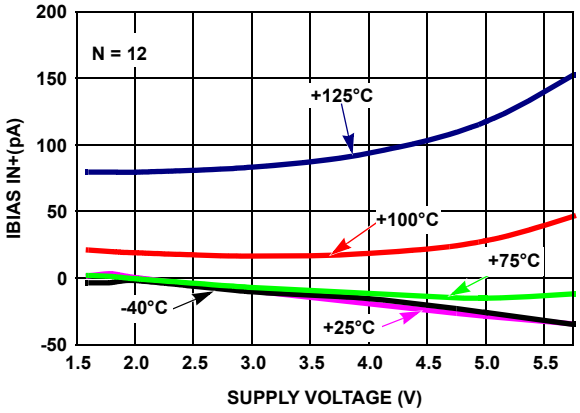


FIGURE 6. I_B+ vs SUPPLY VOLTAGE vs TEMPERATURE

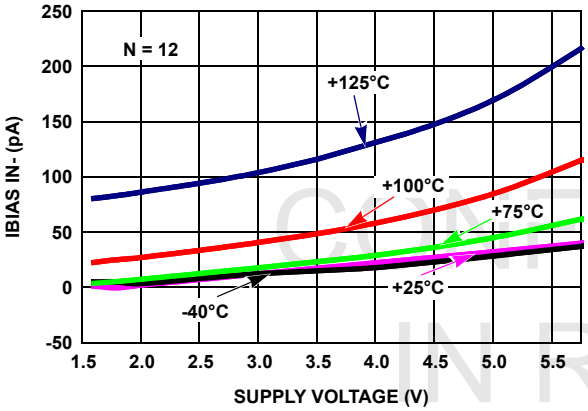


FIGURE 7. I_B- vs SUPPLY VOLTAGE vs TEMPERATURE

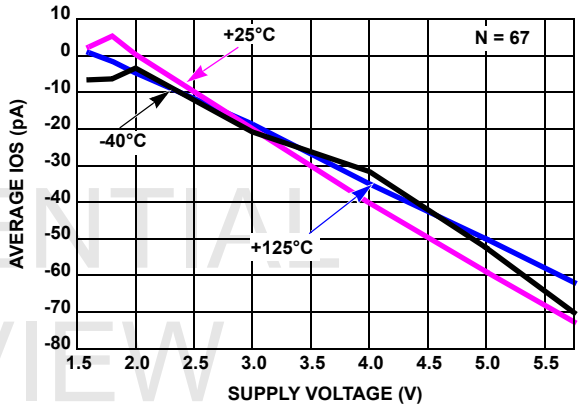


FIGURE 8. IOS vs SUPPLY VOLTAGE vs TEMPERATURE

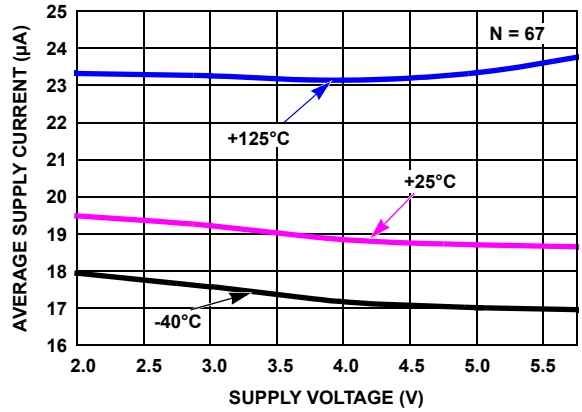


FIGURE 9. AVERAGE SUPPLY CURRENT vs SUPPLY VOLTAGE

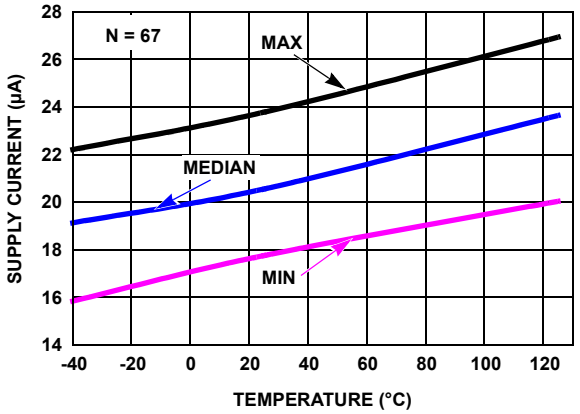


FIGURE 10. MIN/MAX SUPPLY CURRENT vs TEMPERATURE, V_S = ±0.8V, V_{IN} = 0V, R_L = INF

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. **(Continued)**

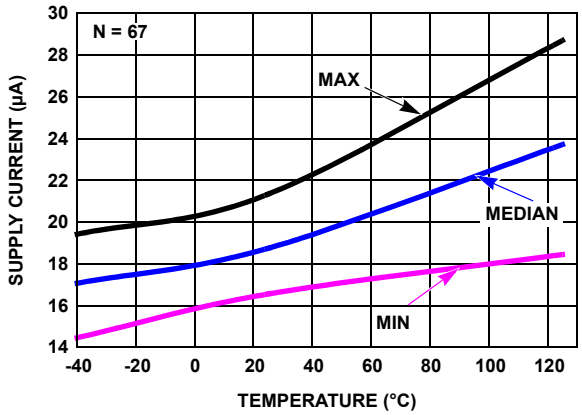


FIGURE 11. MIN/MAX SUPPLY CURRENT vs TEMPERATURE, V_S = ±2.5V, V_{IN} = 0V, R_L = INF

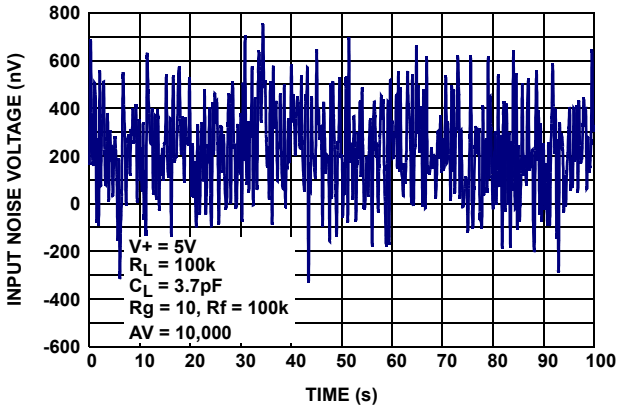


FIGURE 12. INPUT NOISE VOLTAGE 0.01Hz TO 10Hz

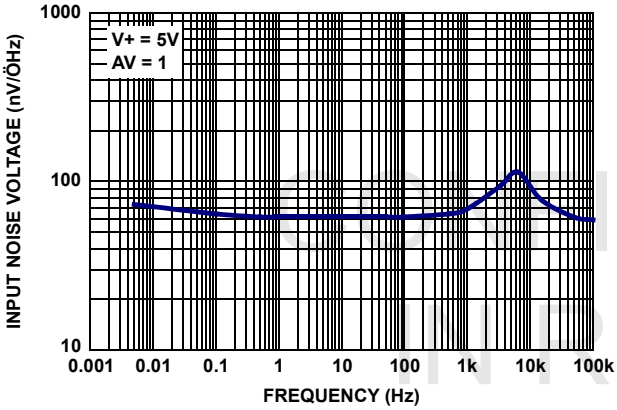


FIGURE 13. INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

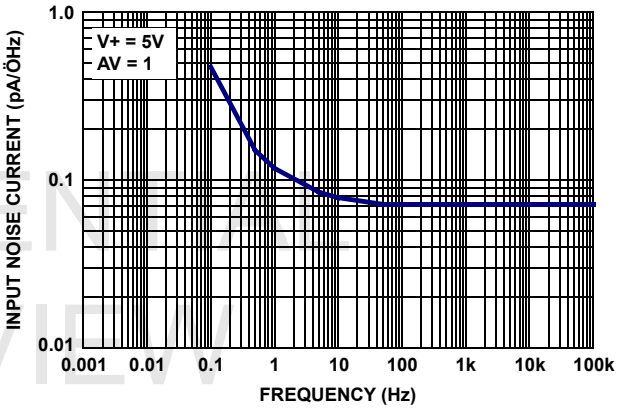


FIGURE 14. INPUT NOISE CURRENT DENSITY vs FREQUENCY

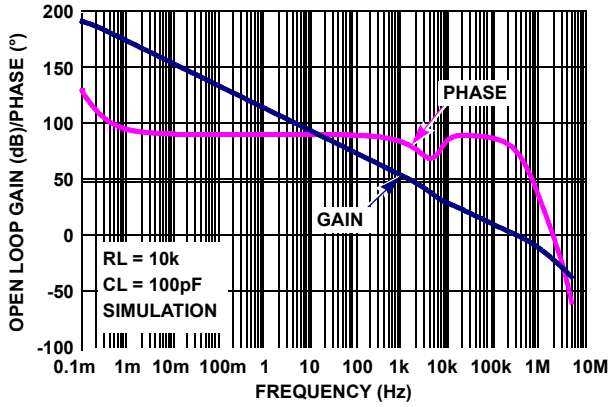


FIGURE 15. FREQUENCY RESPONSE vs OPEN LOOP GAIN, R_L = 10k

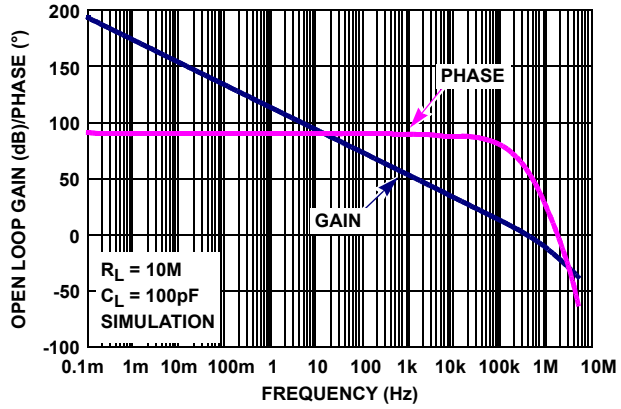


FIGURE 16. FREQUENCY RESPONSE vs OPEN LOOP GAIN, R_L = 10M

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. **(Continued)**

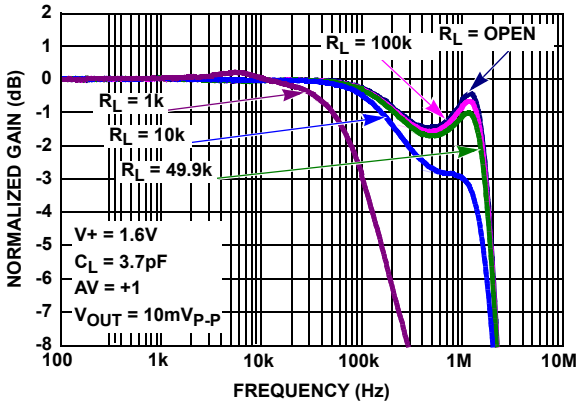


FIGURE 17. GAIN vs FREQUENCY vs R_L, V_S = 1.6V

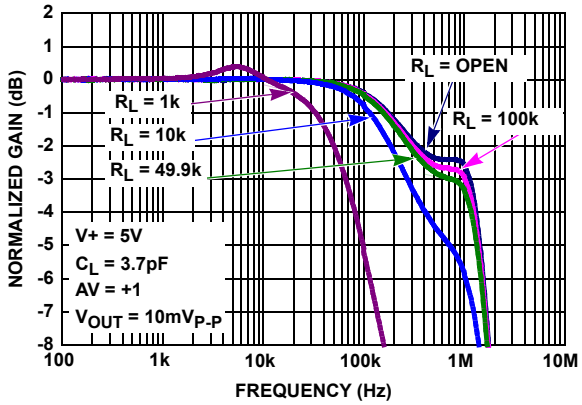


FIGURE 18. GAIN vs FREQUENCY vs R_L, V_S = 5V

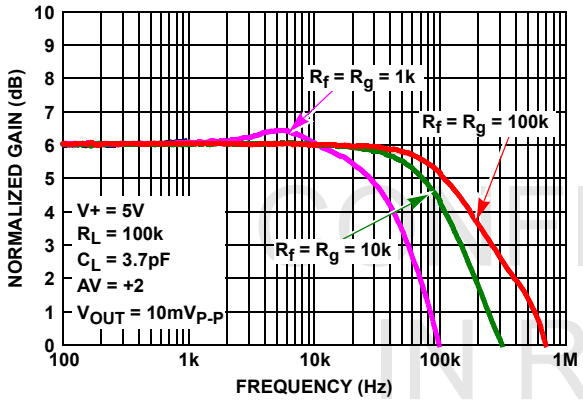


FIGURE 19. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

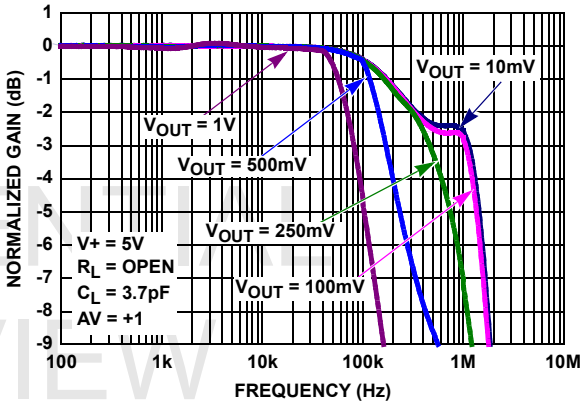


FIGURE 20. GAIN vs FREQUENCY vs V_{OUT}, R_L = OPEN

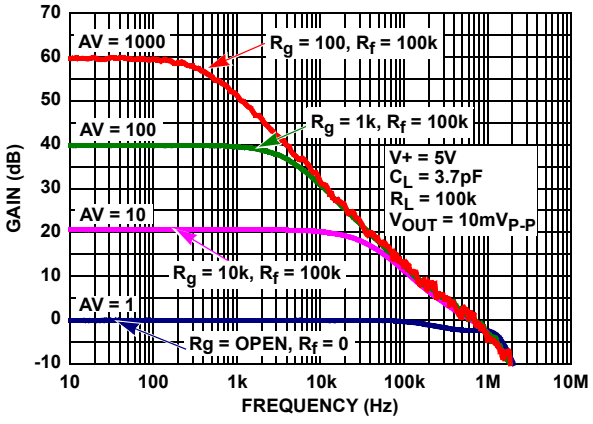


FIGURE 21. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

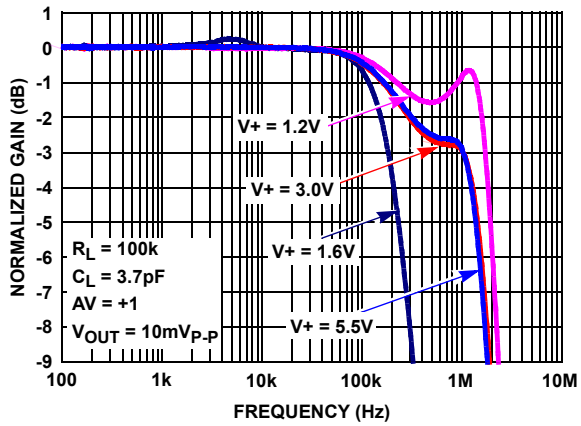


FIGURE 22. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open. **(Continued)**

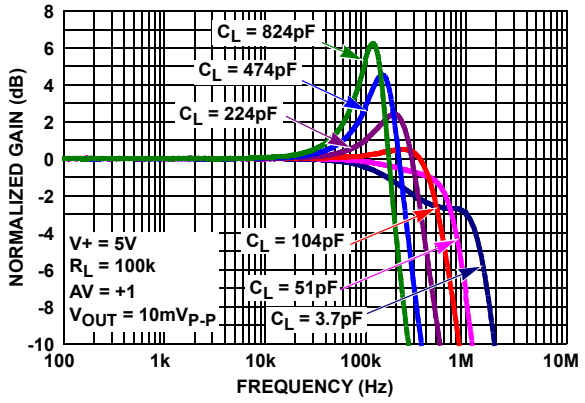


FIGURE 23. GAIN vs FREQUENCY vs C_L

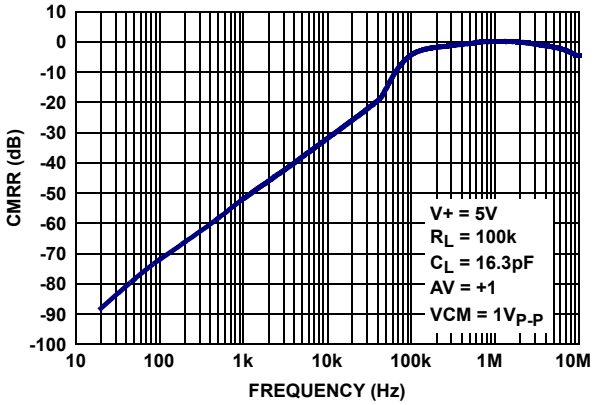


FIGURE 24. CMRR vs FREQUENCY, V_S = 5V

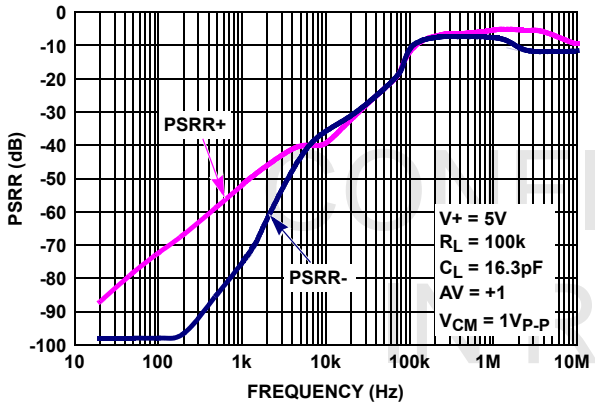


FIGURE 25. PSRR vs FREQUENCY, V_S = 5V

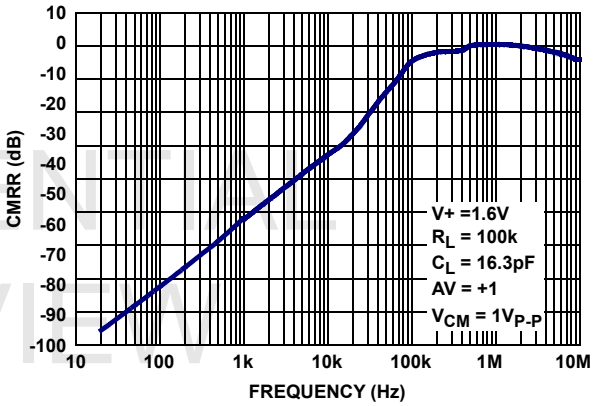


FIGURE 26. CMRR vs FREQUENCY, V_S = 1.6V

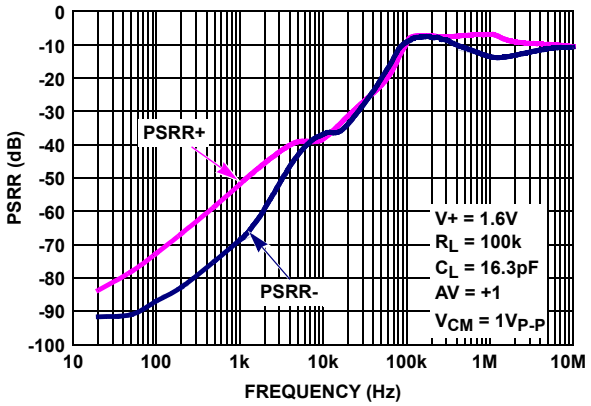


FIGURE 27. PSRR vs FREQUENCY, V_S = 1.6V

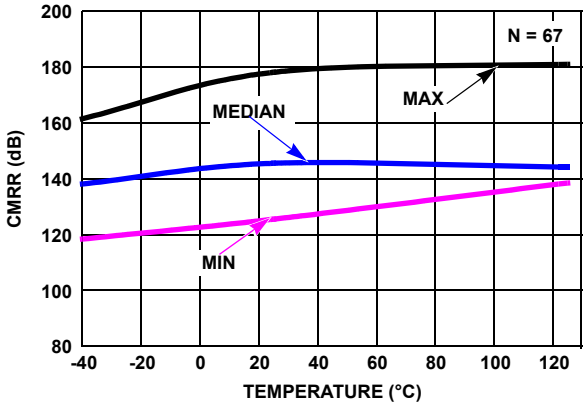


FIGURE 28. CMRR vs TEMPERATURE, VCM = -2.5V TO +2.5V, V+ = ±2.5V

Typical Performance Curves

$V+ = 5V$, $V- = 0V$, $V_{CM} = 2.5V$, R_L = Open. **(Continued)**

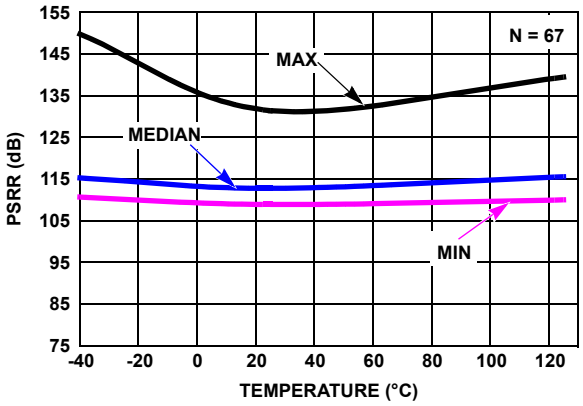


FIGURE 29. PSRR vs TEMPERATURE, V+ = 2V TO 5.5V

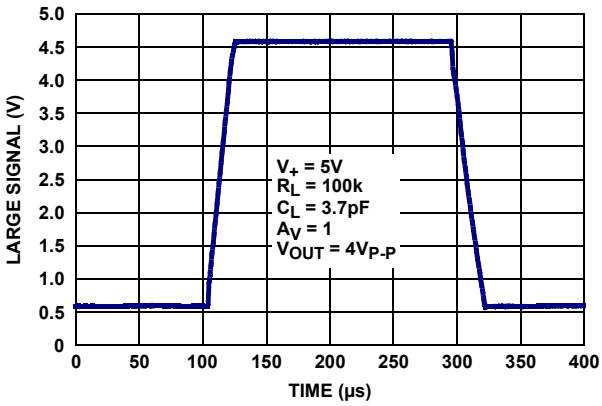


FIGURE 30. LARGE SIGNAL STEP RESPONSE (4V)

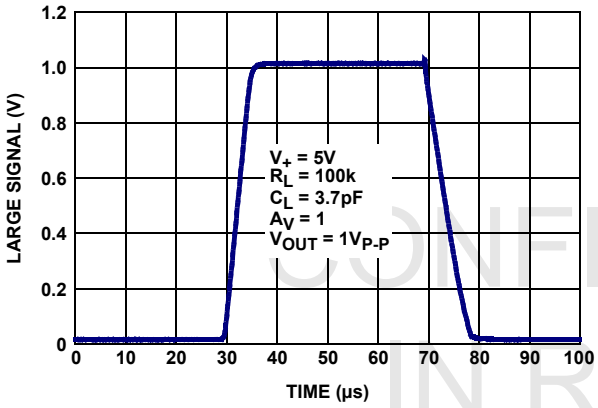


FIGURE 31. LARGE SIGNAL STEP RESPONSE (1V)

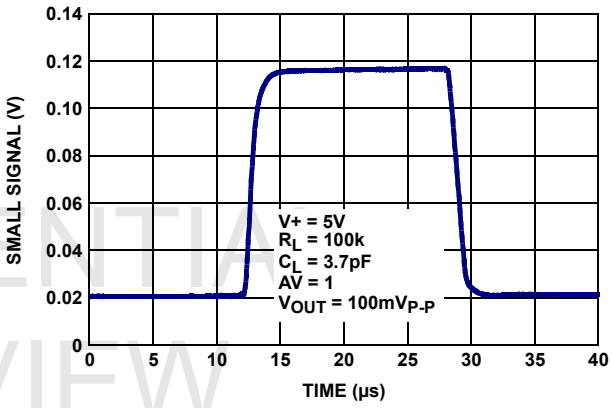


FIGURE 32. SMALL SIGNAL STEP RESPONSE (100mV)

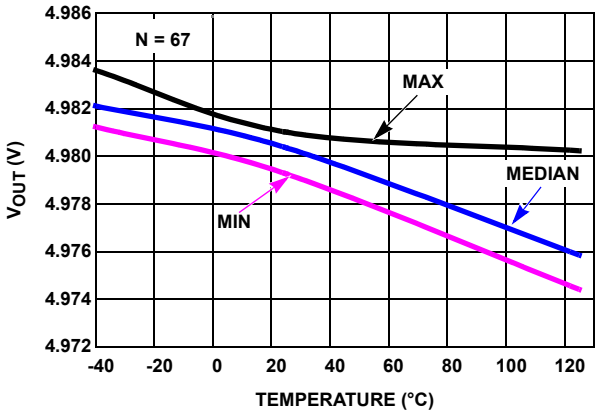


FIGURE 33. V_{OUT} HIGH vs TEMPERATURE, R_L = 10k, V_S = 5V

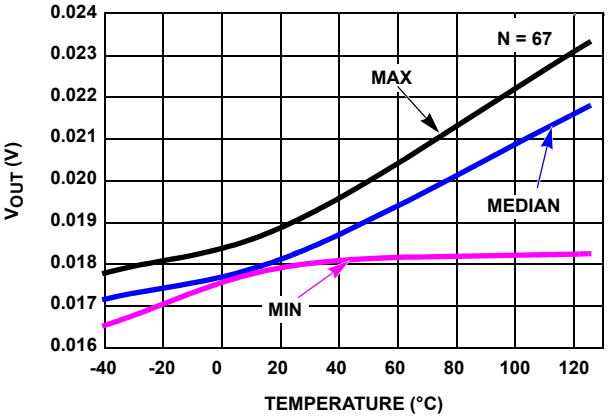


FIGURE 34. V_{OUT} LOW vs TEMPERATURE, R_L = 10k, V_S = 5V

Typical Performance Curves $V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L$ = Open. **(Continued)**

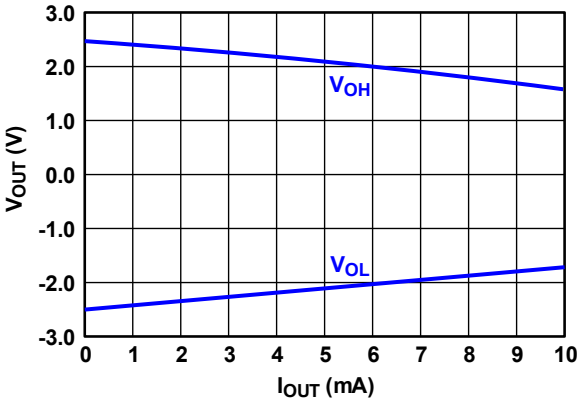


FIGURE 35. V_{OH}, V_{OL} vs I_{OUT}, $V_S = \pm 2.5V$

Applications Information

Functional Description

The ISL28133 uses a proprietary chopper-stabilized architecture shown in the “Block Diagram” on page 2. The ISL28133 combines a 400kHz main amplifier with a very high open loop gain (174dB) chopper stabilized amplifier to achieve very low offset voltage and drift (2µV, 0.02µV/°C typical) while consuming only 18µA of supply current per channel.

This multi-path amplifier architecture contains a time continuous main amplifier whose input DC offset is corrected by a parallel-connected, high gain chopper stabilized DC correction amplifier operating at 100kHz. From DC to ~5kHz, both amplifiers are active with DC offset correction and most of the low frequency gain is provided by the chopper amplifier. A 5kHz crossover filter cuts off the low frequency amplifier path leaving the main amplifier active out to the 400kHz gain-bandwidth product of the device.

The key benefits of this architecture for precision applications are very high open loop gain, very low DC offset, and low 1/f noise. The noise is virtually flat across the frequency range from a few mHz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency (5kHz).

Rail-to-rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and are capable of maintaining high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with 17mA current limit and the capability to swing to within 20mV of either rail while driving a 10kΩ load.

IN+ and IN- Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications where either input is expected to exceed the rails by 0.5V, an external series resistor must be used to ensure the input currents never exceed 20mA (see Figure 36).

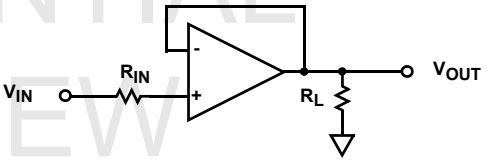


FIGURE 36. INPUT CURRENT LIMITING

Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28133 amplifiers, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 37 implements a single-stage, 10kV/V DC-coupled amplifier with an input DC sensitivity of under 100nV that is only possible using a low VOS amplifier with high open loop gain. This circuit is practical down to 1.8V due to it's rail-to-rail input and output capability. Standard high gain DC amplifiers operating from low voltage supplies are not practical at these high gains using typical low offset precision op amps because the input offset voltage and temperature coefficient consume most of the available output voltage swing. For example, a typical precision amplifier in a gain of 10kV/V with a ±100µV V_{OS} and a temperature coefficient of 0.5µV/°C would produce a DC error at the output of >1V with an additional 5mV°C of temperature dependent error. At 3V, this DC error