IRDC3883 P3V3 user guide

User guide for IRDC3883 evaluation board

About this document

Scope and purpose

The IR3883 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 3mm X 3 mm Power QFN package.

Key features offered by the IR3883 include selectable Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DE), Over Current Protection with three selectable levels, precision 0. 5V reference voltage, Power Good, thermal protection, Enable input, input under-voltage lockout for proper start-up, internal LDO and pre-bias start-up.

Output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous MOSFET for optimum cost and performance and the current limit is thermally compensated.

This user guide contains the schematic and bill of materials for the IRDC3883 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3883 is available in the IR3883 data sheet.

Intended audience

This document is intended as a guide for design engineers evaluating IR3883 performance with the standard IRDC3883 demo board.

Table of contents

1 Board information

1.1 Board features

- V_{in} = +12 V
- Vout = +3.3 V @ 0- 3 A
- F_s=800 kHz @ 0 A (typical)
- L= 2.2 uH (5.28 mm x 5.48 mm x 3.1 mm, DCR=13.2 mΩ)
- C_{in}= 2 x 22 uF (16 V, ceramic 0805) + 1 x 100 uF (25 V, electrolytic, optional)
- C_{out}=2 x 22 uF (6.3 V, ceramic 0805)

1.2 Connections and operating instructions

IR3883 demo board requires a single +12 V for the input power and can deliver up to 3 A load current. The operation modes and OCP limits can be selected through jumpers.

Table 1 Connections

Label		Descriptions
Input	VIN+	Connect input power (+12 V) to this pin
	VIN-	Return of input power
	V_{in}+, V_{in}-	Sense pins for the input voltage
Output	VOUT+	V_{out} (+3.3 V), connect a load (3 A max) to this pin
	VOUT-	Return of Vout
	V_{out}+, V_{out}-	Sense pins for the output voltage
J1	EN/FCCM	J1 is used to enable the POL and to select different operation modes. - POL is off if ENABLE pin is floating. - Connect ENABLE to EN/FCCM to operate POL in Forced Continuous Conduction Mode - Connect ENABLE to EN/DEM to operate POL in Diode Emulation Mode
	ENABLE	
	EN/DEM	
J2	VCC+	J2 is used to set different OCP limits. - Connect OCSet to VCC+: lowest OCP limit - Leave OCSet floating: medium OCP limit - Connect OCSet to GND: maximum OCP limit
	OCSet	
	GND	
P_{Good}	PGOOD	Connect a scope probe to this pin to monitor Power Good Signal
	GND	Ground

1.3 Layout

The PCB of IR3883 demo board is a 2”x 2” 4-layer board using FR4 material. All layers use 2 Oz. copper. The PCB thickness is 0.062”. All components are placed on the top layer except of R1 and R4. R1 and R4 are optional resistors, providing the flexibility to use the internal LDO or an external Vcc bias supply. The standard demo board is configured to use the internal LDO.

The total PCB area of IR3883 and its peripheral components is about 135 mm^2. Please refer to the IR3883 datasheet for detailed layout information.

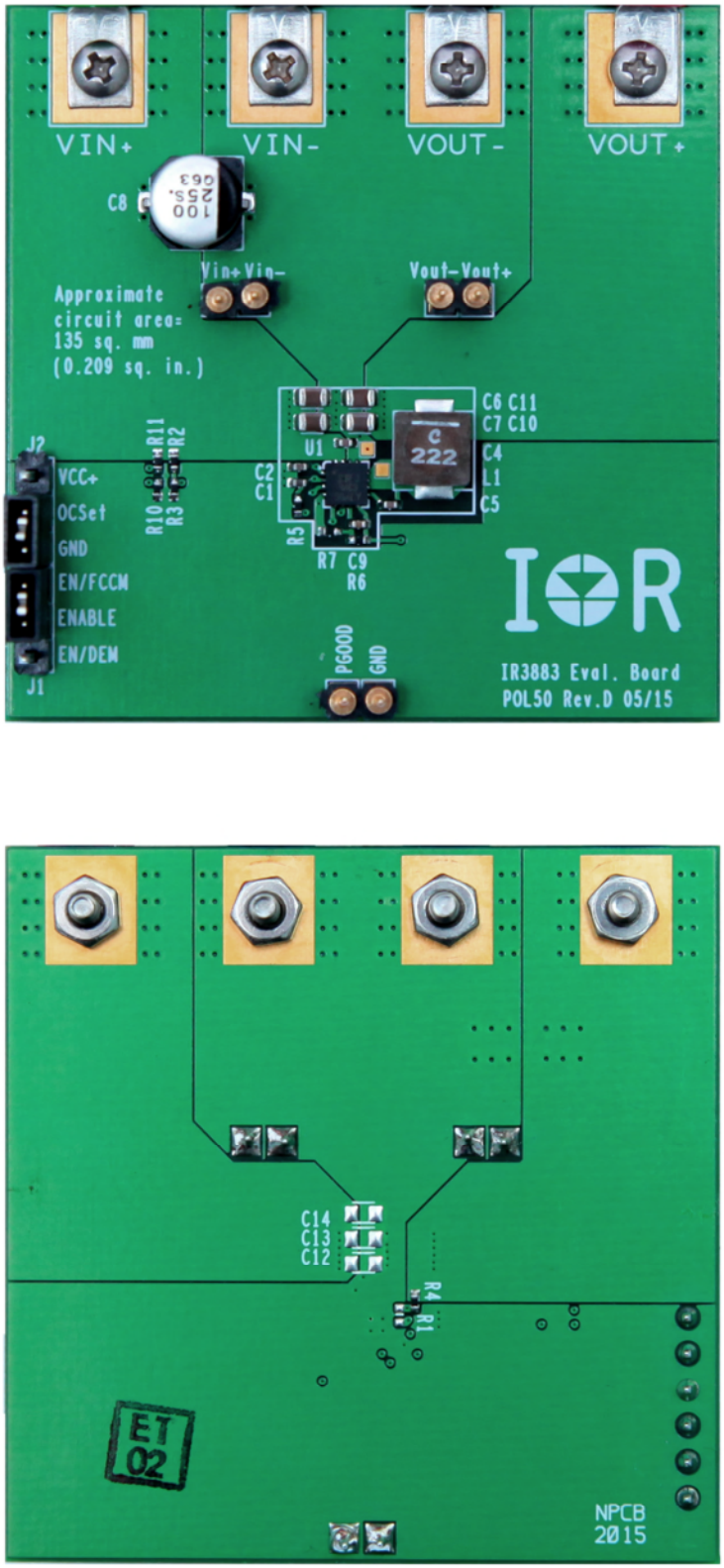

Figure 1 Top and bottom view of IR3883 evaluation board

1.4 PCB Layout

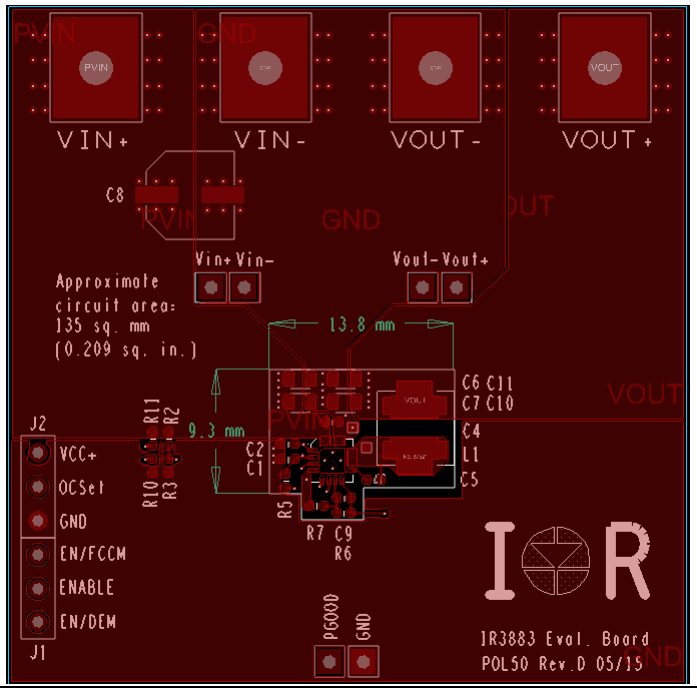

Figure 2 Top layer

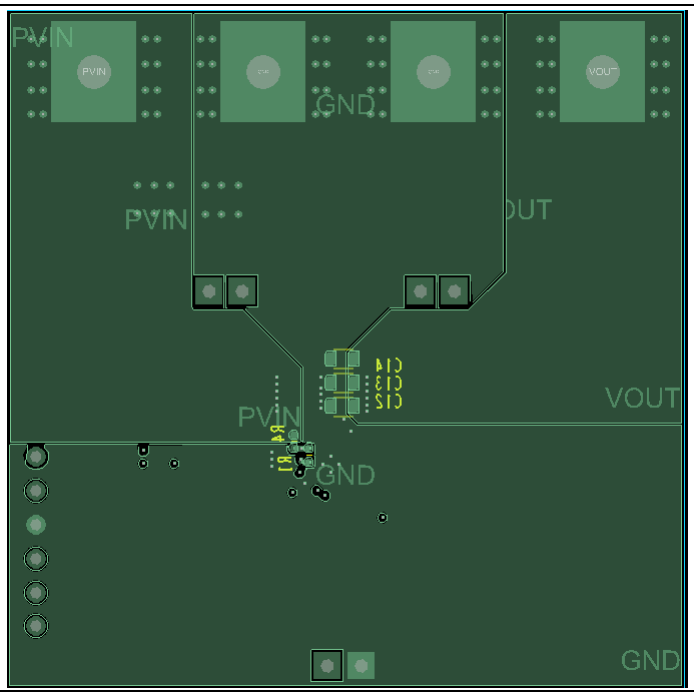

Figure 3 Bottom layer

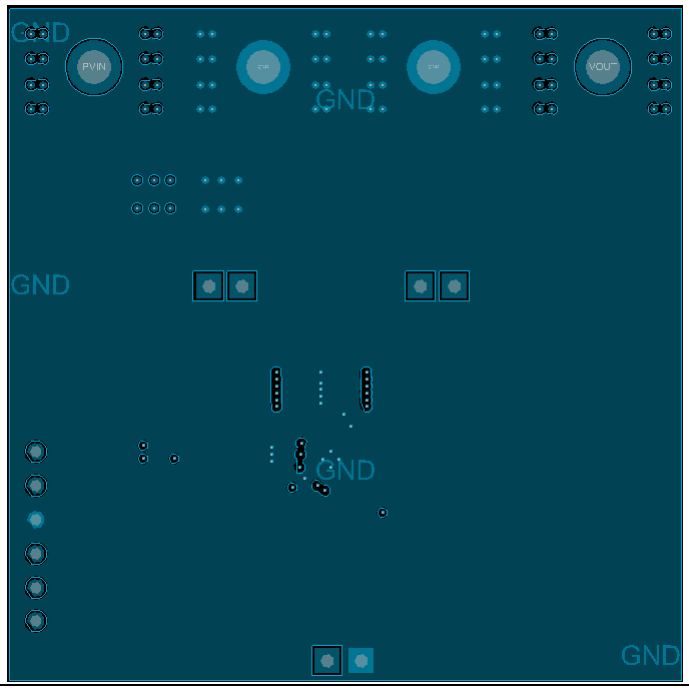

Figure 4 Mid layer 1

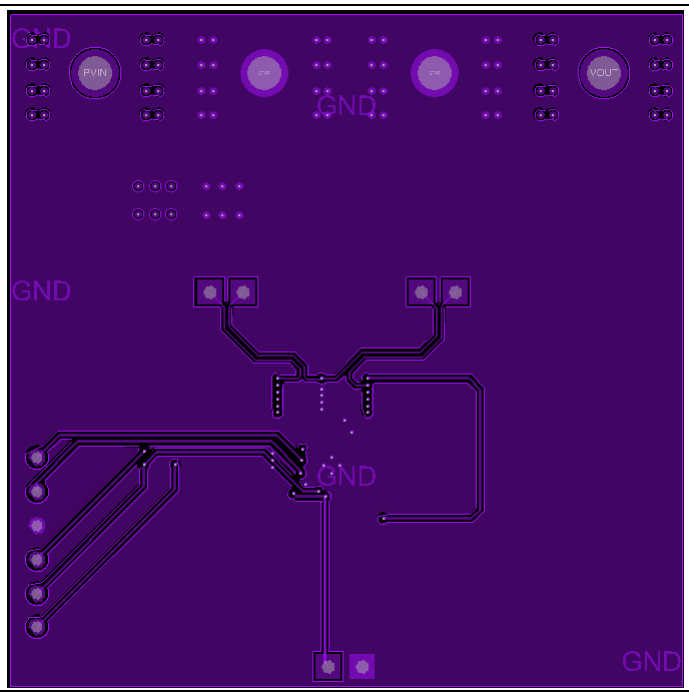

Figure 5 Mid layer 2

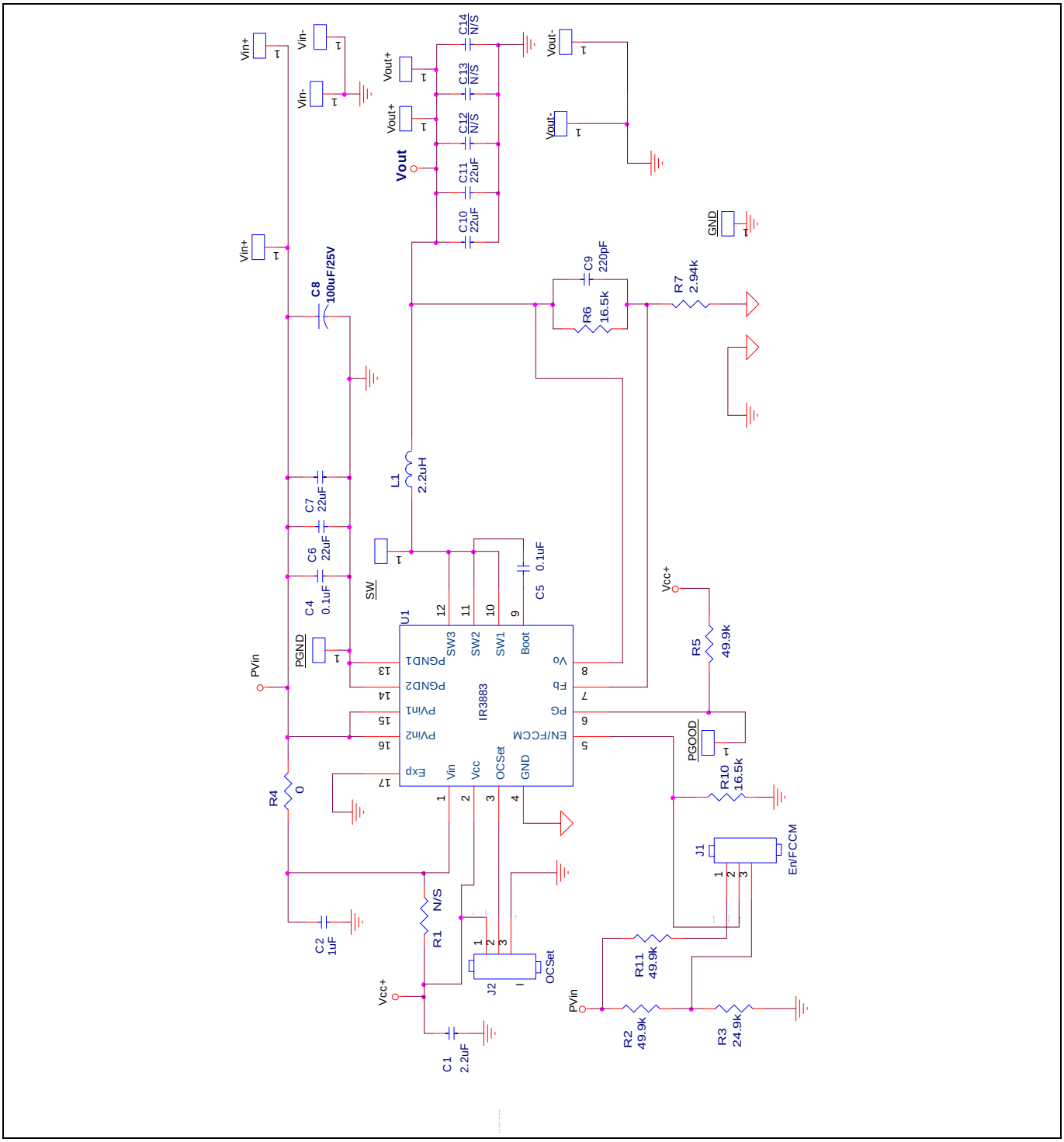

Figure 6 Schematic of the IRDC3883 evaluation board V_{in} = 12 V, V_O = 3.3 V, $I_O$max = 3 A

1.5 Bill of materials

Table 2 Bill of materials

Item	Quantity	Part Reference	Value	Description	Part Number	Manufacture
1	1	C1	2.2 uF	2.2 UF 16 V 10% X5R 0402	GRM155R61C225KE44D	Murata
2	1	C2	1 uF	1 UF 16 V 10% X5R 0402	GRM155R61C105KE01D	Murata
3	2	C4 C5	0.1 uF	0.1 UF 16 V 10% X7R 0402	GRM155R71C104KA88D	Murata
4	2	C6 C7	22 uF	22 UF 16 V 20% X5R 0805	C2012X5R1C226M125AC	TDK
5	2	C10 C11	22 uF	22 uF 6.3 V X5R 20% 0805	C2012X5R0J226M	TDK
6	1	C8	100 uF/25 V	ALUM 100 UF 25 V 20% SMD	EEE-1EA101XP	Panasonic
7	1	C9	220 pF	220 PF 50 V 10% X7R 0402	GCM155R71H221KA37D	Murata
8	1	L1	2.2 uH	5.28 mm x 5.48 mm x 3.1 mm DCR=13.2 mΩ, Isat=7.2 A	XAL5030-222	Coilcraft
9	3	R2 R5 R11	49.9 k	49.9 K OHM 1% 1/10 W 0402	ERJ-2RKF4992X	Panasonic
10	1	R3	24.9 k	24.9 K OHM 1% 1/10 W 0402	ERJ-2RKF2492X	Panasonic
11	1	R4	0	0.0 OHM JUMPER 1/10 W	ERJ-2GE0R00X	Panasonic
12	1	R7	2.94 k	2.94 K OHM 1% 1/10 W 0402	ERJ-2RKF2941X	Panasonic
13	2	R10, R6	16.5 k	16.5 K OHM 1% 1/10 W 0402	ERJ-2RKF1652X	Panasonic
14	1	U1	IR3883	3mmx3mm 3A POL Regulator	IR3883MTRPBF	Infineon

2 Typical operating waveforms

V_{in} = 12.0 V, V_o = 3.3 V, I_o = 0 – 3 A, Room Temperature, no airflow

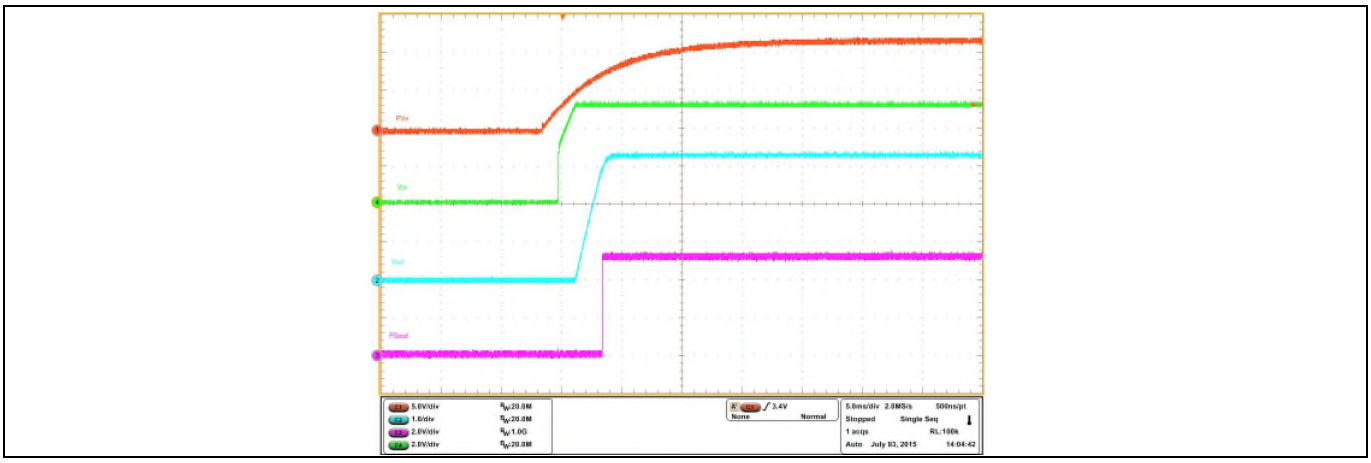

Figure 7 Start up at 3 A Load, Enable = En/FCCM (Ch_1:PV_{in}, Ch_2:V_o, Ch_3:P_{Good} ,Ch_4:V_{cc})

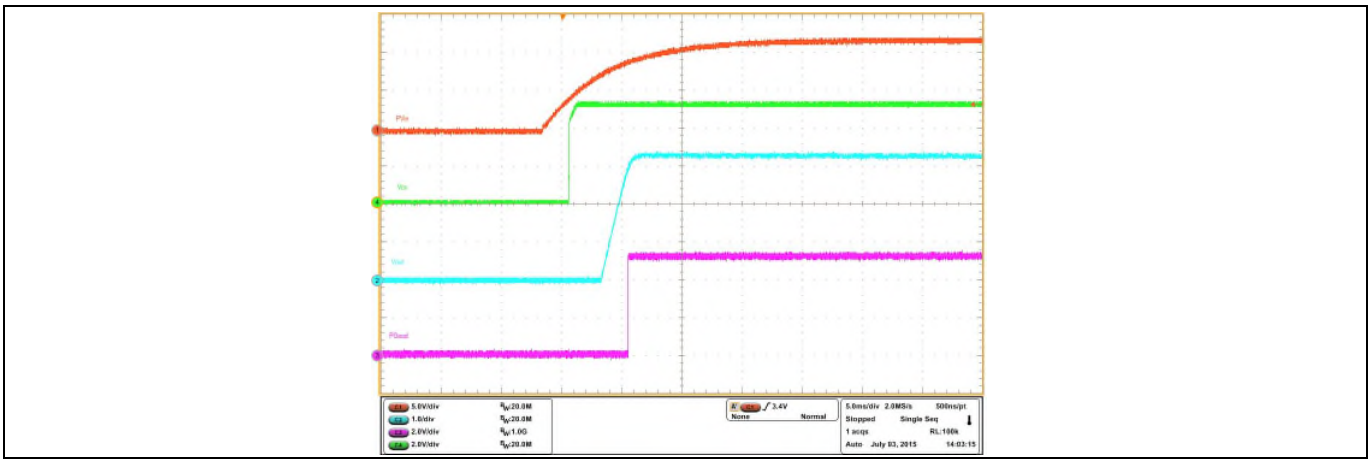

Figure 8 Start up at 0A Load, Enable=En/DEM (Ch_1:PV_{in}, Ch_2:V_o, Ch_3:P_{Good} ,Ch_4:V_{cc})

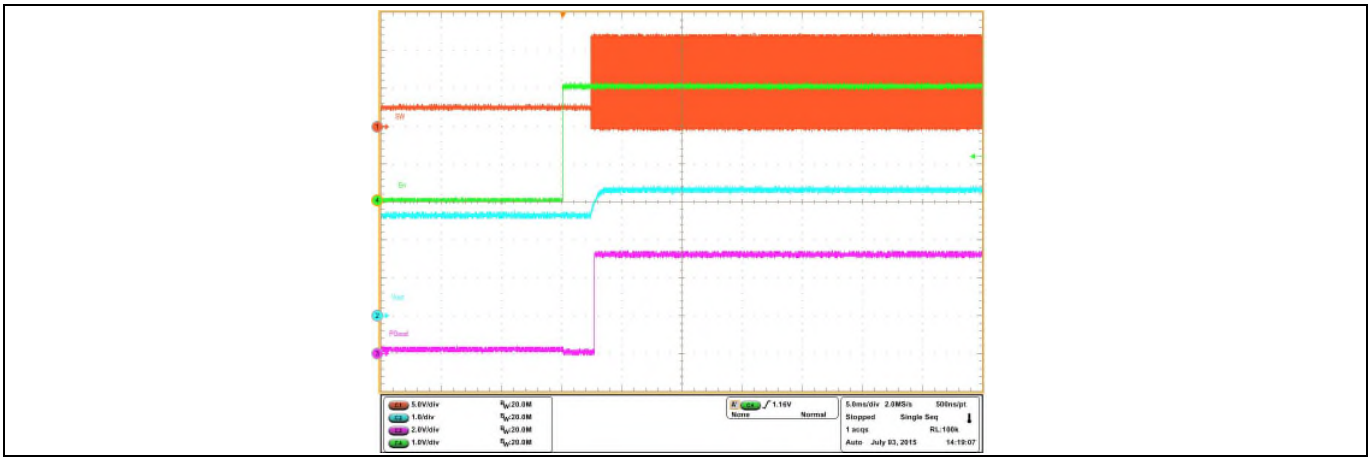

Figure 9 Pre-bias Start up at 0A Load, FCCM (Ch_1:SW, Ch_2:V_o, Ch_3:P_{Good}, Ch_4:En)

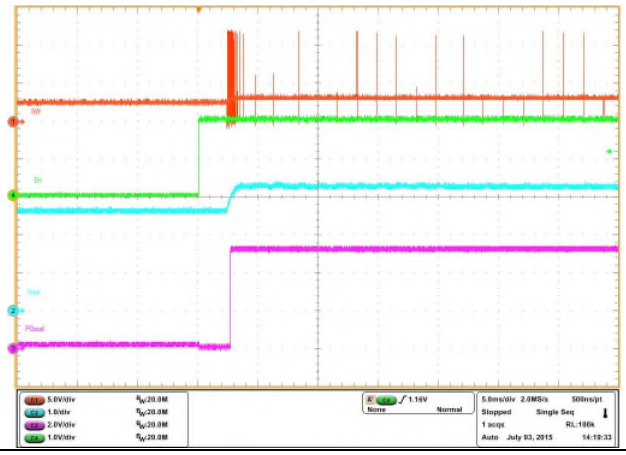

Figure 10 Pre-bias Start up at 0A Load, DEM (Ch_1:SW, Ch_2:V_0, Ch_3:P_{Good}, Ch_4:En)

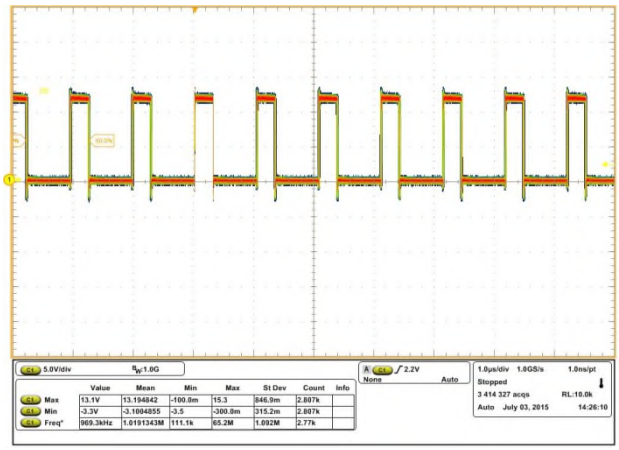

Figure 11 FCCM, SW node, 3A load

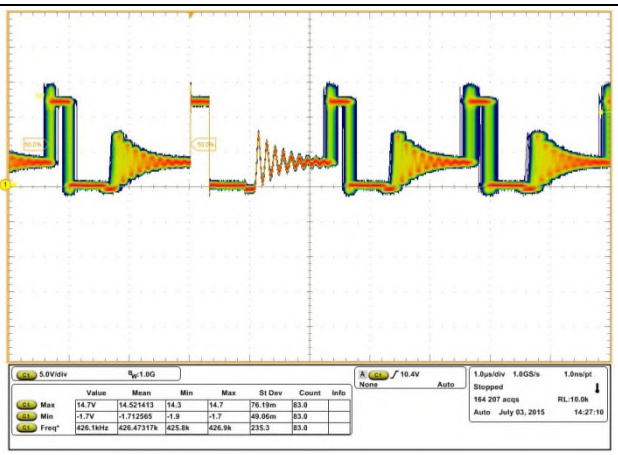

Figure 12 Diode emulation mode, SW node, 0.3A load

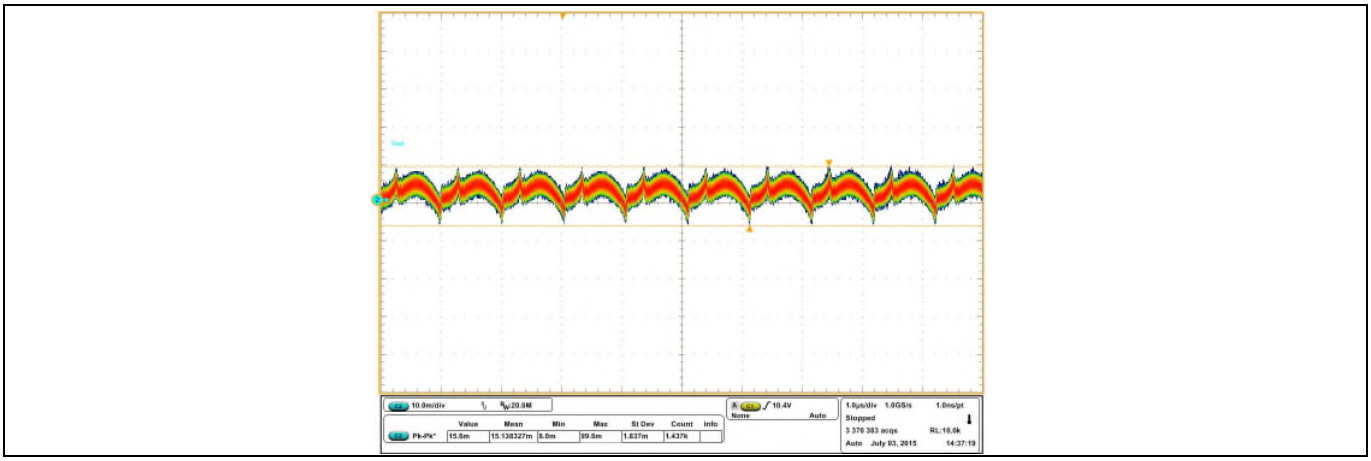

Figure 13 FCCM, Vo ripple, 3A load, V_{out}

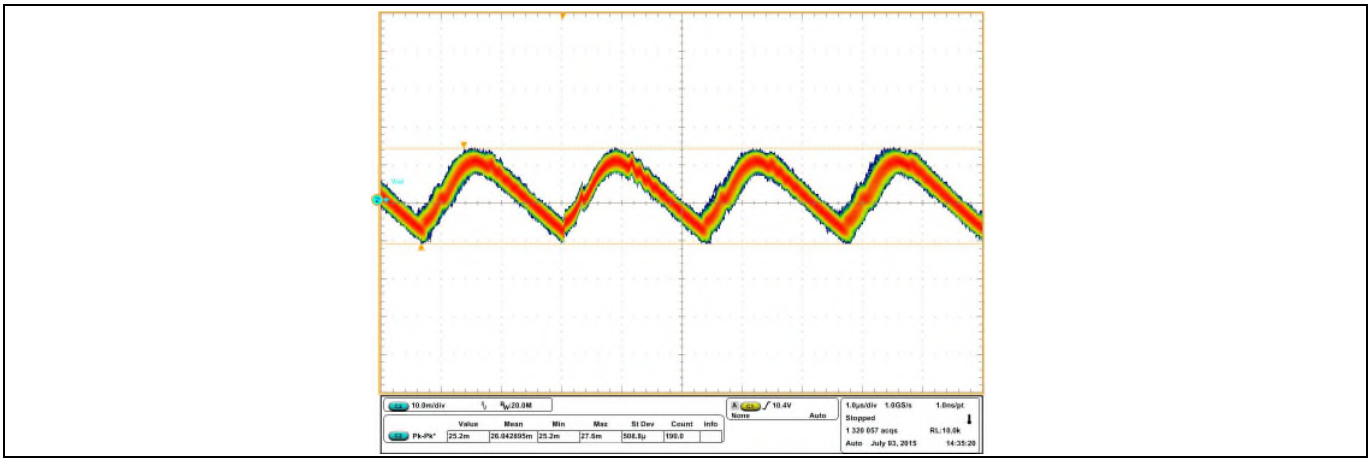

Figure 14 DE, Vo ripple, 0.3A load

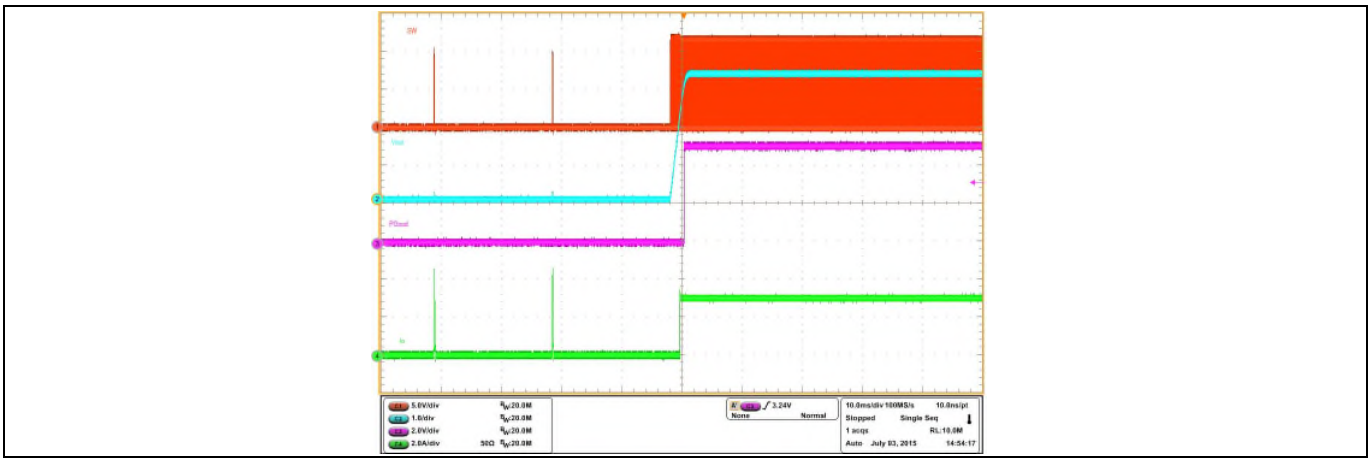

Figure 15 Short circuit (Hiccup) recover (FCCM) (OCSet=GND, CH1=SW, CH2=V_{out}, CH3=PGood, CH4=I_o)

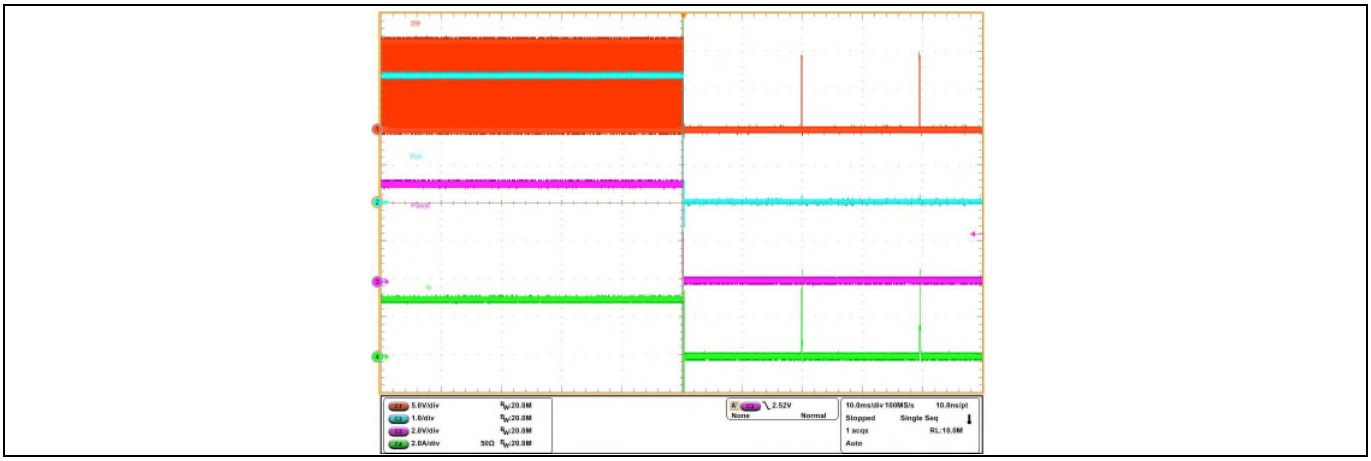

Figure 16 Enter OCP Hiccup mode (FCCM) (OCSet=GND, CH1=SW, CH2=V_{out}, CH3=PGood, CH4=I_o)

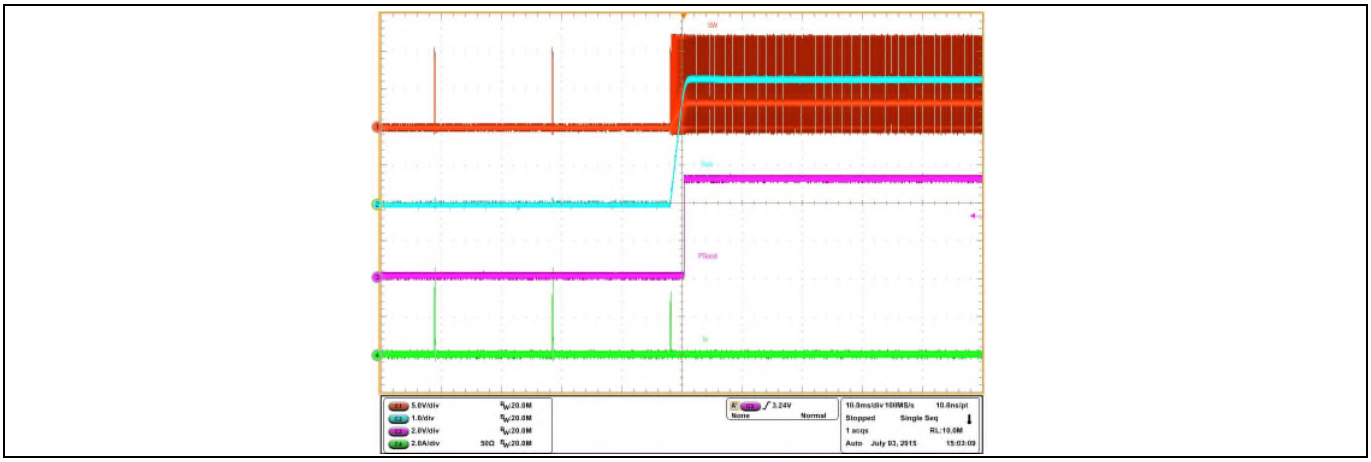

Figure 17 Short circuit (Hiccup) recover (DEM) (OCSet=GND, CH1=SW, CH2=V_{out}, CH3=PGood, CH4=I_o)

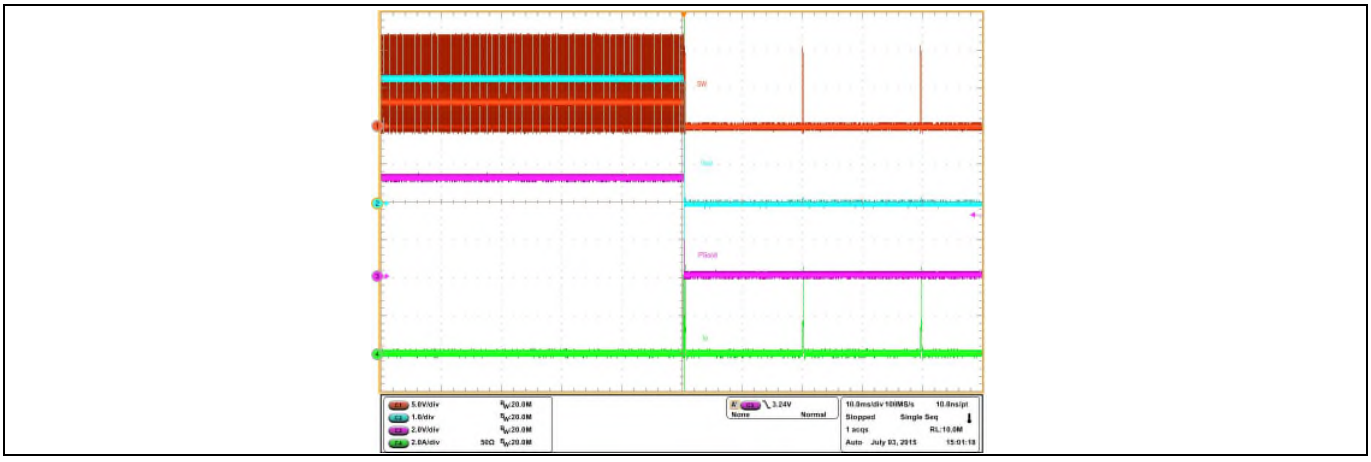

Figure 18 Enter OCP Hiccup mode (DEM) (OCSet = GND, CH1=SW, CH2=V_{out}, CH3=PGood, CH4=I_o)

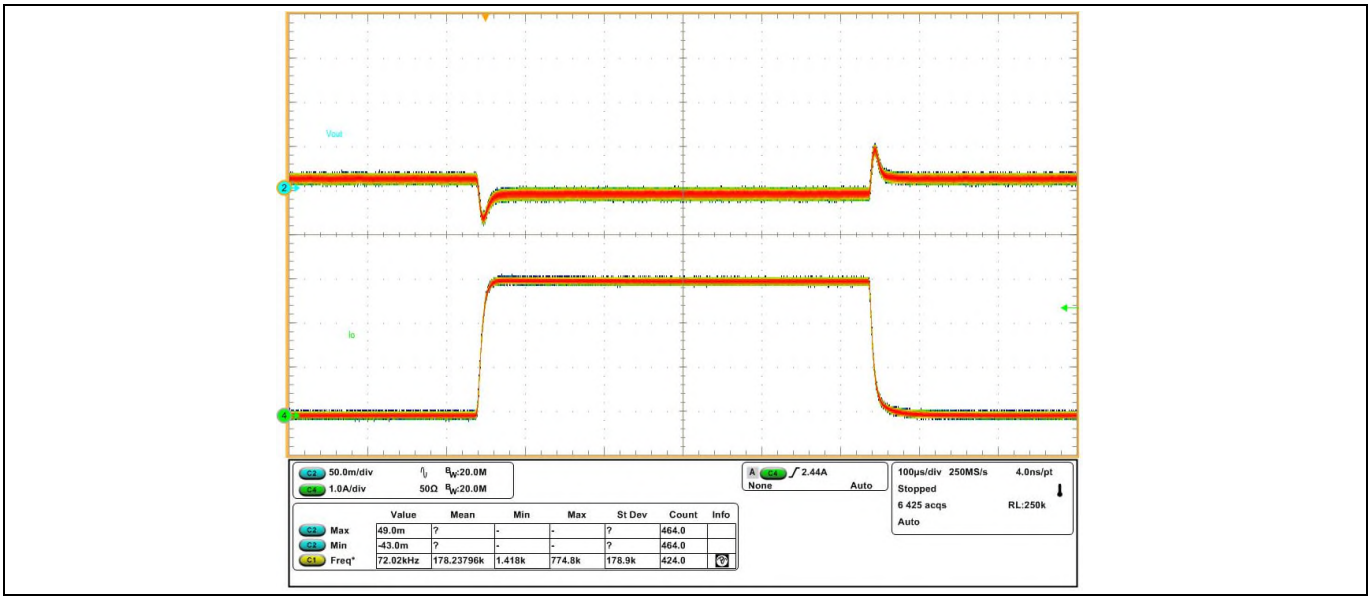

Figure 19 Transient Response, 0 A to 3.0 A step, FCCM
Ch_2: V_{out} Ch_4-I_{out}, Undershoot: -43 mV, Overshoot: 49 mV

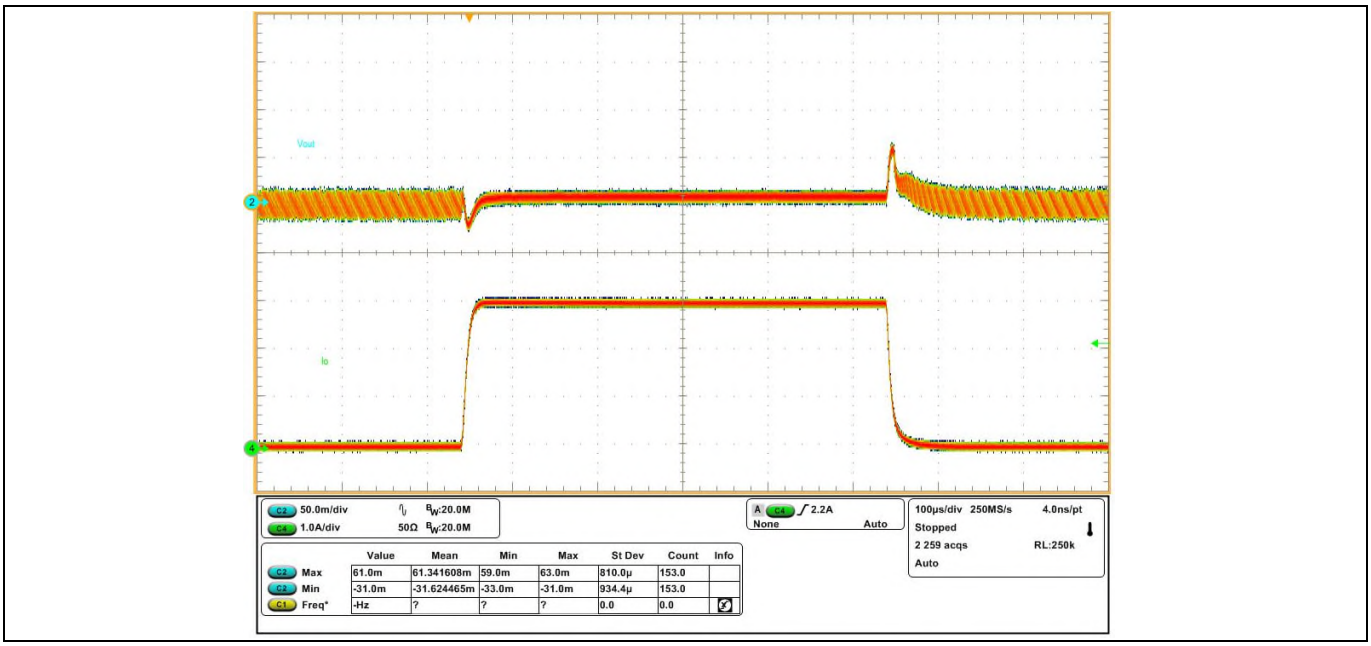

Figure 20 Transient Response, 0.03 A to 3.0 A step, DEM
Ch_2: V_{out} Ch_4-I_{out}, Undershoot: -31 mV, Overshoot: 61 mV

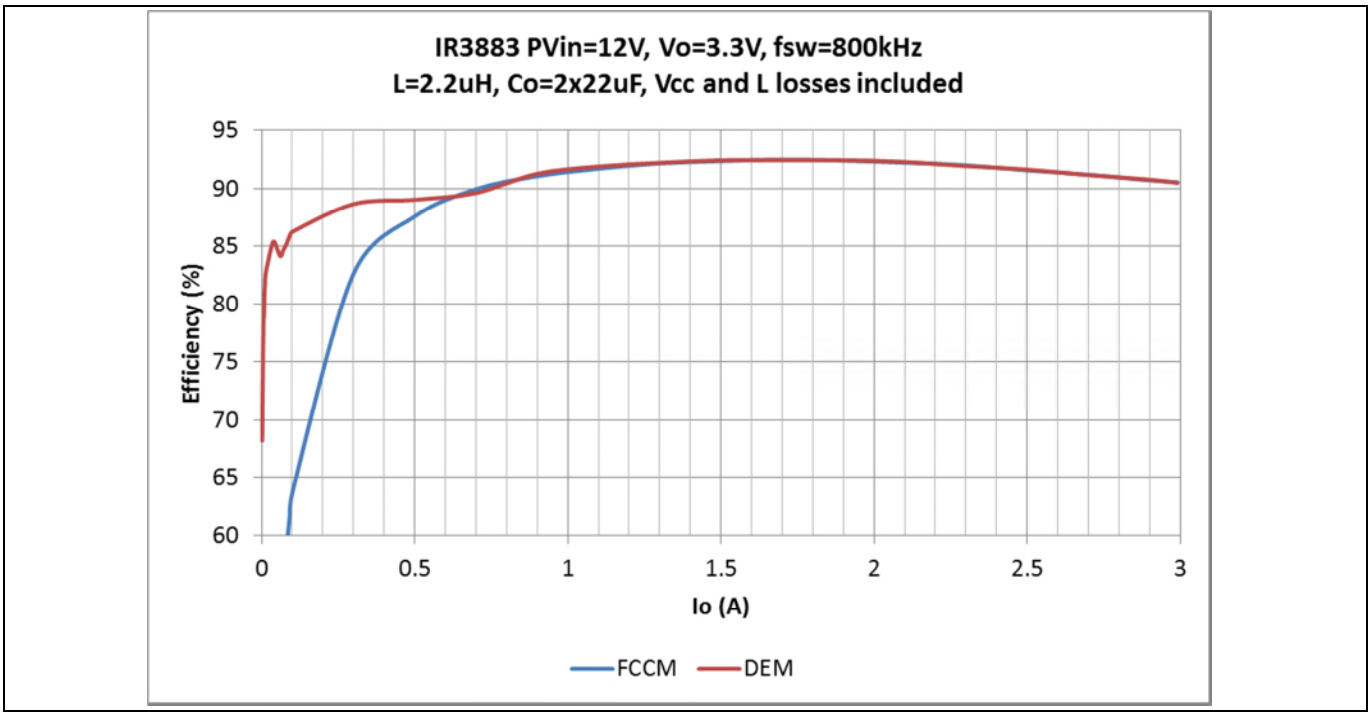

Figure 21 Efficiency versus load current

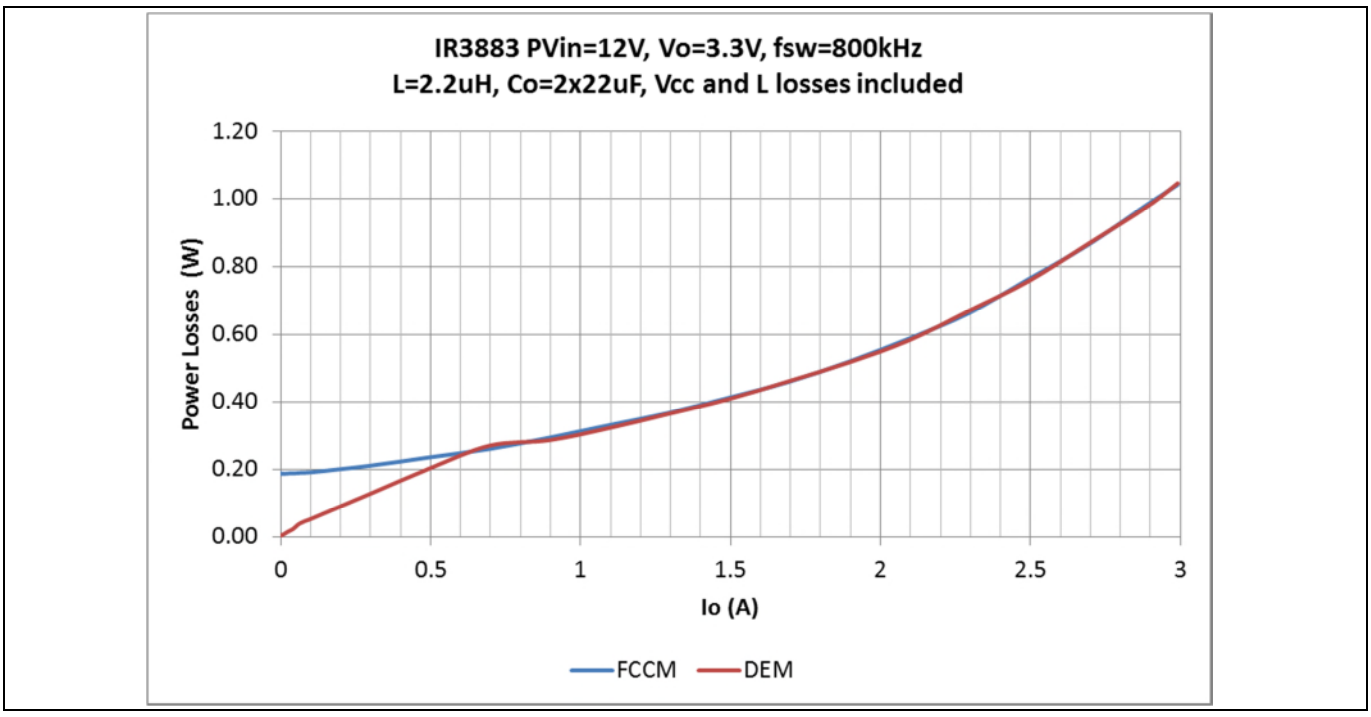

Figure 22 Power loss versus load current

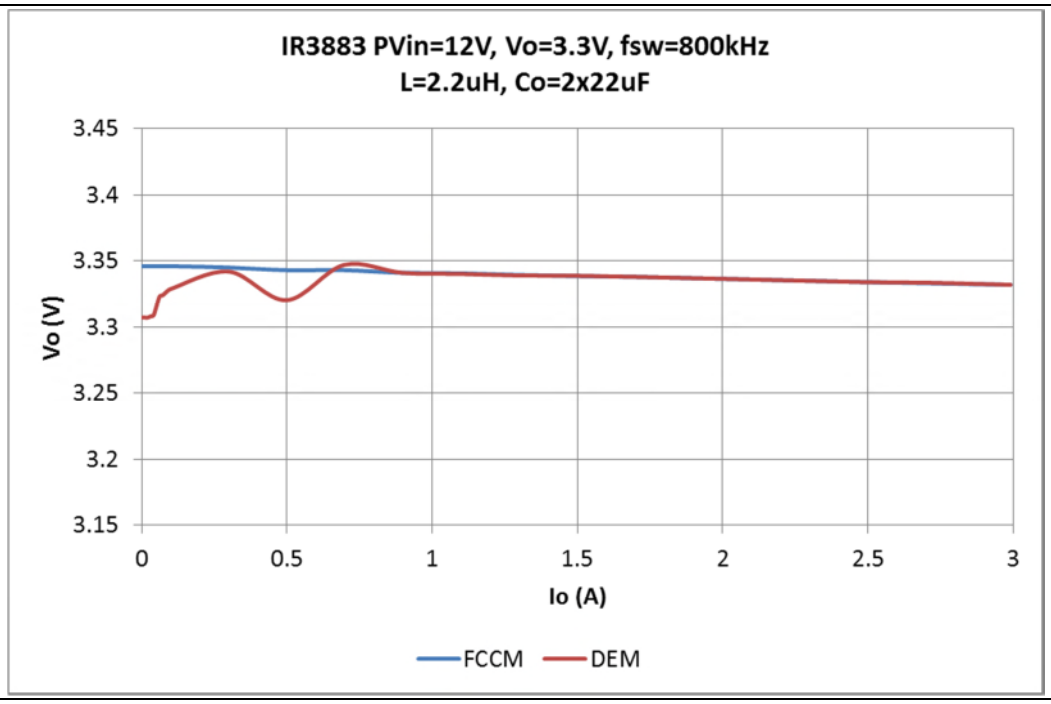

Figure 23 Load regulation

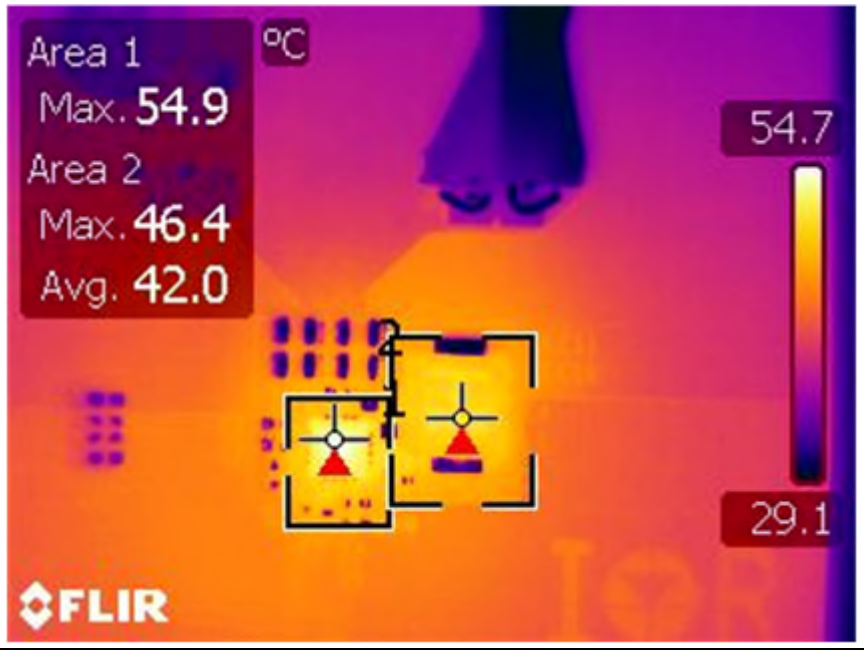

Figure 24 Thermal Image of the board at 3 A load IR3883 = 55 °C, L= 46 °C, Amb = 25 °C

Revision history

Major changes since the last revision

Page or Reference	Description of change

Edition 2016-12-08

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AppNote Number

UG_201612_PL17_02