NCP5383

2 Phase Buck Controller with Integrated Gate Drivers and AVP

The NCP5383 is a two phase buck controller used in low voltage, high current power supplies. Dual−edge pulse−width modulation (PWM) combined with inductor current sensing and adaptive voltage positioning (AVP) reduces system cost by providing the fastest initial response to transient loads thereby requiring less bulk and ceramic output capacitors to satisfy transient load−line requirements.

A high performance operational error amplifier is provided, which allows for easy compensation of the system. Protection features include overcurrent protection, undervoltage lockout (UVLO), thermal shutdown and power good monitor.

Features

- Dual−edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- 1% Internal Reference Voltage Accuracy
- Phase−to−Phase Current Balancing
- "Lossless" Differential Inductor Current Sensing
- Differential Current Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Frequency Range: 100 kHz – 400 kHz Set by the Resistor
- Power Good Output with Internal Delays
- Programmable Soft Start Time
- Integrated Gate Drivers
- This is a Pb−Free Device

Applications

- Pentium IV Processors
- Graphics Cards
- Low Voltage, High Current Power Supplies

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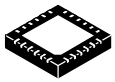


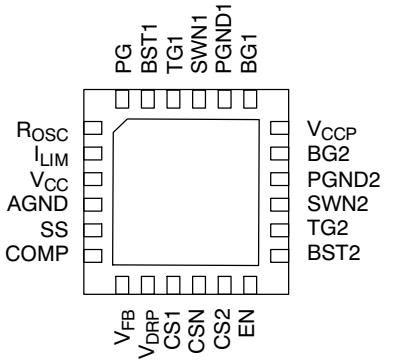
24 PIN QFN, 4x4
MN SUFFIX
CASE 485L

MARKING DIAGRAM

5383	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5383MNR2G	QFN−24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

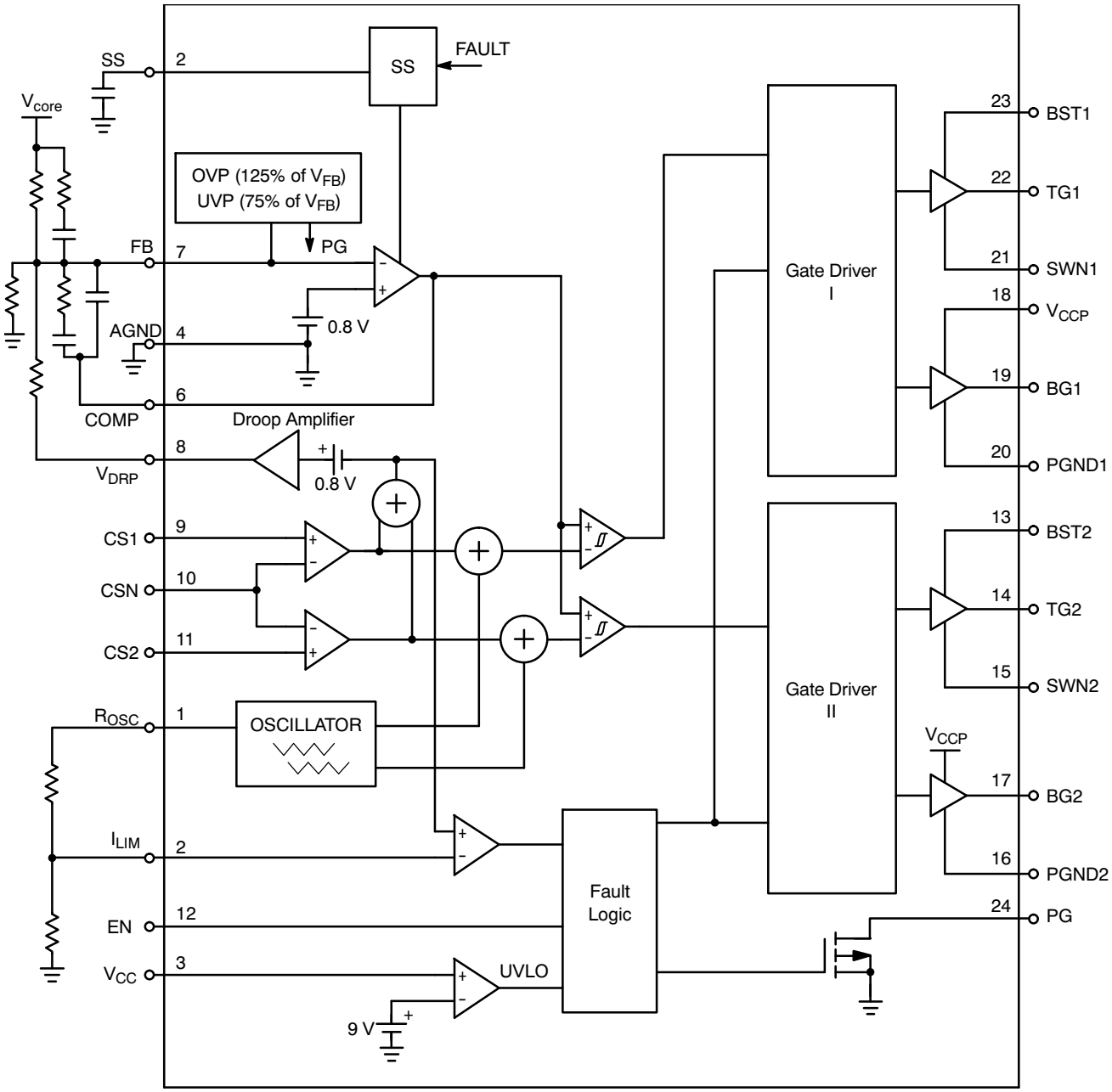


Figure 1. Simplified Block Diagram

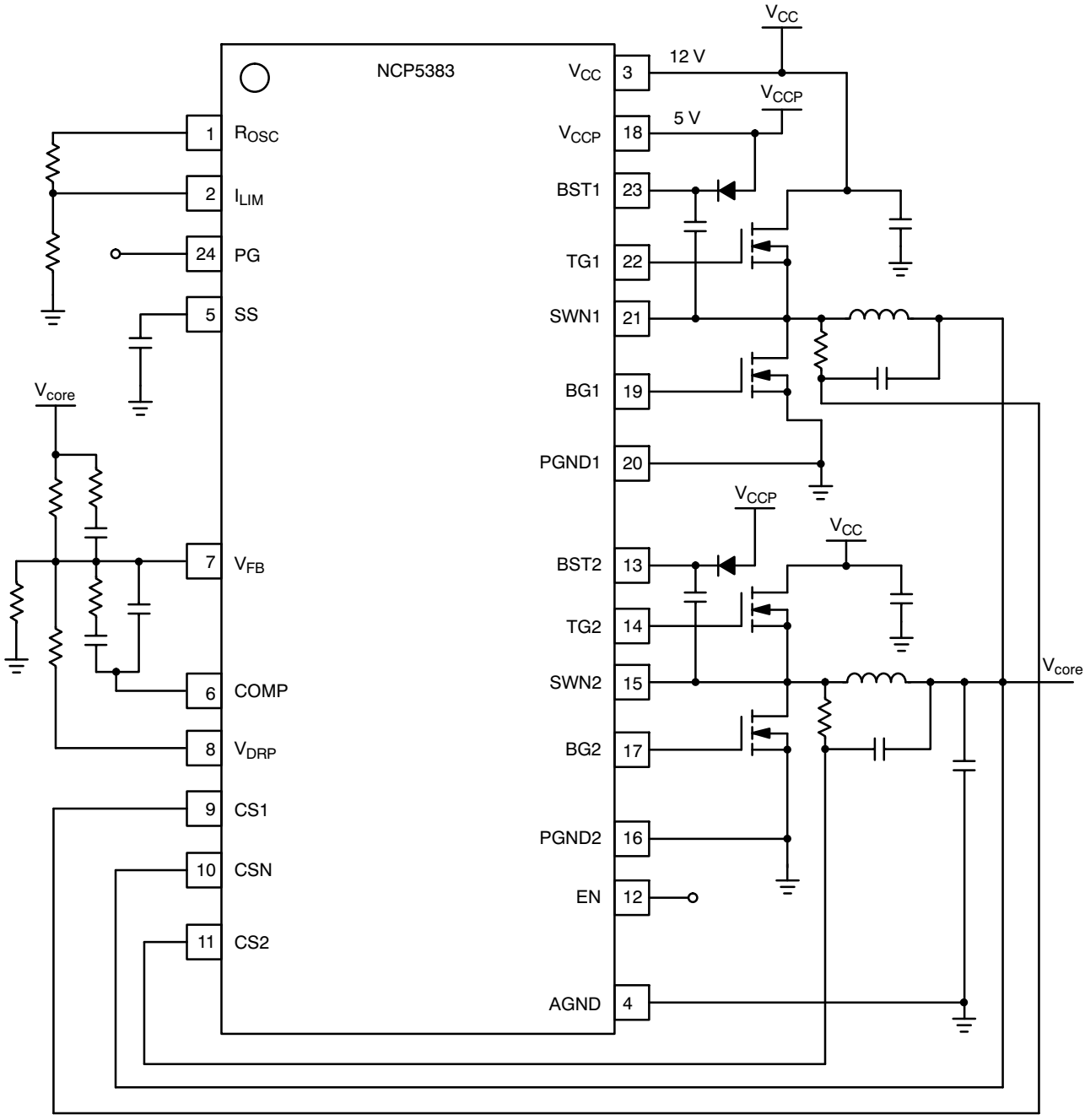


Figure 2. Typical Application Schematic

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	R_{OSC}	A resistance from this pin to ground programs the oscillator frequency according to **f_{SW} = 1 / (R_{OSC} • 100 pF).** Also, this pin supplies a trimmed output voltage of 2.00 V so it may be used to form a voltage divider at the I_{LIM} pin to set the over current shutdown threshold as shown in the Applications Schematics.
2	I_{LIM}	Over current shutdown threshold. To program the shutdown threshold, connect this pin to the R_{OSC} pin via a resistor divider as shown in the Applications Schematics. To disable the over current feature connect this pin directly to the R_{OSC} pin. To guarantee correct operation, this pin should only be connected to the voltage generated by the R_{OSC} pin − do not connect this pin to any externally generated voltages.
3	V_{CC}	Power for the internal control circuits.
4	AGND	Power supply return for the analog circuits that control output voltage.
5	SS	A capacitor from this pin to ground programs the soft−start time.
6	COMP	Output of the error amplifier and input to the inverting pin of the PWM comparators.
7	V_{FB}	Voltage feedback pin and error amplifier inverting input. Connect a resistor from this pin to V_{CORE}. The value of this resistor and the amount of current from the droop resistor (R_{DRP}) will set the amount of output voltage droop (AVP) during load.
8	V_{DRP}	Current signal output for Adaptive Voltage Positioning (AVP). The offset of this pin above the no−load set−point is proportional to the output current. Connect a resistor from this pin to V_{FB} to set the amount of AVP current into the feedback resistor (R_{FB}) that will result in output voltage droop. Leave this pin open for no AVP.
9	CSx	Non−inverting input to current sense amplifier #x, x = 1, 2
10	CSxN	Inverting input to current sense amplifier #x, x = 1 (Tie to V_{CORE})
12	EN	When this pin is pulled High the controller is enabled. When it is pulled Low the controller will be disabled. Either an open−collector output (with a pull−up resistor) or a logic gate (CMOS or totem−pole output) may be used to drive this pin. A Low to High transition on this pin will induce soft start. If the Enable function is not required, this pin should be tied directly to V_{CCP}.
18	V_{CCP}	Power for the gate drivers
19, 17	BG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−channel MOSFET.: Phase #x, x = 1, 2
20, 16	PGND	Ground reference for the bottom gate drivers
21, 15	SWN	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET. : Phase #x, x = 1, 2
22, 14	TG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N−channel MOSFET. : : Phase #x, x = 1,2
23, 13	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (CBST) between this pin and the PHASE pin. Typical values for CBST range from 0.1 μF to 1 μF. Ensure that CBST is placed near the IC.: Phase #x, x = 1, 2.
24	PG	PowerGood output. Open drain type output with internal delays. The output is latched low if V_{fb} is 125% of V_{FB} or 75% of V_{FB}.

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Operating Ambient Temperature Range	0 to 70	°C
Operating Junction Temperature Range	0 to 125	°C
Storage Temperature Range	−55 to 150	°C
Lead Temperature Soldering, Reflow (60 second maximum above 183°C):	230	°C
Thermal Resistance, Junction−to−Ambient ($R_{\theta JA}$) on a thermally conductive PCB in free air	56	°C/W
ESD Susceptibility (Human Body Model)	2.0	kV
JEDEC Moisture Sensitivity Level	1	MSL
Maximum Voltage V_{CC} with respect to AGND	13.2	V
Maximum Voltage V_{CCP} and all other pins with respect to ground	5.5	V
Maximum Voltage V_{BST} and all other pins with respect to ground	18.7	V
Maximum Voltage V_{BST} and all other pins with respect to SWN	5.5	V
Maximum Voltage SWN and all other pins with respect to ground	3.0	V
Minimum Voltage SWN and all other pins with respect to ground	−2.0	V
Minimum Voltage all pins with respect to ground	−0.3	V
Maximum Current into pins: COMP, V_{DRP}	3.0	mA
Maximum Current out of pins: COMP, V_{DRP}, R_{OSC}, SS	3.0	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 70°C; 0°C < T_J < 125°C; 4.5 V < V_{CC} < 13.2 V; F_{sw} = 400 KHz)

Parameter	Test Conditions	Min	Typ	Max	Units
Error Amplifier					
Input Bias Current		−200	−50	−10	nA
Input Offset Voltage		−1.0		1.0	mV
Inverting Input Voltage	1.0 KΩ between V_{FB} and COMP Pins	792	800	808	mV
Open Loop DC Gain	C_L = 100 pF to GND, R_L = 10 KΩ to GND		78		dB
Open Loop Unity Gain Bandwidth	C_L = 100 pF to GND, R_L = 10 KΩ to GND		15		MHz
Open Loop Phase Margin	C_L = 100 pF to GND, R_L = 10 KΩ to GND		65		deg
Slew Rate	ΔV_{in} = 100 mV, G = −1 V/V, ΔV_{out} = 1.0 V − 2.0 V, C_L = 10 pF to GND, Load = ±125 μA to GND		5.0		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.0	3.3		V
Minimum Output Voltage	I_{SINK} = 2.0 mA		0.9	1.05	V
Output Source Current (Note 1)	V_{out} = 3.0 V		2.0		mA
Output Sink Current (Note 1)	V_{out} = 1.0 V		2.0		mA
Boost Current Supply Voltage					
Input Voltage		4.5	12	18	V
V_{CCP} Operating Voltage	V_{CCP}	4.5	5.0	5.5	V
V_{DRP} Adaptive Voltage Positioning Amplifier					
Current Sense Input to V_{DRP} Gain		5.7	6.0	6.3	V/V
Current Sense Input to V_{DRP} Output Unity Gain Bandwidth	C_L = 330 pF to GND, R_L = 10 KΩ to GND		7.2		MHz
Current Sense Input to V_{DRP} Output Slew Rate	ΔV_{in} = 100 mV, G = 6 V/V, ΔV_{out} = 1.3 V − 1.9 V, C_L = 330 pF to GND, Load = ±400 μA to GND		3.7		V/μs
Current Summing Amp Output Offset Voltage	CSx − CSNx = 0, CSx = 1 V		10		mV
Maximum V_{DRP} Output Voltage	CSx − CSNx = 0.12 V, I_{source} = 1 mA	1.2			V
Minimum V_{DRP} Output Voltage	CSx − CSNx = −0.12 V, I_{sink} = 1 mA			0.5	V
Output Source Current (Note 1)	V_{out} = 1.2 V		9.0		mA
Output Sink Current (Note 1)	V_{out} = 1.0 V		2.0		mA
Current Sense Amplifiers					
Input Bias Current	CSx = CSxN = 1.4 V	−200	−50	−1.0	nA
Common Mode Input Voltage Range		−0.3		3.3	V
Differential Mode Input Voltage Range		−120		120	mV
Input Offset Voltage	CSx = CSxN = 1.00 V	−3.0		3.0	mV
Current Sense Input to PWM Gain	0 mV < (CSx− CSxN) < 25 mV T_A = 25°C	5.7	6.0	6.3	V/V

1. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 70°C; 0°C < T_J < 125°C; 4.5 V < V_{CC} < 13.2 V; F_{sw} = 400 KHz)

Parameter	Test Conditions	Min	Typ	Max	Units
Oscillator					
Switching Frequency Range		100		400	KHz
Switching Frequency Accuracy	ROSC = 100 KΩ	90	100	110	KHz
Switching Frequency Accuracy	ROSC = 49.9 KΩ	180	200	220	KHz
Switching Frequency Accuracy	ROSC = 24.9 KΩ	360	400	440	KHz
ROSC Output Voltage		1.92	2.00	2.08	V
Modulators (PWM Comparators)					
Minimum Pulse Width (Note 1)	Fs = 400 KHz		30	40	ns
Propagation Delay			20		ns
Magnitude of the PWM Ramp			1.0		V
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3		V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI		2.3		V
PWM Comparator Offset Mismatch				40	Mv
Phase Angle Error		−15		15	deg
PWM Linear Duty Cycle			90		%
Gate Drivers					
Upper Gate Source	Vbst − Vswn = 5 V, VTG − VSWN = 4 V		1.8		Ω
Upper Gate Sink	Vbst − Vswn = 5 V, VTG − VSWN = 1 V		1.8		Ω
Lower Gate Source	V_{CCP} = 5 V, Vgs = 4 V		1.8		Ω
Lower Gate Sink	V_{CCP} = 5 V, Vgs = 1 V		0.9		Ω
Upper gate transition times	C_{load} = 3 nF		16		ns
	C_{load} = 3 nF		16		ns
Lower gate transition times	C_{load} = 3 nF		16		ns
	C_{load} = 3 nF		7.0		ns
SWN falling to BG rising delay	C_{load} = 3 nF		18		ns
BG falling to TG rising delay	C_{load} = 3 nF		40		ns
Soft−Start					
Soft−Start Pin Source Current			5.0		μA
Soft−Start Pin Discharge Voltage	Fault = 1			50	mV
Soft−Start Pin Discharge Time	From EN = 0 to V_{SS} pin < max discharge voltage, C_{SS} = 0.01 μF		5.0		μs
Enable Input					
Enable High Input Leakage Current	EN = 3.0 V			10	μA
Upper Threshold	V_{UPPER}	0.80	0.85	0.90	V
Total Hysteresis	$V_{UPPER} - V_{LOWER}$	50	100	150	mV
Thermal Shutdown					
Thermal Trip Point	TSD			160	C

1. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: 0°C < T_A < 70°C; 0°C < T_J < 125°C; 4.5 V < V_{CC} < 13.2 V; F_{sw} = 400 KHz)

Parameter	Test Conditions	Min	Typ	Max	Units
Current Limit					
Current Sense Amp to ILIM Gain	20 mV < (Csx − CSxN) < 60 mV T_A = 25°C	5.7	6.0	6.3	V/V
ILIM Pin Input Bias Current	V_{ilim} = 2.0 V		0.1	1.0	μA
ILIM Pin Working Voltage Range		0.3		2.0	V
ILIM Input Offset Voltage		−50		50	mV
Undervoltage Protection					
UVLO Start Threshold UVLO Stop Threshold	V_{CC} = 12 V	8.2 7.2	9.0 8.0	9.5 8.5	V
UVLO Hysteresis			1.0		V
UVLO	V_{CCP} = 5 V	3.7	4.0	4.3	V
Hysteresis			0.5		V
Power Good					
Output Saturation Voltage	I_{PG} = 10 mA, V_{CC} = 12 Vdc			0.4	V
Rise Time	External pull−up of 1 KΩ to 1.25 V, C_{TOT} = 45 pF, ΔV_O = 10% to 90%			150	ns
Output Voltage at Power−up	External PG pull−up resistor of 2 KΩ to 5 V $t_{R\_VCC} \leq 3 \times t_{R\_5V}$, 100 μs ≤ t_{R_VCC} ≤ 20 ms			1.0	V
High − Output Leakage Current	PG = 5.5 V via 1 K			0.1	μA
Upper Threshold Voltage			125		% of V_{FB}
Lower Threshold Voltage			75		% of V_{FB}
Rising Delay	V_{CORE} increasing	0.3	1.40	2	ms
Falling Delay	V_{CORE} decreasing		5		μs

TYPICAL CHARACTERISTICS

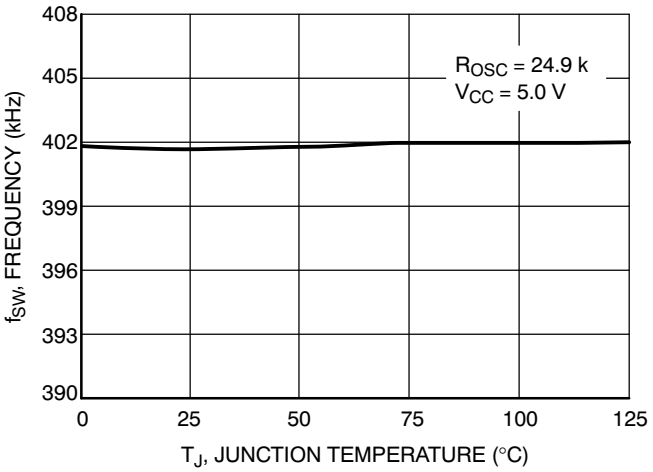


Figure 3. Oscillator Frequency vs. Temperature

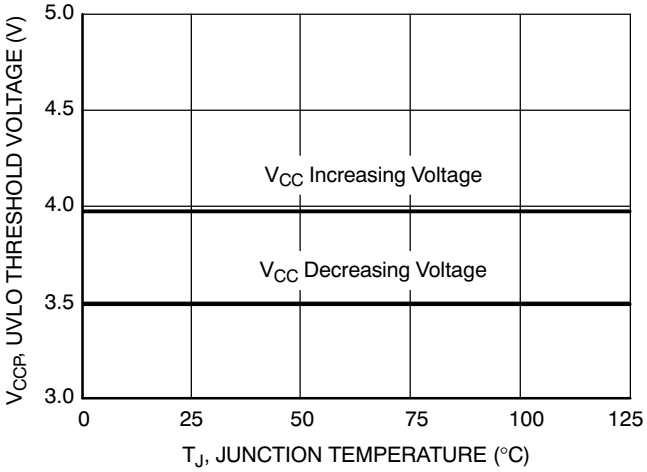


Figure 4. UVLO Threshold Voltage vs. Temperature

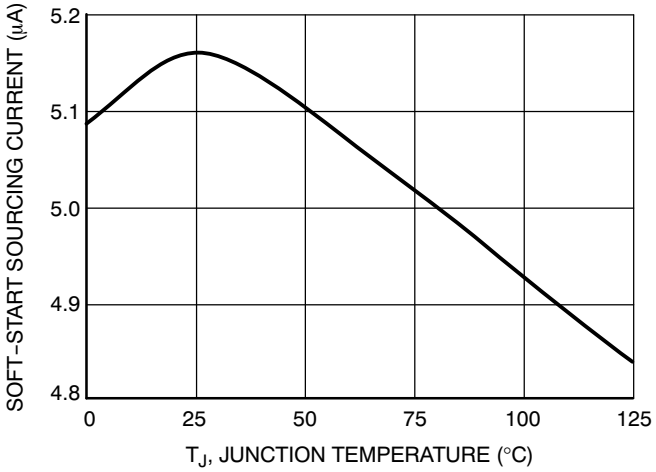


Figure 5. Soft−Start Sourcing Current vs. Temperature

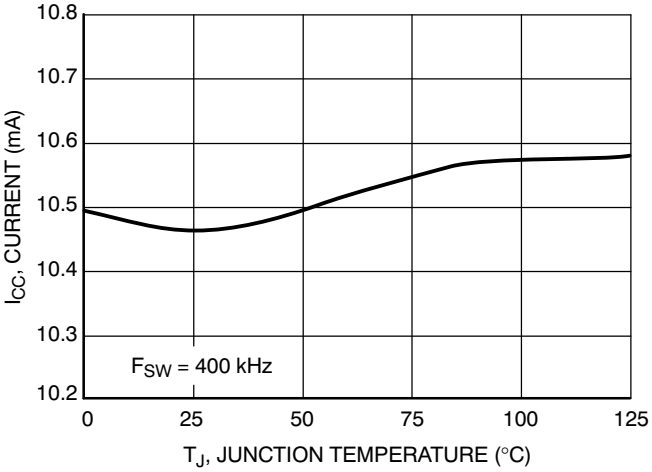


Figure 6. I_{CC} Current vs. Temperature

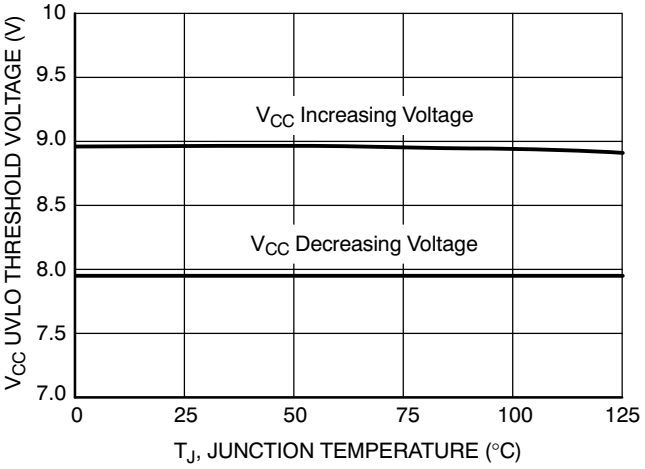


Figure 7. V_{CC} UVLO Threshold Voltage vs. Temperature

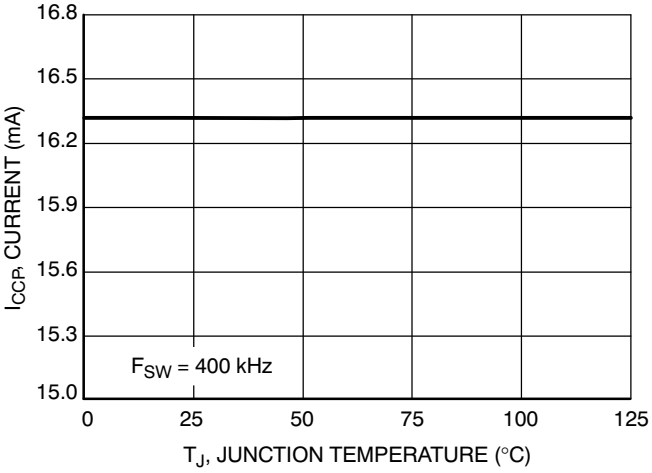


Figure 8. I_{CCP} Current vs. Temperature

TYPICAL CHARACTERISTICS

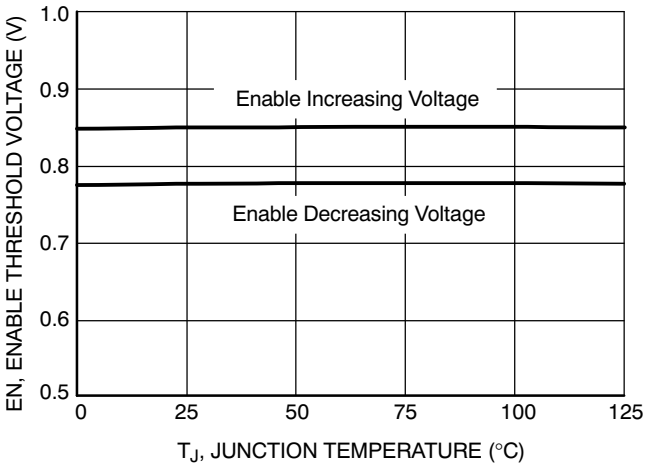


Figure 9. Enable Threshold Voltage vs. Temperature

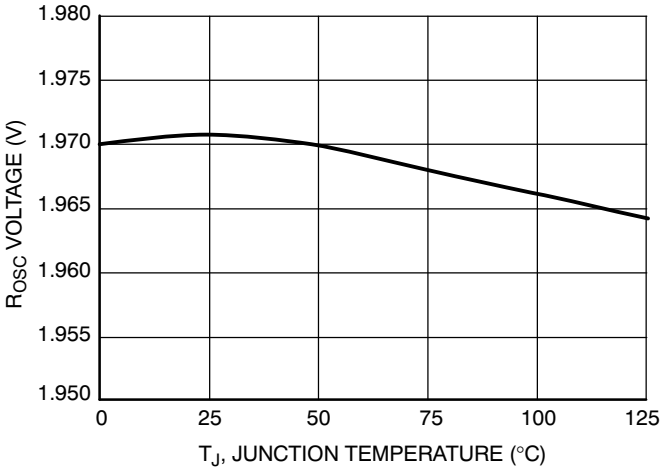


Figure 10. R_{OSC} Voltage vs. Temperature

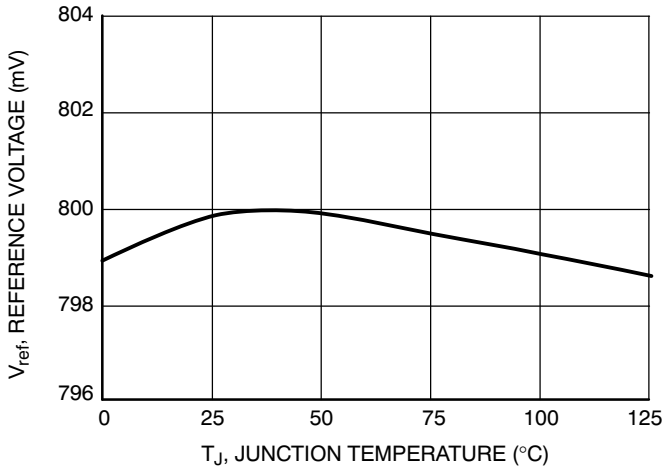


Figure 11. Reference Voltage vs. Temperature

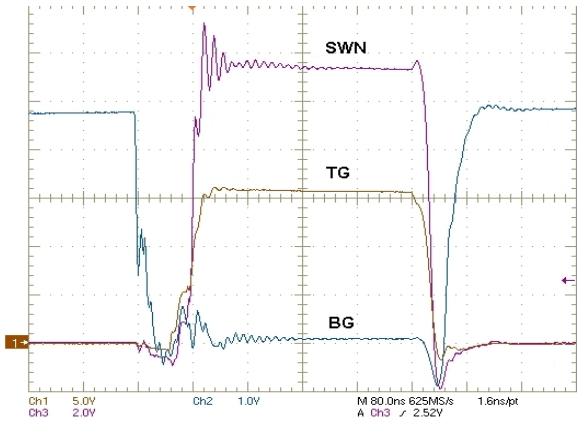


Figure 12. 20 A Sustaining Load

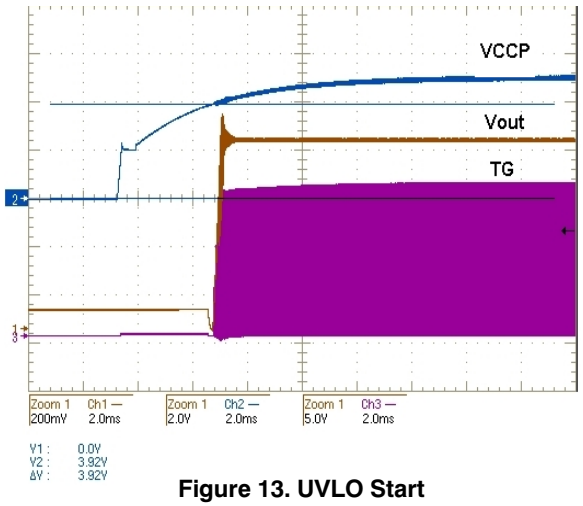


Figure 13. UVLO Start

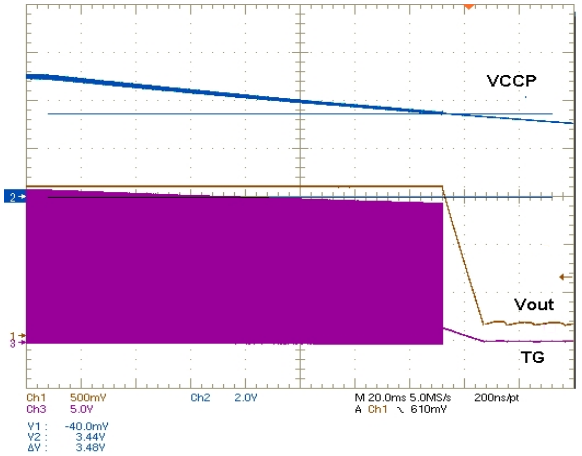


Figure 14. UVLO Stop

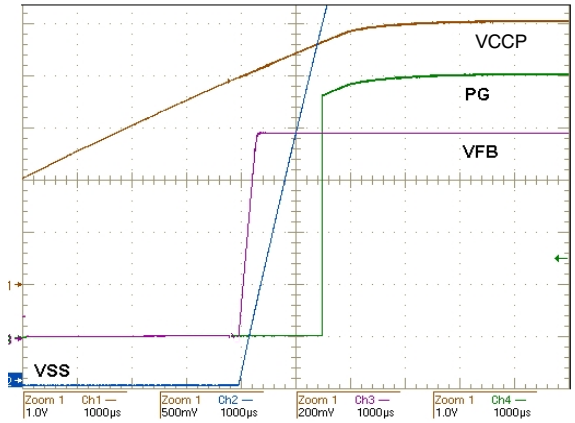


Figure 15. Power−up Waveforms

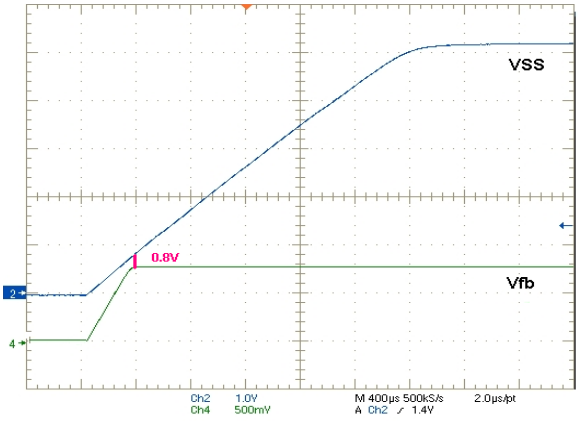


Figure 16. Soft Start Sequence

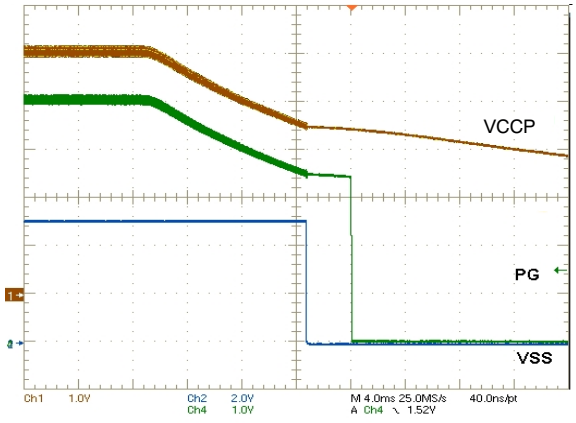


Figure 17. Power−down Waveforms

APPLICATIONS INFORMATION

General

The NCP5383 dual edge modulated multiphase PWM controller is specifically designed with the necessary features for a high current power system. The IC consists of the following blocks: High Performance Voltage Error Amplifier, Precision Oscillator and Triangle Wave Generators, and PWM Comparators. Protection features include Undervoltage Lockout, Soft−Start, Overcurrent Protection, Thermal Shutdown and Power Good Monitor.

High Performance Voltage Error Amplifier

The error amplifier is designed to provide high slew rate and bandwidth. A capacitor from COMP to V_{FB} is required for stable unity gain test configurations.

Oscillator and Triangle Wave Generator

A programmable precision oscillator is provided. The oscillator 's frequency is programmed by the resistance connected from the R_{OSC} pin to ground. The user will usually form this resistance from two resistors in order to create a voltage divider that uses the R_{OSC} output voltage as the reference for creating the current limit setpoint voltage. The oscillator frequency range is 100 kHz/phase to 400 kHz/phase. The oscillator generates 2 triangle waveforms (symmetrical rising and falling slopes) between 1.3 V and 2.3 V. The triangle waves have a phase delay between them such that for 2 phase operation the PWM outputs are separated by 180 degrees.

PWM Comparators with Hysteresis

Two PWM comparators receive the error amplifier output signal at their non inverting input. Each comparator receives one of the triangle waves offset by 1.3 V at it's inverting input. During steady state operation, the duty cycle will center on the valley of the triangle waveform, with steady state duty cycle calculated by V_{out}/V_{in}. During a transient event, both high and low comparator output transitions shift phase to the points where the error amplifier output intersects the down and up ramp of the triangle wave.

PROTECTION FEATURES

Undervoltage Lockout

An undervoltage lockout (UVLO) senses the V_{CC} input. During powerup, the input voltage to the controller is monitored, and the PWM outputs and the soft−start circuit are disabled until the input voltage exceeds the threshold voltage of the UVLO comparator. The UVLO comparator incorporates hysteresis to avoid chattering, since V_{CC} is likely to decrease as soon as the converter initiates soft−start. There is a separate undervoltage lockout (UVLO) for the drivers that sense the V_{CCP} inputs.

Overcurrent Shutdown

A programmable overcurrent function is incorporated within the IC. A comparator and latch makeup this function. The inverting input of the comparator is connected to the ILIM pin. The voltage at this pin sets the maximum output current the converter can produce. The ROSC pin provides a convenient and accurate reference voltage from which a resistor divider can create the overcurrent setpoint voltage. Although not actually disabled, tying the ILIM pin directly to the ROSC pin sets the limit above useful levels – effectively disabling overcurrent shutdown. The comparator non inverting input is the summed current information from the current sense amplifiers. The overcurrent latch is set when the current information exceeds the voltage at the ILIM pin. The outputs are immediately, and the soft−start is pulled low. The outputs will remain disabled until the V_{CC} voltage is removed and re−applied, or the ENABLE input is brought low and then high.

Power Good Monitor

NCP5383 has a power good monitor set at 125% of Vfb or 75% of Vfb for upper and lower thresholds respectively. It is an open drain type output.

Soft−Start

The NCP5383 incorporates an externally programmable soft−start. The soft−start circuit works by controlling the ramp−up of the Vref voltage during powerup. The initial soft−start pin voltage is 0 V. The soft−start sequence ends when V_{SS} = 0.8 V. The soft−start pin is pulled to 0 V if there is an overcurrent shutdown, if V_{CC} is below the UVLO threshold, or if V_{CCP} is below the UVLO threshold.

Programming the Current Limit and Oscillator Frequency

The OSC pin provides a 2.0 V reference voltage which is divided down with a resistor divider and fed into the current limit pin ILIM. Calculate the total series resistance to set the frequency and then calculate the individual values for current limit divider. The series resistors RLIM1 and RLIM2 sink current to ground. This current is internally mirrored into a capacitor to create an oscillator. The period is proportional to the resistance and frequency is inversely proportional to the resistance.

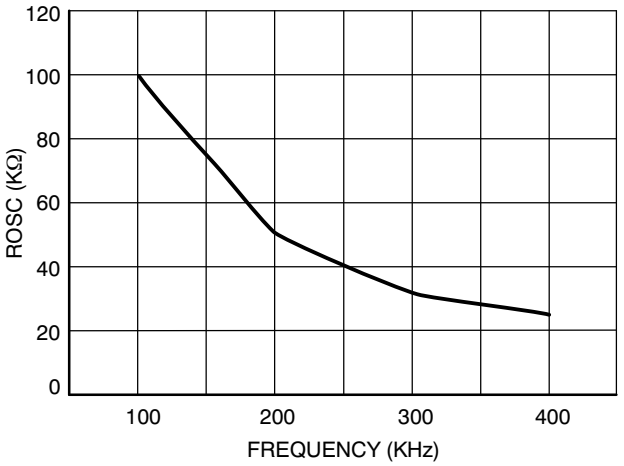


Figure 18. ROSC vs. Phase Frequency

Calculate the current limit voltage:

The current limit function is based on the total sensed current of two phases multiplied by a gain of 5.94. DCR sensed inductor current is function of the winding temperature. The best approach is to set the maximum current limit based on the expected average maximum temperature of the inductor windings.

$$DCR_{Tmax} = DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1} (T_{Tmax} - 25 \cdot C)) \quad \text{(eq. 1)}$$

$$V_{ILIMIT} \cong 5.94 \cdot \left(I_{MIN\_OCP} \cdot DCR_{Tmax} + \frac{DCR_{50C} \cdot Vout}{2 \cdot Vin \cdot F_s} \cdot \left(\frac{Vin - Vout}{L} - (N-1) \cdot \frac{Vout}{L} \right) \right) - 0.02 \quad \text{(eq. 2)}$$

Solve for the individual resistors:

$$RLIM2 = \frac{V_{ILIMIT} \cdot ROSC}{2 \cdot V} \qquad RLIM1 = ROSC - RLIM2 \quad \text{(eq. 3)}$$

Final Equation for the Current Limit Threshold

$$I_{LIMIT}(T_{inductor}) \cong \frac{\left(\frac{2 \cdot V \cdot RLIM2}{RLIM1 + RLIM2}\right) + 0.02}{5.94 \cdot (DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1}(T_{Inductor} - 25 \cdot C)))} - \frac{Vout}{2 \cdot Vin \cdot F_s} \cdot \left(\frac{Vin - Vout}{L} - 1 \cdot \frac{Vout}{L} \right) \quad \text{(eq. 4)}$$

Selecting the closest available values of 16.9 KΩ for RLIM1 and 15.8 KΩ yield a nominal operating frequency of 305 Khz and an approximate current limit of 180 A at 100C. The total sensed current can be observed at the VDRP pin added to a positive, no−load offset of approximately 0.8 V.

Inductor Selection:

When using the inductor current sensing it is recommended that the inductor does not saturate by more than 10% at the maximum load. The inductor also must not go into hard saturation before current limit trips. Small DCR values can be used, however current sharing accuracy and droop accuracy decrease as DCR decreases.

Inductor Current Sense Compensation

The NCP5383 uses the inductor current sensing method. This method uses an RC filter to cancel out the inductance of the inductor and recover the voltage that is the result of the current flowing through the inductor's DCR. This is done by matching the RC time constant of the current sense filter to the L/DCR time constant. The first cut approach is to use a 0.47 μF capacitor for C and then solve for R.

$$Rsense(T) = \frac{L}{0.47 \cdot \mu F \cdot DCR_{25C} \cdot (1 + 0.00393 \cdot C^{-1} \cdot (T - 25 \cdot C))} \quad \text{(eq. 5)}$$

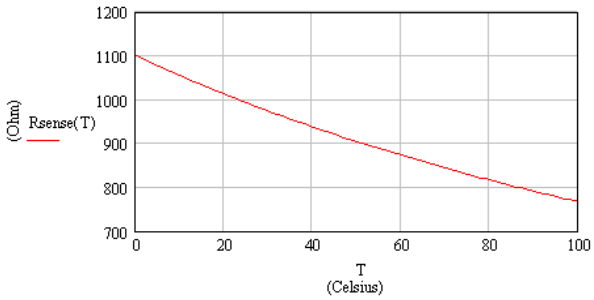


Figure 19.

The demoboard inductor measured 950 nH and 0.75 mΩ at room temp. The actual value used for Rsense matches the equation for Rsense at approximately 50C. Because the inductor value is a function of load and inductor temperature final selection of R is best done experimentally on the bench by monitoring the Vdroop pin and performing a step load test on the actual solution.

It is desirable to keep the Rsense resistor value below 1.0 k whenever possible by increasing the capacitor values in the inductor compensation network. The bias current flowing out of the current sense pins is approximately 100 nA. This current flows through the current sense resistor and creates an offset at the capacitor which will appear as a load current at the Vdroop pin. A 1.0 k resistor will keep this offset at the droop pin below 2.5 mV.

Simple Average PSPICE Model

A simple state average model shown in Figure 20 can be used to determine a stable solution and provide insight into the control system.

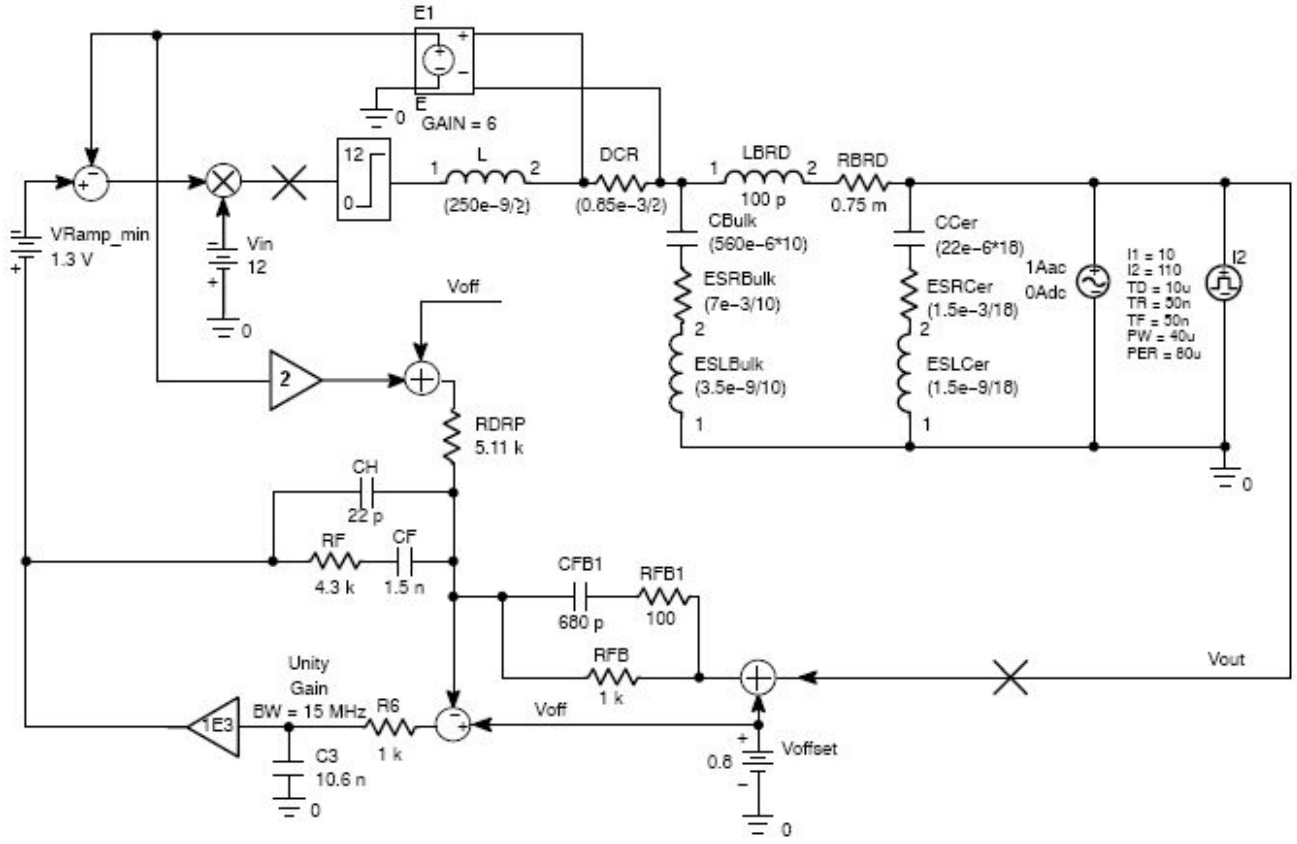


Figure 20.

Droop Injection

The VDRP signal is generated by summing the sensed output currents for each phase and applying a gain of approximately six. VDRP is externally summed into the feedback network by the resistor RDRP. This induces an offset which is proportional to the output current thereby forcing the controlled resistive output impedance.

RRDP determines the target output impedance by the basic equation:

$$\frac{Vout}{Iout} = Zout = \frac{RFB \cdot DCR \cdot 5.94}{RDRP} \qquad \text{(eq. 6)}$$

$$RDRP = \frac{RFB \cdot DCR \cdot 5.94}{Zout}$$

Thermal Shutdown

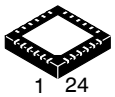
The NCP5383 also provides Thermal Shutdown (TSD) for added protection. The TSD circuit monitors the die temperature and turns off the top and bottom gate drivers if an over temperature condition is detected. The internal soft−start capacitor is also discharged. This is a latched state and requires a power cycle to reset.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

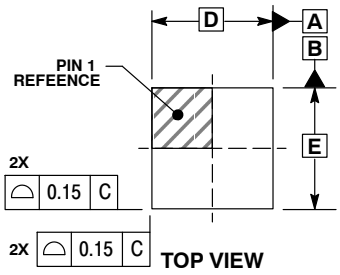
ON Semiconductor®

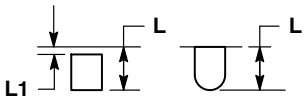
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

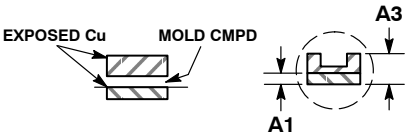
DATE 05 JUN 2012

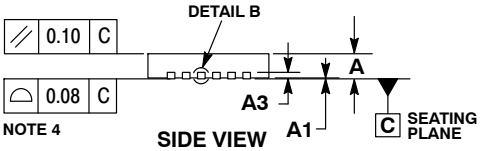


SCALE 2:1



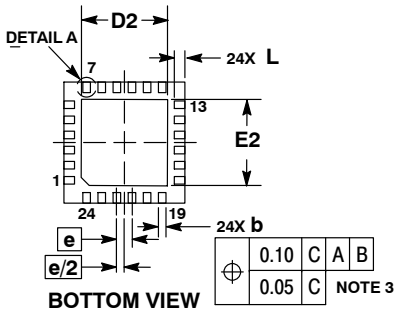






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50
L1	0.05	0.15



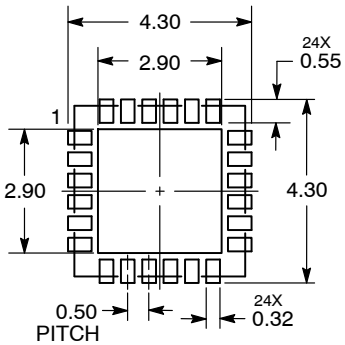
GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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