8T49N282 Evaluation Board Quick Reference User Guide

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Introduction

The 8T49N282I evaluation board is designed to help the customer evaluate the IDT8T49N281, IDT8T49N282, and IDT8T49N283 devices, the latest additions to IDT's 3rd generation Universal Frequency Translator family. When the board is connected to a PC running IDT Timing Commander™ software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Requirements

1. PC Requirements:

- IDT Timing Commander software installed.
- **USB 2.0 interface**. The evaluation board USB module is not compatible with USB 3.0. If using a computer with high speed USB ports, please check if there's a standard USB 2.0 port available for use. The hardware drivers are automatically installed during the Timing Commander installation.
- Windows XP SP3 or later.
- Processor: Minimum 1GHz.
- Memory: Minimum 512MB, recommended 1GB.
- Available Disk Space: Min 600MB (1.5GB 64bit), recommended 1GB (2GB 64bit)
- Network access during installation if the .NET framework is not currently installed on the system.

2. Power Supply with 3.3V and 1000mA rating

3. Three banana plug cables to connect the power supply to the board.

Quick Start: Powering Up the Board

(1) Set 3.3V supply current limit to 500mA.

(2) Remove all output terminations.

(3) Set Dip Switch selectors to the middle position.

(4) Connect a cable from a PC to the USB port.

(5) Connect VEE to the black GND jack.

(6) Connect 3.3V to VCC_J and VDDO_J.

(7) Power on the Power Supply.

(8) Press the Reset Button.

Once correct operation is verified, set the power supply limit for the number of outputs to be active.

The USB port must be powered by the PC in order to have the correct I^2C bus voltage levels.

Default Power-Up Condition

The board ships with a 38.88MHz crystal and will have a default frequency of 155.52MHz on Q0. If all outputs are unterminated, current should measure ~256mA with 3.3V on VCC_J and VDDO_J. If all outputs are terminated, current should measure ~262mA.

When evaluating performance with the default hardware configuration, it is recommended that all active outputs be terminated 50ohms to VEE by either terminator plugs or an instrument.

Inputs:

Differential Inputs

Connect the input signal to CLKx and nCLKx. For CLK0, the CLK0_S and nCLK0_s sense lines are available for observation of the signal. They can be connected with 50ohm impedance cables to an oscilloscope with 50ohm termination, otherwise, they should be terminated with 50ohm plugs in order prevent reflections.

Single-ended Input

Connect the input signal to CLKx and float nCLKx. For CLK0, connect CLK0_S with a 50ohm impedance cable to an oscilloscope with 50ohm termination or terminate with a 50ohm plug.

Input Signals Below 1MHz

For slow-frequency signals below 1MHz, we recommend that the coupling capacitors for the corresponding input be replaced with zero-ohm resistors and that the signal input dc-offset be set so that it meets the device's Vcmr requirements. Refer to the schematics for location of the ac-coupling capacitors.

Outputs:

The outputs are ac-coupled, allowing for maximum flexibility for observation of the output whether configured for LVPECL, LVDS, or LVCMOS levels. The default termination scheme can be used to measure either of the three output level-types.

Output Signals Below 1MHz

For slow-frequency output signals below 1MHz, we recommend that the 1µF ac-coupling capacitors be replaced with 0ohm resistors and that the correct terminations be provided at the receiver.

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