Ultra-Low Capacitance ESD Protection Diodes

Micro−Packaged Diodes for ESD Protection

ESDL3552B

The ESDL3552B is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, high breakdown voltage, high linearity, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. It has industry leading capacitance linearity over voltage making it ideal for high−speed data line protection applications.

Features

- Industry Leading Capacitance Linearity Over Voltage
- Ultra−Low Capacitance: 0.25 pF
- Insertion Loss: 0.26 dB @ 5 GHz
- 0201 Isolated DSN Package: 0.62 mm x 0.32 mm
- Stand−off Voltage: 5.0 V
- Low Leakage: < 50 nA
- Low Dynamic Resistance: < 1.0 Ω
- These Devices are Pb−Free, Halogen−Free/BFR−Free and are RoHS Compliant

Typical Applications

- High Speed Data Line Protection
- USB 2.0, USB 3.0, USB 3.1

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

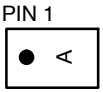
Rating	Symbol	Value	Unit
IEC 61000−4−2 Level 4 (Contact) (Note 1) IEC 61000−4−2 Level 4 (Air) (Note 1)	ESD	±20 ±20	kV
Maximum Peak Pulse Current IEC 61000−4−5 8/20 μs (Lightning) (Note 2)	I_{PP}	2.0	A
Total Power Dissipation (Note 3) @ T_A = 25°C Thermal Resistance, Junction−to−Ambient	P_D $R_{\theta JA}$	300 400	mW °C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

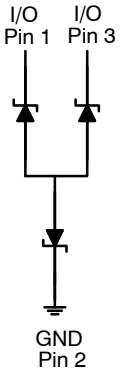
1. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−2 waveform.
2. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.
3. Mounted with recommended minimum pad size, DC board FR−4

X4DFN3
CASE 718AB

MARKING DIAGRAM



A = Specific Device Code



ORDERING INFORMATION

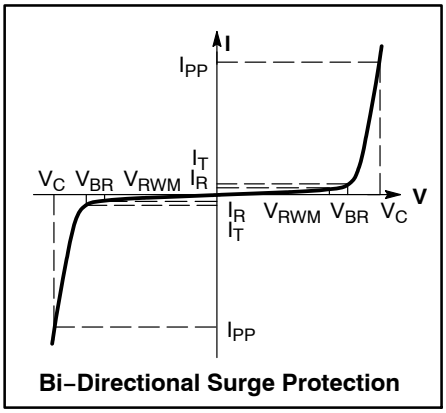
Device	Package	Shipping†
ESDL3552BPFCT5G	X4DFN3 (Pb−Free/ Halide Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS
(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional Surge Protection

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Between any two pins (−40°C to +85°C)			5.0	V
Breakdown Voltage	V_{BR}	I_T = 10 mA, Between any two pins (−40°C to +85°C)	6.5	10.2	11.5	V
		I_T = 1 mA, Between any two pins	7.0	9.3	11	
Reverse Leakage Current	I_R	V_{RWM} = 5.0 V, T_A = 25°C		0.001	0.05	μA
		V_{RWM} = 5.0 V, T_A = 85°C		0.001	0.25	μA
Clamping Voltage TLP	V_C	I_{PP} = 4 A } IEC 61000−4−2 Level 1 equivalent (±2 kV Contact, ±4 kV Air) Pin 1 to Pin 2, Pin 3 to Pin 2		14.5		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±16 kV Air) Pin 1 to Pin 2, Pin 3 to Pin 2		21.5		V
Reverse Peak Pulse Current	I_{PP}	IEC61000−4−5 (8x20 μs), Between any two pins	2.0	3.0		A
Clamping Voltage (8x20 μs)	V_C	I_{PP} = 2 A		14	18	V
Dynamic Resistance	R_{DYN}	100 ns TLP, Pin 1 to Pin 2, Pin 3 to Pin 2		0.58		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz, Between any two pins		0.25	0.30	pF
Capacitance Linearity	C_Δ	V_R = 0 V to 5 V, f = 1 MHz		0.03		pF
Insertion Loss	I_L	f = 2.5 GHz f = 5.0 GHz f = 10.0 GHz		0.16 0.26 0.41		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

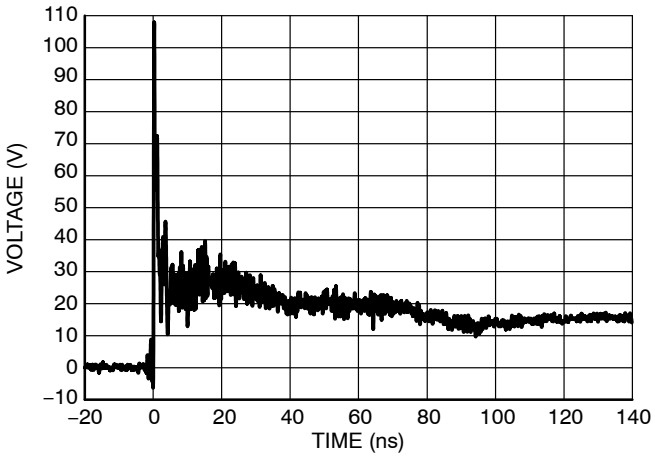


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

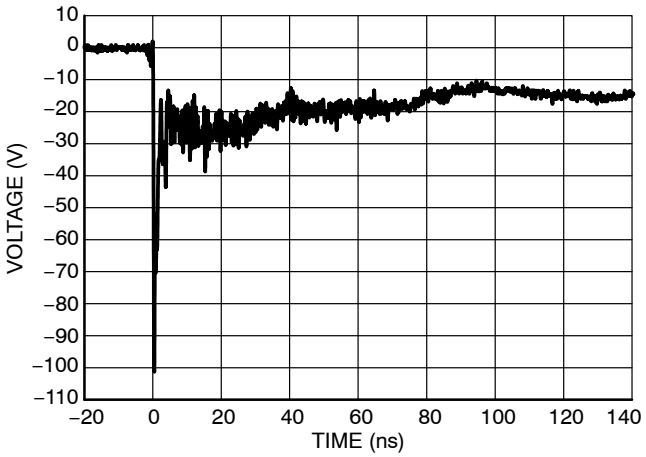


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

TYPICAL CHARACTERISTICS

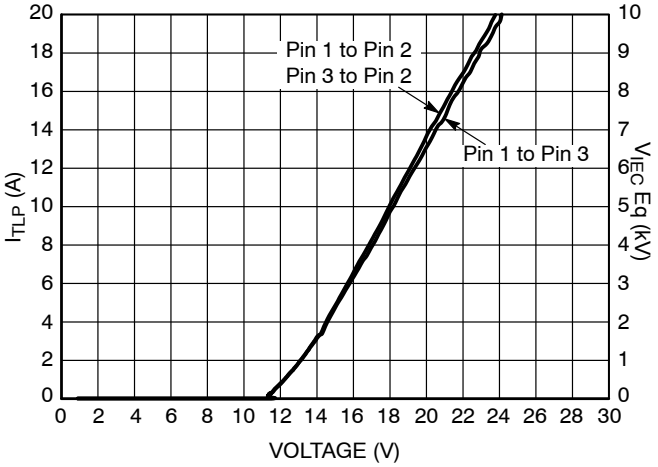


Figure 3. Positive TLP I–V Curve

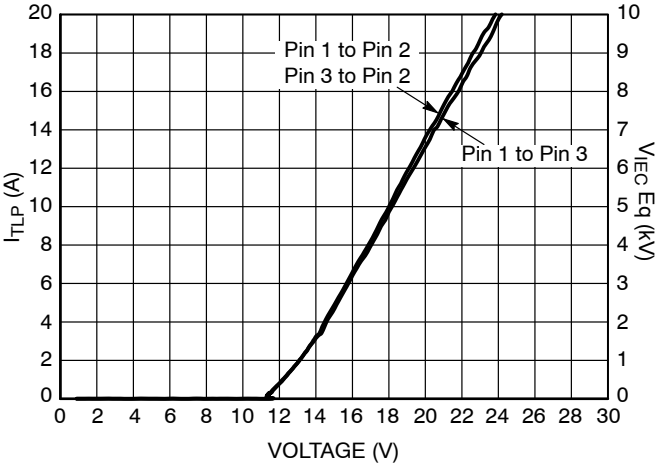


Figure 4. Negative TLP I–V Curve

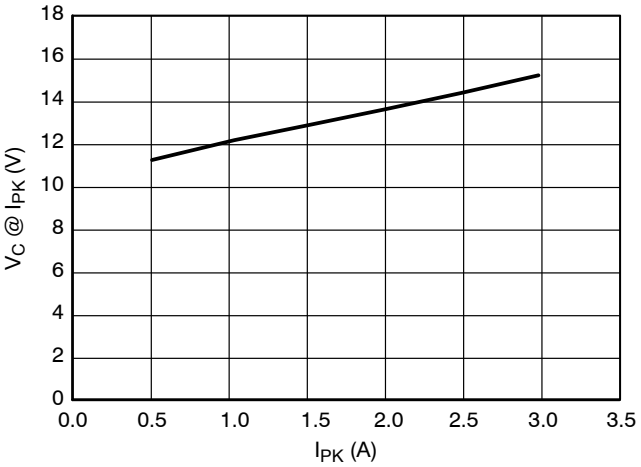


Figure 5. Positive Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs)

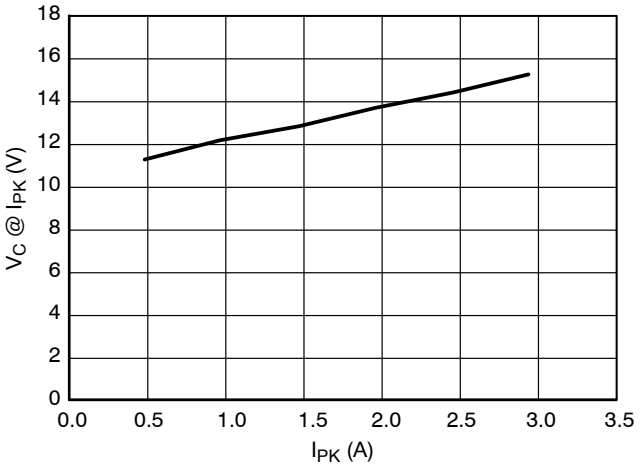


Figure 6. Negative Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs)

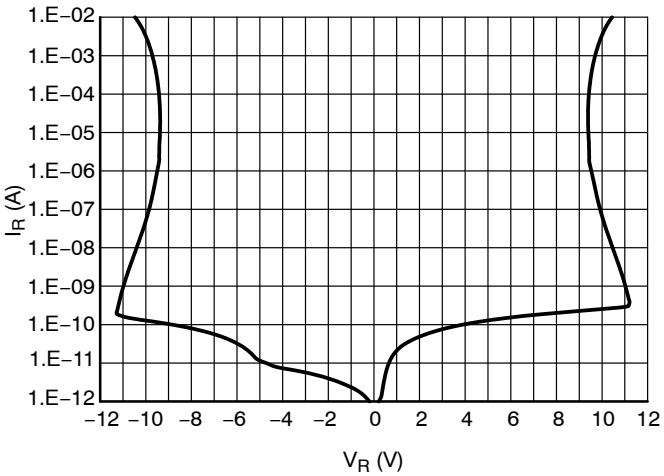


Figure 7. Breakdown Voltage

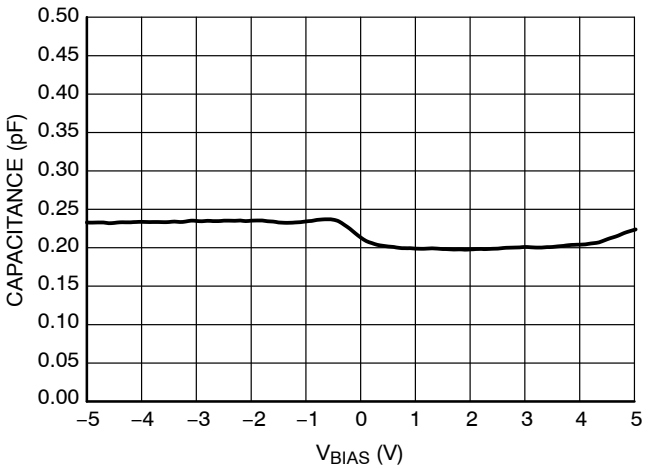


Figure 8. Line Capacitance, f = 1 MHz

TYPICAL CHARACTERISTICS

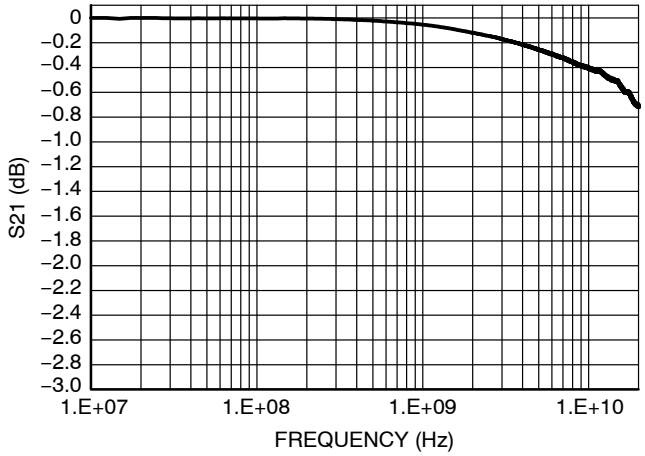


Figure 9. Insertion Loss

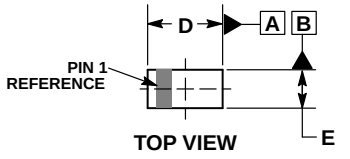
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

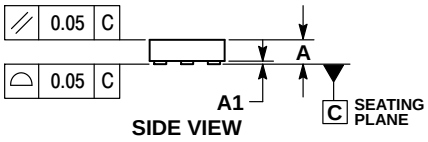
X4DFN3 0.62x0.32, 0.225P
CASE 718AB
ISSUE A

SCALE 8:1

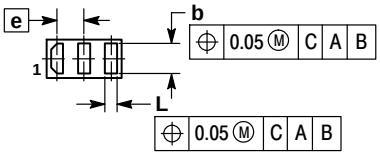
DATE 13 MAR 2018



TOP VIEW



SIDE VIEW

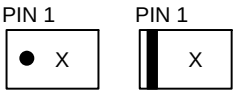


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

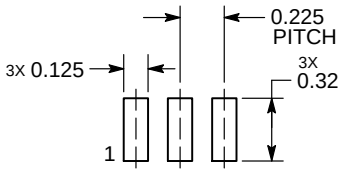
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.175	0.20	0.225
A1	0.000	0.015	0.030
b	0.23	0.25	0.27
D	0.595	0.620	0.645
E	0.295	0.320	0.345
e	0.225 BSC		
L	0.08	0.10	0.12

GENERIC MARKING DIAGRAMS*



X = Specific Device Code

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**X4DFN3 0.62x0.32, 0.225P**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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