

## KAI-1003 Imager Board User's Manual



ON Semiconductor®

<http://onsemi.com>

### Eval Board User's Manual

#### KAI-1003 Imager Evaluation Board Description

The KAI-1003 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be used as part of a two-board set, used in conjunction with a Timing Generator Board. ON Semiconductor offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAI-1003 Image Sensor.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J3). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KAI-1003 Imager Board has been designed to operate the KAI-1003 with the specified performance at 20 MHz pixel clocking rate and nominal operating conditions. (See the KAI-1003 performance specification for details).

For testing and calibration purposes, the KAI-1003 Imager board provides the ability to adjust the CCD substrate bias voltages and Reset Low CCD clock level voltage by adjusting potentiometers on the board.

### IMAGER BOARD INPUT REQUIREMENTS

Table 1. POWER REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5.0	5.1	V
-5 V_MTR Supply	-5.1	-5.0	-4.9	V
VPLUS Supply	18	20	21	V
VMINUS Supply	-21	-20	-18	V

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V <sub>min</sub>	V <sub>threshold</sub>	V <sub>max</sub>	Units	Comments
H1A (±)	0	±0.1	2.4	V	H1A clock
H1B (±)	0	±0.1	2.4	V	H1B clock
H2 (±)	0	±0.1	2.4	V	H2A clock
R (±)	0	±0.1	2.4	V	Reset clock
V1 (±)	0	±0.1	2.4	V	V1 clock
V2 (±)	0	±0.1	2.4	V	V2 clock
FDG	0	±0.1	2.4	V	Fast Dump clock
V3RD (±)	0	±0.1	2.4	V	V1 Clock 3 <sup>rd</sup> level
VES (±)	0	±0.1	2.4	V	Electronic Shutter

**KAI-1003 IMAGER BOARD ARCHITECTURE OVERVIEW**

The following sections describe the functional blocks of the KAI-1003 Imager board (Refer to Figure 1).

**Power Filtering and Regulation**

Power is supplied to the Imager Board via the J3 interface connector. The power supplies are de-coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V and -15 V supplies from the VPLUS and VMINUS supplies.

**LVDS Receivers / TTL Buffers**

LVDS timing signals are input to the Imager Board via the J3 interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

**CCD Pixel-Rate Clock Drivers (H1, H2 & Reset Clocks)**

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL-level input clock signals to the voltage levels required by the CCD. The low and high levels of the reset CCD clock are set by potentiometers.

Please note that the silkscreen text has been removed near H1A, H2A, and H2B, as it was incorrect. The silkscreen for the Test Points is correct and may be used to probe the pixel rate clocks as shown in Table 3.

**Table 3. PIXEL RATE CLOCK TEST POINT LOCATIONS**

Testpoint	Pixel Rate Clock
TP8	H2A_CCD
TP10	H1B_CCD
TP12	H2B_CCD
TP13	H1A_CCD

**Reset Clock One-Shot (U9; not populated)**

The pulse width of the RESET\_CCD clock used to be set by a programmable One-Shot. It was configured to provide a pulse width from 5 ns to 15 ns. Now, the pulse width control functionality is provided by the KSC-1000 based Timing Generator Board, and the one-shot has been bypassed by removing U9 and inserting a shorting resistor on pads 1 and 2 of U9.

**CCD VCLK Drivers**

The vertical clock (VCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL-level clock signals to the voltage levels required by the CCD. The current sources for these voltage levels are high current (up to 600 mA) transistors. The V2\_CCD high level clock voltage is switched from V\_MID to V\_HIGH once per frame to transfer the charge from the photodiodes to the vertical CCDs.

**CCD FDG Driver**

The KAI-1003 does not use a Fast Dump Gate (FDG) circuit. The FDG signal is located on the interface connector but is not connected beyond the TTL buffer IC.

**VES Circuit**

The quiescent CCD substrate voltage (VSUB) is set by a potentiometer. For electronic shutter operation, the VES signal drives a transistor amplifier circuit that AC-couples the voltage difference between the VPLUS and VMINUS supplies onto the Substrate voltage. This creates the necessary potential to clear all charge from the photodiodes, thereby acting as an electronic shutter to control exposure.

**CCD Bias Voltages**

All CCD bias voltages are fixed on the KAI-1003 Imager Board except VSUB, which can be set by a potentiometer.

**CCD Image Sensor**

This evaluation board supports the KAI-1003 Image Sensor.

**Emitter-Follower**

The VOUT\_CCD signals are buffered using bipolar junction transistors in an emitter-follower configuration that also provides the necessary 5 mA current sink for the CCD output circuits.

**Line Drivers**

The buffered VOUT\_CCD signals are AC-coupled and driven from the Imager Board by operational amplifiers in a non-inverting configuration. The operational amplifiers are configured to have a gain of 1.25, to correctly drive 75 Ω video coaxial cabling from the SMB connectors.

**KAI-1003 OPERATIONAL SETTINGS**

The Imager board is configured to operate the KAI-1003 CCD image sensor under the following operating conditions:

were correct at the time of this document's publication, but may be subject to change; refer to the KAI-1003 device specification.

**Bias Voltages**

The following voltages are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 4

**Table 4. BIAS VOLTAGES**

Description	Symbol	Min	Nom	Max	Units	Potentiometer
Output Amplifier Supply	VDD	12.0	15.0	15.0	V	
Output Amplifier Return	VSS		0		V	
Output Gate	VOG	1.8	2.0	2.2	V	
Reset Drain	VRD	10.0	10.5	11.0	V	
Ground, P-Well	GND		0		V	
Substrate	VSUB	8.0	Vsub	18.0	V	R56
Disable ESD Protection	VMIN		-8.5		V	
Output Amplifier Load Gate	VLG	1.4	1.5	1.6	V	

**Clock Voltages**

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The nominal values listed in

Table 5 were correct at the time of this document's publication, but may be subject to change; refer to the KAI-1003 device specification.

**Table 5. CLOCK VOLTAGES**

Description	Symbol	Level	Min	Nom	Max	Units	Potentiometer
Horizontal CCD Clocks	Hxx_CCD	Low	-6.5	-6.0	-5.5	V	
		High	4.5	5.0	5.5	V	
Vertical CCD Clock V1	V1_CCD	Low	-9.0	-8.5	-8.0	V	
		High	-0.8	-0.5	0.0	V	
Vertical CCD Clock V2	V2_CCD	Low	-9.0	-8.5	-8.0	V	
		Mid	-0.8	-0.5	0.0	V	
		High	9.5	10.5	11.5	V	
Reset Clock	RESET_CCD	Low	0	TBS	5.0	V	R28
		Amplitude		5.0		V	R64
Electronic Shutter Pulse	VES_CCD		37	40	45	V	

BLOCK DIAGRAM AND PERFORMANCE DATA

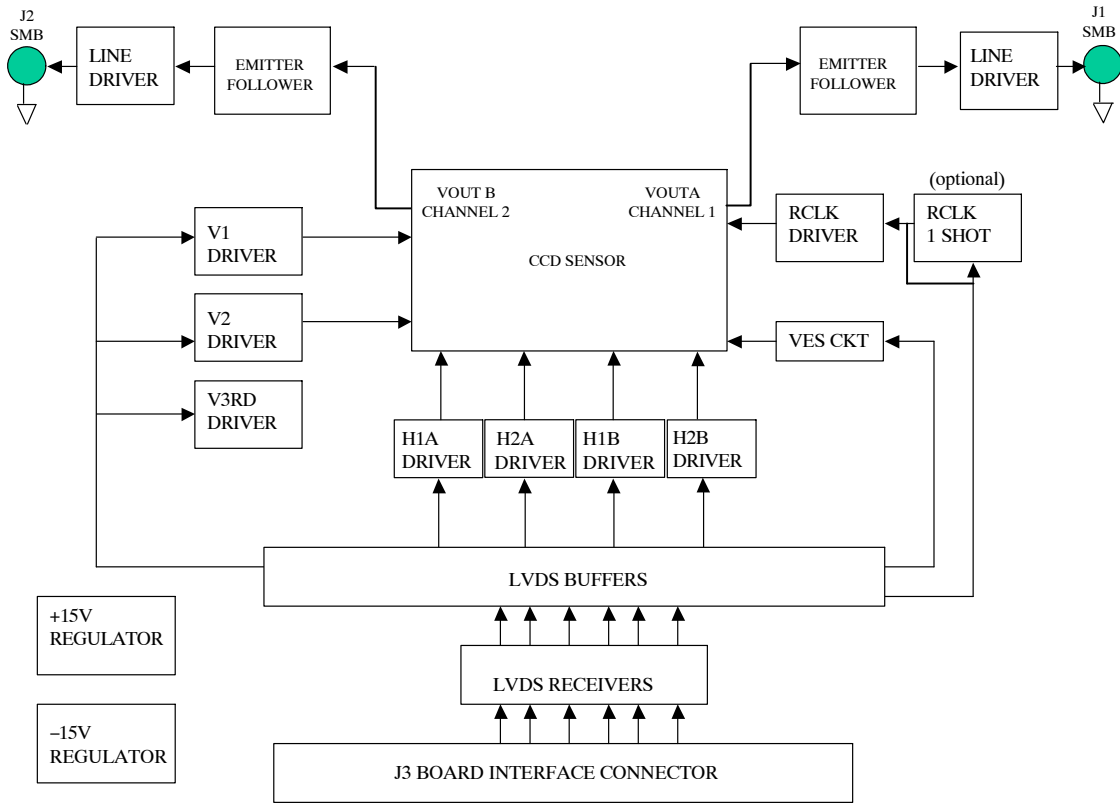


Figure 1. KAI-1003 Imager Board Block Diagram

LINEARITY

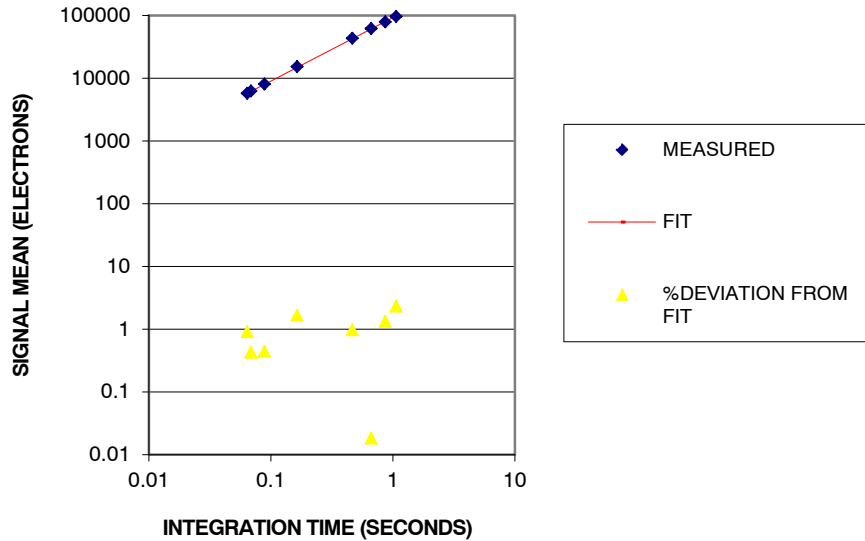


Figure 2. Measured Performance – Linearity

# EVBUM2269/D

## Photon Transfer

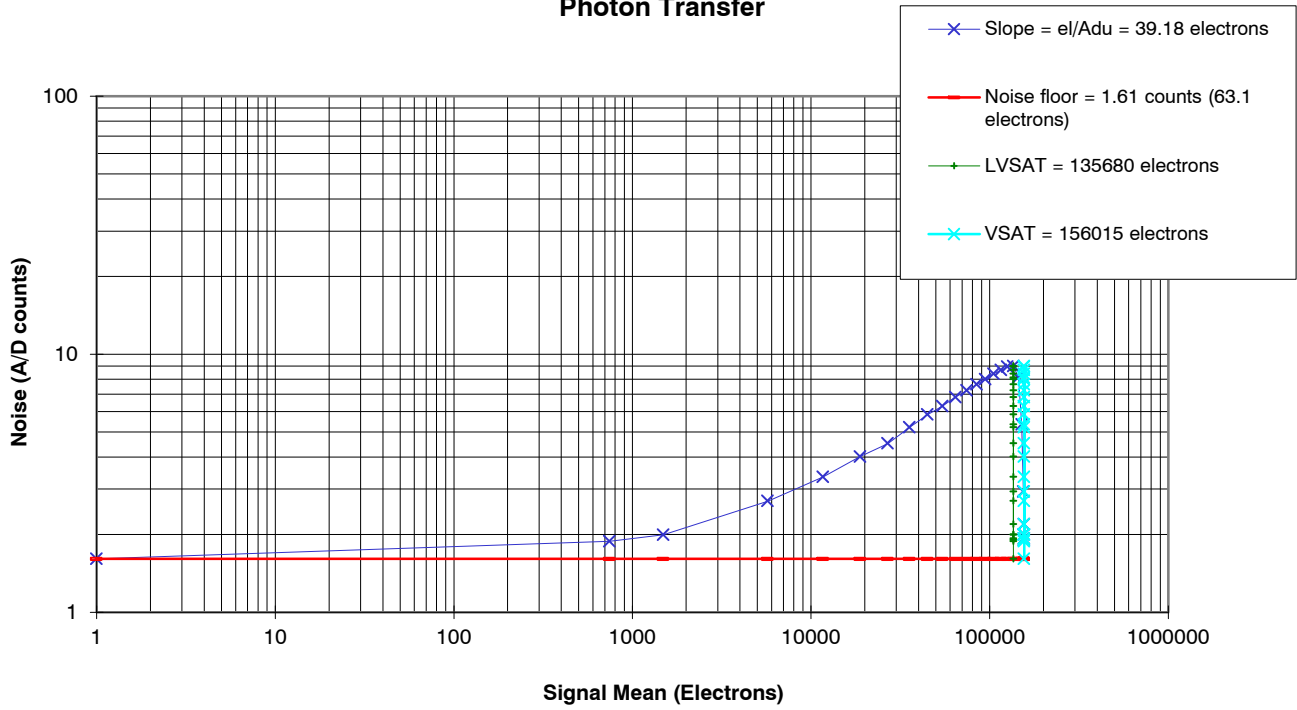


Figure 3. Measured Performance – Dynamic Range and Noise Floor

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J1 and J2

The emitter–follower buffered CCD\_VOUT signals are driven from the Imager Board via the SMB connectors J1 and J2. Coaxial cable with a characteristic impedance of

75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Table 6. J4 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	VES+	6	VES-
7	AGND	8	AGND
9	FDG+	10	FDG-
11	AGND	12	AGND
13	V3RD+	14	V3RD-
15	AGND	16	AGND
17	V2B+	18	V2B-
19	AGND	20	AGND
21	V2+	22	V2-
23	AGND	24	AGND
25	V1+	26	V1-
27	AGND	28	AGND
29	R+	30	R-
31	AGND	32	AGND
33	H2B+	34	H2B-
35	AGND	36	AGND
37	H2A+	38	H2A-
39	AGND	40	AGND
41	H1B+	42	H1B-
43	AGND	44	AGND
45	H1A+	46	H1A-
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	N.C.	60	N.C.
61	-5 V_MTR	62	-5 V_MTR
63	N.C.	64	N.C.
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

## Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the ON Semiconductor Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

## Ordering Information

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.  
1964 Lake Avenue  
Rochester, New York 14615  
Phone: (585) 784-5500  
E-mail: info@truesenseimaging.com

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

The evaluation board/kit (research and development board/kit) (hereinafter the "board") is not a finished product and is not available for sale to consumers. The board is only intended for research, development, demonstration and evaluation purposes and will only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. This person assumes full responsibility/liability for proper and safe handling. Any other use, resale or redistribution for any other purpose is strictly prohibited.

**THE BOARD IS PROVIDED BY ONSEMI TO YOU "AS IS" AND WITHOUT ANY REPRESENTATIONS OR WARRANTIES WHATSOEVER. WITHOUT LIMITING THE FOREGOING, ONSEMI (AND ITS LICENSORS/SUPPLIERS) HEREBY DISCLAIMS ANY AND ALL REPRESENTATIONS AND WARRANTIES IN RELATION TO THE BOARD, ANY MODIFICATIONS, OR THIS AGREEMENT, WHETHER EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, INCLUDING WITHOUT LIMITATION ANY AND ALL REPRESENTATIONS AND WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, NON-INFRINGEMENT, AND THOSE ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE CUSTOM OR TRADE PRACTICE.**

**onsemi** reserves the right to make changes without further notice to any board.

You are responsible for determining whether the board will be suitable for your intended use or application or will achieve your intended results. Prior to using or distributing any systems that have been evaluated, designed or tested using the board, you agree to test and validate your design to confirm the functionality for your application. Any technical, applications or design information or advice, quality characterization, reliability data or other services provided by **onsemi** shall not constitute any representation or warranty by **onsemi**, and no additional obligations or liabilities shall arise from **onsemi** having provided such information or services.

**onsemi** products including the boards are not designed, intended, or authorized for use in life support systems, or any FDA Class 3 medical devices or medical devices with a similar or equivalent classification in a foreign jurisdiction, or any devices intended for implantation in the human body. You agree to indemnify, defend and hold harmless **onsemi**, its directors, officers, employees, representatives, agents, subsidiaries, affiliates, distributors, and assigns, against any and all liabilities, losses, costs, damages, judgments, and expenses, arising out of any claim, demand, investigation, lawsuit, regulatory action or cause of action arising out of or associated with any unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of any products and/or the board.

This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and may not meet the technical requirements of these or other related directives.

FCC WARNING – This evaluation board/kit is intended for use for engineering development, demonstration, or evaluation purposes only and is not considered by **onsemi** to be a finished end product fit for general consumer use. It may generate, use, or radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment may cause interference with radio communications, in which case the user shall be responsible, at its expense, to take whatever measures may be required to correct this interference.

**onsemi** does not convey any license under its patent rights nor the rights of others.

LIMITATIONS OF LIABILITY: **onsemi** shall not be liable for any special, consequential, incidental, indirect or punitive damages, including, but not limited to the costs of requalification, delay, loss of profits or goodwill, arising out of or in connection with the board, even if **onsemi** is advised of the possibility of such damages. In no event shall **onsemi**'s aggregate liability from any obligation arising out of or in connection with the board, under any theory of liability, exceed the purchase price paid for the board, if any.

The board is provided to you subject to the license and other terms per **onsemi**'s standard terms and conditions of sale. For more information and documentation, please visit [www.onsemi.com](http://www.onsemi.com).

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative