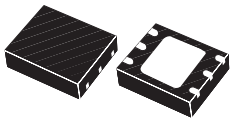
ST1S30

3 A, 1.5 MHz PWM step-down switching regulator with synchronous rectification

Datasheet - production data



DFN8 (4 x 4 mm)

Features

- 1.5 MHz fixed frequency PWM with current control mode
- 3 A output current capability
- Typical efficiency: > 90%
- 2 % DC output voltage tolerance
- Two versions available: power good or inhibit
- Integrated output over-voltage protection
- Non switching quiescent current: (typ.) 1.5 mA over temperature range
- R_{DSon} (typ.) 100 mΩ
- Utilizes tiny capacitors and inductors
- Operating junction temp. -25 °C to 125 °C
- Available in DFN8 (4 x 4 mm) exposed pad

Description

The ST1S30 is a step-down DC-DC converter optimized for powering low output voltage applications. It supplies a current in excess of 3 A over an input voltage range from 2.7 V to 6 V.

A high PWM switching frequency (1.5 MHz) allows the use of tiny surface-mount components.

Moreover, since the required synchronous rectifier is integrated, the number of the external components is reduced to minimum: a resistor divider, an inductor and two capacitors. The Power Good function continuously monitors the output voltage. An open drain Power Good flag is released when the output voltage is within regulation. In addition, a low output ripple is guaranteed by the current mode PWM topology and by the use of low ESR SMD ceramic capacitors. The device is thermally protected and the output current limited to prevent damages due to accidental short circuit. The ST1S30 is available in the DFN8 (4 x 4 mm) package.

Table 1. Device summary

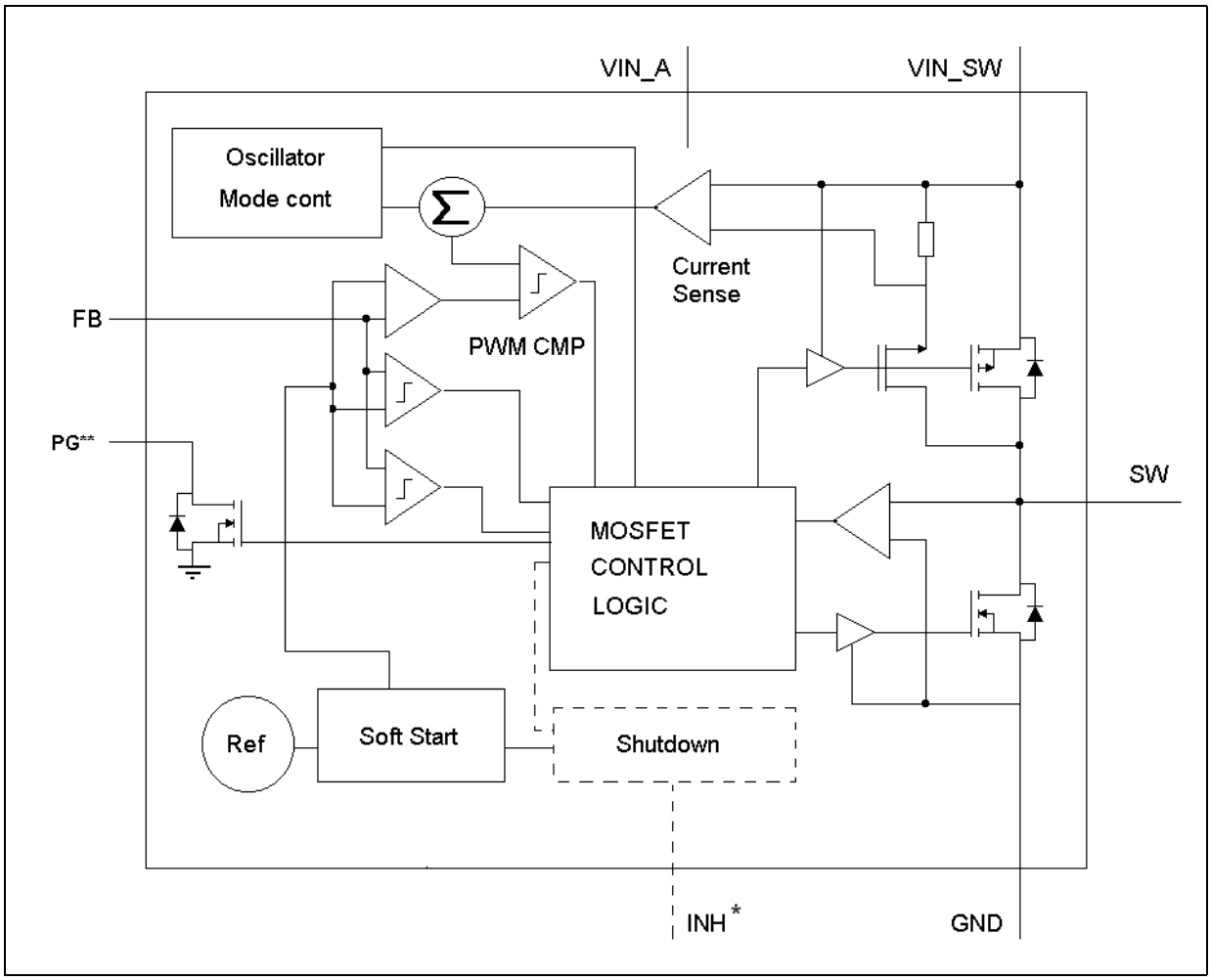
Order codes	Package	Note
ST1S30PUR (1)	DFN8 (4 x 4 mm)	PG version
ST1S30IPUR		INHIBIT version

1. Available on request.

Contents

1 Diagram

Figure 1. Schematic diagram



(*) Only for ST1S30I

(**) Only for ST1S30

2 Pin configuration

Figure 2. Pin connections (bottom view)

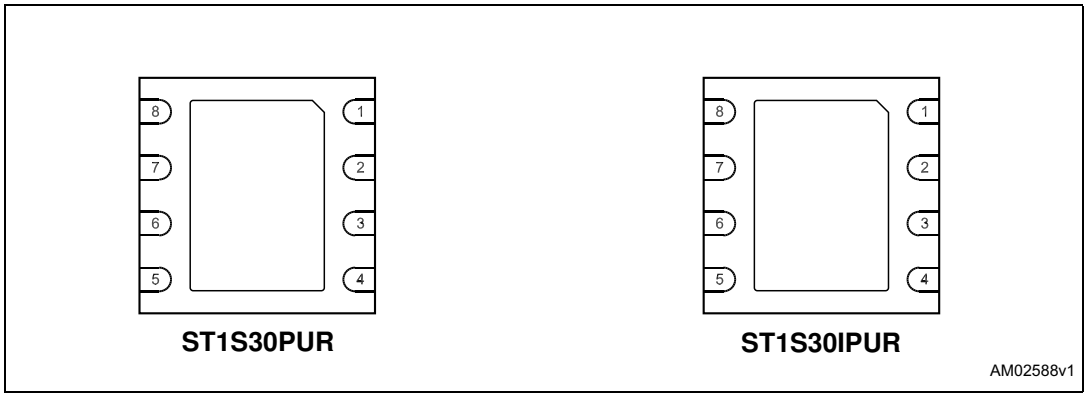


Table 2. Pin description

Pin n°	Symbol	Name and function
1	FB	Feedback voltage
2	GND	System ground
3	SW	Switching pin
6	V_{IN_SW}	Power supply for the MOSFET switch
7	V_{IN_A}	Power supply for analog circuit
8	INH/PG	Inhibit (INH) for ST1S30IPUR or Power Good (PG) for ST1S30PUR
Exposed pad	GND	To be connected to PCB ground plane for optimal electrical and thermal performance
4, 5	NC	Not internally connected. Can be connected to GND or left floating

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_SW}	Positive power supply voltage	-0.3 to 7	V
V_{IN_A}	Positive power supply voltage	-0.3 to 7	V
V_{INH}	Inhibit voltage (I version)	-0.3 to V_I + 0.3	V
SWITCH voltage	Max. voltage of output pin	-0.3 to 7	V
V_{FB}	Feedback voltage	-0.3 to 3	V
PG	Power Good open drain	-0.3 to 7	V
T_J	Max junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec	260	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	10	°C/W
R_{thJA}	Thermal resistance junction-ambient	40	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
ESD	ESD protection voltage	MM	500	V

4 Electrical characteristics

Refer to *Figure 3* application circuit $V_{IN\_SW} = V_{IN\_A} = 5$ V, $V_O = 1.2$ V, C1 = 10 µF, $C_2 = 22$ µF, L1 = 2.2 µH, $T_J = -25$ to 125 °C (unless otherwise specified. Typical values are referred to 25 °C)

Table 6. Electrical characteristics for ST1S30

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FB	Feedback voltage		784	800	816	mV
I_{FB}	V_{FB} pin bias current				600	nA
V_I	Input voltage	I_O = 10 mA to 3 A	2.7		5.5	V
UV_{LO}	Under voltage lock out threshold	V_I Rising		2.3		V
		Hysteresis		150		mV
OVP	Overvoltage protection threshold	V_O rising	1.05 V_O	1.1 V_O		V
	Overvoltage protection hysteresis	V_O falling		5		%
I_{OVP}	Overvoltage clamping current	V_O = 1.2 V		300		mA
I_Q	Quiescent current	V_{INH} > 1.2 V, not switching		1.5	2.5	mA
		V_{INH} < 0.0 V, T = - 30 °C to 85 °C			1	
I_O	Output current	V_I = 2.7 to 5.5 V (1)	3			A
$\%V_O/\Delta V_I$	Output line regulation	V_I = 2.7 V to 5.5 V, I_O = 100 mA (1)		0.16		$\%V_O/\Delta V_I$
$\%V_O/\Delta I_O$	Output load regulation	I_O = 10 mA to 3 A (1)		0.2		%
$PWMf_S$	PWM switching frequency	V_{FB} = 0.65 V	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle		80	87		%
PG	Power good output threshold			0.92 V_O		V
	Power good output voltage low	I_{SINK} = 6 mA open drain output			0.4	V
R_{DSON}-N	NMOS switch on resistance	I_{SW} = 750 mA		0.1		W
R_{DSON}-P	PMOS switch on resistance	I_{SW} = 750 mA		0.1		W
I_{SWL}	Switching current limitation	(1)	3.7	4.4	5.1	A
n	Efficiency (1)	I_O = 10 mA to 100 mA, V_O = 3.3 V	65			%
		I_O = 100 mA to 3 A, V_O = 3.3 V		85		
T_{SHDN}	Thermal shutdown			150		°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
$\%V_O/\Delta I_O$	Load transient response	I_O = 100 mA to 1 A, T_A = 25 °C $t_R = t_F \geq 200$ ns (1)	-10		+10	$\%V_O$
$\%V_O/\Delta I_O$	Short circuit removal response	I_O = 10 mA to I_O = short, T_A = 25 °C (1)	-10		+10	$\%V_O$

1. Guaranteed by design, but not tested in production.

Refer to *Figure 4* application circuit $V_{IN\_SW} = V_{IN\_A} = V_{INH} = 5$ V, $V_O = 1.2$ V, C1 = 10 µF, C_2 = 22 µF, C3 = 1 µF, L1 = 2.2 µH, T_J = -25 to 125 °C (unless otherwise specified. Typical values are referred to 25 °C)

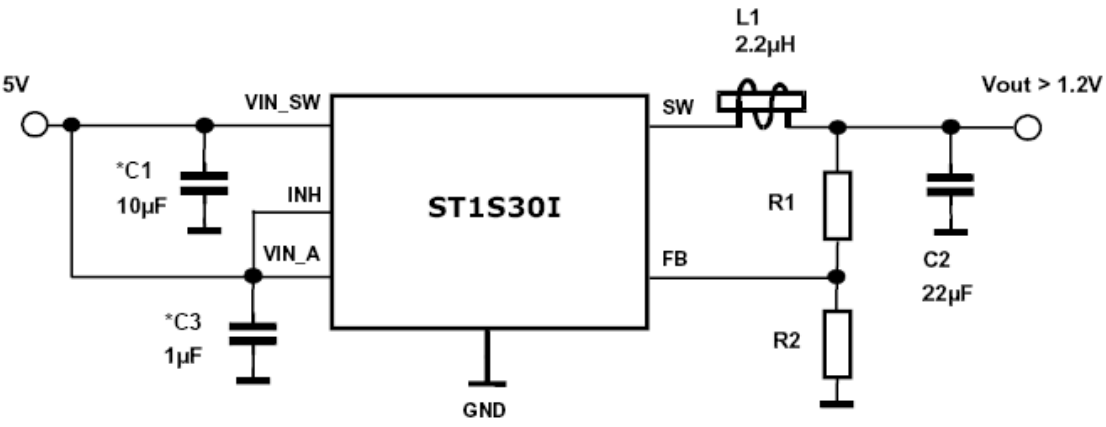
Table 7. Electrical characteristics for ST1S30I

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FB	Feedback voltage		784	800	816	mV
I_{FB}	V_{FB} pin bias current				600	nA
V_I	Minimum input voltage	I_O = 10 mA to 2 A	2.7			V
OVP	Overvoltage protection threshold	V_O rising	1.05 V_O	1.1 V_O		V
	Overvoltage protection hysteresis	V_O falling		5		%
I_Q	Quiescent current	V_{INH} > 1.2 V, not switching		1.5	2.5	mA
		V_{INH} < 0.0 V, T = - 30 °C to 85 °C			1	µA
I_O	Output current	V_I = 2.7 to 5.5 V (1)	3			A
V_{INH}	Inhibit threshold	Device ON, V_I = 2.7 to 5.5 V	1.3			V
		Device ON, V_I = 2.7 to 5 V	1.2			
		Device OFF			0.4	
I_{INH}	Inhibit pin current				2	µA
$\%V_O/\Delta V_I$	Output line regulation	V_I = 2.7 V to 5.5 V, I_O = 100 mA (1)		0.16		$\%V_O/\Delta V_I$
$\%V_O/\Delta I_O$	Output load regulation	I_O = 10 mA to 2 A (1)		0.2	0.6	$\%V_O/\Delta I_O$
$PWMf_S$	PWM switching frequency	V_{FB} = 0.65 V	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle		80	87		%
R_{DSON}-N	NMOS switch on resistance	I_{SW} = 750 mA		0.1		W
R_{DSON}-P	PMOS switch on resistance	I_{SW} = 750 mA		0.1		W
I_{SWL}	Switching current limitation	(1)	3.7	4.4	5.1	A
n	Efficiency (1)	I_O = 10 mA to 100 mA, V_O = 3.3 V	65			%
		I_O = 100 mA to 3 A, V_O = 3.3 V		85		
T_{SHDN}	Thermal shutdown			150		°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
$\%V_O/\Delta I_O$	Load transient response	I_O = 100 mA to 1 A, T_A = 25 °C $t_R = t_F \geq 200$ ns (1)	-10		+10	$\%V_O$
$\%V_O/\Delta I_O$	Short circuit removal response	I_O = 10 mA to I_O = short, T_A = 25 °C (1)	-10		+10	$\%V_O$

1. Guaranteed by design, but not tested in production.

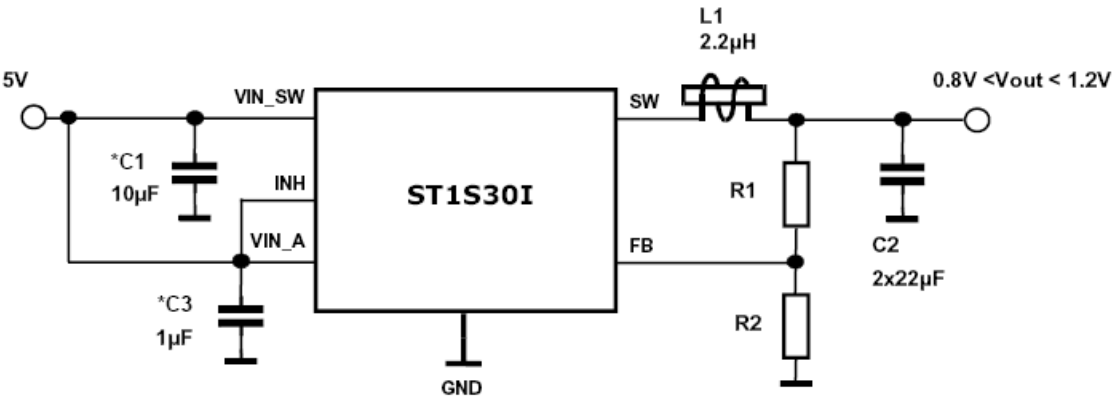
5 Typical application circuits

Figure 3. Application circuit fot V_{OUT} > 1.2 V



(*) C1 and C2 capacitors must be placed as close as possible respectively to VIN SW and VIN A pins

Figure 4. Application circuit for 0.8 V < V_{OUT} < 1.2 V



(*) C1 and C2 capacitors must be placed as close as possible respectively to VIN SW and VIN A pins

Note: These typical application circuits are provided to help designing the external components. However, we recommend to thoroughly validate any circuit solution in the real application environment conditions.

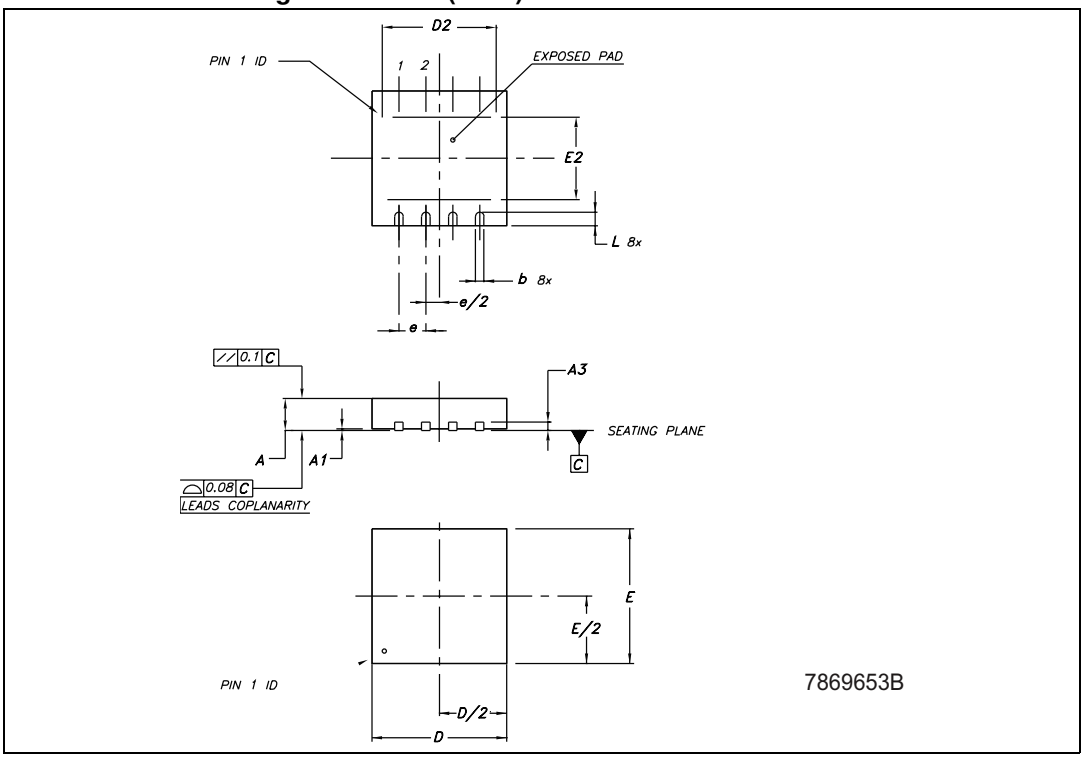
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 8. DFN8 (4 x 4) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.23	0.30	0.38
D	3.90	4.00	4.10
D2	2.82	3.00	3.23
E	3.90	4.00	4.10
E2	2.05	2.20	2.30
e		0.80	
L	0.40	0.50	0.60

Figure 5. DFN8 (4 x 4) mechanical dimensions



7 Revision history

Table 9. Document revision history

Date	Revision	Changes
09-Sep-2010	1	First release
04-May-2022	2	Updated title in *Figure 2*