

# ***TPS54672/872/972 Evaluation Module***

## *User's Guide*

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265

## EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

**EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.**

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265

## **EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM within the input and output voltage range specified in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265

# Read This First

---

---

---

### ***About This Manual***

This user's guide describes the characteristics, operation, and the use of the TPS54672EVM-222, TPS54872EVM-222, and TPS54972EVM-222 evaluation modules. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

### ***How to Use This Manual***

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

### ***Information About Cautions and Warnings***

This book may contain cautions and warnings.

**This is an example of a caution statement.**

**A caution statement describes a situation that could potentially damage your software or equipment.**

**This is an example of a warning statement.**

**A warning statement describes a situation that could potentially cause harm to you.**

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

### ***Related Documentation From Texas Instruments***

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477 – 8924 or the Product Information Center (PIC) at (972) 644 – 5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through our website at [www.ti.com](http://www.ti.com).

<b>Data Sheets:</b>	<b>Literature Number:</b>
TPS54672	SLVS397
TPS54872	SLVS436
TPS54972	SLVS437

### ***FCC Warning***

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

### ***Trademarks***

TI Logo is a trademark of Texas Instruments Incorporated. PowerPAD is a trademark of Texas Instruments Incorporated.

# Contents

---

---

---

<b>1</b>	<b>Introduction</b> .....	<b>1-1</b>
1.1	Background .....	1-2
1.2	Performance Specification Summary .....	1-3
1.3	Modifications .....	1-4
<b>2</b>	<b>Test Setup and Results</b> .....	<b>2-1</b>
2.1	Input/Output Connections .....	2-2
2.2	Efficiency .....	2-3
2.3	Power Dissipation .....	2-4
2.4	Output Voltage Regulation .....	2-5
2.5	Load Transients .....	2-6
2.6	Source-Sink Transient Response .....	2-8
2.7	Loop Characteristics .....	2-10
2.8	Output Voltage Ripple .....	2-13
2.9	Input Voltage Ripple .....	2-15
2.10	Start-Up .....	2-17
<b>3</b>	<b>Board Layout</b> .....	<b>3-1</b>
3.1	Layout .....	3-2
<b>4</b>	<b>Schematic and Bill of Materials</b> .....	<b>4-1</b>
4.1	Schematic .....	4-2
4.2	Bill of Materials .....	4-3

# Figures

---

---

---

1-1	Frequency Trimming Resistor Selection Graph	1-5
2-1	Connection Diagram	2-2
2-2	Measured Efficiency	2-3
2-3	Power Dissipation	2-4
2-4	Load Regulation	2-5
2-5	Line Regulation	2-5
2-6	Load Transient Response, TPS54672	2-6
2-7	Load Transient Response, TPS54872	2-6
2-8	Load Transient Response, TPS54972	2-7
2-9	Source-Sink Current Transient Response, TPS54672	2-8
2-10	Source-Sink Current Transient Response, TPS54872	2-8
2-11	Source-Sink Current Transient Response, TPS54972	2-9
2-12	Measured Loop Response, TPS54672, $V_I = 3\text{ V}$	2-10
2-13	Measured Loop Response, TPS54672, $V_I = 6\text{ V}$	2-10
2-14	Measured Loop Response, TPS54872, $V_I = 4\text{ V}$	2-11
2-15	Measured Loop Response, TPS54872, $V_I = 6\text{ V}$	2-11
2-16	Measured Loop Response, TPS54972, $V_I = 3\text{ V}$	2-12
2-17	Measured Loop Response, TPS54972, $V_I = 4\text{ V}$	2-12
2-18	Measured Output Voltage Ripple, TPS54672	2-13
2-19	Measured Output Voltage Ripple, TPS54872	2-13
2-20	Measured Output Voltage Ripple, TPS54972	2-14
2-21	Input Voltage Ripple, TPS54672	2-15
2-22	Input Voltage Ripple, TPS54872	2-15
2-23	Input Voltage Ripple, TPS54972	2-16
2-24	Measured Start-Up Waveform, TPS54672	2-17
2-25	Measured Start-Up Waveform, TPS54872	2-17
2-26	Measured Start-Up Waveform, TPS54972	2-18
3-1	Top-Side Layout	3-2
3-2	Internal Layer 1 Layout	3-3
3-3	Internal Layer 2 Layout	3-3
3-4	Bottom Side Layout (Looking From Top Side)	3-4
3-5	Top Side Assembly	3-4
3-6	Bottom Side Assembly (Showing Optional Components)	3-5
4-1	TPS54x72EVM-222 Schematic	4-2



# Tables

---

---

---

1-1	Input Voltage and Output Current Summary .....	1-2
1-2	TPS54672EVM-222 Performance Specification Summary .....	1-3
1-3	TPS54872EVM-222 Performance Specification Summary .....	1-3
1-4	TPS54972EVM-222 Performance Specification Summary .....	1-4
4-1	TPS54x72EVM-222 Bill of Materials .....	4-3

# Introduction

---

---

---

---

This chapter contains background information for the TPS54672, TPS54872, and TPS54972 as well as support documentation for the TPS54672EVM-222, TPS54872EVM-222, and TPS54972EVM-222 evaluation modules (SLVP222). The TPS54x72EVM-222 performance specifications are given, as well as the schematic and bill of material for the TPS54x72EVM-222.

<b>Topic</b>	<b>Page</b>
1.1 Background .....	1-2
1.2 Performance Specification Summary .....	1-3
1.3 Modifications .....	1-4

## 1.1 Background

The TPS54x72EVM-222 evaluation modules use the TPS54672, TPS54872, or TPS54972 synchronous buck tracking/termination regulators to provide an output voltage of from 0.46 V to 1.75 V from a nominal 3.3 V input or 0.7 V to 1.75 V for a nominal 5-V input. Rated input voltage and output current range is given in . These evaluation modules are designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54x72 family of regulators. The swicthing frequency is set at a nominal 700 kHz, allowing the use of a small footprint 0.65  $\mu$ H output inductor. The MOSFETs of the TPS54x72 are incorporated inside the TPS54x72 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs gives the TPS54x72 high efficiency and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC, and allow for an adjustable output voltage and a customizable loop reponse.

*Table 1–1. Input Voltage and Output Current Summary*

<b>EVM</b>	<b>Input Voltage Range</b>	<b>Output Current Range</b>
TPS54672EVM-222	3.0 V to 6.0 V	–6 A to 6 A
TPS54872EVM-222	4.0 V to 6.0 V	–8 A to 8 A
TPS54972EVM-222	3.0 V to 4.0 V	–9 A to 9 A

## 1.2 Performance Specification Summary

A summary of the TPS54x72EVM–222 performance specifications is provided by Table 1–2, Table 1–3, and Table 1–4. All specifications are given for an output voltage of 1.25 V and an ambient temperature of 25°C, unless otherwise noted.

Table 1–2. TPS54672EVM-222 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		3.0	3.3 or 5.0	6.0	V
Output voltage set point		0.42	1.25	1.75	V
Output current range	$V_I = 3\text{ V to }6\text{ V}$	–6		6	A
Line regulation	$I_O = 3\text{ A}$		0.4		mV
Load regulation	$V_I = 5\text{ V}, I_O = 0\text{ A to }6\text{ A}$		8.0		mV
Load transient response	$I_O = 1.5\text{ A to }4.5\text{ A}, t_r = 40\text{ }\mu\text{s}$		–15		mV <sub>PK</sub>
			100		$\mu\text{s}$
	$I_O = 4.5\text{ A to }1.5\text{ A}, t_f = 40\text{ }\mu\text{s}$		15		mV <sub>PK</sub>
			50		$\mu\text{s}$
Loop bandwidth	$V_I = 3\text{ V}$		80		kHz
Phase margin	$V_I = 3\text{ V}$		48		°
Loop bandwidth	$V_I = 6\text{ V}$		100		kHz
Phase margin	$V_I = 6\text{ V}$		47		°
Input ripple voltage			245	275	mV <sub>PP</sub>
Output ripple voltage			7	10	mV <sub>PP</sub>
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	$V_I = 5.0\text{ V}, V_O = 1.25\text{ V}, I_O = 2.5\text{ A}$		86.2%		

Table 1–3. TPS54872EVM-222 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		4.0	5.0	6.0	V
Output voltage set point		0.56	1.25	1.75	V
Output current range	$V_I = 4\text{ V to }6\text{ V}$	–8		8	A
Line regulation	$I_O = 4\text{ A}$		0.4		mV
Load regulation	$V_I = 5\text{ V}, I_O = 0\text{ A to }8\text{ A}$		8.0		mV
Load transient response	$I_O = 2\text{ A to }6\text{ A}, t_r = 40\text{ }\mu\text{s}$		–25		mV <sub>PK</sub>
			75		$\mu\text{s}$
	$I_O = 6\text{ A to }2\text{ A}, t_f = 40\text{ }\mu\text{s}$		25		mV <sub>PK</sub>
			75		$\mu\text{s}$
Loop bandwidth	$V_I = 4\text{ V}$		80		kHz
Phase margin	$V_I = 4\text{ V}$		48		°
Loop bandwidth	$V_I = 6\text{ V}$		100		kHz
Phase margin	$V_I = 6\text{ V}$		46		°
Input ripple voltage			245	275	mV <sub>PP</sub>
Output ripple voltage			7	10	mV <sub>PP</sub>
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	$V_I = 5.0\text{ V}, V_O = 1.25\text{ V}, I_O = 2.5\text{ A}$		85.5%		

Table 1–4. TPS54972EVM-222 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		3.0	3.3	4.0	V
Output voltage set point		0.42	1.25	1.75	V
Output current range	$V_I = 3\text{ V to }4\text{ V}$	-9		9	A
Line regulation	$I_O = 4.5\text{ A}$		0.4		mV
Load regulation	$V_I = 5\text{ V}, I_O = 0\text{ A to }9\text{ A}$		8.0		mV
Load transient response	$I_O = 2.25\text{ A to }6.75\text{ A}, t_r = 40\text{ }\mu\text{s}$		-35		mV <sub>PK</sub>
			75		$\mu\text{s}$
	$I_O = 6.75\text{ A to }2.25\text{ A}, t_f = 40\text{ }\mu\text{s}$		40		mV <sub>PK</sub>
			75		$\mu\text{s}$
Loop bandwidth	$V_I = 3\text{ V}$		71		kHz
Phase margin	$V_I = 3\text{ V}$		41		°
Loop bandwidth	$V_I = 3.6\text{ V}$		80		kHz
Phase margin	$V_I = 3.6\text{ V}$		42		°
Input ripple voltage			340	400	mV <sub>PP</sub>
Output ripple voltage			7	10	mV <sub>PP</sub>
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	$V_I = 3.3\text{ V}, V_O = 1.25\text{ V}, I_O = 2.5\text{ A}$		89.7%		

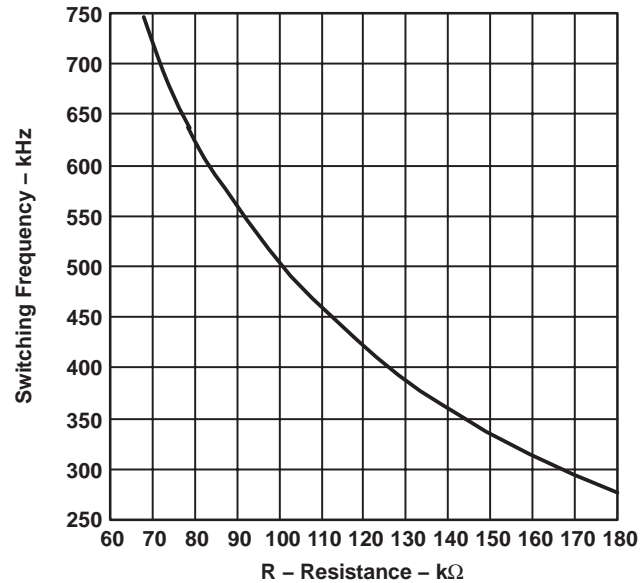
### 1.3 Modifications

The TPS54x72EVM–222 is designed to demonstrate the small size that can be attained when designing with the TPS54x72, so many of the features which allow for extensive modifications have been omitted from this EVM. Changing the  $V_{(DDQ)}$  voltage from 0.92 V to 3.5 V can change the output voltage in the range of 0.46 V to 1.75 V. Output voltages above 1.75 V can be obtained by modifying the REFIN voltage divider of R6 and R7, and scaling the output feedback voltage into the VSENSE pin using the voltage divider of R1 and R9 (normally not used). To maintain the output-tracking rate of one half the  $V_{(DDQ)}$  input, the R6/R7 divider should scale  $V_{(DDQ)}$  by a factor of four and R1/R9 divider should scale  $V_{(TTQ)}$  by a factor of two. To accomplish this, replace R6 with a 30.1 k $\Omega$  resistor and add R9 as a 10 k $\Omega$  resistor. The minimum output voltage is limited by the minimum controllable ontime of the device, 200 ns, and is dependent upon the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using :

$$V_{\text{OUTMIN}} = 200\text{ ns} \times f_s \times V_{\text{INMIN}} \quad (1)$$

The switching frequency may be trimmed to any value between 280 kHz and 700 kHz by changing the value of R5. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased. A plot of the value of RT versus the switching frequency is given in Figure 1–1.

Figure 1–1. Frequency Trimming Resistor Selection Graph



The slow start time is typically 3.6 ms, and is controlled internally. The slow start time cannot be made faster than 3.6 ms.

The TPS54x72EVM–222 EVM also supports alternate output filter configurations by means of pads located on the back side of the PCB. The positions for C15, C16, and C17 provide space for up to three electrolytic type surface mount capacitors, while the position for L2 accommodates popular inductors such as Vishay IHLP-5050 series with a 0.5 in. × 0.5 in. package. Since changes in the output filter affect the overall loop response, the user may find it desirable to change the values used in the compensation network (R1, R2, R3, C1, C2, and C3). The 0-Ω resistor R8 in the feedback path is provided as a convenient place to break the loop for testing any compensation value changes. While the provided compensation network can provide a stable output for a wide variety of output filter component values, it is always a good idea to verify any changes to the output filter or compensation network.



# Test Setup and Results

---

---

---

This chapter describes how to properly connect, set up, and use the TPS54x72EVM–222 evaluation module. The chapter also includes test results typical for the TPS54x72EVM–222 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

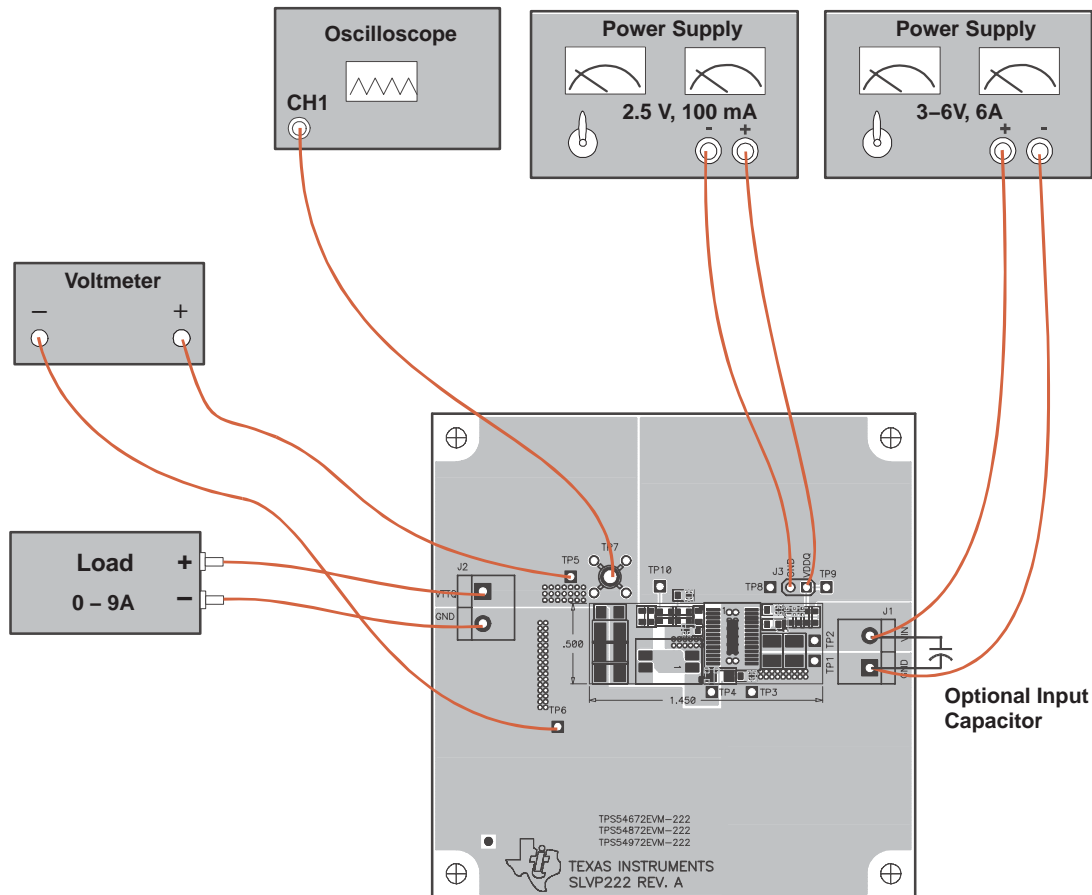
<b>Topic</b>	<b>Page</b>
<b>2.1 Input/Output Connections</b> .....	<b>2-2</b>
<b>2.2 Efficiency</b> .....	<b>2-3</b>
<b>2.3 Power Dissipation</b> .....	<b>2-4</b>
<b>2.4 Output Voltage Regulation</b> .....	<b>2-5</b>
<b>2.5 Load Transients</b> .....	<b>2-6</b>
<b>2.6 Source-Sink Transient Response</b> .....	<b>2-8</b>
<b>2.7 Loop Characteristics</b> .....	<b>2-10</b>
<b>2.8 Output Voltage Ripple</b> .....	<b>2-13</b>
<b>2.9 Input Voltage Ripple</b> .....	<b>2-15</b>
<b>2.10 Start-Up</b> .....	<b>2-17</b>



## 2.1 Input/Output Connections

The TPS54x72EVM-222 has the following four input/output connections: input, input return, output, and output return. A diagram showing the connection points is shown in Figure 2-1. A power supply capable of supplying 6 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J2 through a pair of 16 AWG wires. The maximum load current may be reduced from 9 A if 6 A or 8 A versions of the TPS54x72EVM-222 are used. Wire lengths should be minimized to reduce losses in the wires. Test point TP7 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54X72 is intended to be used as a point of load regulator. In typical applications, it is usually located close to the input voltage source. When using the TPS54x72EVM-222 with an external power supply as the source for  $V_I$ , an additional bulk capacitor may be required, depending upon the output impedance of the source and length of the hookup wires. The test results presented were obtained using a 470  $\mu\text{F}$ , 16-V additional input capacitor. Connection is shown for source current only. To sink current, increase the current capacity of the 2.5-V supply, and connect a load resistor between the positive load terminal and the positive terminal of the 2.5-V supply.

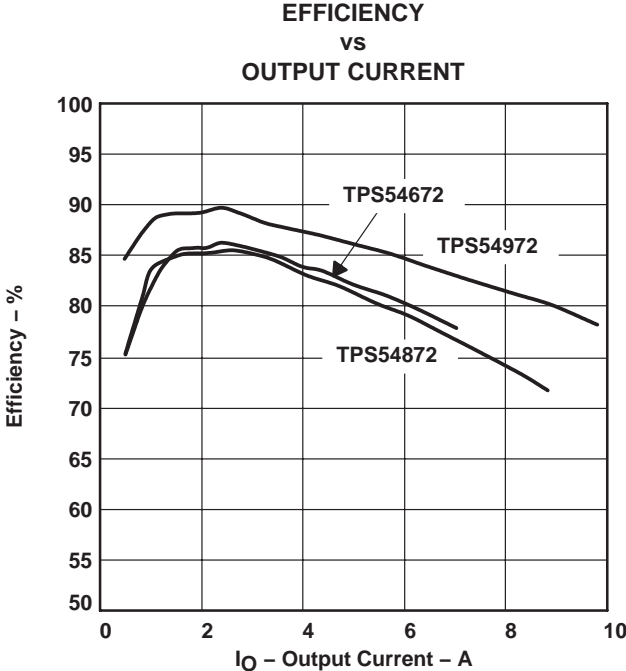
Figure 2-1. Connection Diagram



## 2.2 Efficiency

The TPS54x72EVM-222 efficiency peaks at load current of about 2 A, and then decreases as the load current increases towards full load. The efficiency shown in Figure 2-2 is for 5-V (TPS54672, TPS54872) and 3.3 V (TPS54972) inputs at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies, due to the gate and switching losses in the MOSFETs.

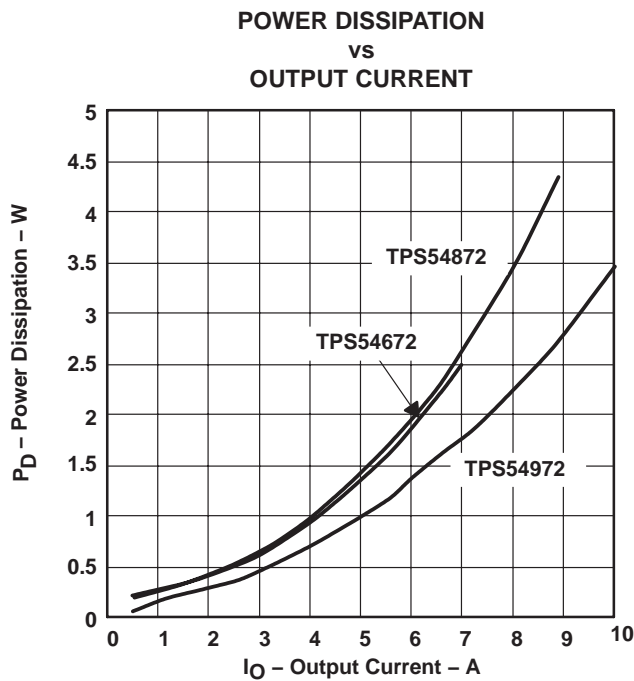
Figure 2-2. Measured Efficiency



### 2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a good board layout, allows the TPS54x72EVM–222 EVMs to output full rated load current while maintaining safe junction temperatures. With a 3.3-V input source and a 6-A load, the junction temperature is approximately 60°C, while the case temperature is approximately 55°C. The total circuit losses at 25°C are shown in Figure 2–3. The input voltage for the TPS54972 is 3.3 V and for the TPS54672 and TPS54872, 5.0 V. Note that for a given output current the TPS54972 dissipates less power due to the lower drain-to-source on resistance of the MOSFETs. For additional information on the dissipation ratings of the devices, see the individual product data sheets.

Figure 2–3. Power Dissipation



## 2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54x72EVM-222 is shown in Figure 2-4, while the output voltage line regulation is shown in Figure 2-5. Measurements are given for an ambient temperature of 25°C.

Figure 2-4. Load Regulation

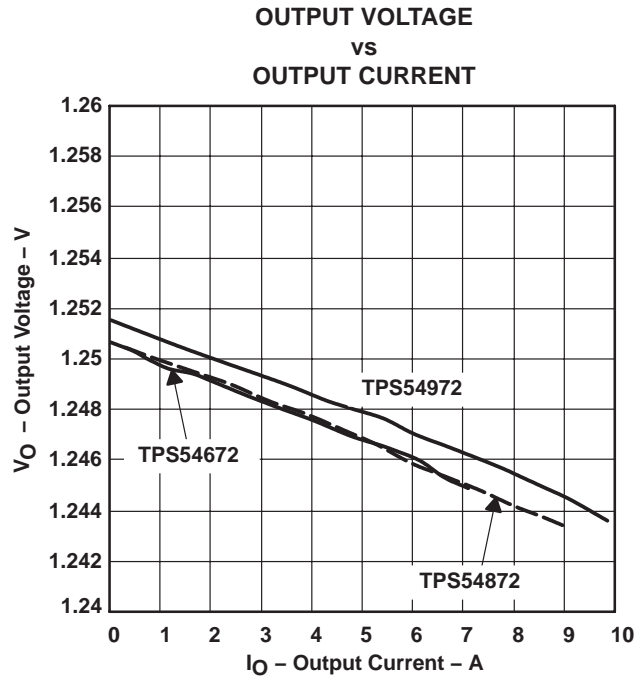
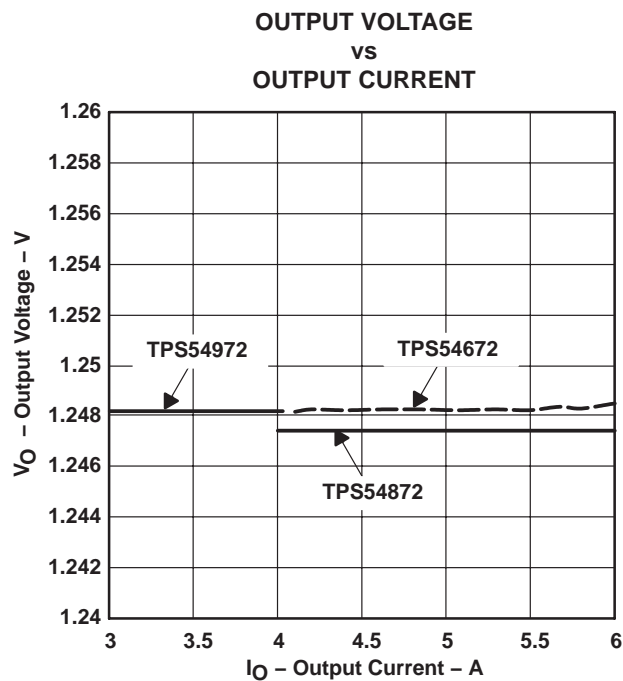


Figure 2-5. Line Regulation



## 2.5 Load Transients

The TPS54x72EVM-222 response to load transients is shown in Figure 2-6, Figure 2-7, and Figure 2-8. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2-6. Load Transient Response, TPS54672

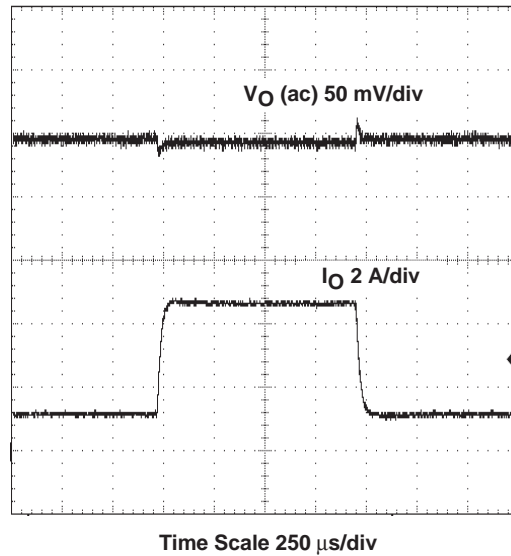


Figure 2-7. Load Transient Response, TPS54872

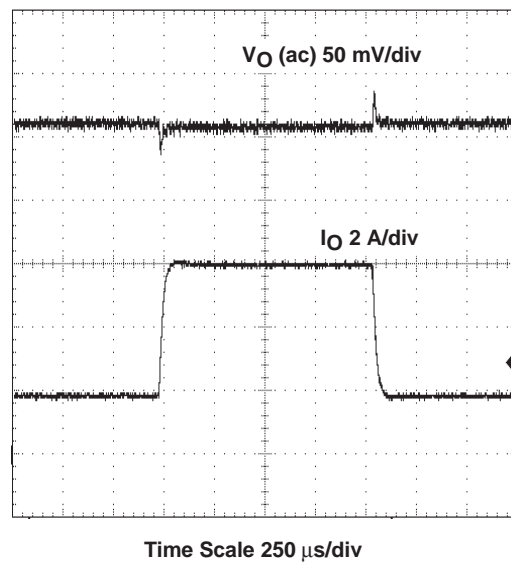
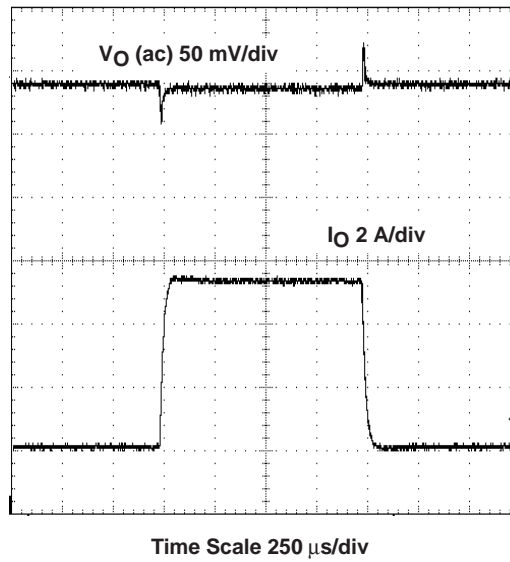


Figure 2–8. Load Transient Response, TPS54972



## 2.6 Source-Sink Transient Response

The TPS54x72EVM-222 response to source-sink current transients is shown in Figure 2-9, Figure 2-10, and Figure 2-11. The current step is from -50% to 50% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2-9. Source-Sink Current Transient Response, TPS54672

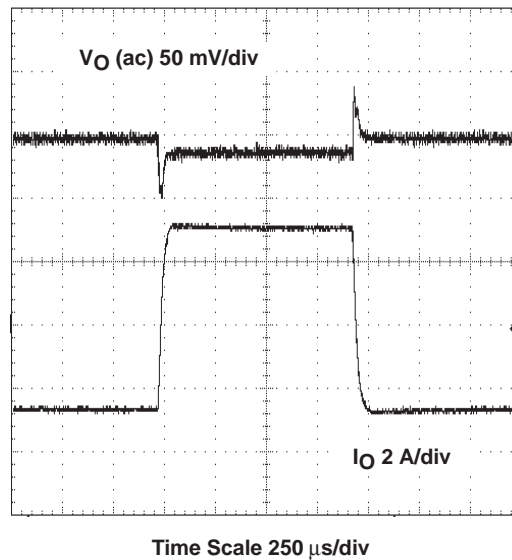


Figure 2-10. Source-Sink Current Transient Response, TPS54872

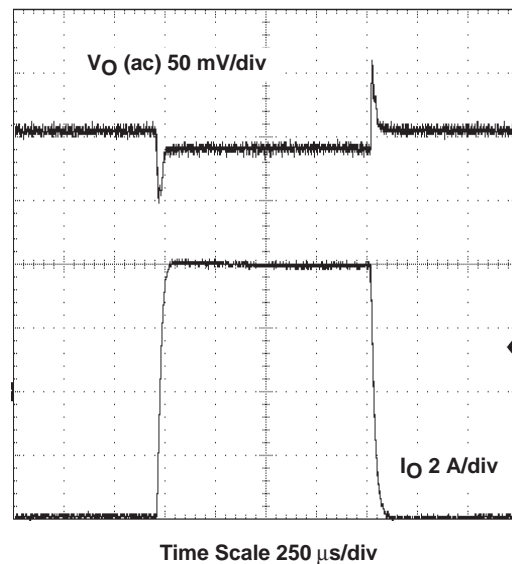
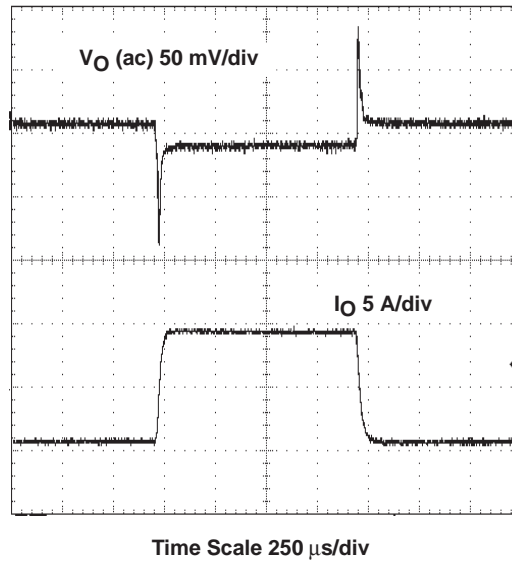


Figure 2–11. Source-Sink Current Transient Response, TPS54972





## 2.7 Loop Characteristics

The TPS54x72EVM-222 loop response characteristics are shown in Figure 2-12 through Figure 2-17. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

Figure 2-12. Measured Loop Response, TPS54672,  $V_I = 3\text{ V}$

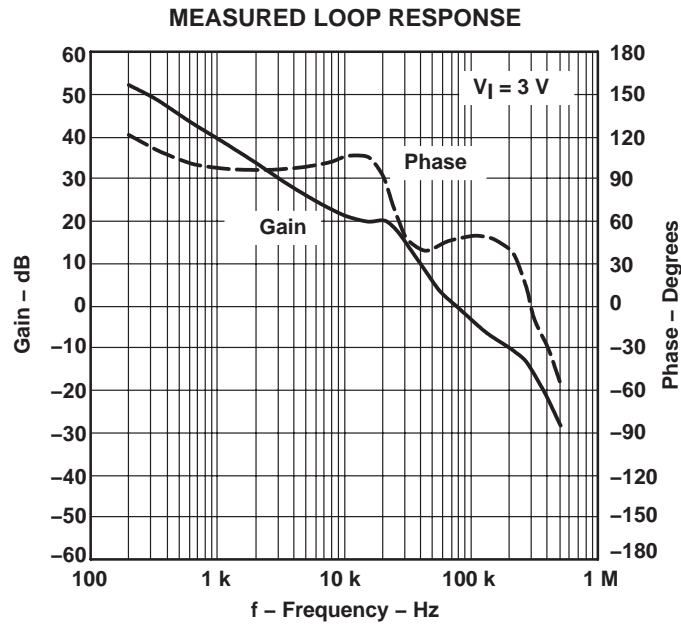


Figure 2-13. Measured Loop Response, TPS54672,  $V_I = 6\text{ V}$

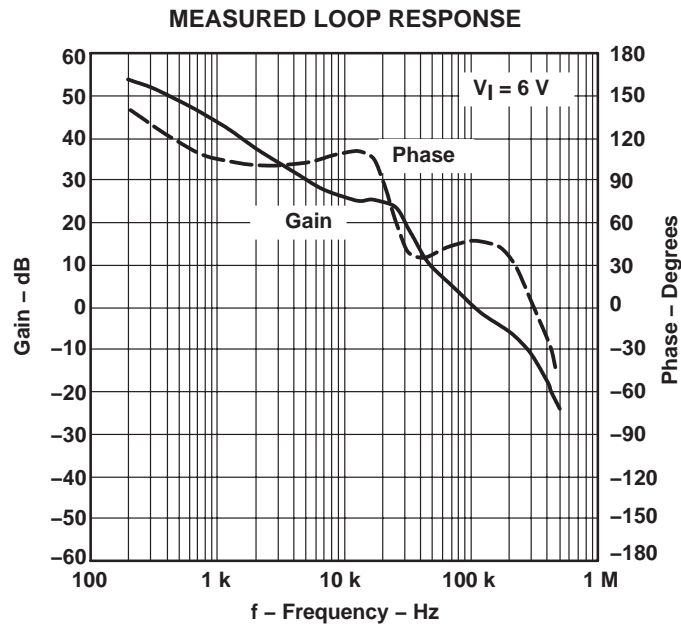


Figure 2-14. Measured Loop Response, TPS54872,  $V_I = 4\text{ V}$

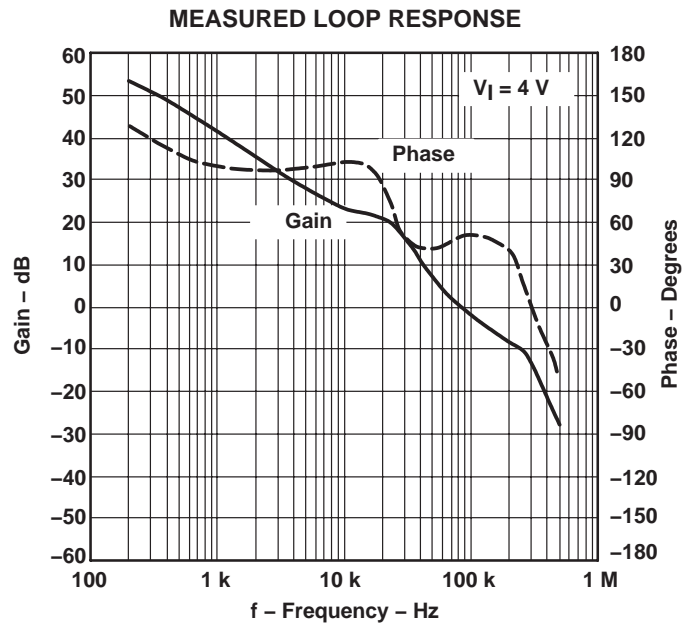


Figure 2-15. Measured Loop Response, TPS54872,  $V_I = 6\text{ V}$

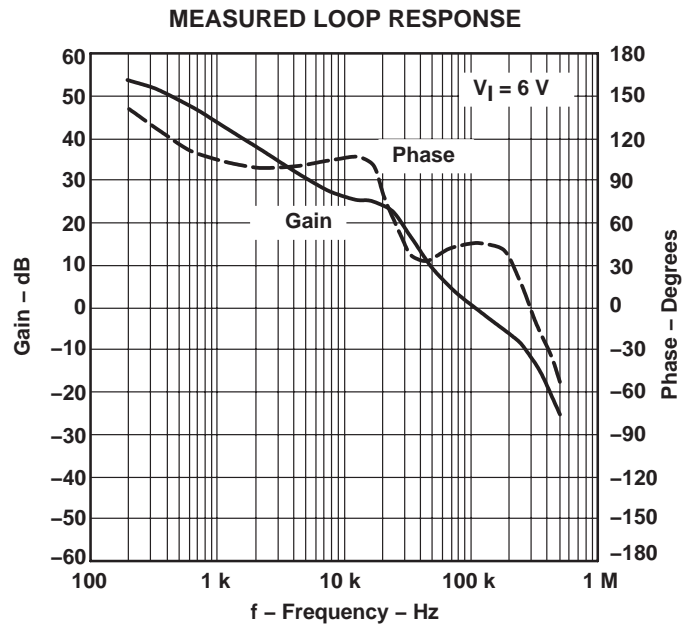


Figure 2-16. Measured Loop Response, TPS54972,  $V_I = 3\text{ V}$

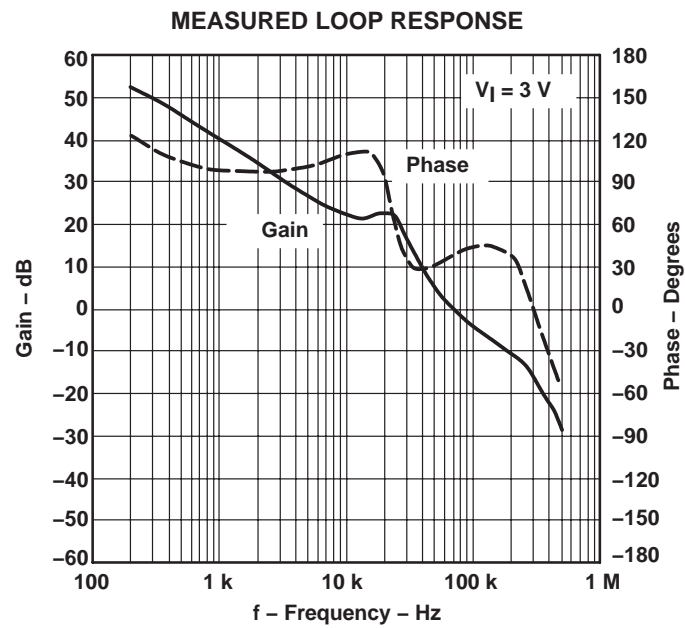
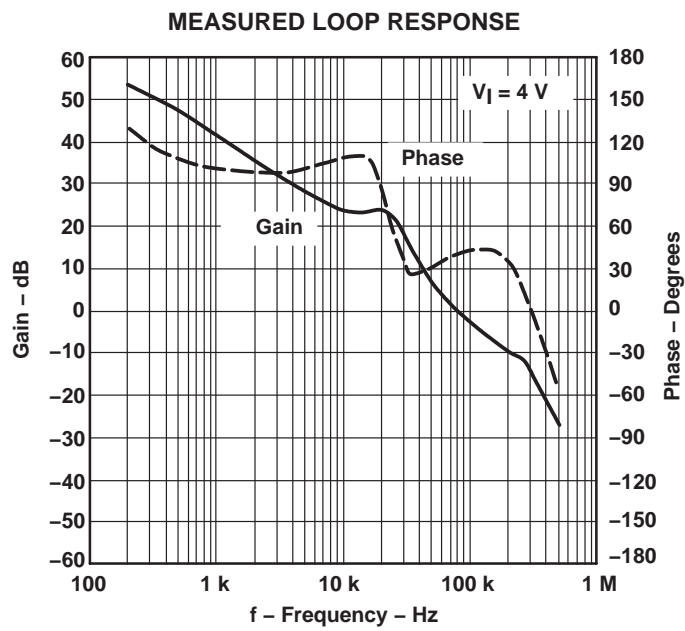


Figure 2-17. Measured Loop Response, TPS54972,  $V_I = 4\text{ V}$



## 2.8 Output Voltage Ripple

The TPS54x72EVM-222 output voltage ripple is shown in Figure 2-18, Figure 2-19, and Figure 2-20 for each device type. The input voltage is 3.3 V for the TPS54672 and TPS54972. The input voltage is 5 V for the TPS54872. Output current for each device is the rated full load. Voltage is measured directly across output capacitors.

Figure 2-18. Measured Output Voltage Ripple, TPS54672

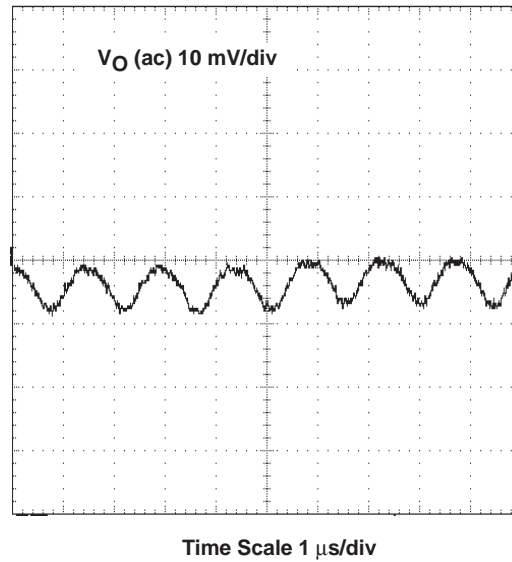


Figure 2-19. Measured Output Voltage Ripple, TPS54872

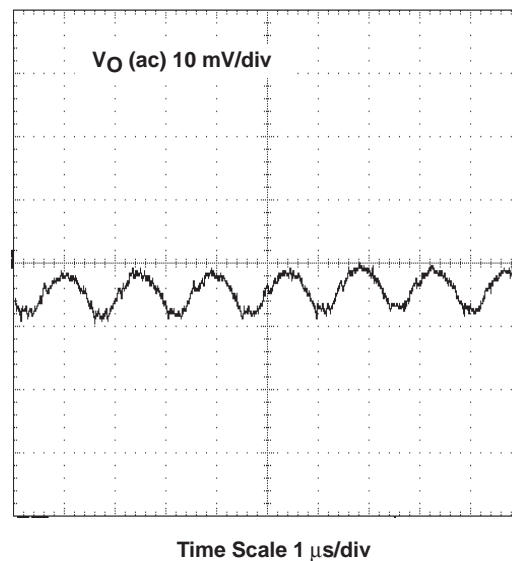
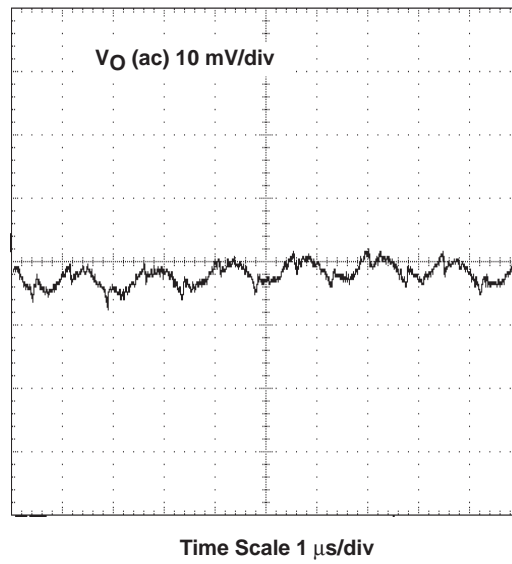


Figure 2–20. Measured Output Voltage Ripple, TPS54972



## 2.9 Input Voltage Ripple

The TPS54x72EVM-222 output voltage ripple is shown in Figure 2-21, Figure 2-22, and Figure 2-23 for each device type. The input voltage is 3.3 V for the TPS54672 and TPS54972. The input voltage is 5 V for the TPS54872. Output current for each device is rated full load.

Figure 2-21. Input Voltage Ripple, TPS54672

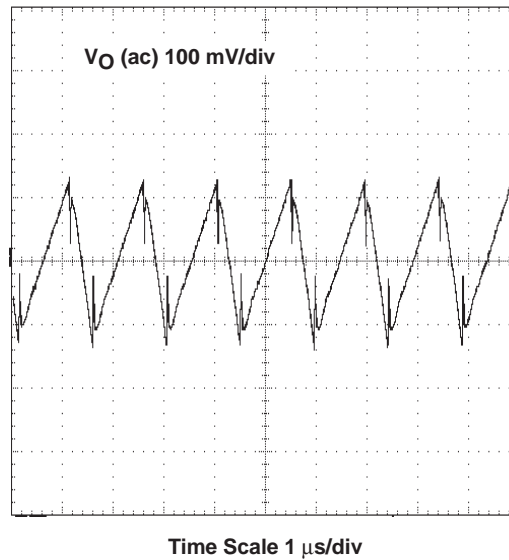


Figure 2-22. Input Voltage Ripple, TPS54872

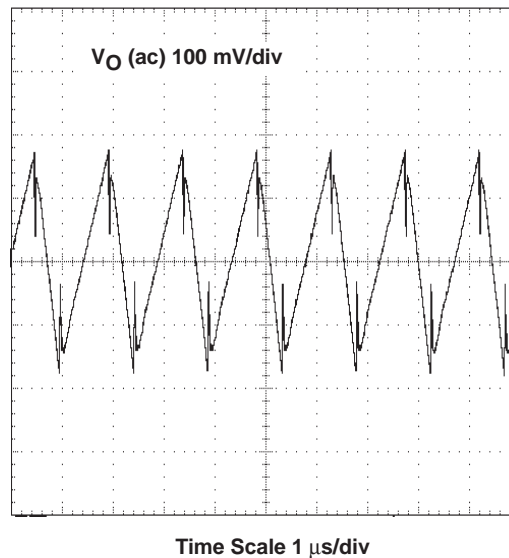
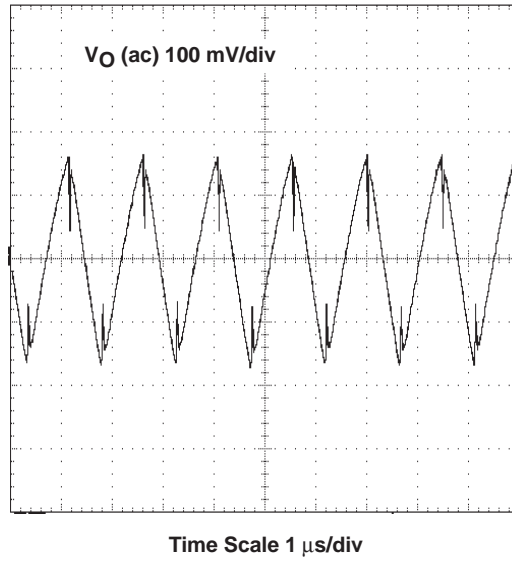


Figure 2-23. Input Voltage Ripple, TPS54972



## 2.10 Start-Up

The start-up voltage waveform of the TPS54x72EVM-222 is shown in Figure 2-24, Figure 2-25, and Figure 2-26. There is approximately a 3.6-ms delay after the input voltage rises above the 2.9 V (3.8 V for the TPS54872) startup voltage threshold until the output voltage begins to ramp up to the final value of 1.25 V. The output voltage tracks the greater of the internal and external slow start voltages, accounting for the change in ramp rates.

Figure 2-24. Measured Start-Up Waveform, TPS54672

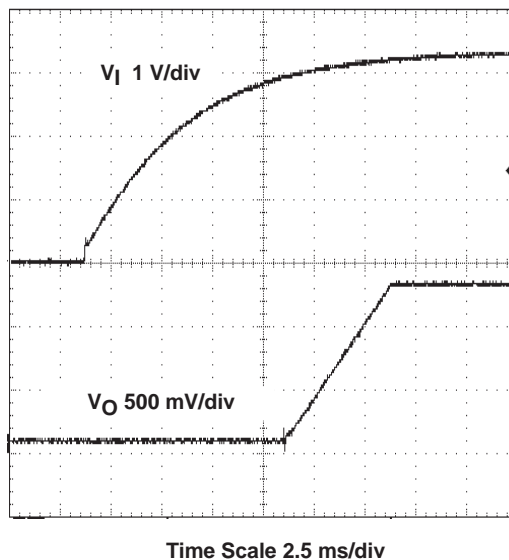


Figure 2-25. Measured Start-Up Waveform, TPS54872

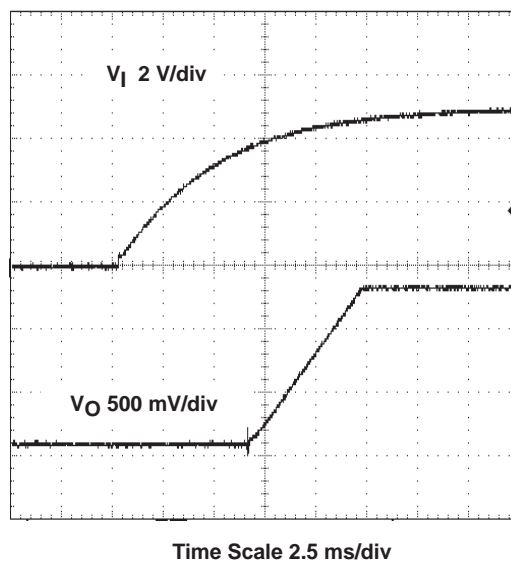
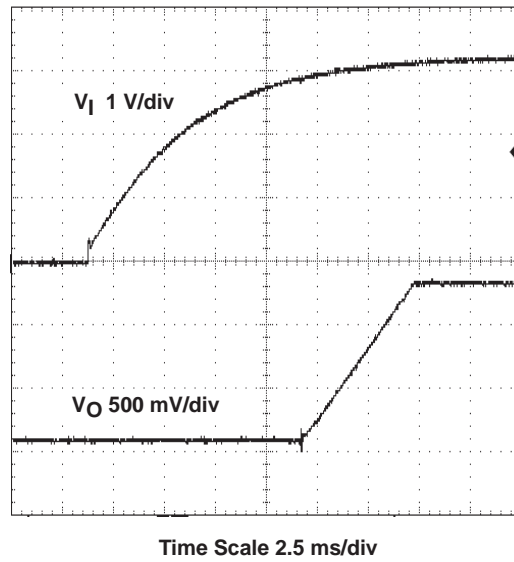




Figure 2-26. Measured Start-Up Waveform, TPS54972



# Board Layout

---

---

---

---

This chapter provides a description of the TPS54x72EVM–222 board layout and layer illustrations.

<b>Topic</b>	<b>Page</b>
3.1 Layout .....	3-2

### 3.1 Layout

The board layout for the TPS54x72EVM–222 is shown in Figure 3–1 through Figure 3–6. The top side layer of the TPS54x72EVM–222 is laid out in a manner typical of a user application. The bottom layer of the TPS54x72EVM–222 is designed to accommodate an optional alternate output filter configuration. The top and bottom layers are 1.5 oz. copper, while the two internal layers are 0.5 oz. copper.

The top layer contains the main power traces for  $V_I$ ,  $V_O$ , and  $V_{(phase)}$ . Also on the top layer are connections for the remaining pins of the TPS54x72 and a large area filled with ground. The two internal layers are identical and are dedicated ground planes. The bottom layer contains pads for an optional alternate output filter including space for three D3 or D4 case size electrolytic capacitors and an alternate inductor of 0.5 in. x 0.5 in. size ground traces. The top and bottom ground traces are connected to the internal ground planes with 45 vias placed around the board including 12 directly under the TPS54x72 device to provide a thermal path from the PowerPAD™ land to ground.

The input-decoupling capacitors (C4 and C8), bias-decoupling capacitor (C9), and boot-strap capacitor (C6) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

Figure 3–1. Top-Side Layout

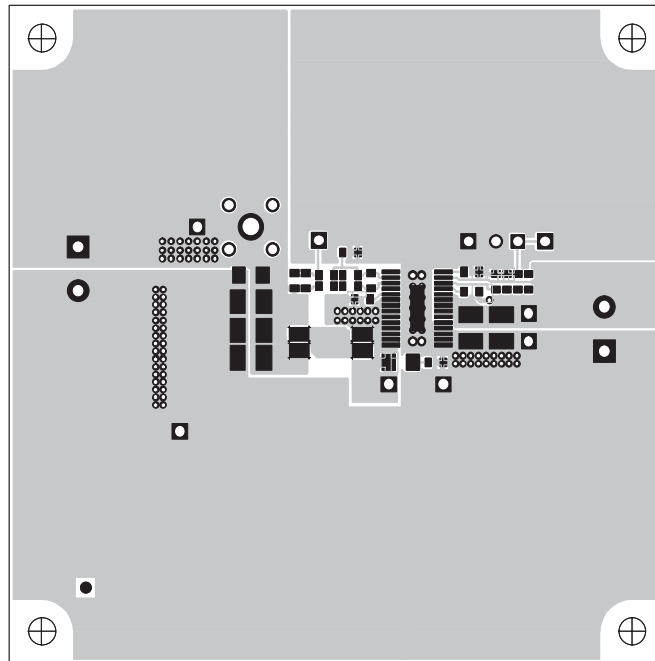


Figure 3–2. Internal Layer 1 Layout

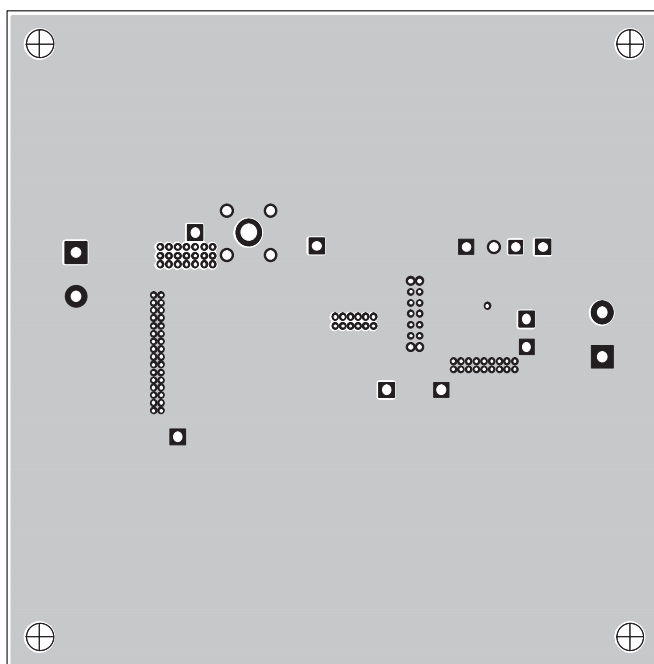


Figure 3–3. Internal Layer 2 Layout

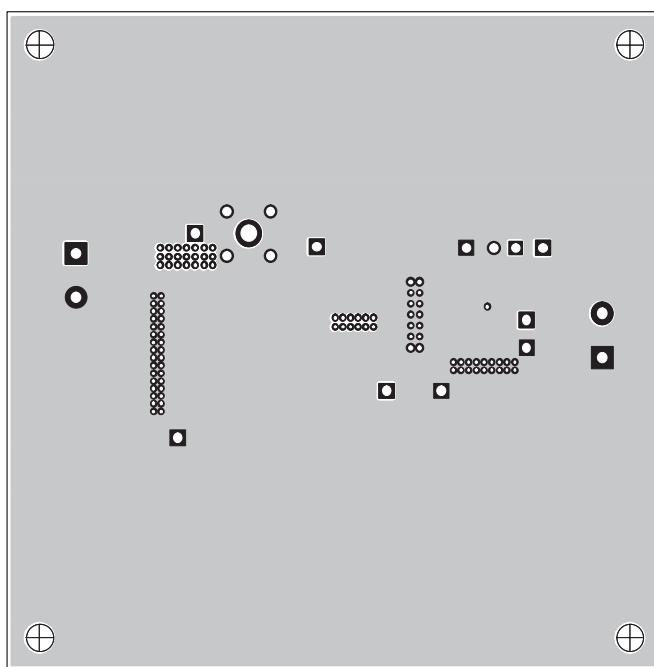


Figure 3–4. Bottom Side Layout (Looking From Top Side)

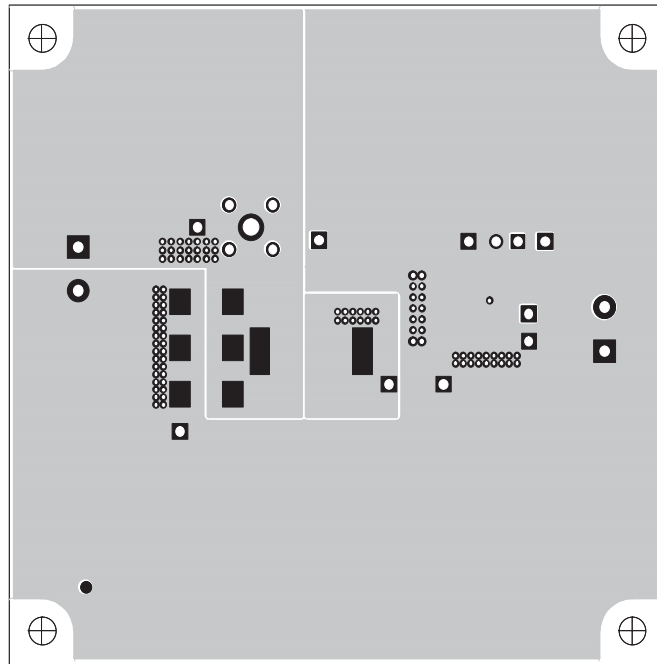


Figure 3–5. Top Side Assembly

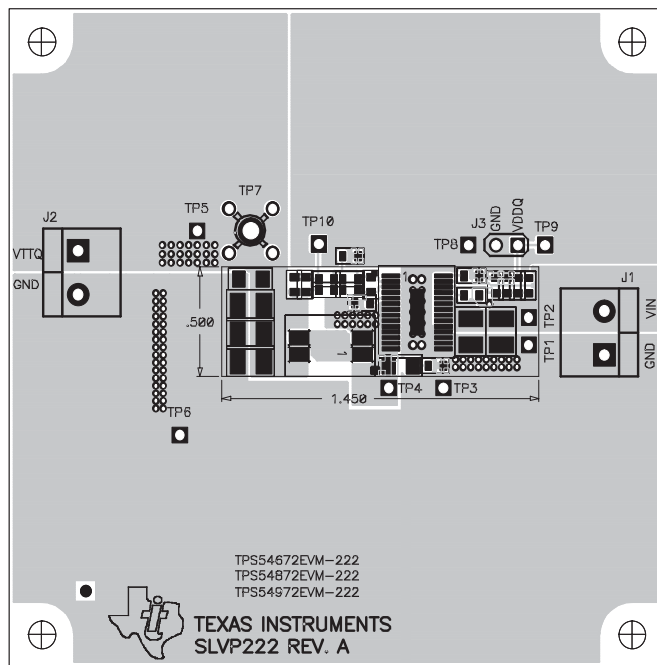
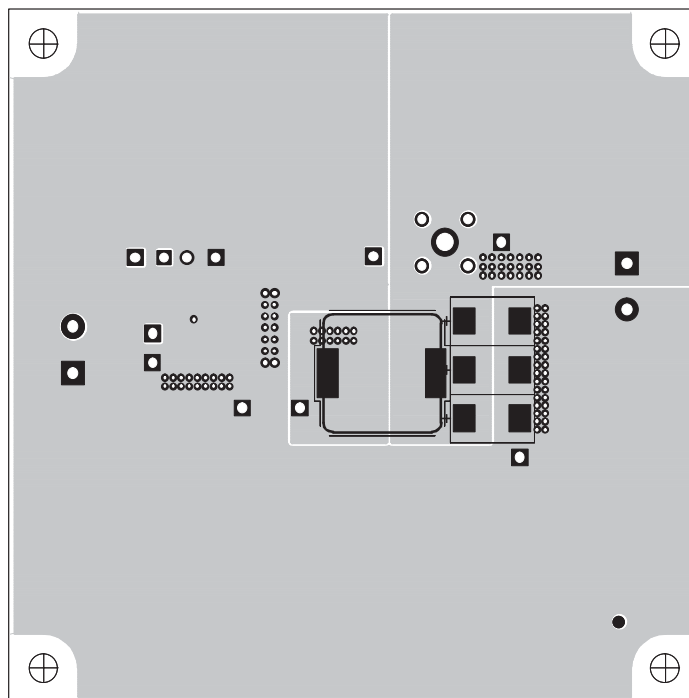


Figure 3–6. Bottom Side Assembly (Showing Optional Components)





# Schematic and Bill of Materials

---

---

---

The TPS54x72EVM–222 schematic and bill of materials are presented in this chapter.

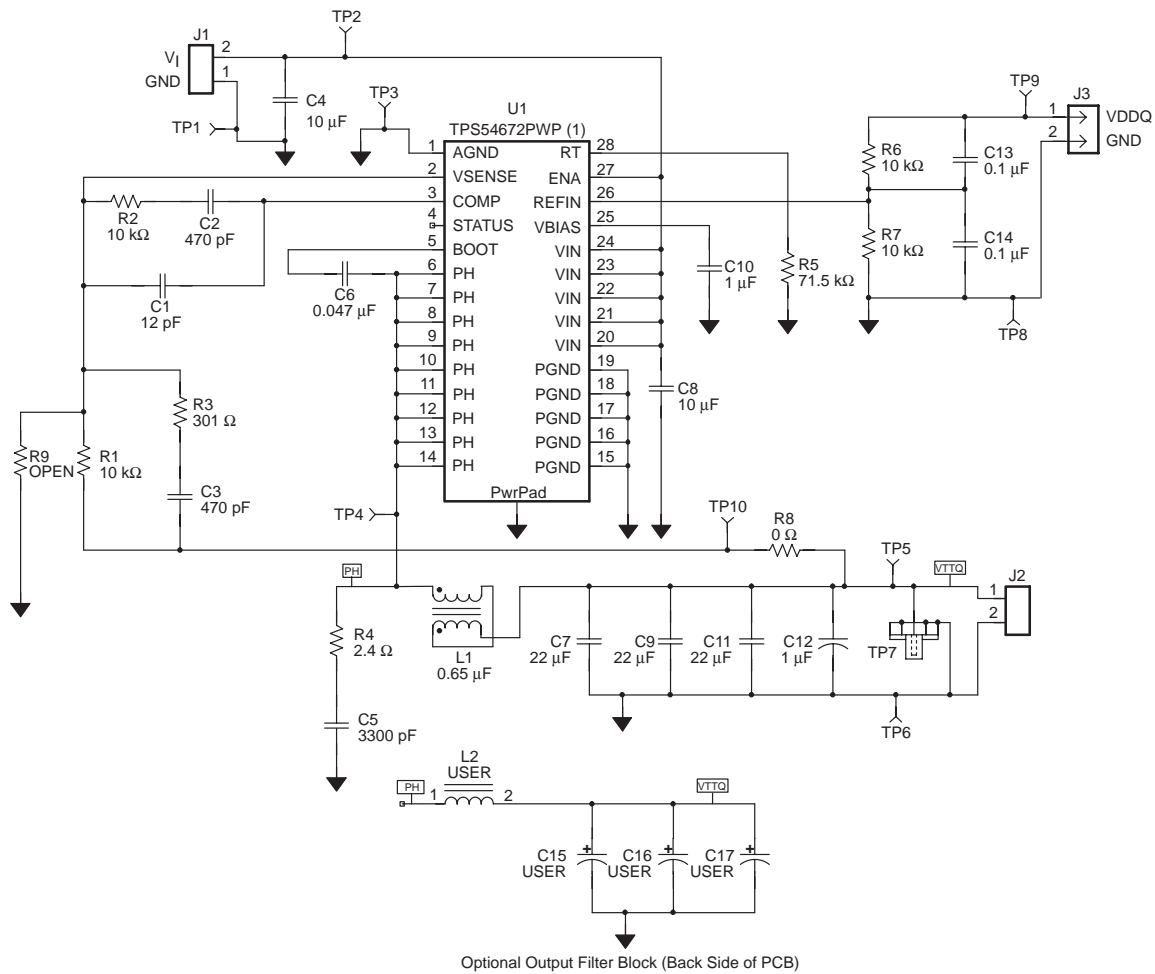
<b>Topic</b>	<b>Page</b>
4.1 Schematic .....	4-2
4.2 Bill of Materials .....	4-3



## 4.1 Schematic

The schematic for the TPS54x72EVM-222 is shown in Figure 4-1.

Figure 4-1. TPS54x72EVM-222 Schematic



(1) TPS54672 or TPS5472 or TPS54972

## 4.2 Bill of Materials

The bill of materials for the TPS54x72EVM–222 is shown in Table 4–1.

Table 4–1. TPS54x72EVM–222 Bill of Materials

Count			RefDes	Description	SIZE	MFR	Part Number
–001	–002	–003					
1	1	1	C1	Capacitor, ceramic, 12 pF, 50 V, C0G, 5%	603	Murata	GRM1885C1H120JZ01
1	1	1	C10	Capacitor, ceramic, 1.0 μF, 10 V, X5R, 20%	603	TDK	C1608X5R1A105K
1	1	1	C12	Capacitor, ceramic, 1.0 μF, 16 V, X7R, 10 %	1206	Panasonic	ECJ–3YB1C105K
2	2	2	C13, C14	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	603	Panasonic	ECJ–2VB1E104K
–	–	–	C15, C16, C17	Capacitor, polymer aluminum,	62100		
2	2	2	C2, C3	Capacitor, ceramic, 470 pF, 50 V, C0G, 5%	603	Panasonic	GRM1885C1H471JA01
2	2	2	C4, C8	Capacitor, ceramic, 10 μF, 10 V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	1	1	C5	Capacitor, ceramic, 3300 pF, 50 V, X7R, 10%	603	Panasonic	ECJ–1VB1H332K
1	1	1	C6	Capacitor, ceramic, 0.047 μF, 25 V, X7R, 10%	603	Panasonic	ECJ–2VB1E473K
3	3	3	C7, C9, C11	Capacitor, ceramic, 22 μF, 6.3 V, X5R, 20%	1210	Taiyo Yuden	JMK325BJ226MN
2	2	2	J1, J2	Terminal block, 2 pin, 15 A, 5.1 mm	0.40 × 0.35	OST	ED1609
1	1	1	J3	Header, 2 pin, 100 mil spacing, (36-pin strip)	23100	Sullins	PTC36SAAN
1	1	1	L1	Inductor, 0.65 μH, 12 A	0.340×0.250	Pulse	PA0277
–	–	–	L2	Inductor, SMT, user defined	0.51 × 0.51		
4	4	4	R1, R2, R6, R7	Resistor, chip, 10.0 kΩ, 1/16–W, 1%	603	Std	Std
1	1	1	R3	Resistor, chip, 301 Ω, 1/16 W, 1%	603	Std	Std
1	1	1	R4	Resistor, chip, 2.4 Ω, 1/8 W, 1%	1206	Std	Std
1	1	1	R5	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
1	1	1	R8	Resistor, chip, 0 Ω, 1/16 W, 1%	603	Std	Std
1	1	1	R9	Resistor, chip, OPEN Ω, 1/16 W, 1%	603	Std	Std
4	4	4	TP1, TP3, TP6, TP8	Test point, black, 1 mm	0.038", 6400"	Farnell	240–333
5	5	5	TP2, TP4, TP5, TP9, TP10	Test point, red, 1 mm	0.038", 6400"	Farnell	240–345

Bill of Materials

---

1	1	1	TP7	Adaptor, 3,5-mm probe clip ( or 131-5031-00)	72900	Tektronix	131-4244-00
1	-	-	U1	IC, tracking/termination synch. PWM switcher.	PWP28	TI	TPS54672PWP
-	1	-	U1	IC, tracking/termination synch. PWM switcher.	PWP28	TI	TPS54872PWP
-	-	1	U1	IC, tracking/termination synch. PWM switcher.	PWP28	TI	TPS54972PWP
1	1	1	-	PCB, 3 in. × 3 in. × 0.063 in.		Any	SLVP222

**Note:** SLVP222-001 is TPS54672EVM-222  
SLVP222-002 is TPS54872EVM-222  
SLVP222-003 is TPS54972EVM-222