TEXAS INSTRUMENTS

THS1030/31EVM Evaluation Module for the THS1030/THS1031 10-Bit ADC

User's Guide

2000

AAP Data Conversion

SLAU040

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Preface

Read This First

About This Manual

This manual describes the physical characteristics, functions, modes of operation, and configuration of the THS1030/31EVM evaluation module (EVM).

How to Use This Manual

- ❑ Chapter 1 – Overview
- ❑ Chapter 2 – Physical Description
- ❑ Chapter 3 – Circuit Description
- ❑ Chapter 4 – Modes of Operation

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Chapter 1

Overview

This chapter gives a general overview of the THS1030/31EVM evaluation module (EVM), and describes some of the factors that must be considered in using this module.

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1.1 Purpose

The THS1030/31EVM evaluation module (EVM) provides a platform for evaluation of the THS1030 and THS1031 10-bit analog-to-digital converters (ADC) under various signal, reference, and supply conditions. Unless stated explicitly, the functionality described in this user's guide applies to both THS1030 and THS1031 devices.

1.2 EVM Basic Functions

Analog input to the THS1030/31 is provided via an external SMA connector. The input can be configured onboard to be ac, dc, or transformer coupled to the input of the device.

An external SMA connector is provided on the THS1031 for the clamp input. This allows external digital control of the ADC's clamping function. The ADC can be clamped to either the device reference or to ground via an onboard jumper.

The EVM provides an external SMA connection for ADC clock input. This can be configured to be either ac or dc coupled. Space is reserved on the board for a crystal oscillator to perform this function, and can be populated when required.

In addition to the internal reference from the THS1030/31 device, options are provided on the EVM to allow adjustment of the ADC reference via an onboard reference circuit.

Output from the EVM is via a 40-pin header connector. The digital lines from the THS1030/31 are buffered using the SN74LVCC4245A before going to the header. This allows the THS1030/31 supplies to be varied without affecting the output signal levels.

Power connections to the EVM are via 4-mm banana sockets. Separate input connectors are provided for the analog and digital supply to the device, and for the reference and output buffer circuits.

The THS1031 has a number of programmable registers that can be programmed using DIL switches on the EVM.

1.3 Power Requirements

The EVM has 4 dc-power supply connections: 5 V for the output buffers, 2.7 V to 5 V for the analog and digital supplies to the ADC, and 2.7 V to 5 V for the reference circuit. Each of these supplies is independent, but it should be noted that the input thresholds of the ADC will vary dependent on the digital and analog supply voltages, as per the datasheet specification.

Voltage Limits

Exceeding the 5-V maximum can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 THS1030/31EVM Operational Procedure

The THS1030/31EVM provides a flexible means of evaluating the THS1030 and THS1031 in a number of modes of operation. These are described more fully in chapter 4. The following basic setup procedure can be used as a board-confidence check:

❑ Verify all jumper settings against the following schematic jumper table:

Device	Jumper Table (connection)
THS1030	H1 pin 2–3, H2 pin 2–3, H3 pin 1–2, H4 pin 2–3, H6 pin 1–2, H8 pin 1–2, H9 pin 1–2, H10 pin 1–2, H11 pin 1–2, LINK4, LINK6, LINK10, LINK11, LINK12, LINK13, LINK14, LINK16.
THS1031	H1 pin 2–3, H2 pin 2–3, H3 pin 1–2, H4 pin 2–3, H6 pin 1–2, H8 pin 2–3, H9 pin 1–2, H10 pin 1–2, H11 pin 2–3, LINK4, LINK6, LINK10, LINK11, LINK12, LINK13, LINK14, LINK16.

❑ Check that T1 is unpopulated.

❑ Connect supplies to the EVM: 5 V on J9, J6, J7, and J8; GND on J10 and J11.

❑ Switch power supplies on.

❑ Use a DVM to monitor the voltage from TP24 to TP21. Use a potentiometer adjusting tool to adjust P2 such that the DVM reads 2.5 V.

❑ Use a DVM to monitor the voltage from TP26 to TP21. Use a potentiometer adjusting tool to adjust P3 such that the DVM reads 0.5 V.

❑ Use a function generator with 50-Ω output to input a 10-MHz, 2.5-V offset, 5-Vp–p amplitude signal into J2.

❑ Use a function generator with 50-Ω output to input a 50-kHz, 1.5-V offset, 1.5-Vp-p amplitude signal into J3.

❑ The digital pattern on the output header J4 should now represent a sine wave, and can be monitored using a logic analyzer.

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM, and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a 4-layer, 151-mm (5.94″) × 115-mm (4.54″), 1.57-mm (0.062″) thick PCB using FR-4 material. Figures 2–1 through 2–6 show the individual layers.

Figure 2–1. Silk Top

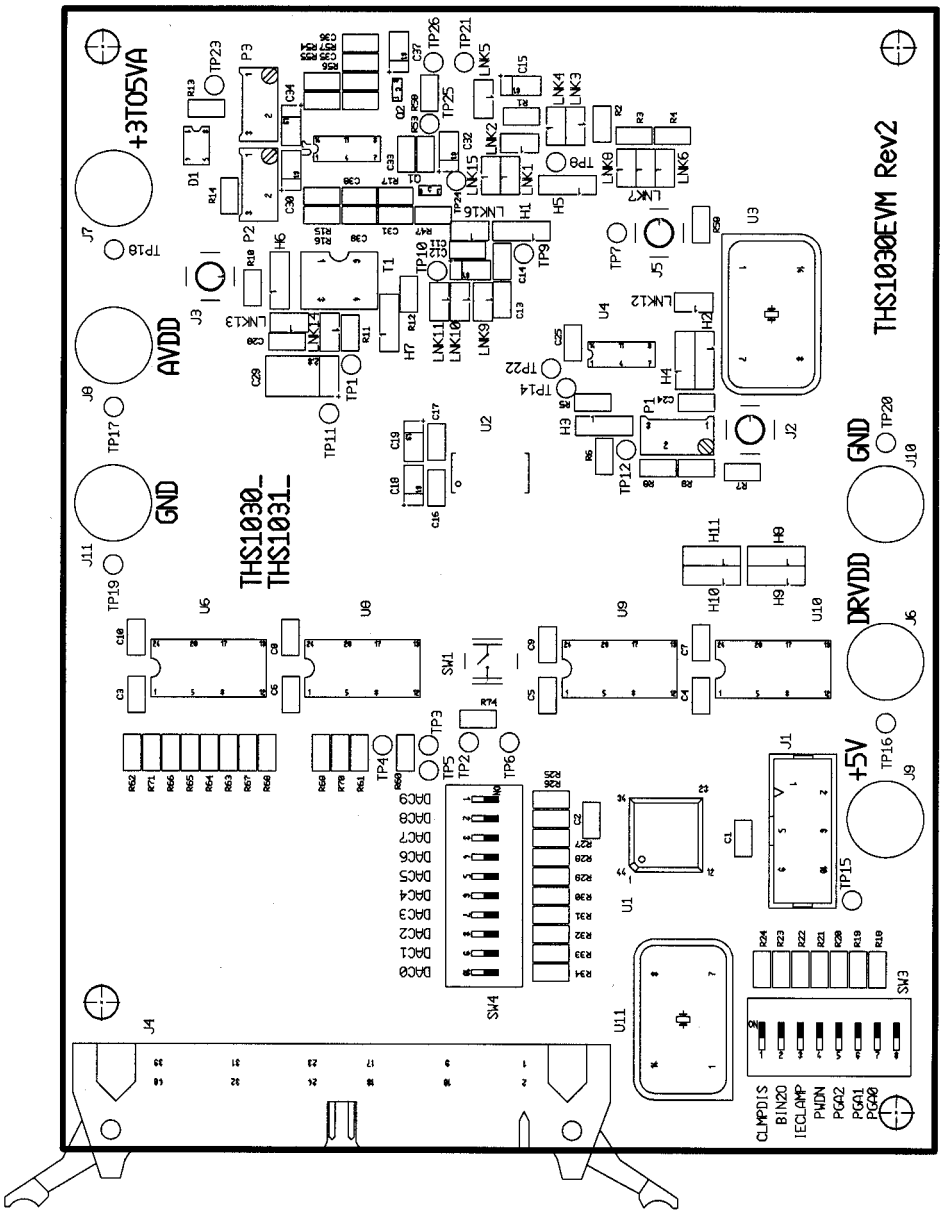


Figure 2–2. Silk Bottom

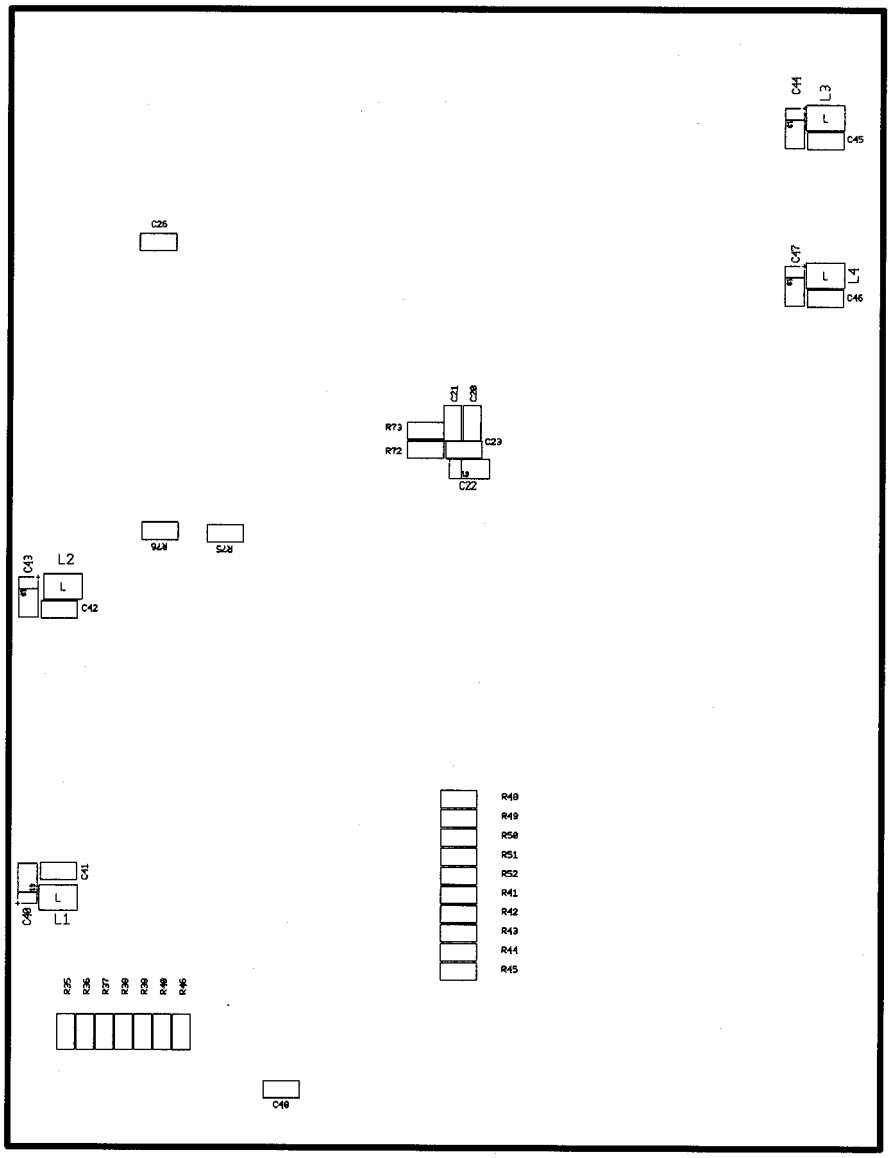


Figure 2–3. Top

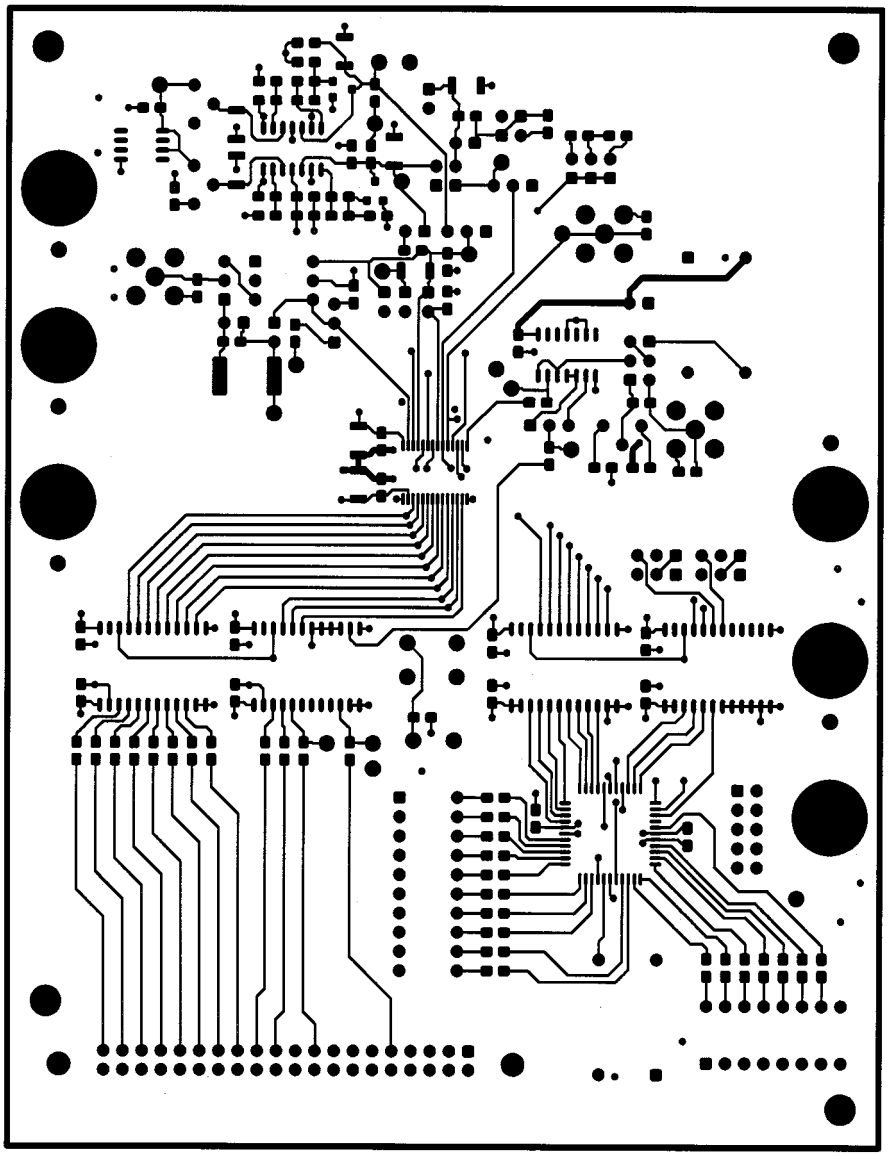


Figure 2–4. Inner 1

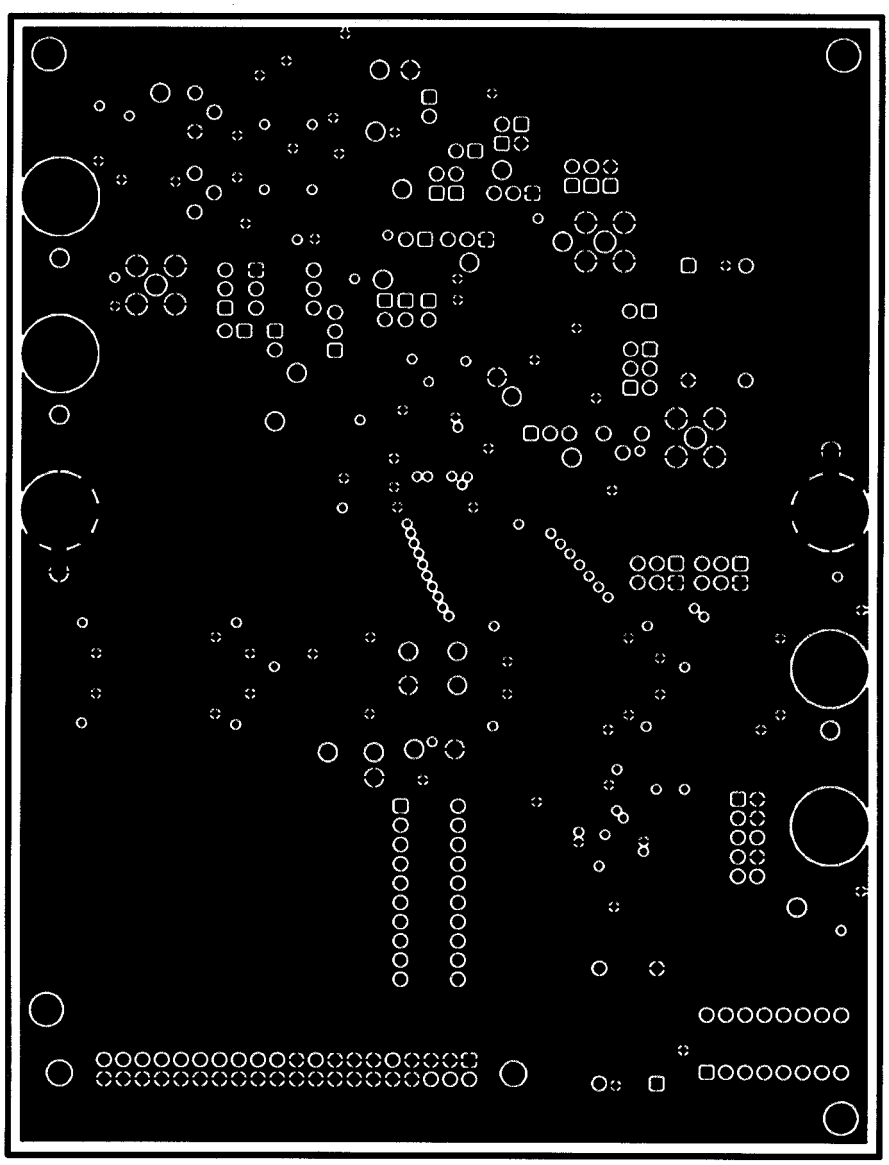


Figure 2–5. Inner 2

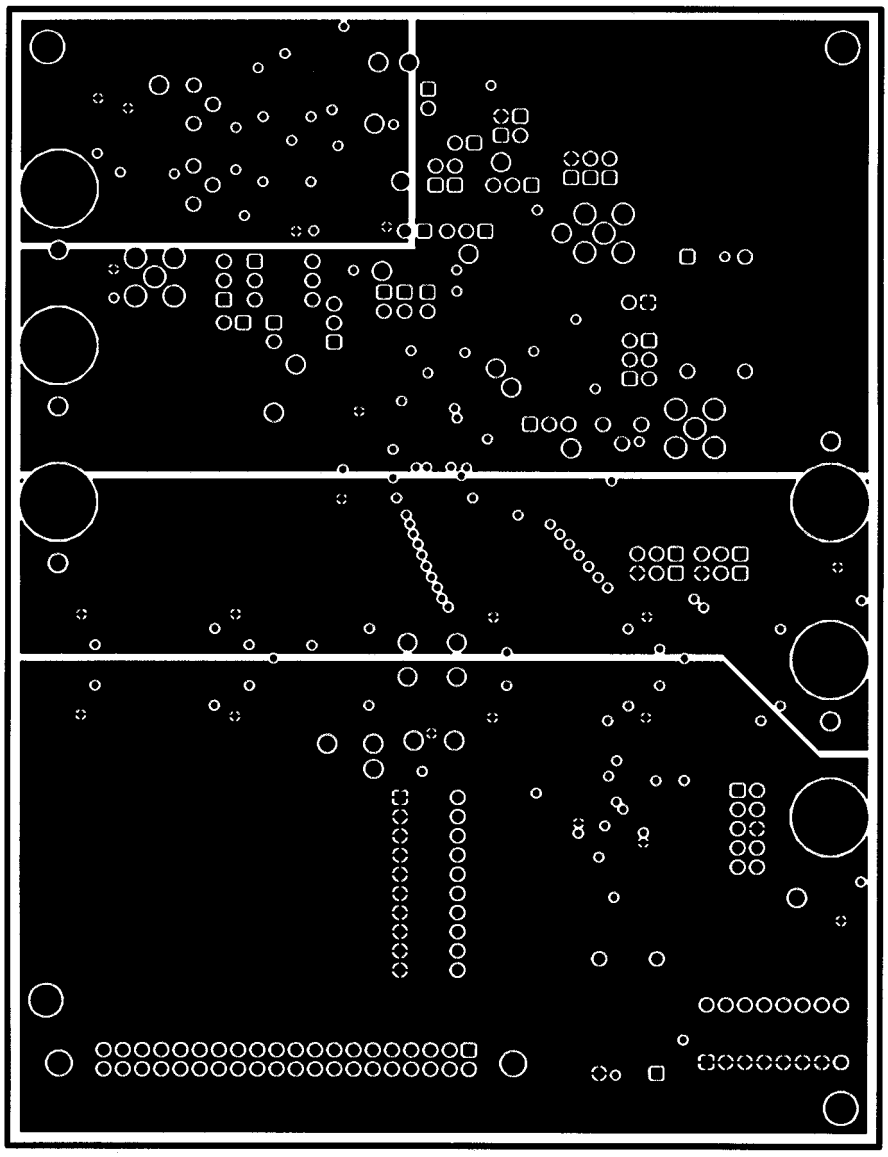
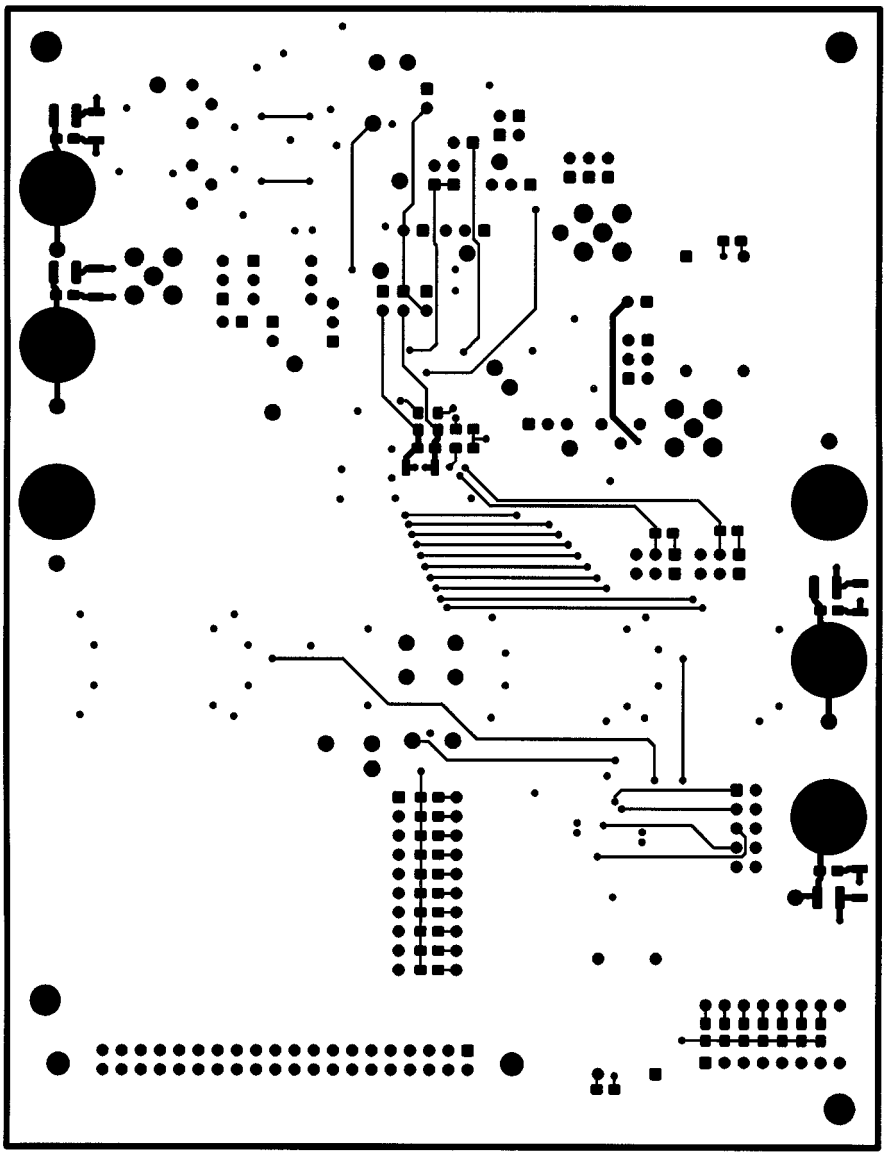


Figure 2–6. Bottom



2.2 Parts LIst

Table 2–1 lists the parts used in constructing the EVM.

Table 2–1. Parts List

Qty	Reference Description	Description	Manufacturer	Part Number
1	D1	LT1004-1.2 voltage reference	TI	LT1004CD-1-2
1	U4	SN74AHC14D hex inverter	TI	SN74AHC14D
4	U6 U8 U9 U10	SN74LVCC4245ADW bus transceiver	TI	SN74LVCC4245ADW
1	U7	TLV2464CD quad opamp	TI	TLV2464CD
1	U11	CMOS Dil 14 oscillator, 4-MHz	IQD	IQXO-100C 4MHz
1	SW1	6x6 mm flat push-button switch	Omron	B3F1000
6	TP5, TP6, TP19, TP20, TP21, TP22	1.32-mm test pin, black	W Hughes	100-103
18	TP2, TP3, TP4, TP7, TP8, TP9, TP10, TP11, TP12, TP14, TP15, TP16, TP17, TP18, TP23, TP24, TP25, TP26	1.32-mm test pin, red	W Hughes	100-107
1	TP1	1.32-mm test pin, green	W Hughes	100-108
1	SW3	0.1″ spacing TH 8 way Dil switch	Multicomp	MCDS08
3	J2, J3, J5	SMB connector vertical PCB	MACOM	B65N07G999X
1	P1	2-kΩ 3296Y potentiometer	Bourns	3296Y-001-202
2	P2, P3	10-kΩ potentiometer	Bourns	3296Y-001-106
6	J6, J7, J8, J9, J10, J11	4-mm panel socket	Hirschmann	BO10
1	C38	470-pF 0805 SMD ceramic capacitor NPO	AVX	08051A471JAT00J
16	LNK1, LNK2, LNK3, LNK4, LNK5, LNK6, LNK7, LNK8, LNK9, LNK10, LNK11, LNK12, LNK13, LNK14, LNK15, LNK16	0.1″ spacing 1X2 header	Harwin	M20-9990206
11	H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11	0.1″ spacing 1X3 header straight	Harwin	M20-9990306
1	SW4	0.1″ spacing TH 10 way Dil switch	Multicomp	DS10
3	R7, R10, R59	51R 0805 thick-film resistor 5%	Multicomp	CR10510JT
1	R74	2K 0805 thick-film resistor 1%	Multicomp	CR10202JT
3	R8, R9, R16	5K1 0805 thick-film resistor 5%	Multicomp	CR10512JT
1	R55	11K 0805 thick-film resistor 5%	Multicomp	CR10113JT
4	L1, L2, L3, L4	0R 1206 thick-film resistor	Multicomp	CR8XXXJTZ32

Table 2–1. Parts List (Continued)

Qty	Reference Description	Description	Manufacturer	Part Number
14	R5, R6, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71	39R 0805 thick-film resistor 1%	Multicomp	CR10390FT
2	R11, R12	100R 0805 thick-film resistor 1%	Multicomp	CR10101FT
2	R53, R58	180R 0805 thick-film resistor 1%	Multicomp	CR10181FT
2	R47, R57	330R 0805 thick-film resistor 1%	Multicomp	CR10331FT
2	R17, R56	820R 0805 thick-film resistor 1%	Multicomp	CR10821FT
1	R13	1-kΩ 0805 thick-film resistor 1%	Multicomp	CR10102FT
1	R14	1K5 0805 thick-film resistor 1%	Multicomp	CR10152FT
17	R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34	4K7 0805 thick-film resistor 1%	Multicomp	CR10472FT
5	R3, R4, R54, R75, R76,	10-kΩ 0805 thick-film resistor 1%	Multicomp	CR10103FT
1	R15	15-kΩ 0805 thick-film resistor 1%	Multicomp	CR10153FT
17	R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R48, R49, R50, R51, R52	100-kΩ 0805 thick-film resistor 1%	Multicomp	CR10104FT
1	J4	40-way male PCB mounting header, 0.05” cable pitch, 90-deg	Multicomp	9.18541E+11
1	J1	0.1” spacing 2X5 header straight	Elco	008380010000010
12	C15, C18, C19, C22, C30, C32, C34, C37, C40, C43, C44, C47	10-µF case B SMD tantalum capacitor, 16-V	Multicomp	TAJB10M16RFX
1	C29	47-µF case D SMD tantalum capacitor, 16-V	Multicomp	TAJD47M16RFX
29	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C16, C17, C20, C21, C23, C24, C25, C26, C28, C31, C33, C35, C36, C39, C41, C42, C45, C46, C48	0.1-µF 0805 SMD ceramic capacitor, X7R, 16-V	AVX	08053C104KA800J
1	Q2	2N3904 SOT23 transistor	General Semiconductor	IMBT3904
1	Q1	2N3906 SOT23 transistor	General Semiconductor	IMBT3906
1	T1	TT1-6-X65 RF transformer	Mini Circuits	TT1-6-X65
1	U2	THS1031CDB ADC	TI	THS1031CDB
1	U1	Vantis Mach4_32_32_44TQFP	Vantis	M4-32/32-15VC

Chapter 3

Circuit Description

This chapter contains the EVM schematic diagram and discusses the various functions on the EVM.

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3.1 Schematic Diagram

Figures 3–1 through 3–5 show the schematic diagram for the EVM. The following paragraphs describe the EVM circuits.

Figure 3–1. EVM Schematic Diagram

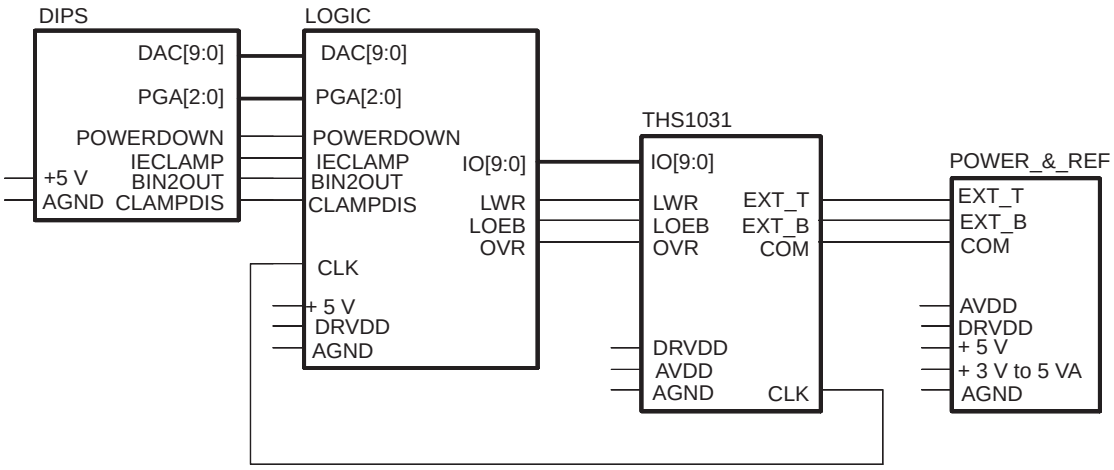


Figure 3–2. EVM Schematic Diagram – DIPS

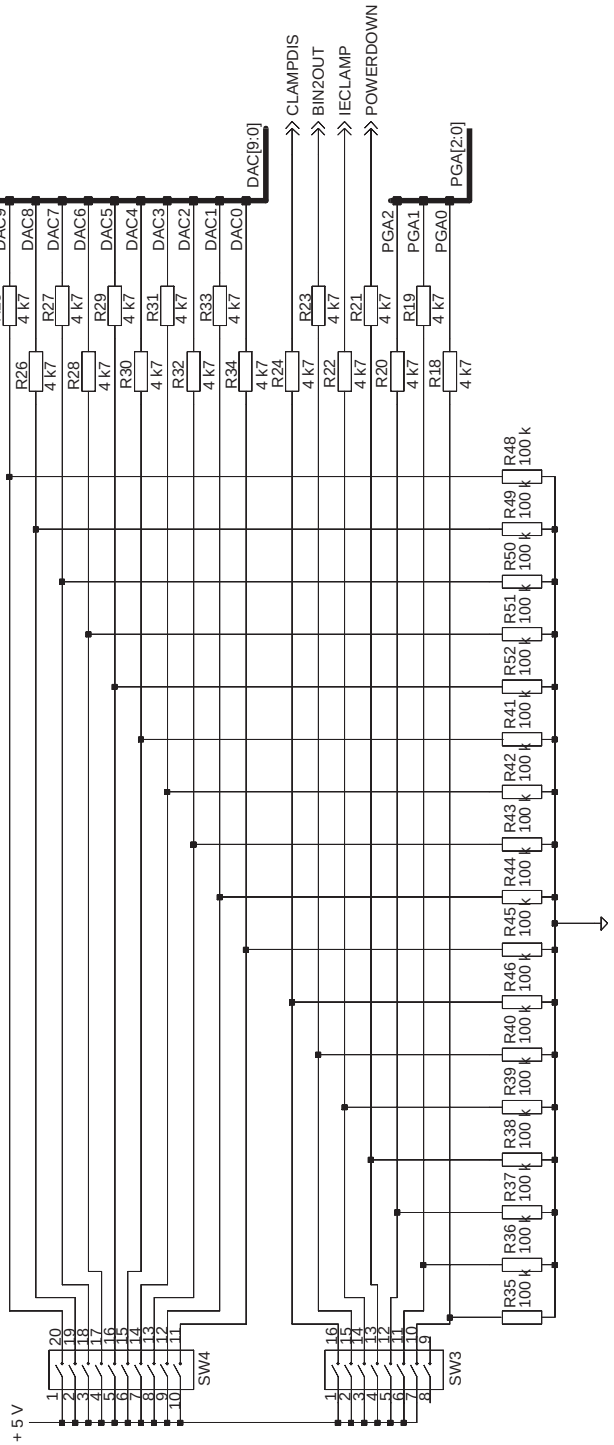


Figure 3–3. EVM Schematic Diagram – LOGIC

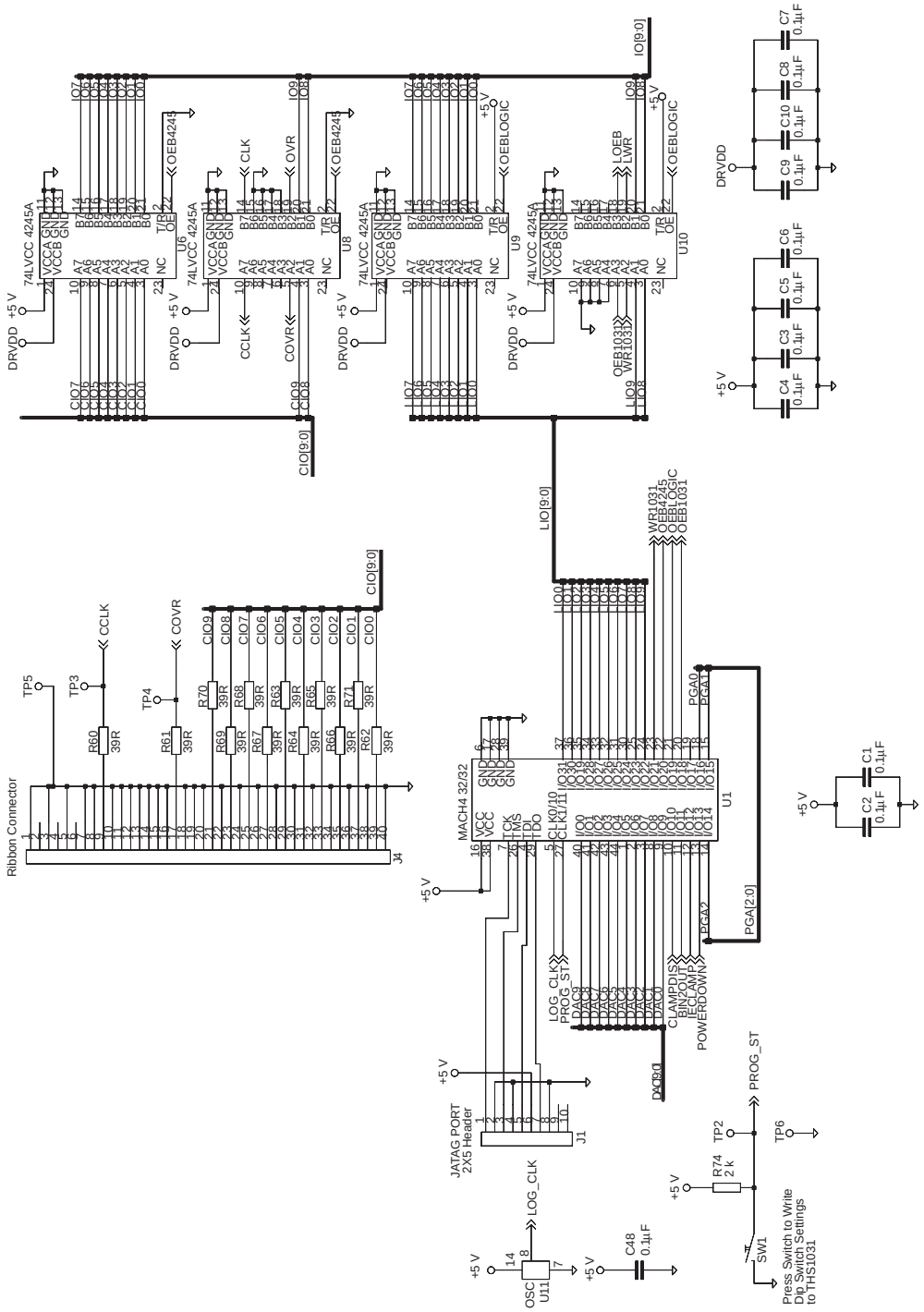


Figure 3–4. EVM Schematic Diagram – THS1031

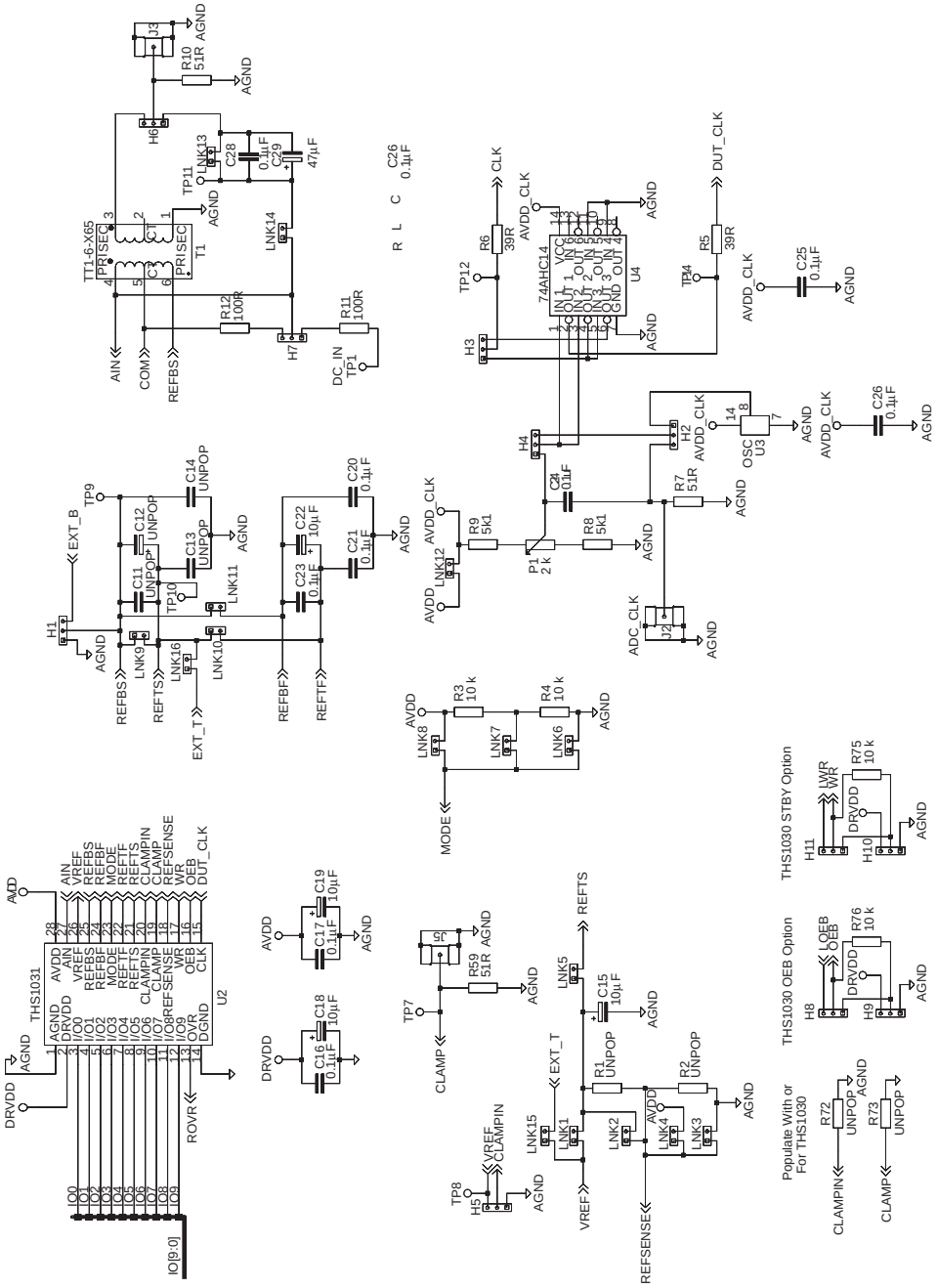
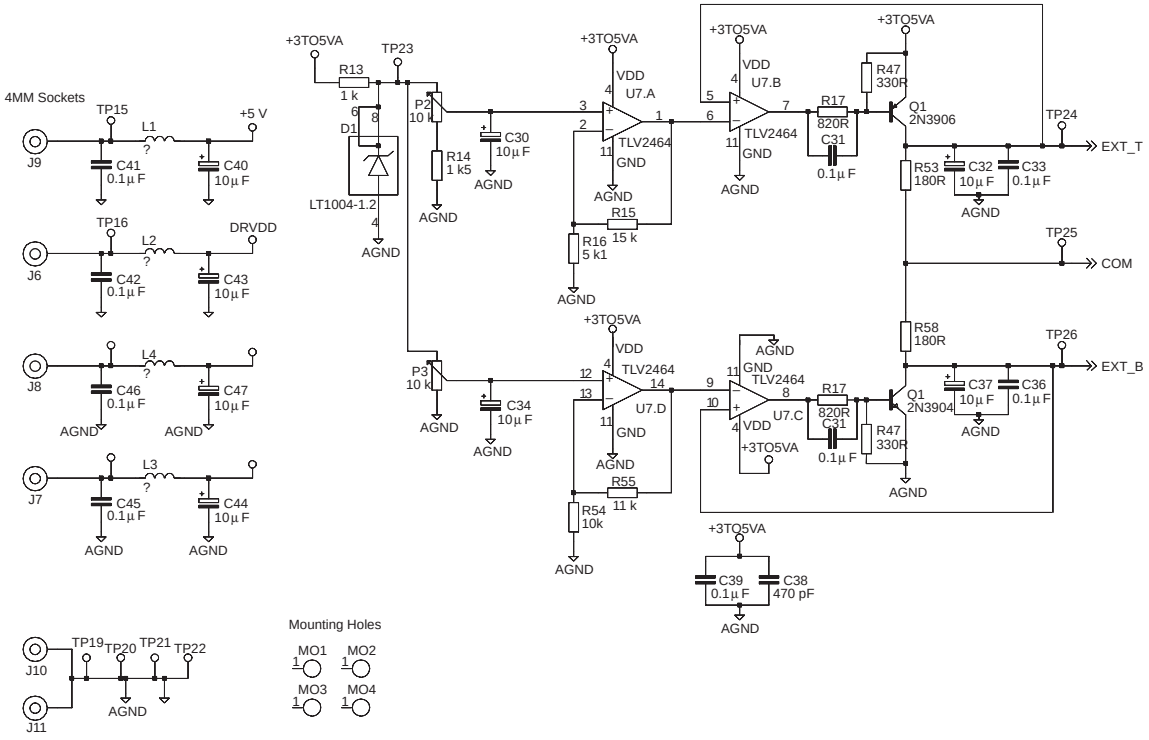


Figure 3–5. EVM Schematic Diagram – POWER_&_REF



3.2 Circuit Function

The following paragraphs describe the function of individual circuits. Refer to Chapter 4 for jumper configurations for various modes of operation, and to the relevant data sheet for device operating characteristics.

3.2.1 Inputs

The EVM has one analog input via SMA connector J3. The path from this connector to the THS1030/31 AIN pin can be configured to cater to different operating modes and input signal levels. The main operating modes are ac, dc, and transformer coupled.

Note:

The transformer should be removed from the board in modes that do not use the signal path through it.

The THS1031 has a clamp input that can be fed in directly via SMA connector J5. This affords external digital control of the ADC's clamping function. The ADC can be clamped (via the clamping pin) to either the device reference or to ground using a jumper on H5.

SMA Connector J2 can be used to input a clock signal to the board from an external source. If the source does not have the correct dc level for input to the

74AHC14 hex inverter IC (U4), then it should be ac-coupled through C24, with its dc level trimmed using potentiometer P1 if necessary.

3.2.2 Clock Options

The EVM provides flexibility as to the source of the ADC conversion clock: this can come from an external source as described above, or from a crystal-oscillator module when U3 is populated with a standard DIL14 HCMOS.

Note:

Care should be taken when selecting a crystal oscillator module to make sure that it operates at the AVDD supply voltage being used.

To synchronize the output data from the ADC to external circuitry, a buffered version of the conversion clock is provided to output header J4 via U4 and U8. The phase relationship between the conversion clock and the output clock can be selected using header H3.

3.2.3 References

In addition to the capability to configure the on-chip reference via jumpers, a reference circuit has been included on the EVM. This uses a 1.2-V shunt reference diode (D1) as its primary source, and allows adjustment of the REFTS and REFBS signals to the ADC using potentiometers P2 and P3, respectively. The ranges of the external reference signals are: REFTS, 0.60 V to 2.68 V on a 2.7-V supply, and 0.60 V to 4.85 V on a 5-V supply; REFBS, 0 V to 1.79 V on a 2.70-V supply, and 0V to 2.00V on a 5 V supply. See Chapter 4 for further details on the jumper settings required to use this mode.

3.2.4 Power

Power is supplied to the EVM via 4-mm banana sockets. Separate input connectors are provided for the analog (J8) and digital (J6) supplies to the device, and for the reference (J7) and output buffer (J9) circuits. The supply for J9 should be 5 V, with the supply for J6, J7, and J8 being between 2.7 V and 5.5 V. Power-supply return paths (GND) are via connectors J10 and J11. Each of these supplies is independent, but it should be noted that the input thresholds of the ADC will vary depending on the digital and analog supply voltages, in accordance with the data sheet specifications.

3.2.5 Outputs

The data outputs from the ADC are buffered using SN74LVCC4245A before going to header J4. This allows the supplies on the THS1030/31 to be varied without affecting the output signal levels. Header J4 is a standard 40-pin device on a 100-mil grid, and allows easy connection to a logic analyzer. The connector test points are listed in Table 3–1.

Table 3–1. Output Connector J4

J4 Pin	Output	Function	J4 Pin	Output	Function
1		GND	21	I/O9	DATA
2		NC	22		GND
3		GND	23	I/O8	DATA
4		NC	24		GND
5		GND	25	I/O7	DATA
6		NC	26		GND
7		GND	27	I/O6	DATA
8		GND	28		GND
9	CLK	CLK	29	I/O5	DATA
10		GND	30		GND
11		GND	31	I/O4	DATA
12		GND	32		GND
13		GND	33	I/O3	DATA
14		GND	34		GND
15		GND	35	I/O2	DATA
16		GND	36		GND
17	OVR	OVR	37	I/O1	DATA
18		GND	38		GND
19		GND	39	I/O0	DATA
20		GND	40		GND

3.2.6 THS1031 Register Write

The THS1031 has a number of registers that can be written to put the device into various modes of operation (see data sheet). This can be accomplished easily on the EVM using the two banks of DIL switches SW3 and SW4. A write operation to the THS1031 is performed as follows :

1) Set the DIL switches to the value to be programmed into the THS1031 registers. Each DIL switch refers to a register bit in either clamp register1, clamp register2, or in the control register. DAC0 DIL switch refers to bit 0 of clamp register1, BIN2O DIL switch refers to bit 5 of the control register. A DIL switch in the *on* position represents a logic 1.

2) Press and release the push button switch SW1.

3) The THS1031 registers are now programmed with the DIL switch values.

Note:

After first application of power, the values on the DIL switches only represent what is programmed into the THS1031 after switch SW1 has been pressed. Prior to this, the device is in its default power-up state.

Chapter 4

Modes of Operation

The EVM can be easily configured, via jumper connections, to operate the THS1030/31 in various modes of operation. Figures 4–1 to 4–7 depict various modes of operation, with Tables 4–1 and 4–2 listing the corresponding jumper settings. For further information on these modes of operation, please refer to the relevant device data sheet.

Figure 4–1. Common Mode Input VREF/2 – 1Vp-p Input Span (top/bottom mode)

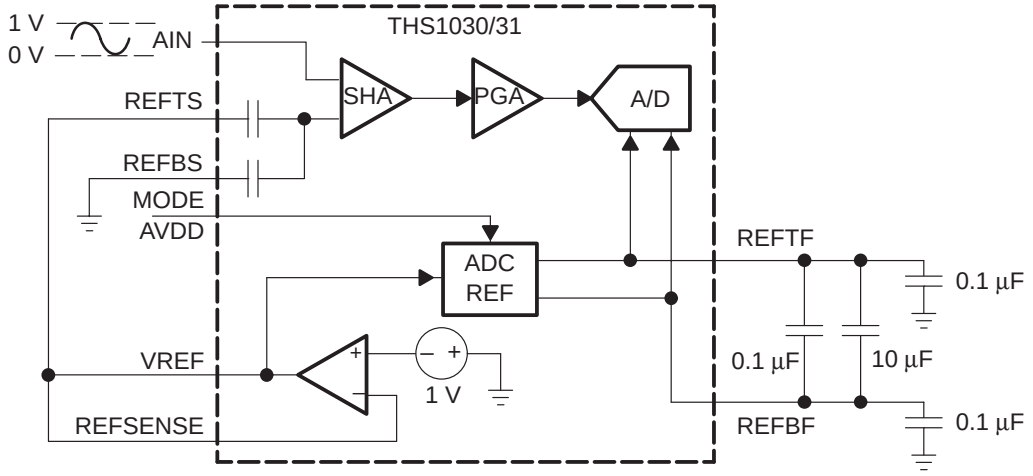


Figure 4–2. Common Mode Input VREF/2 – 2Vp-p Input Span (top/bottom mode)

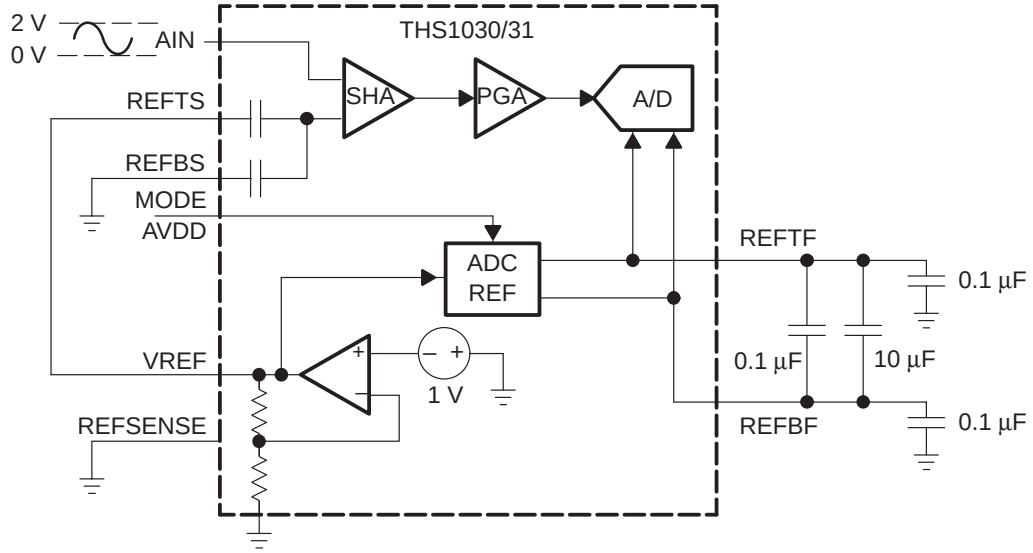


Figure 4–3. External Common Mode Input – 1Vp-p Input Span (center span mode)

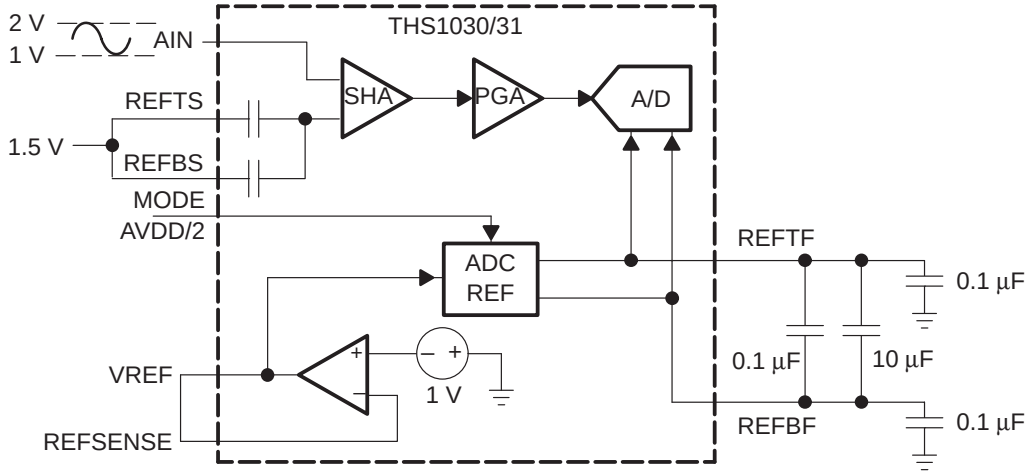


Figure 4–4. External Common Mode Input – 2Vp-p Input Span (center span mode)

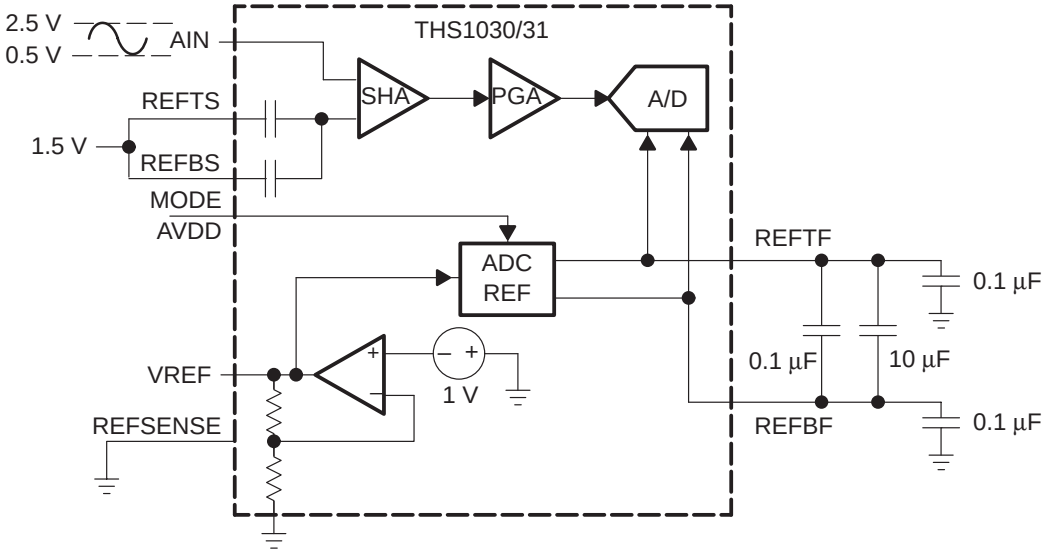


Figure 4–5. Differential Input – 1Vp-p Input Span (differential input mode)

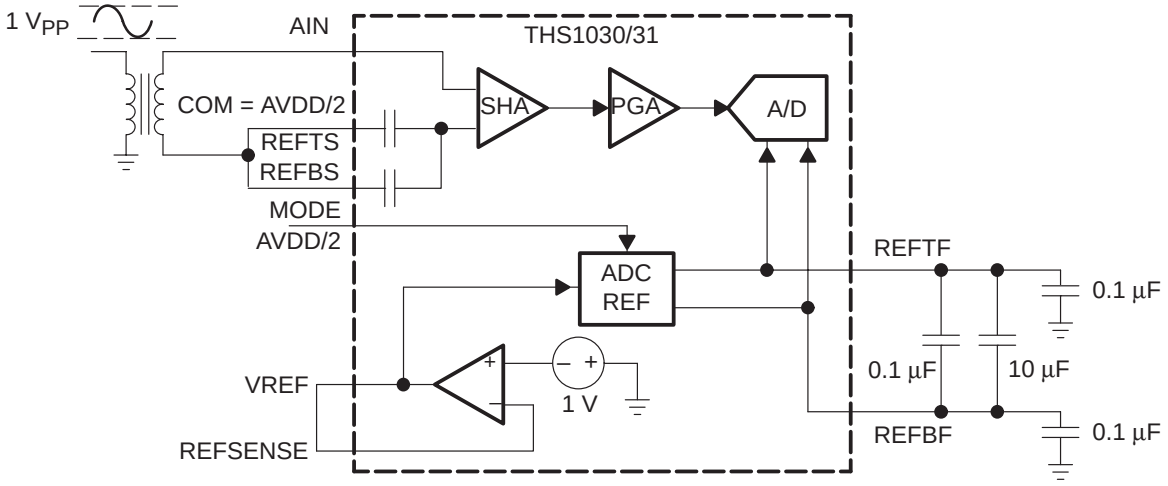


Figure 4–6. Differential Input – 2Vp-p Input Span (differential input mode)

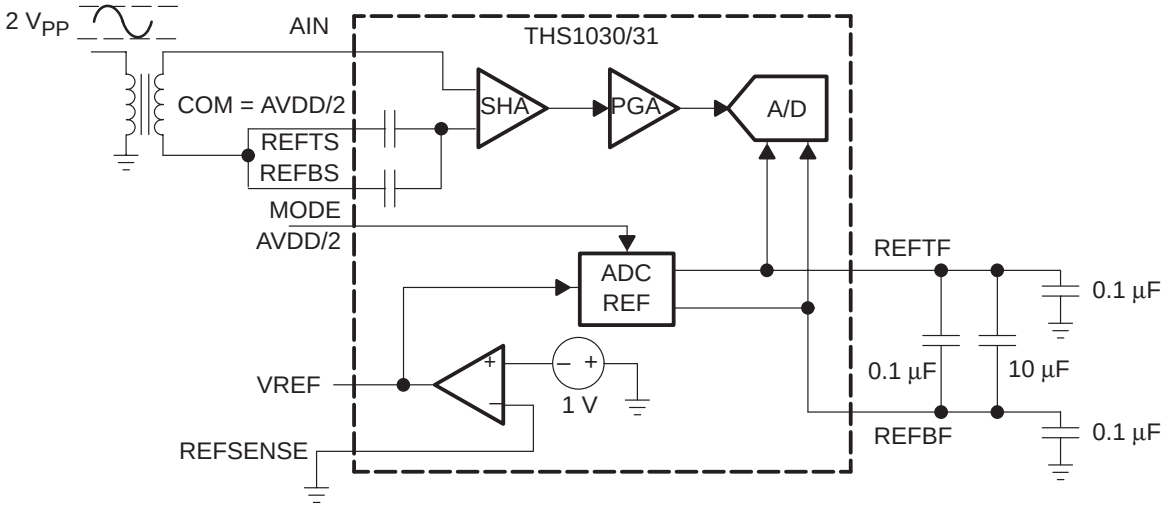


Figure 4–7. External Reference – Input Span and Bias Set by on Board Reference Circuit (potentiometer P2 sets EXT_T, potentiometer P3 sets EXT_B)

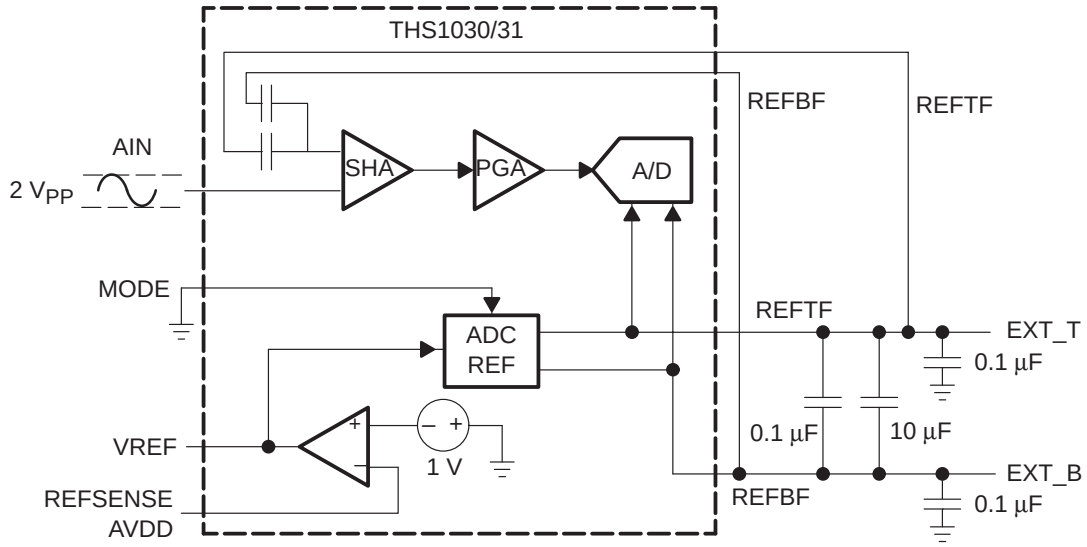


Table 4–1. Board Jumper Settings for Various Modes of Operation

Mode :	Top/Bottom (1V)	Top/Bottom (2V)	Cent. Span (1V)	Cent. Span (2V)	Differential (1V)	Differential (2V)	Ext. Ref.	
Reference:	Int	Int	Int	Int	Int	Int	Ext. Only	
Refbs/bf	–	–	POT P3	POT P3	–	–	POT P3	
Refts/tf	–	–	–	–	–	–	POT P2	
Clampin	H 5	H 5	H 5	H 5	H 5	H 5	H 5	THS1031 only
Clamp	J 5	J 5	J 5	J 5	J 5	J 5	J 5	THS1031 only
Header/link								
H 1	1–2	1–2	2–3	2–3	NO	NO	2–3	
H 6	1–2	1–2	1–2	1–2	2–3	2–3	1–2	
H 7	NO	NO	NO	NO	NO	NO	NO	
H 8	2–3	2–3	2–3	2–3	2–3	2–3	2–3	
H 9	1–2	1–2	1–2	1–2	1–2	1–2	1–2	
H 10	1–2	1–2	1–2	1–2	1–2	1–2	1–2	
H 11	2–3	2–3	2–3	2–3	2–3	2–3	2–3	
LINK 1	YES	YES	YES	NO	YES	NO	NO	
LINK 2	YES	NO	YES	NO	YES	NO	NO	
LINK 3	NO	YES	NO	YES	NO	YES	NO	
LINK 4	NO	NO	NO	NO	NO	NO	YES	
LINK 5	YES	YES	NO	NO	NO	NO	NO	
LINK 6	NO	NO	NO	NO	NO	NO	YES	
LINK 7	NO	NO	YES	YES	YES	YES	NO	
LINK 8	YES	YES	NO	NO	NO	NO	NO	

LINK 9	NO	NO	YES	YES	YES	YES	NO	
LINK 10	NO	NO	NO	NO	NO	NO	YES	
LINK 11	NO	NO	NO	NO	NO	NO	YES	
LINK 13	YES	YES	YES	YES	NO	NO	YES	
LINK 14	YES	YES	YES	YES	NO	NO	YES	
LINK 15	NO	NO	NO	NO	NO	NO	NO	
LINK 16	NO	NO	NO	NO	NO	NO	YES	
	Figure 4–1	Figure 4–2	Figure 4–3	Figure 4–4	Figure 4–5	Figure 4–6	Figure 4–7	

Table 4–2. Jumper Settings for Clock Options

Clock Options	Onboard Oscillator	External AC coupled Via J2	External DC coupled Via J2
H 2	1–2	1–2	2–3
H 3	1–2, 2–3	1–2, 2–3	1–2, 2–3
H 4	2–3	1–2	2–3
LINK 12	YES	YES	YES