# How to use the evaluation board for the STPMIC1x high integration power management IC

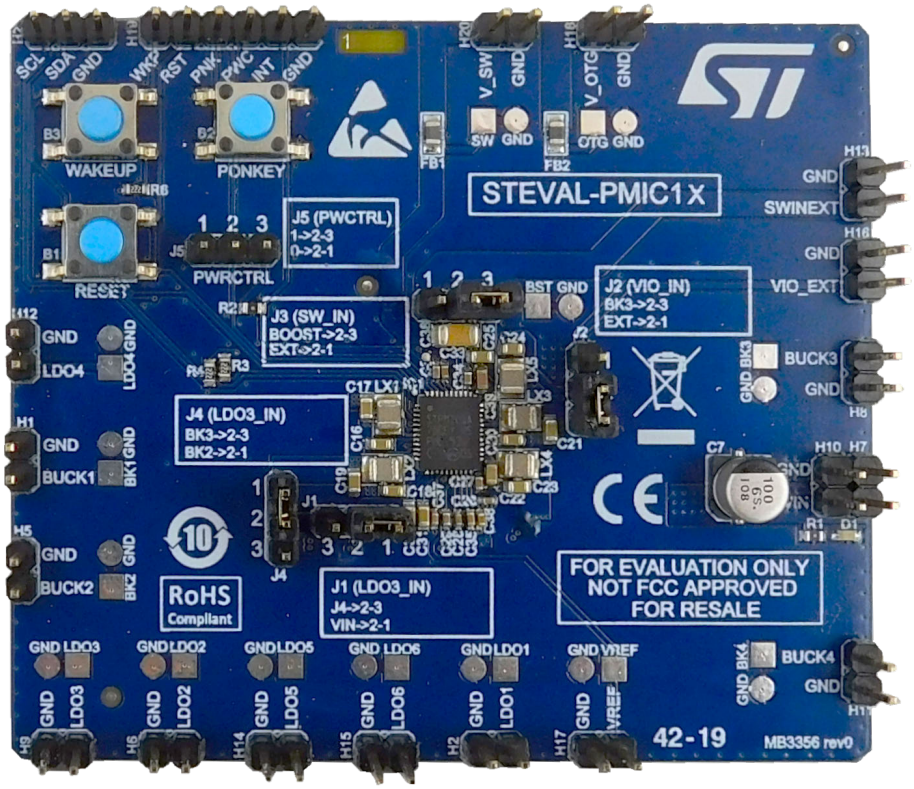
## Introduction

The STEVAL-PMIC1K1 evaluation board is designed for testing and evaluation of the STPMIC1 power management IC for application processors requiring low power and high efficiency. The STPMIC1 integrates a range of regulators, converters, and switches to manage the power requirements of STM32MP1 series microprocessors as well as other application processors and peripherals such as DDR, Flash, USB and other system devices.

The evaluation board is highly configurable and can be programmed via I²C to suit many power supply requirements of MPU-based applications such as IoT, human machine interfaces, Smart Home, etc.

The 6.1x7.2cm evaluation board is provided with 2.54mm header for each regulators output, some jumpers are present on the board for fast and easy setup accordingly to the application needs. For each output a TP is present for sensing the output voltage. User management buttons, Reset, Wakeup and Ponkey, are available for easy work. Dedicated connectors for digital section are present for I/O and I²C communication up to 1Mb/s

**Figure 1. Evaluation board with STPMIC1APQR device**




## RELATED LINKS

*For more details, see the STPMIC1 datasheet on the ST website*

# 1 PMIC evaluation board overview

## 1.1 STEVAL-PMIC1K1 board ordering information

**Table 1. Evaluation board order code**

| Evaluation board order code | STPMIC1 part number | Marking |
|---|---|---|
| STEVAL-PMIC1K1 | STPMIC1APQR | STPMIC1A |

**RELATED LINKS**

*For more details, see the STPMIC1 datasheet on the ST website*

## 1.2 STEVAL-PMIC1K1 output voltages

**Table 2. Output voltage of each regulator**

| Header | Regulator | Output Voltage (V) | Programming step (mV) | Output current (mA) |
|---|---|---|---|---|
| H2 | LDO1 | 1.7 to 3.3 | 100 | 350 |
| H6 | LDO2 | 1.7 to 3.3 | 100 | 350 |
| H9 | LDO3 Normal mode | 1.7 to 3.3 | 100 | 100 |
| | LDO3 Sink/Source mode | VOUT2 / 2 (BUCK2) | - | ±120 (±200peak) |
| | LDO3 Bypass mode | LDO3IN-VDROP_LDO3 | - | 50 |
| H12 | LDO4 | 3.3 (fixed) | - | 50 |
| H14 | LDO5 | 1.7 to 3.9 | 100 | 350 |
| H15 | LDO6 | 0.9 to 3.3 | 100 | 150 |
| H17 | REFDDR | VOUT2 / 2 (BUCK2) | - | ±5 |
| H1 | BUCK1 | 0.725 to 1.5 | 25 | 1500 |
| H5 | BUCK2 | 1 to 1.5 | 50 | 1000 |
| H8 | BUCK3 | 1 to 3.4 | 100 | 500 |
| H11 | BUCK4 | 0.6 to 3.9 | 25 (0.6V to 1.3V)<br>50 (1.3V to 1.5V)<br>100 (1.5 to 3.9V) | 2000 |
| - | BOOST | 5.2V (fixed) | - | 1100 |
| H18 | VBUSOTG_SW | ~BSTOUT | - | 100/500 mA(1) |
| H20 | PWR_SW | ~SWIN | - | 1000 |

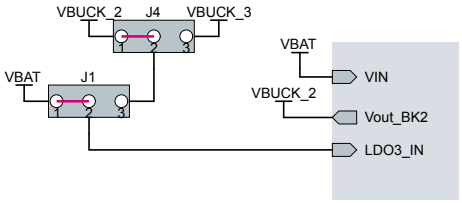
1. *depending on USB configuration*

## 1.3 STEVAL-PMIC1K1 interfaces

### 1.3.1 Jumper configurations

#### J1, J4: LDO3 input source

**Figure 2. J1, J4 LDO3 input source selection**



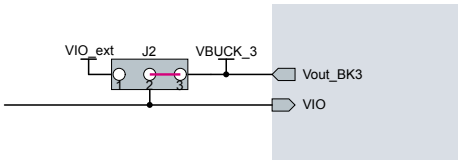

The J1 and J4 settings depend on application needs, user can choose the appropriate value in terms of power dissipation.

**Table 3. Jumper configuration for LDO3 input source**

| J1 position | J4 position | LDO3 input |
|---|---|---|
| 2-1 | - | VIN |
| 2-3 | 2-1 | BUCK2 out |
| 2-3 | 2-3 | BUCK3 out |

#### J2: VIO input source

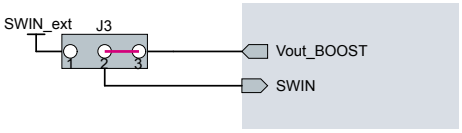
**Figure 3. J2 VIO input source selection**




This jumper selects the input source of VIO. If a jumper is located in position 2-1, external voltage is selected from H16 connector, if it is located in position 2-3, the output voltage of BUCK3 is selected.

#### J3: PWR_SW input source selection

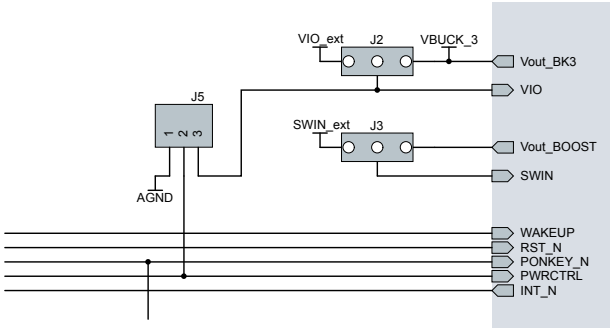
**Figure 4. J3 PWR_SW input source selection**




This jumper selects the input source of internal switch PWR_SW. If a jumper is located in position 2-1, external voltage is selected from H13 connector, if is located in position 2-3, output of BOOST is selected.

**J5: Power control mode**

**Figure 5. J5 power control mode jumper**




This jumper selects the power control mode. If a jumper is located in position 2-1, PWCTRL pin is forced to zero, if is located in position 2-3, PWCTRL pin is forced to VIO.

### 1.3.2 User interface buttons

- B1 pulls RESETn pin of PMIC to GND level:
  - this button allow tying the RSTn signal to GND to perform a Reset operation
- B2 pulls PONKEYn pin of PMIC to GND level:
  - this button allows tying the PONKEYn signal to GND to perform a Turn ON operation
- B3 pulls WAKEUP pin of PMIC to VIN:
  - this button allows tying the WAKEUP signal to High to perform a WAKEUP operation

## 1.4 Schematic diagrams

Figure 6. **STEVAL-PMIC1K1 board schematic**

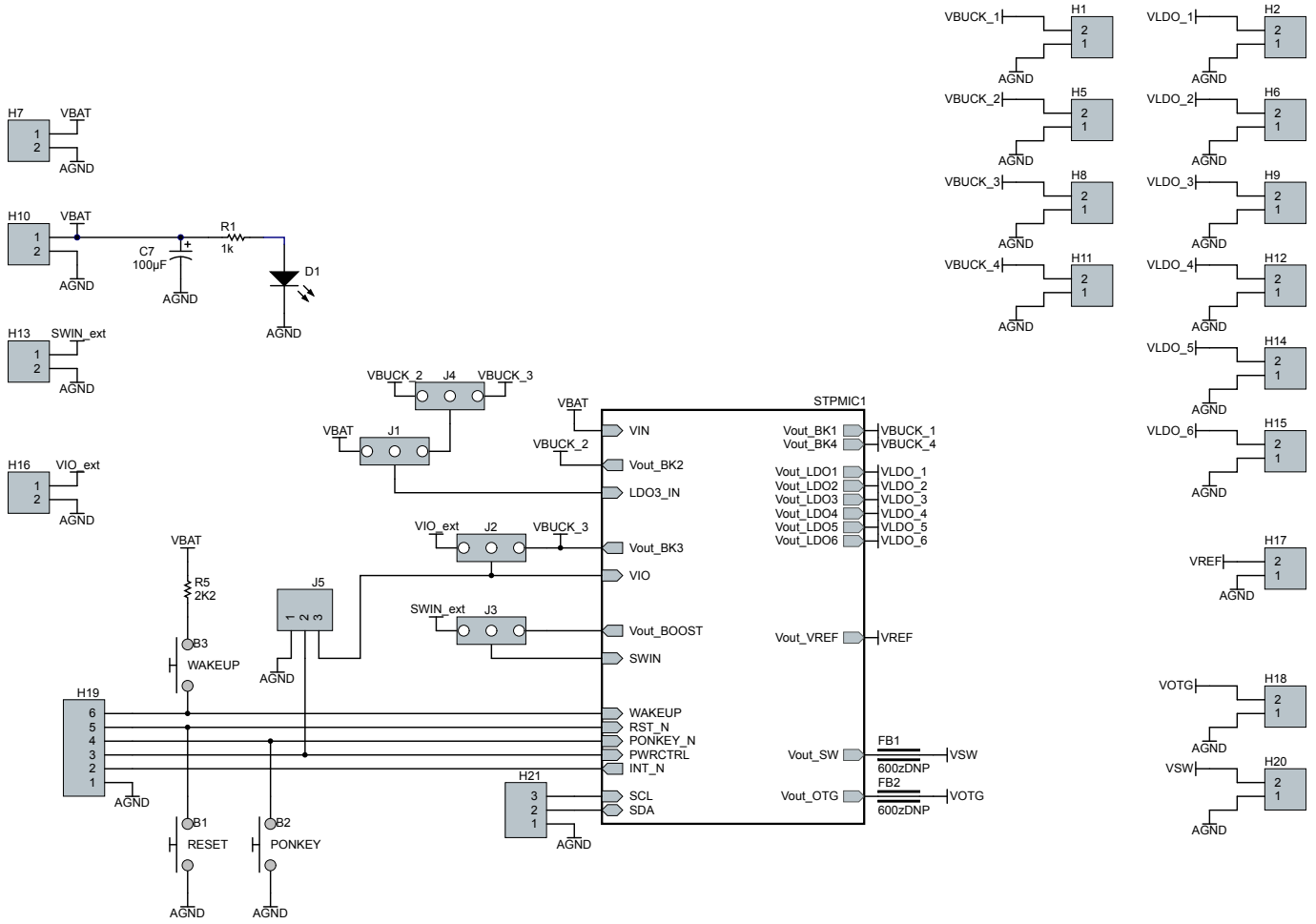
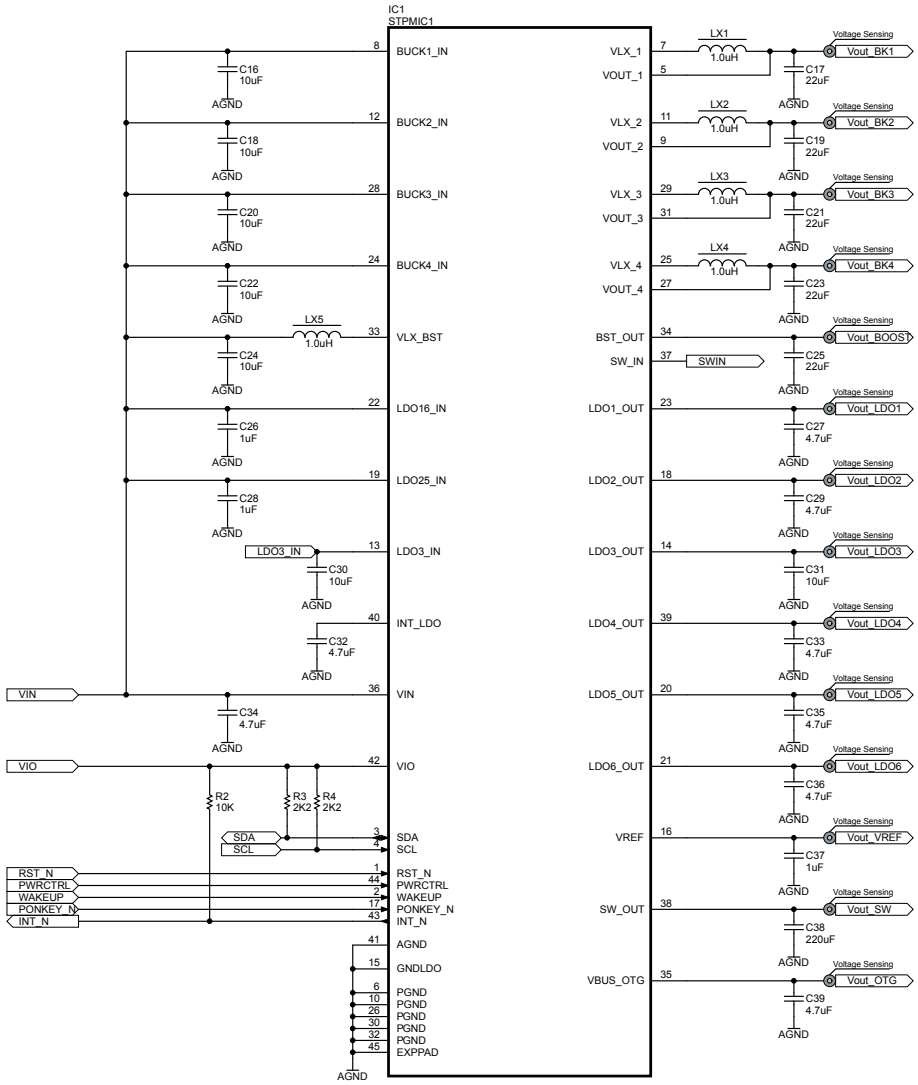


**Figure 7. STEVAL-PMIC1K1 power management IC schematic**



# 2 Board power supply setups

The STEVAL-PMIC1K1 can be configured to be powered from different sources. Follow the instructions below for the correct jumper settings associated with the different power supply options.

When using an external VIO voltage, all the digital information remains available for status readings, but when using a single power supply, the VIO also goes OFF when the device changes status to OFF, and an I²C error occurs.

## 2.1 Single 3.6$V_{IN}$ to 5$V_{IN}$ power supply

**Step 1.** Supply LDO3 input voltage from the BUCK2 output:

**Step 1a.** set J1 to position 2-3

**Step 1b.** set J4 to position 1-2

**Step 2.** Supply SW_IN input voltage from the BOOST output:

**Step 2a.** set J3 to position 2-3

**Step 3.** Supply VIO input voltage from the BUCK3 output:

**Step 3a.** set J2 to position 2-3

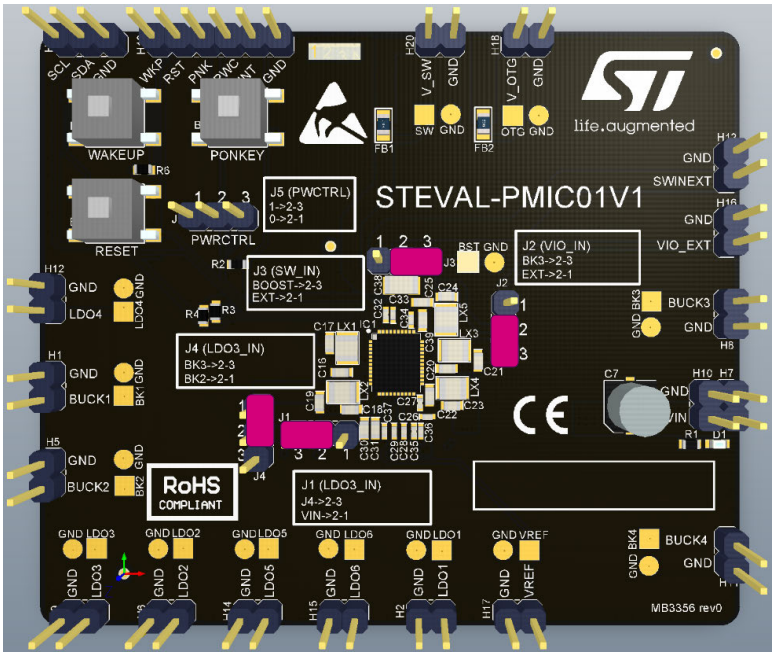
**Step 4.** Supply input power supply on H7 and H10 connectors (parallel):

**Step 4a.** set J5 to for power control polarity input

1-2 = active 0; 2-3 = active 1

**Step 4b.** supply 3.6V to 5V on H7 and H10

**Figure 8. Jumper setup for single power supply 3.6$V_{IN}$ to 5$V_{IN}$**



## 2.2 $5V_{IN}$ and external 3.3VIO power supply

**Step 1.** Supply LDO3 input voltage from the BUCK3 output:

**Step 1a.** set J1 to position 2-3

**Step 1b.** set J4 to position 2-3

**Step 2.** Supply SW_IN input voltage from the BOOST output:

**Step 2a.** set J3 to position 2-3

**Step 3.** Supply VIO_EXT through H16:

**Step 3a.** set J2 to position 1-2

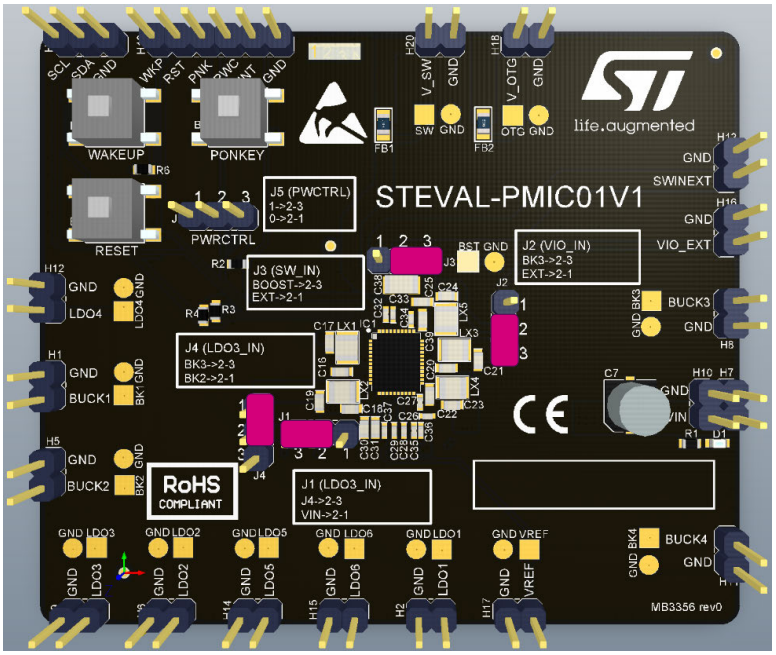
**Step 3b.** supply 3.3V at H16

**Step 4.** Supply input power supply on H7 and H10 connectors (parallel):

**Step 4a.** set J5 to for power control polarity input
1-2 = active 0; 2-3 = active 1

**Step 4b.** supply 5V on H7 and H10

**Figure 9. Jumper setup for single power supply 3.6$V_{IN}$ to 5$V_{IN}$**



# 3 STPMIC1 configuration registers

The configuration registers in the STPMIC1 non-volatile Flash can be programmed to suit different application requirements. The parameters that can be modified include VOUT, rank order in turn-on and turn-off sequences, VINOK threshold and hysteresis, etc.

The following register tables show the memory addresses in the STPMIC1 NVM for the configurable parameters of the corresponding STPMIC configuration A.

After loading the values into the NVM shadow register, writing the value 0x01 into the address 0xB9 renders the changes effective on the next power-on of the device.

Below is an example of using commands via I²C interface:

1. set device address to 0x33
2. read address 0xF8 = 0xEE
   - LOCK_OCP[0] → 0 = Short-circuit does not turn OFF PMIC
   - AUTO_TURN_ON[1] → 1 = PMIC starts automatically on VIN rising
   - PEKYLKP_OFF[2] → 1 = Turn OFF on long key press active
   - FORCE_LDO4[3] → 1 = LDO4 follows normal ranking
   - VINOK_THRES[5:4] → 1:0 = VINOK threshold voltage 3.5V
   - VINOK_HYS[7:6] → 1:1 = 500mV VINOK hysteresis voltage

   To change VINOK threshold from 3.5 V to 4.5 V, you need to change:
   - VINOK_THRES[5:4] → 1:1=VINOK threshold voltage 4.5V
3. write address 0xF8 = 0xFE
4. write address 0xB9 = 0x01
5. after cycle power OFF and power ON, the changes will take effect

**Table 4. Default NVM data STPMIC1A**

| ADDRESS | DATA | NVM shadow register | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0xF8 | 0xEE | VINOK_HYS[1:0] | | VINOK_THRES[1:0] | | FORCE_LDO4 | PEKYLKP_OFF | AUTO_TURN_ON | LOCK_OCP |
| | | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0xF9 | 0x92 | BUCK4_RANK[1:0] | | BUCK3_RANK[1:0] | | BUCK2_RANK[1:0] | | BUCK1_RANK [1:0] | |
| | | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0xFA | 0xC0 | LDO4_RANK[1:0] | | LDO3_RANK[1:0] | | LDO2_RANK[1:0] | | LDO1_RANK[1:0] | |
| | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0xFB | 0x02 | BUCK4_CLAP | LDO3_BYPASS | REFDDR_RANK[1:0] | | LDO6_RANK[1:0] | | LDO5_RANK[1:0] | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0xFC | 0xF2 | BUCK4_VOUT[1:0] | | BUCK3_VOUT[1:0] | | BUCK2_VOUT[1:0] | | BUCK1_VOUT[1:0] | |
| | | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0xFD | 0x80 | SWOUT_BOOST_OVP | reserved | LDO3_VOUT[1:0] | | LDO2_VOUT[1:0] | | LDO1_VOUT[1:0] | |
| | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0xFE | 0x02 | reserved | reserved | reserved | reserved | LDO6_VOUT[1:0] | | LDO5_VOUT[1:0] | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0xFF | 0x33 | LOCK_NVM | I2C_ADDR[6:0] | | | | | | |
| | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

## RELATED LINKS

*Refer to the STPMIC1 datasheet for more information regarding the NVM shadow register*

# 4 Power on/off sequence

The table below shows the configurations for the power management IC with different setups in terms of ranking and output voltage values; the ranking feature only impacts the LDO and buck converter regulators.

**Table 5. Default output voltage configuration**

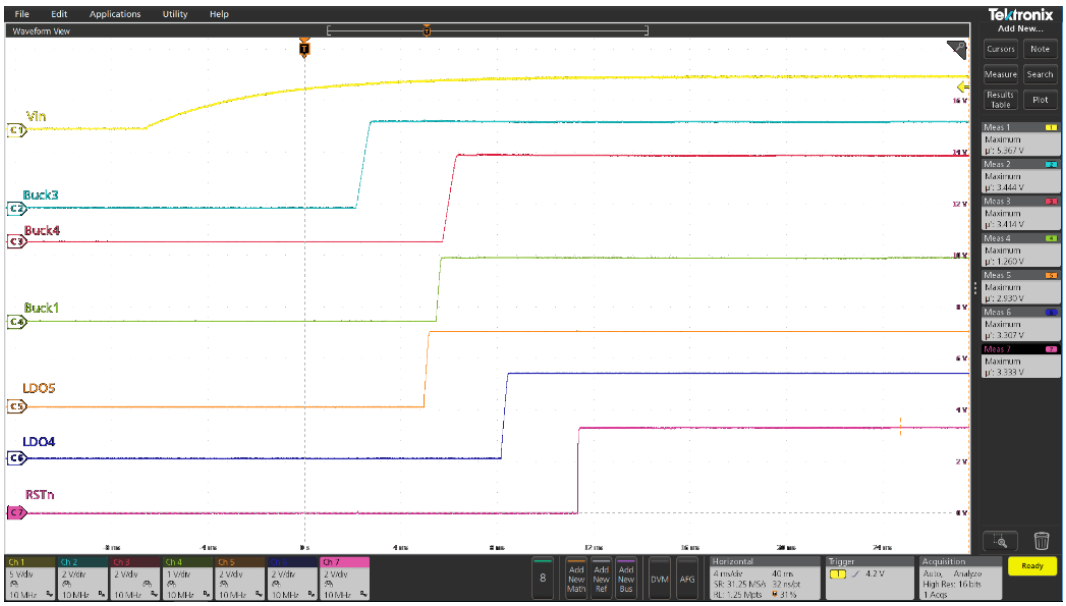
| Header | Output | STEVAL-PMIC1K1 | |
|---|---|---|---|
| | | Voltage | Rank |
| H2 | LDO1 | 0V | 0 |
| H6 | LDO2 | 0V | 0 |
| H9 | LDO3 | 0V | 0 |
| H12 | LDO4 | 3.3V | 3 |
| H14 | LDO5 | 2.9V | 2 |
| H15 | LDO6 | 0V | 0 |
| H1 | BUCK1 | 1.2V | 2 |
| H5 | BUCK2 | 0V | 0 |
| H8 | BUCK3 | 3.3V | 1 |
| H11 | BUCK4 | 3.3V | 2 |

The following waveforms show the turn-on and turn-off sequences of the STPMIC1A configuration. The delay between each rank is 3.0 ms typical. The same applies for the power-down sequence, but in reverse order.

The following figure shows the auto turn-on waveforms when power is first applied to the PMIC. In the STPMIC1A configuration, BUCK3 is programmed to start first (rank 1), followed by LDO5, BUCK1 and BUCK4 (rank 2), and finally LDO4 (rank 3).

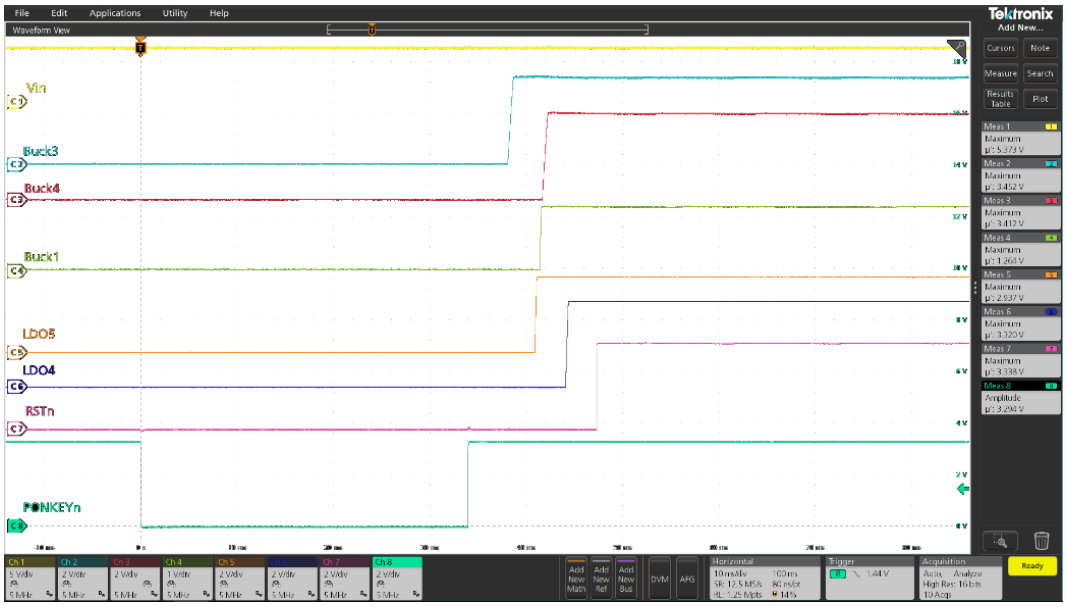
The 3 ms delay between each is clearly shown. RSTn signal goes HIGH after all rails are ON.

**Figure 10. Auto turn-on $V_{IN}$ 0 to 5V for STPMIC1A configuration**



The following figure shows the same sequence after pressing the PONKEYn button.

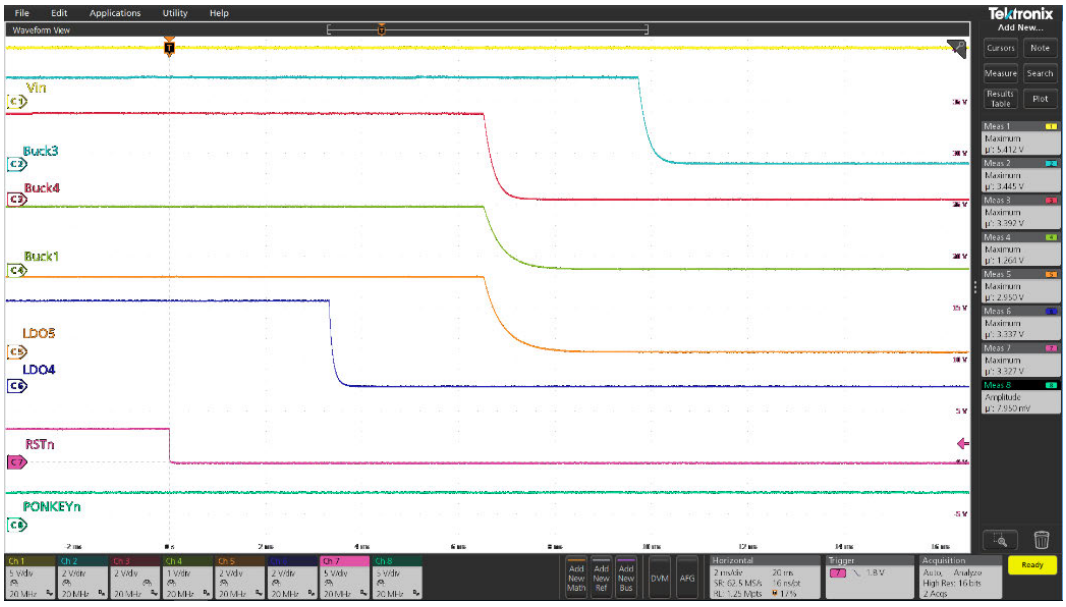
**Figure 11. Turn-on with PONKEYn for STPMIC1A configuration**




The following figure shows the power-off sequence triggered via the STPMIC1 I²C interface. Following the reverse ranking order for the turn-off sequence in the STPMIC1A configuration, LDO4 (rank 3) turns off first, followed by BUCK4, BUCK1 and LDO5 (rank 2), and finally BUCK3 (rank 1).

The RSTn signal goes LOW when the STPMIC1 device starts the turn-off sequence.

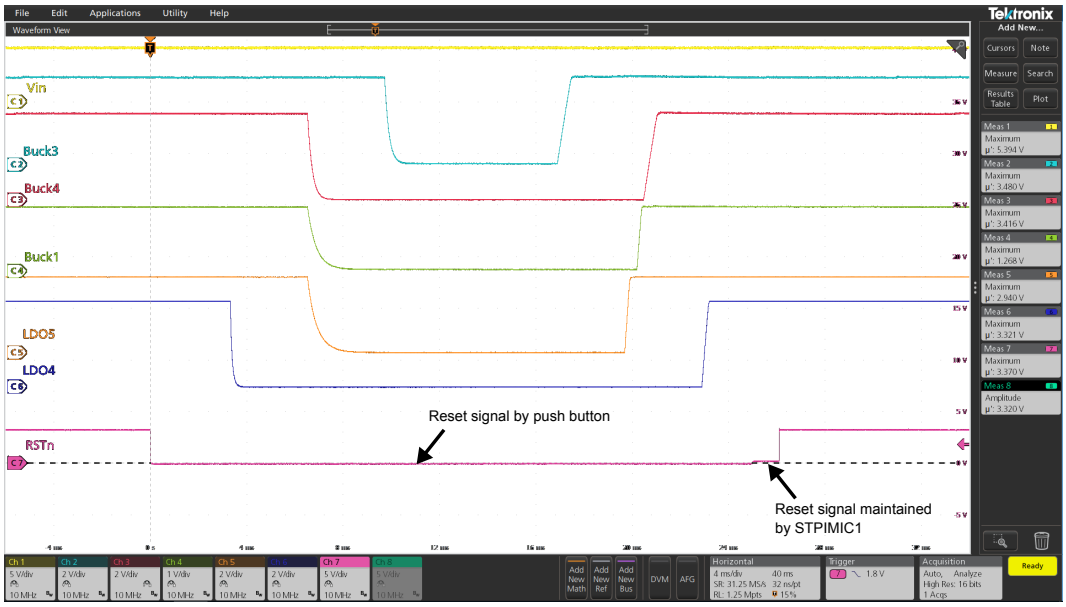
**Figure 12. Turn-off sequence for STPMIC1A configuration**




The following figure shows a reset sequence triggered by the RESET button. The turn-off and turn-on sequences follow the converter rank numbers in the STPMIC1A configuration.

The reset pin RSTn is bidirectional open-drain (internal pull-up), so the STPMIC1 maintains the reset line asserted during the reset phase until the turn-on sequence is completed.

Figure 13. **Reset sequence for STPMIC1A configuration**



# 5 Bill of materials

Table 6. **Bill of materials**

| Item | Q.ty | Ref. | Part / Value | Description | Manufacturer | Order code |
|---|---|---|---|---|---|---|
| 1 | 1 | B1 | 0.05A 12V | SWITCH TACTILE SPST-NO, TactButton | C&K | PTS645SM43SMTR92 LFS |
| 2 | 1 | B2 | 0.05A 12V | SWITCH TACTILE SPST-NO, TactButton | C&K | PTS645SM43SMTR92 LFS |
| 3 | 1 | B3 | 0.05A 12V | SWITCH TACTILE SPST-NO, TactButton | C&K | PTS645SM43SMTR92 LFS |
| 4 | 1 | C7 | 100µF, 6.3V, ±20% | CAP ALUM SMD, CAP_5.3x5.3mm | Panasonic Electronic Components | EEE-0JA101WR |
| 5 | 7 | C16, C18, C20, C22, C24, C30, C31 | 10µF, 10V | CAP CER X5R 0603, C-0603 | Murata Electronics North America | GRM188R61A106KE69D |
| 6 | 5 | C17, C19, C21, C23, C25 | 22µF, 6.3V | CAP CER X5R 0603, C-0603 | Murata Electronics North America | GRM188R60J226MEA0 |
| 7 | 3 | C26, C28, C37 | 1µF, 6.3V | CAP CER X5R 0402, C-0402 | Murata Electronics North America | GRM155R61E105KA12 |
| 8 | 7 | C27, C29, C32, C33, C34, C35, C36 | 4.7µF, 6.3V | CAP CER X5R 0402, C-0402 | Murata Electronics North America | GRM155R60J475ME47D |
| 9 | 1 | C38 | 220µF, 6.3V | CAP CER X5R 1206, C-1206 | Murata Electronics North America | GRM31CR60J227ME11L |
| 10 | 1 | C39 | 4.7µF, 16V | CAP CER X5R 0603, C-0603 | Murata Electronics North America | GRM188R61C475KE11D |
| 11 | 1 | D1 | - | MINI-MOLD CHIP LED (IVRANK REDUC, LED-0603 | Rohm Semiconductor | SML-D12U1WT86 |
| 12 | 2 | FB1, FB2 | 200Ω | FERRITE BEAD 0805 1LN, L-0805 | Murata Electronics North America | BLM21PG221SN1D |
| 13 | 17 | H1, H2, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H20 | - | Header, 2-Pin, Header_2x_100mils | Wurth Electronics Inc. | 61300211121 |
| 14 | 1 | H19 | - | CONN HEADER 6 POS 2.54, Header_6x_100mils | Wurth Electronics Inc. | 61300611121 |
| 15 | 2 | H21, J5 | - | CONN HEADER 3 POS 2.54mm, Header_3x_100mils | Wurth Electronics Inc. | 61300311121 |
| 16 | 1 | IC1 | - | Power Management IC, QFN44_5x6 | ST | STPMIC1A |

| Item | Q.ty | Ref. | Part / Value | Description | Manufacturer | Order code |
|---|---|---|---|---|---|---|
| 17 | 4 | J1, J2, J3, J4 | - | CONN HEADER 3 POS 2.54mm, Header_3x_100mils | Wurth Electronics Inc. | 61300311121 |
| 18 | 5 | LX1, LX2, LX3, LX4, LX5 | 1.0µH, 3.5A, 42mΩ | FIXED IND SMD, L-2512 | Murata | DFE252012P-1R0M=P2 |
| 19 | 1 | R1 | 1K, 1/4W, ±5% | RES SMD 0603, R-0603 | Rohm Semiconductor | ESR03EZPJ102 |
| 20 | 1 | R2 | 10K, 1/4W, ±5% | RES SMD 0603, R-0603 | Rohm Semiconductor | ESR03EZPJ103 |
| 21 | 3 | R3, R4, R5 | 2K2, 1/10W, ±1% | RES SMD 0603, R-0603 | Rohm Semiconductor | KTR03EZPF2201 |
| 22 | 4 | J1, J2, J3, J4 J1, J2 - pin 1-2 J2, J3 - pin 2-3 | - | JUMPER SKT OPEN TOP BLACK | Harwin Inc. | M7582-46 |

# 6 PCB layout

The following table shows the layer stack-up for the signals and power tracks.

**Table 7. Four-layer Stack-UP**

| Layer | Stack-up |
|---|---|
| Top Layer | Component and signal |
| Mid Signal 1 | GND |
| Mid Signal 2 | POWER and GND |
| Bottom Layer | Small signal and feedback |

The following figures show the layouts of the various layers in the STEVAL-PMIC1K1 evaluation board.

**Figure 14. STEVAL-PMIC1K1 assembly layer**

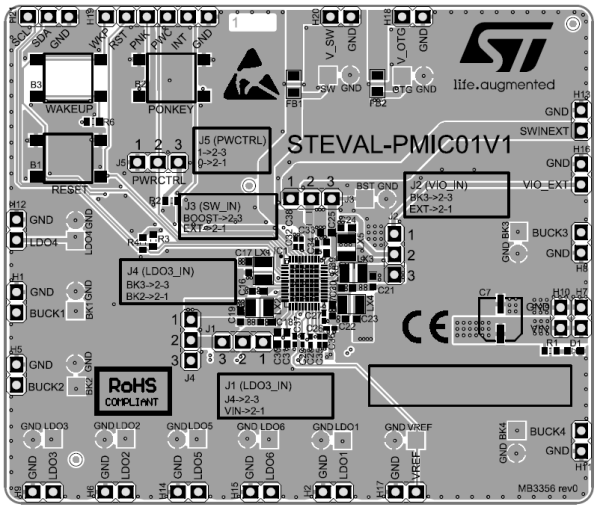



**Figure 15. STEVAL-PMIC1K1 top layer**

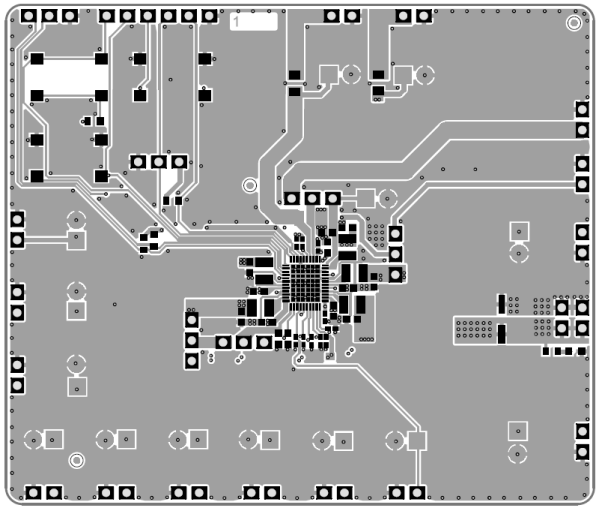


Figure 16. **STEVAL-PMIC1K1 mid layer 1**

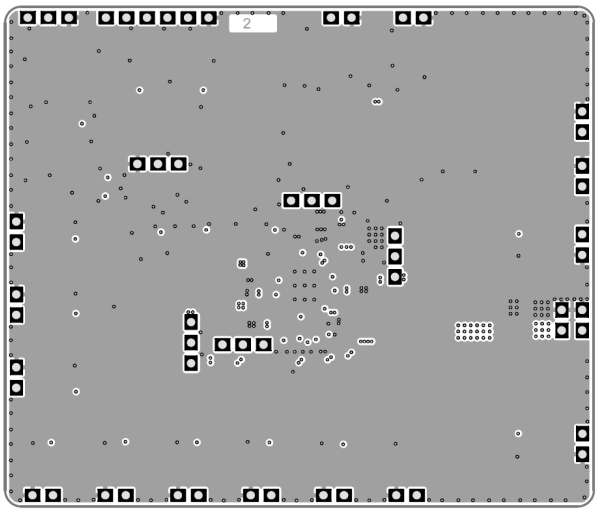



Figure 17. **STEVAL-PMIC1K1 mid layer 2**

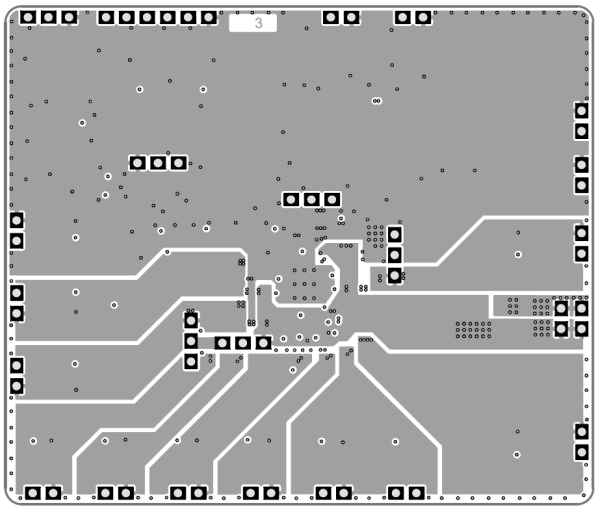
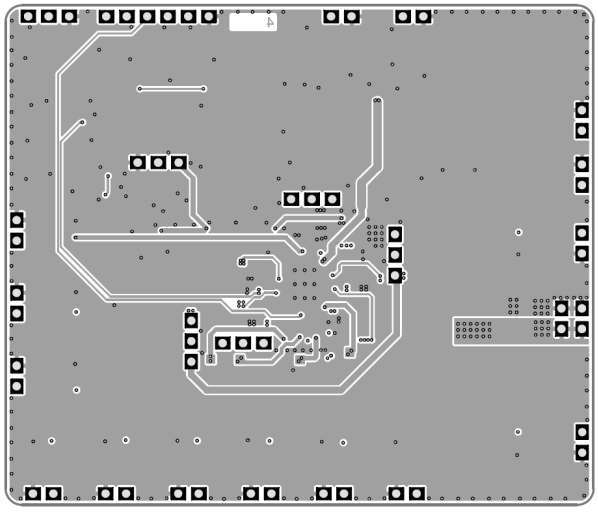



Figure 18. **STEVAL-PMIC1K1 bottom layer**



# Revision history

Table 8. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 12-Nov-2019 | 1 | Initial release. |

# Contents

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