Click here for production status of specific part numbers.

MAX5861

DOCSIS 3.1 High-Density SCQAM and OFDM Downstream Cable Modulator

General Description

The MAX5861 is an integrated, high-density, SCQAM and OFDM downstream cable modulator, digital up-converter (DUC) and RF digital-to-analog converter (RF-DAC). The MAX5861 is DOCSIS 3.1-compliant and is optimized for converged cable access platform (CCAP) hardware. The MAX5861 performs baseband I/Q symbols to RF up-conversion to digitally synthesize a selectable combination of SCQAM and OFDM blocks on a single RF port. A combination of up to six 192MHz blocks of SCQAM or OFDM channels can be powered on at any one time, where a block is defined as either 32 X 6MHz (or 24 X 8MHz) SCQAM channels or an OFDM channel (up to 192MHz wide). The MAX5861 features three differential time-multiplexed input data ports that support LVDS or SSTL 1.2/1.5 in DDR mode.

The MAX5861 SCQAM input port A accepts 10-bit Forward Error Correction (FEC)-encoded data for up to 160 (6MHz) individually programmable channels. The SCQAM path performs QAM mapping, root raised cosine (RRC) pulse shaping, and resampling, compliant with ITU-T J.83 Annex A, B, and C. This port also supports 1024-QAM with the use of an offset bias bit. Up to four channels can be operated in RRC filter bypass mode at up to 2.5Msym/s for legacy communications to older generation devices.

Each of two available 9-bit OFDM ports, B or C, support up to three 12-bit OFDM IFFT-processing channels. Each IFFT-processing channel supports OFDM blocks of up to 192MHz bandwidth with selectable 4k or 8k subcarriers and up to 4096-QAM modulation options. Each of the two OFDM ports also allow bypassing of the IFFT processing with a single 18-bit I/Q data path to support user-defined modulation at up to 192MHz bandwidth.

A cascade of interpolation filters, complex modulators, channel combiners and Direct Digital Frequency Synthesizers (DDFS) up-convert the SCQAM and/or OFDM signals with full frequency agility from 43MHz to 1218MHz. The up-converted spectrum is fed to a Digital Pre-Distortion (DPD) block to compensate for distortion performance limitations in the DAC and external output amplifiers.

***Ordering Information* appears at end of data sheet.**

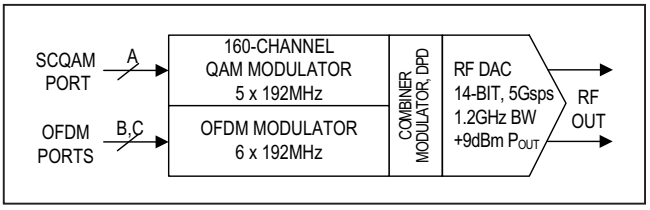
Benefits and Features

- High-Density Cable Downstream Modulator
  - Combine Up to Six 192MHz Blocks of 32 x 6MHz SCQAM Channels and DOCSIS 3.1 OFDM Channels
  - Integrated 14-Bit 4.9152Gsps RF-DAC
- Highly Flexible and Configurable
  - ITU-T J.83 Annex A, B, and C SCQAM Channels
  - IFFT Processing D3.1 OFDM Channels
  - LVDS or SSTL 1.2/1.5 DDR Data Ports
  - One 10-Bit SCQAM Port with 160-Channel Capacity
  - Two 9-Bit OFDM Ports with 6 OFDM-Channel Capacity
  - Channel Bandwidths:
    - 1MHz to 8MHz SCQAM
    - 24MHz/48MHz/96MHz/192MHz OFDM
    - 192MHz IFFT Bypass Mode
  - Full SCQAM Agility within 192MHz Block
  - Block Agility within 1218MHz Output Bandwidth
- Additional Features Ease RF Design
  - Programmable Digital Predistortion
  - High Output Power: 9dBm (Peak CW)
- Low-Power, Compact Solution
  - 5.9W with 128 SCQAMs + 2 OFDM Channels
  - Operating Temperature Range T_A= -40°C to T_J = +110°C
  - 12mm x 18mm, 308-Ball LFBGA

Applications

- DOCSIS 3.0/3.1 and DVB-C/C2
- CCAP, Edge QAM, CMTS
- Remote PHY, Coax Media Converters
- Multi-Dweller Units (MDU), Mini-Headends

Simplified Block Diagram



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AVDD3 to GND .....-0.5V to +3.60V
AVDD18 to GND .....-0.5V to +2.05V
AVCLK to GND .....-0.5V to +2.05V
VDD09 to GND .....-0.5V to +1.05V
VDD18 to GND .....-0.5V to +2.05V
VDD18I to GND .....-0.5V to +2.05V
VDD18O to GND .....-0.5V to +2.05V
VDD18BI to GND .....-0.5V to +2.05V
VDD18BO to GND .....-0.5V to +2.05V
Continuous Power Dissipation 10W
Ambient Temperature .....-40°C (Minimum)
Operating Junction Temperature .....+110°C (Maximum)
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

308 LFBGA

308 LFBGA Package Drawing Link

PACKAGE CODE	X30828FM+1
Outline Number	**21-0749**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	8.73
Junction-to-Case Thermal Resistance (θ_{JC})	0.86

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient Temperature			-40			°C
Junction Temperature		(Note 1)			110	°C
Junction-to-Ambient Thermal Resistance	Θ_{JA}	(Notes 2, 3 and 5)		8.73		°C/W
Junction-to-Board Thermal Resistance	Θ_{JB}	(Notes 4 and 5)		4.45		°C/W
Junction-to-Case Thermal Resistance	Θ_{JC}	(Notes 4 and 5)		0.86		°C/W
Junction-to-Top Center-of-Package Thermal Resistance	Ψ_{JT}	(Note 5)		0.20		°C/W

Note 1: Temperature measured using the on-chip thermal diode.
Note 2: Package mounted in horizontal position.
Note 3: The thermal performance of the MAX5861 SBSMFC LFBGA 18 x 12 308-lead package cannot meet thermal requirements (maximum junction temperature < 110°C) without the use of a heatsink.
Note 4: Package mounted on JEDEC standard four-layer PCB.
Note 5: Airflow at 0m/s.

Electrical Characteristics (continued)

(V_{AVDD3} = 3.3V, V_{AVDD18} = V_{VDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V, f_{CLK} = 2457.6MHz, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Electrical Characteristics / CMOS LOGIC INPUTS						
High-Level Input Voltage	V_{IH}		1.17			V
Low-Level Input Voltage	V_{IL}				0.63	V
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{VDD18}	-10	±1	+10	µA
DC Electrical Characteristics / CMOS LOGIC OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA	1.35			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA			0.45	V
High-Impedance Output Current	I_{OZ}	0V < V_{OUT} < V_{VDD18}	-10		+10	µA
DC Electrical Characteristics / DIFFERENTIAL LOGIC INPUTS CONFIGURED FOR LVDS COMPATIBILITY						
High-Level Differential Input Voltage	$V_{IH,LVDS}$	(Note 15)	100			mV
Low-Level Differential Input Voltage	$V_{IL,LVDS}$	(Note 15)			-100	mV
Input Common-Mode Voltage	$V_{ICM,LVDS}$	(Note 15)	1	1.25	1.425	V
Differential Input Resistance	$R_{IN,LVDS}$			100		Ω
Input Capacitance	$C_{IN,LVDS}$			3		pF
DC Electrical Characteristics / DIFFERENTIAL LOGIC INPUTS CONFIGURED FOR SSTL 1.5V COMPATIBILITY						
High-Level Differential Input Voltage	$V_{IH,SSTL15}$	(Notes 2 and 15)	100			mV
Low-Level Differential Input Voltage	$V_{IL,SSTL15}$	(Notes 2 and 15)			-100	mV
Input Common-Mode Voltage	$V_{IX,SSTL15}$		0.55	0.75	0.95	V
Differential Input Resistance	$R_{IN,SSTL15}$			100		Ω
Input Capacitance	$C_{IN,SSTL15}$			3		pF
DC Electrical Characteristics / DIFFERENTIAL LOGIC INPUTS CONFIGURED FOR SSTL 1.2V COMPATIBILITY						
High-Level Differential Input Voltage	$V_{IH,SSTL12}$	(Notes 2 and 15)	100			mV
Low-Level Differential Input Voltage	$V_{IL,SSTL12}$	(Notes 2 and 15)			-100	mV
Input Common-Mode Voltage	$V_{IX,SSTL12}$		0.41	0.60	0.79	V
Differential Input Resistance	$R_{IN,SSTL12}$			100		Ω
Input Capacitance	$C_{IN,SSTL12}$			3		pF

Electrical Characteristics (continued)

(V_{AVDD3} = 3.3V, V_{AVDD18} = V_{VDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V, f_{CLK} = 2457.6MHz, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Electrical Characteristics / DIFFERENTIAL OUTPUTS CONFIGURED FOR LVDS COMPATIBILITY						
High-Level Differential Output Voltage	$V_{OH,LVDS}$	External load = 100Ω (Note 15)	250	350	450	mV
Low-Level Differential Output Voltage	$V_{OL,LVDS}$	External load = 100Ω (Note 15)	-450	-350	-250	mV
Common-Mode Output Voltage	$V_{OCM,LVDS}$	External load = 100Ω (Note 15)	1.120	1.25	1.375	V
Differential Output Resistance	$R_{OUT,LVDS}$	In high-current mode only		100		Ω
DC Electrical Characteristics / DIFFERENTIAL LOGIC OUTPUTS CONFIGURED FOR SSTL 1.5V COMPATIBILITY						
High-Level Differential Output Voltage	$V_{OH,SSTL15}$	(Notes 2 and 15) (Note 3 for SSTL termination)	250	350	470	mV
Low-Level Differential Output Voltage	$V_{OL,SSTL15}$	(Notes 2 and 15) (Note 3 for SSTL termination)	-470	-350	-250	mV
Differential Output Resistance	$R_{OUT,SSTL12}$	In high-current mode only (Reg 0x000[1] = 1)		100		Ω
DC Electrical Characteristics / DIFFERENTIAL LOGIC OUTPUTS CONFIGURED FOR SSTL 1.2V COMPATIBILITY						
High-Level Differential Output Voltage	$V_{OH,SSTL12}$	(Notes 2 and 15) (Note 3 for SSTL termination)	250	350	470	mV
Low-Level Differential Output Voltage	$V_{OL,SSTL12}$	(Notes 2 and 15) (Note 3 for SSTL termination)	-470	-350	-250	mV
Differential Output Resistance	$R_{OUT,SSTL12}$	In high-current mode only (Reg 0x000[0] = 1)		100		Ω
DC Electrical Characteristics / POWER SUPPLIES						
Analog Supply Voltage Range	V_{AVDD3}		3.2	3.3	3.5	V
Clock Supply Voltage Range	AVCLK		1.8	1.85	1.9	V
DAC 1.8V Supply Voltage Range	AVDD18		1.7	1.8	1.9	V
Analog Clock Supply and DAC 1.8V Supply Relationship	AVCLK - AVDD18		0	50	100	mV
1.8V Supply Voltage Range	VDD18	Includes VDD18I, VDD18O, VDD18BI, and VDD18BO	1.7	1.8	1.9	V
Core Supply Voltage Range	VDD09	(Note 12)	0.9	0.9	0.99	V
Analog Supply Current	I_{AVDD33}	f_{DAC} = 4915.2Msps, f_{OUT} = 400MHz, 8 SCQAM (Note 4)		335	370	mA
Clock Supply Current	I_{AVCLK}	f_{DAC} = 4915.2Msps, f_{OUT} = 400MHz, 8 SCQAM (Note 4)		550	600	mA

Electrical Characteristics (continued)

(V_{AVDD3} = 3.3V, V_{AVDD18} = V_{VDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V, f_{CLK} = 2457.6MHz, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC 1.8V Supply Current	I_{AVDD18}	f_{DAC} = 4915.2Msps, f_{OUT} = 400MHz, 8 SCQAM (Note 4)		250	310	mA
Digital 1.8V Supply Current	I_{VDD18}	External PRBS data on ports A, B, and C, SDCLK = 409.6MHz, PCLK = 633MHz, LVDS mode. Includes VDD18, VDD18I, VDD18O, VDD18BI, and VDD18BO. 8 SC-QAM + 2 OFDM (OFDM Ch 1 and Ch 2)		286	450	mA
Active Core Supply Current (Note 13)	I_{VDD09}	Current is measured using internal PRBS generators as the source, configured for 24 SCQAM + 2 OFDM channels (OFDM Ch 1 and Ch 2)		1750	3500	mA
		Current is measured using internal PRBS generators as the source, configured for 128 SCQAM + 2 OFDM channels (OFDM Ch 1 and Ch 2)		2975	5800	
Standby Core Supply Current	I_{VDD09B}	RST_N = 0, SCLK = 0MHz, PCLK = 633MHz, SDCLK = 409.6MHz		600		mA
Static Core Supply Current	$I_{VDD09ST}$	RST_N = 0, SCLK = 0MHz, CLKP/N = 0MHz, PCLK = 0MHz and SDCLK = 0MHz (Note 14)		575		mA
Minimum Power-Down Core Supply Current (All Internal 192MHz Blocks Powered Down)	$I_{VDD09PD}$	RST_N = 1, SCLK = 0MHz, PCLK = 633MHz, SDCLK = 409.6MHz, all eleven blocks in PWR_CFG2 (0x008) turned off by SPI command or CFG pin configuration		700		mA
Total Operating Power Dissipation	P_{DISS}	Using internal PRBS generators as the source, configured for 128 SCQAM + 2 OFDM Channels (OFDM Ch 1 and Ch 2)		5.9	8.2	W
AC Electrical Characteristics / DAC STATIC PERFORMANCE						
Resolution				14		Bits
Full-Scale Output Current Range	I_{OUT}	(Note 8)	10		80	mA
Full-Scale Output Power	P_{OUT}	Differential, into 50Ω load, f_{OUT} = 103.5MHz		9		dBm
Output-Power Gain Error	GE		-0.7		0.7	dB
Output Power Drift		Internal reference		-0.003		dB/°C
		External reference		-0.0025		
Output Resistance	R_{OUT}	Differential		50		Ω

Electrical Characteristics (continued)

(V_{AVDD3} = 3.3V, V_{AVDD18} = V_{VDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V, f_{CLK} = 2457.6MHz, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC Electrical Characteristics / DAC DYNAMIC PERFORMANCE (Note 4)						
DAC Clock Rate	f_{CLK}				2457.6	MHz
DAC Output Update Rate	f_{DAC}				4915.2	MHz
Out-of-Band Noise and Spurious, Eight 6MHz SCQAM Carriers, Average Total Power = -14.3dBFS	ACPR400 (f_{OUT} = 400MHz)	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)	-64	-70		dBc
		Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)	-65.8	-71		
		Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)	-66	-71		
		Noise in any other channel (Note 9)		-67		
	ACPR860 (f_{OUT} = 860MHz)	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-67		
		Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-66		
		Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-66		
		Noise in any other channel (Note 9)		-66		
	ACPR1194 (f_{OUT} = 1194MHz)	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-65		
		Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-65		
		Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-65		
		Noise in any other channel (Note 9)		-65		
Harmonic Distortion, Block of Four 6MHz SCQAM Carriers, Average Total Power = -12.7dBFS	HD300 (f_{OUT} = 300MHz)	In each of eight 6MHz channels coinciding with 2nd harmonic components		-72	-64	dBc
		In each of twelve 6MHz channels coinciding with 3rd harmonic components		-72	-65	
Gain Flatness	GF	Over any single 6MHz channel		0.05		dB
		Within 45MHz to 1218MHz band		2		

Electrical Characteristics (continued)

(V_{AVDD3} = 3.3V, V_{AVDD18} = V_{VDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V, f_{CLK} = 2457.6MHz, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Spurs		f_{DAC}/4 Spur, 8 SCQAM carriers		-80		dBm
		f_{DAC}/8 Spur, 8 SCQAM carriers		-100		
f_{DAC}/2 - f_{OUT} Image		8 SCQAM carriers covering the band from 1170MHz to 1218MHz, no DPD correction		-30		dBc
		8 SCQAM carriers covering the band from 1170MHz to 1218MHz, with DPD correction		-63		
f_{DAC}/2 - 2f_{OUT} Spurious		8 SCQAM carriers covering the band from 1170MHz to 1218MHz, no DPD correction		-63		dBc
		8 SCQAM carriers covering the band from 1170MHz to 1218MHz, with DPD correction		-68		
AC Electrical Characteristics / BIAS REFERENCE						
Internal Reference Voltage Range	V_{REFIO}		1.1	1.2	1.3	V
Reference Input Voltage Compliance Range	V_{REFIOR}		0.5		1.8	V
Reference Input Resistance	R_{REFIO}			10		kΩ
Reference Voltage Drift	TCO_{REF}	T_A = -40ºC, T_J = +110ºC		50		ppm/°C
AC Electrical Characteristics / AC CLOCK INPUTS (CLKP, CLKN)						
Minimum Clock Input Power	$P_{CLK,MIN}$	(Note 5)		6		dBm
Maximum Clock Input Power	$P_{CLK,MAX}$	Power measured into clock input with 100Ω external differential termination resistor		12		dBm
Common-Mode Voltage	V_{COMCLK}	Input is self-biased		ACLK/3		V
Input Resistance	R_{CLK}	Differential		100		Ω
Input Capacitance	C_{CLK}			2		pF
AC Electrical Characteristics / DIFFERENTIAL LOGIC INPUTS CONFIGURED FOR SSTL 1.5V COMPATIBILITY (Note 6)						
High-Level Differential Input Voltage	$V_{IH,SSTL15(AC)}$			300		mV
Low-Level Differential Input Voltage	$V_{IL,SSTL15(AC)}$			-300		mV
AC Electrical Characteristics / DIFFERENTIAL LOGIC INPUTS CONFIGURED FOR SSTL 1.2V COMPATIBILITY (Note 6)						
High-Level Differential Input Voltage	$V_{IH,SSTL12(AC)}$			300		mV
Low-Level Differential Input Voltage	$V_{IL,SSTL12(AC)}$			-300		mV

Electrical Characteristics (continued)

(V_{AVDD3} = 3.3V, V_{AVDD18} = V_{VDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V, f_{CLK} = 2457.6MHz, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC Electrical Characteristics / LVDS PORT CLOCK INPUT (PCLK)						
Clock Frequency	f_{PCLK}	$1/t_{TP}$ (Note 7)			633	MHz
Input Capacitance				3		pF
Clock Duty Cycle				50 ±5		%
AC Electrical Characteristics / LVDS DATA INPUTS						
Input Capacitance				3		pF
Input Resistance	R_{CLK}	Differential		100		Ω
AC Electrical Characteristics / SERIAL PORT INTERFACE TIMING (SCLK, SDI, SDO, CS_n)						
SCLK Frequency	f_{SCLK}				60	MHz
CS_n Setup Time	t_{SS}	(Note 6)		5		ns
Input Hold Time	t_{SDH}	(Note 6)		0		ns
Input Setup Time	t_{SDS}	(Note 6)		3.5		ns
Data Valid Duration	t_{SDV}	(Note 6)		7.5		ns
AC Electrical Characteristics / TIMING CHARACTERISTICS						
DAC DLL Frequency Range	f_{DLL}	$f_{DLL} = f_{CLK}/2$ GDLLOFF[1:0]=10, GDELAY[1:0]=11	1075		1228.8	MHz
		$f_{DLL} = f_{CLK}/2$ GDLLOFF[1:0]=10, GDELAY[1:0]=00	950		1075	
Parity Error Pulse Width	t_{ERR}	Pulse width of PERR when a parity error is detected		48		Data Clock Cycles
Output Data Latency	t_{DL}	SCQAM, f_{DAC} = 4915.2MHz, default delay values		2.33		ms
		OFDM, 4k IFFT, NCP = 1024, SDCLK = 409.6MHz, f_{DAC} = 4915.2MHz		38.5		µs
AC Electrical Characteristics / ANALOG OUTPUT TIMING						
Output Bandwidth	BW	(Note 11)		2		GHz
AC Electrical Characteristics / PORT A DATA SETUP/HOLD (PCLK)						
Data Setup		All Port A input signals		123		ps
Data Hold		All Port A input signals		63		ps
AC Electrical Characteristics / PORT A OUTPUT SKEW						
Output Data Skew		All Port A output signals		148		ps
AC Electrical Characteristics / PORT B/C DATA SETUP/HOLD (SDCLK)						
Data Setup		All Port B/C input signals		181		ps
Data Hold		All Port B/C input signals		148		ps
AC Electrical Characteristics / PORT B/C CLOCK INPUT (SDCLK)						
OFDM SDCLK Rate	f_{SDCLK}	$1/t_{TP}$ (Note 7)			409.6	MHz

Electrical Characteristics (continued)

(V_{AVDD3} = 3.3V, V_{AVDD18} = V_{VDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V, f_{CLK} = 2457.6MHz, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

Note 1: All specifications are 100% tested at T_J = +65°C and T_J = +110°C with an accuracy of ±15°C. Specifications at T_J < +65°C are guaranteed by design and characterization.

Note 2: When using SSTL levels, maximum recommended PCB routing separation between MAX5861 differential I/O pins and source/drive differential pins is 6in. See the *IOL_CFG6* register for settings.

Note 3: Back termination circuit diagram (V_S = 1.5V or 1.2V).

Note 4: CLKP/N input = +9dBm, AC-coupled sine wave.

Note 5: Transformer-coupled clock input.

Note 6: Design guideline, not measured in production.

Note 7: A continuous clock and must not be gapped.

Note 8: Nominal full-scale current I_{OUT}= 128 x I_{REF}.

Note 9: Excludes clock, clock images, $f_{DAC}/2 - f_{OUT}$, and $f_{DAC}/2 - 2f_{OUT}$ spurs, which are specified separately.

Note 10: Measured single-ended into a double-terminated 50Ω load.

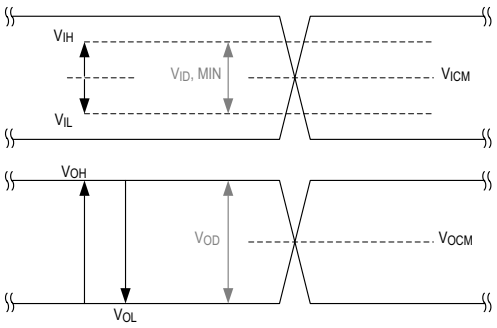
Note 11: Excludes impulse-response dependent SINC roll-off inherent in the DAC.

Note 12: Set VDD09 above 0.9V to account for device supply tolerance but keep as low as possible to minimize supply current requirement. (Do not exceed absolute maximum of 1.05V.)

Note 13: See the *Typical Operating Characteristics* section for configuration-based supply current vs. temperature graphs.

Note 14: Tested at CLKP - CLKN = -316mV.

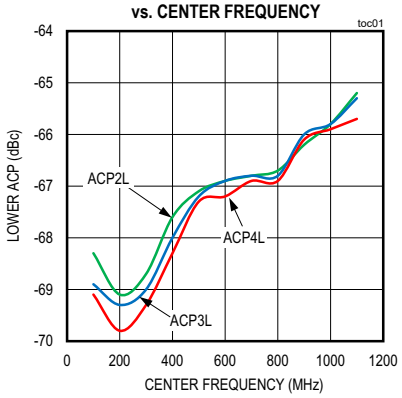
Note 15:



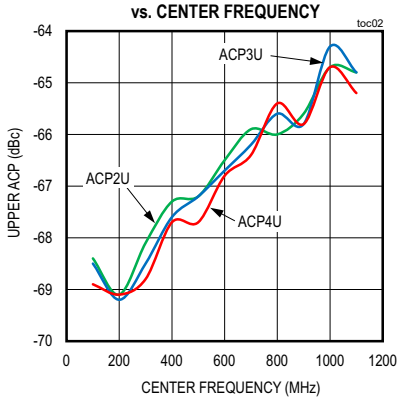
Typical Operating Characteristics

(Nominal supplies (V_{AVDD33} = 3.3V, V_{VDD18} = V_{AVDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V), T_A = +25°C, and DPD enabled, unless otherwise noted.)

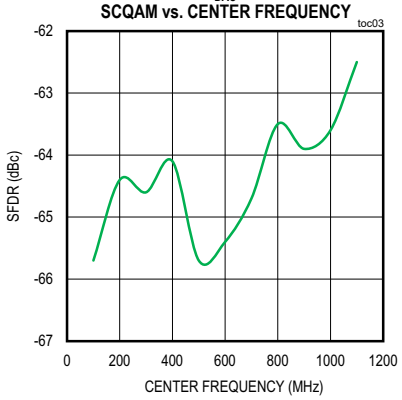
LOWER ACP (dBc) FOR 8-CHANNEL SCQAM vs. CENTER FREQUENCY



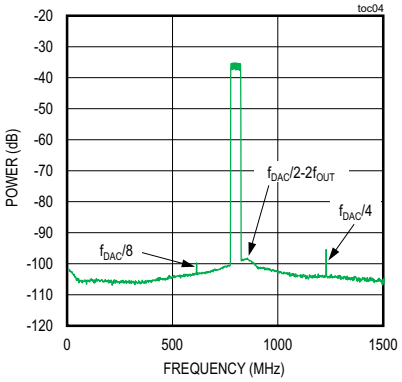
UPPER ACP (dBc) FOR 8-CHANNEL SCQAM vs. CENTER FREQUENCY



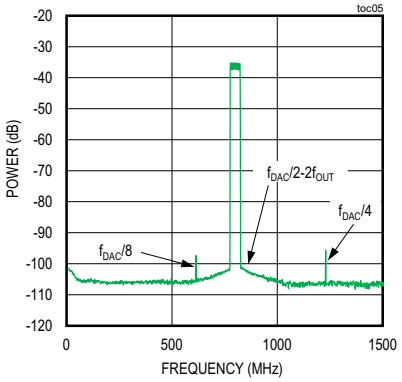
SFDR (dBc) UP TO $f_{DAC}/4$ FOR 8-CHANNEL SCQAM vs. CENTER FREQUENCY



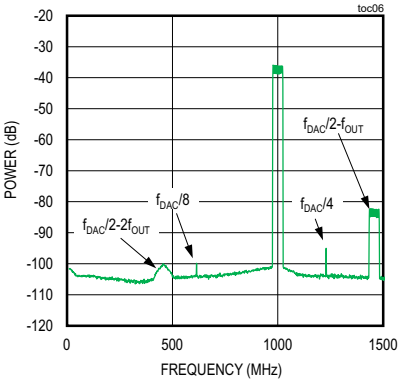
8-CHANNEL SCQAM 800MHz DPD OFF OUTPUT SPECTRUM



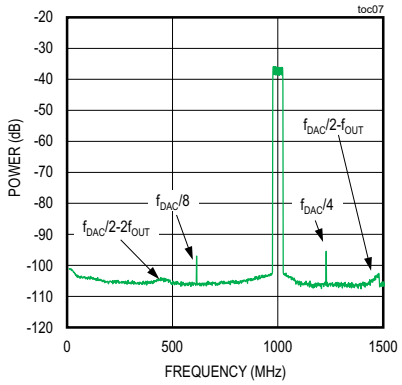
8-CHANNEL SCQAM 800MHz DPD ON OUTPUT SPECTRUM



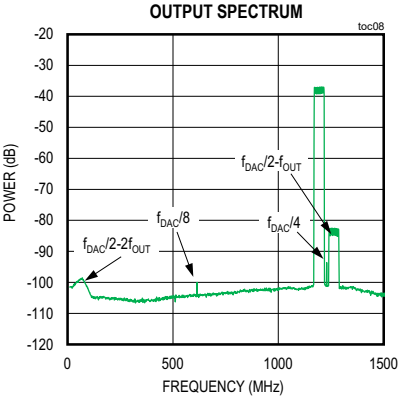
8-CHANNEL SCQAM 1000MHz DPD OFF OUTPUT SPECTRUM



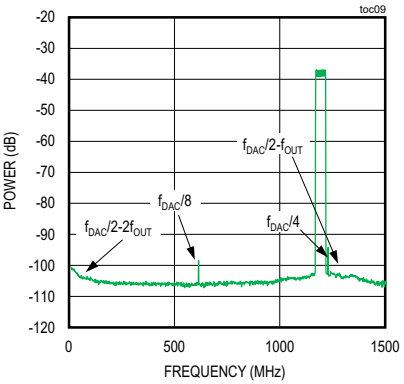
8-CHANNEL SCQAM 1000MHz DPD ON OUTPUT SPECTRUM



8-CHANNEL SCQAM 1194MHz DPD OFF OUTPUT SPECTRUM



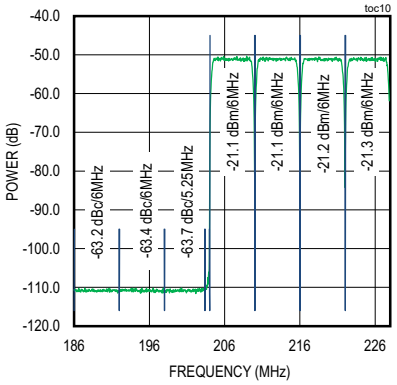
8-CHANNEL SCQAM 1194MHz DPD ON OUTPUT SPECTRUM



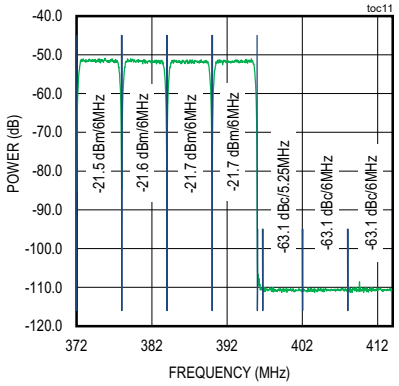
Typical Operating Characteristics (continued)

(Nominal supplies (V_{AVDD33} = 3.3V, V_{VDD18} = V_{AVDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V), T_A = +25°C, and DPD enabled, unless otherwise noted.)

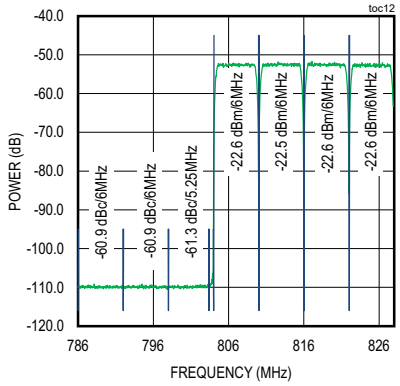
32-CHANNEL 256QAM
LOWER ACP FOR CF = 300MHz



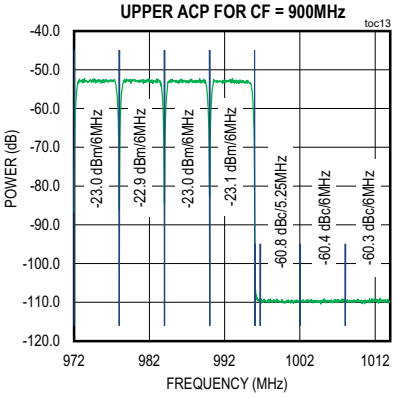
32-CHANNEL 256QAM
UPPER ACP FOR CF = 300MHz



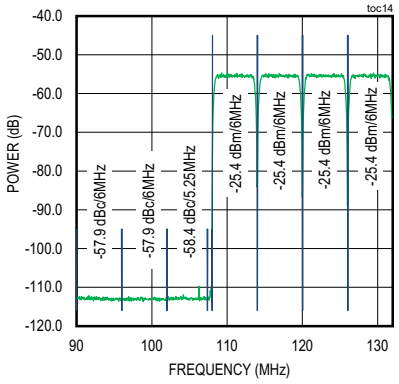
32-CHANNEL 256QAM
LOWER ACP FOR CF = 900MHz



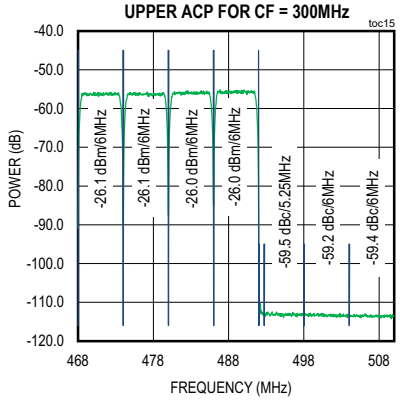
32-CHANNEL 256 QAM
UPPER ACP FOR CF = 900MHz



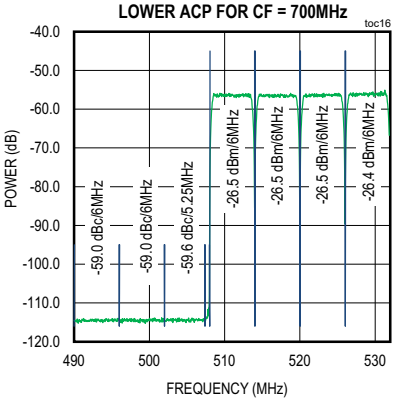
64-CHANNEL 256 QAM
LOWER ACP FOR CF=300MHz



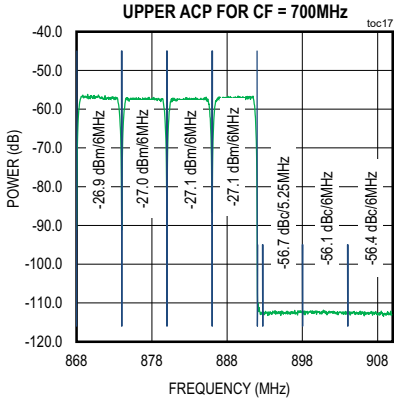
64-CHANNEL 256 QAM
UPPER ACP FOR CF = 300MHz



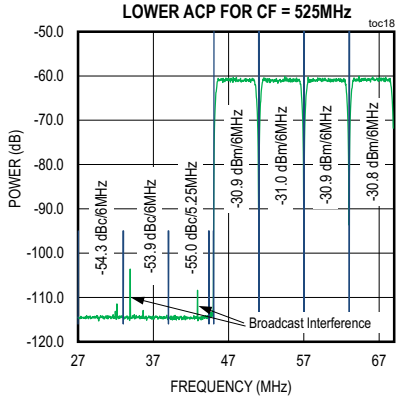
64-CHANNEL 256 QAM
LOWER ACP FOR CF = 700MHz



64-CHANNEL 256 QAM
UPPER ACP FOR CF = 700MHz



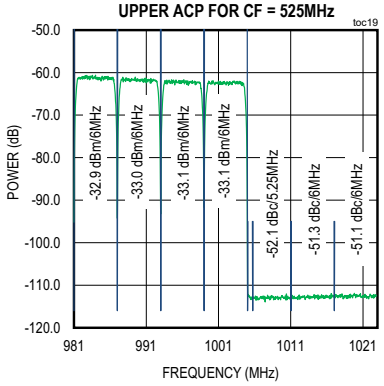
160-CHANNEL 256 QAM
LOWER ACP FOR CF = 525MHz



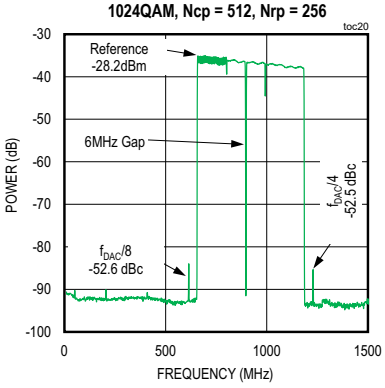
Typical Operating Characteristics (continued)

(Nominal supplies (V_{AVDD33} = 3.3V, V_{VDD18} = V_{AVDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V), T_A = +25°C, and DPD enabled, unless otherwise noted.)

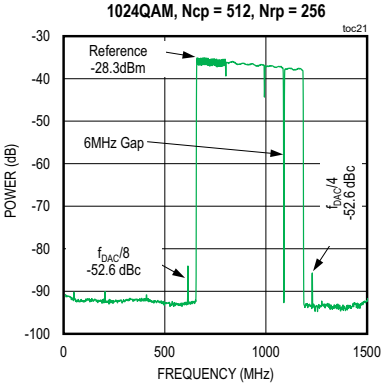
160-CHANNEL 256 QAM
UPPER ACP FOR CF = 525MHz



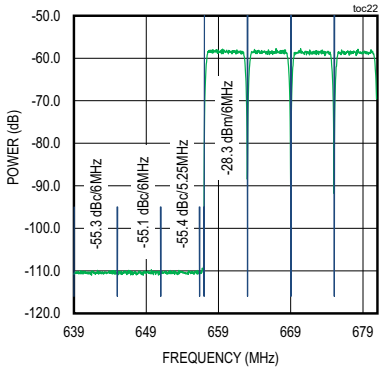
24x 256QAM ANNEX B + 2x 192MHz WIDE OFDM
1024QAM, Ncp = 512, Nrp = 256



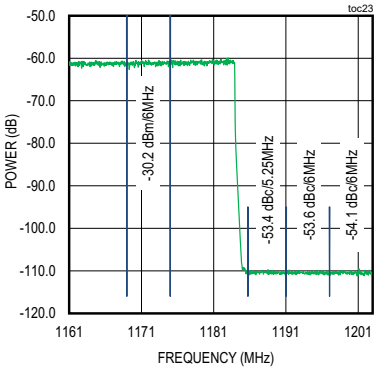
24x 256QAM ANNEX B + 2x 192MHz WIDE OFDM
1024QAM, Ncp = 512, Nrp = 256



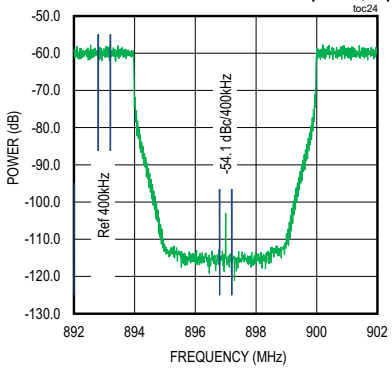
LOWER ACP FOR MIXED 2OFDM + 24SCQAM CF = 921MHz
OFDM 192MHz 1024 QAM Ncp = 512, Nrp = 256



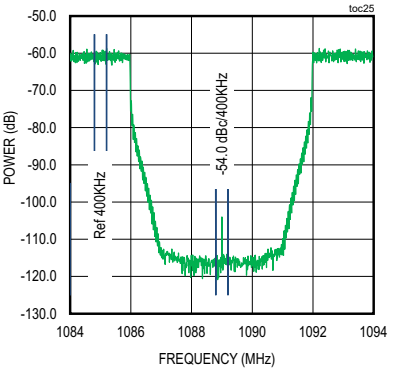
UPPER ACP FOR MIXED 2OFDM + 24 SCQAM CF = 921MHz
OFDM 192MHz 1024 QAM Ncp = 512, Nrp = 256



GAP SUBCARRIER POWER FOR MIXED 2OFDM + 24 SCQAM
CF = 921MHz OFDM 192MHz 1024 QAM Ncp = 512, Nrp = 256



GAP SUBCARRIER POWER FOR MIXED 2OFDM + 24 SCQAM
CF = 921MHz OFDM 192MHz 1024 QAM Ncp = 512, Nrp = 256

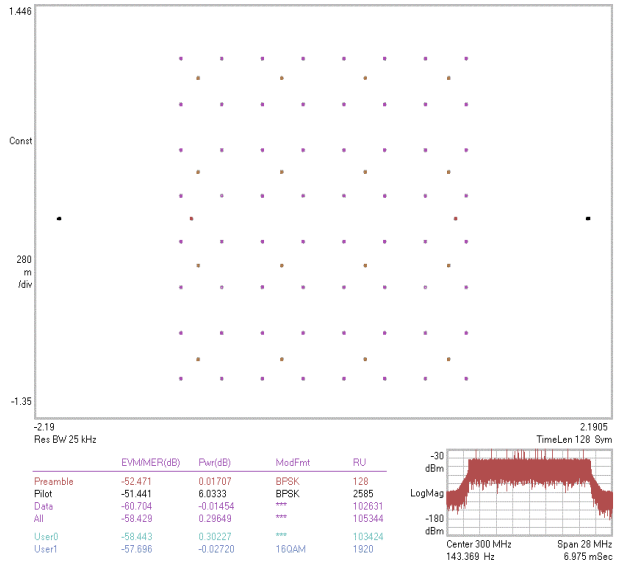


Typical Operating Characteristics (continued)

(Nominal supplies (V_{AVDD33} = 3.3V, V_{VDD18} = V_{AVDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V), T_A = +25°C, and DPD enabled, unless otherwise noted.)

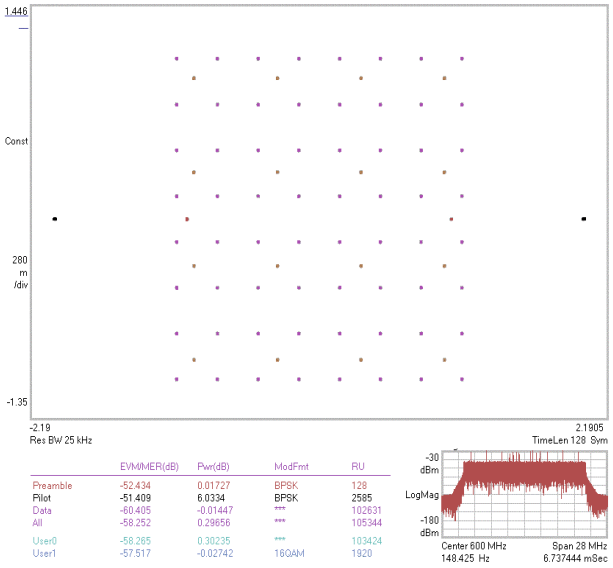
MER FOR 24MHz OFDM 64 QAM 25kHz SPACING
Ncp = 1024, Nrp = 128, CF = 300MHz

toc26



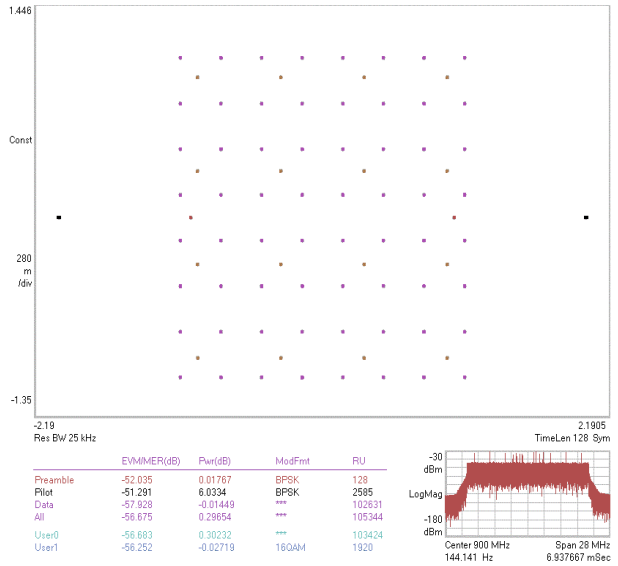
MER FOR 24MHz OFDM 64 QAM 25kHz SPACING
Ncp = 1024, Nrp = 128, CF = 600MHz

toc27



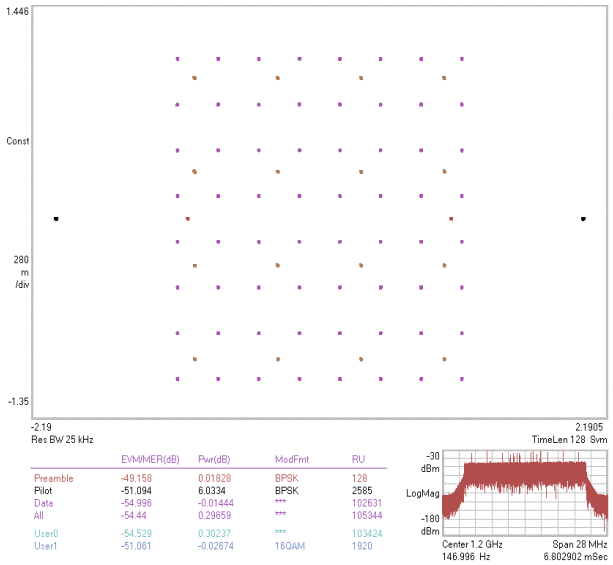
MER FOR 24MHz OFDM 64 QAM 25kHz SPACING
Ncp = 1024, Nrp = 128, CF = 900MHz

toc28



MER FOR 24MHz OFDM 64 QAM 25kHz SPACING
Ncp = 1024, Nrp = 128, CF = 1200MHz

toc29

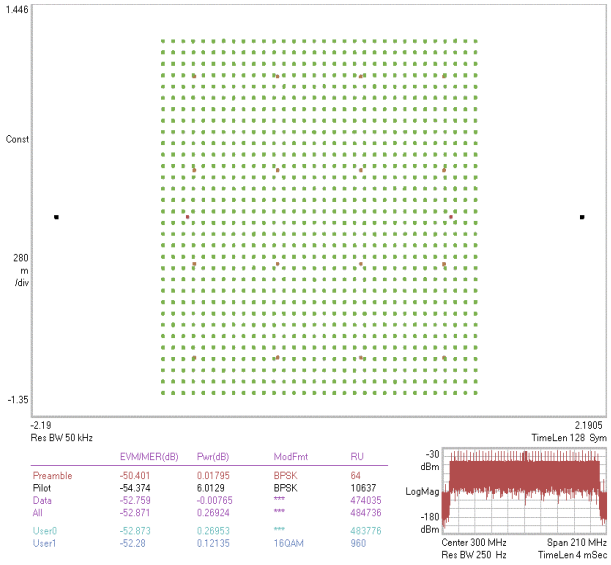


Typical Operating Characteristics (continued)

(Nominal supplies (V_{AVDD33} = 3.3V, V_{VDD18} = V_{AVDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V), T_A = +25°C, and DPD enabled, unless otherwise noted.)

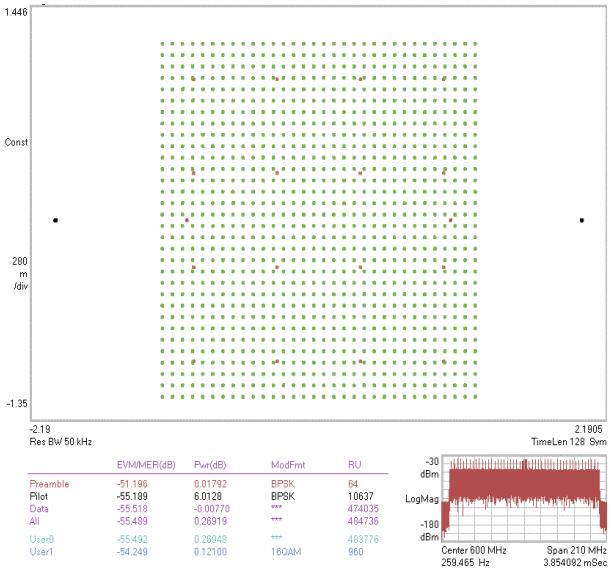
MER FOR 192MHz OFDM 1024 QAM 50kHz SPACING
Ncp = 1024, Nrp = 192, CF = 300MHz

toc30



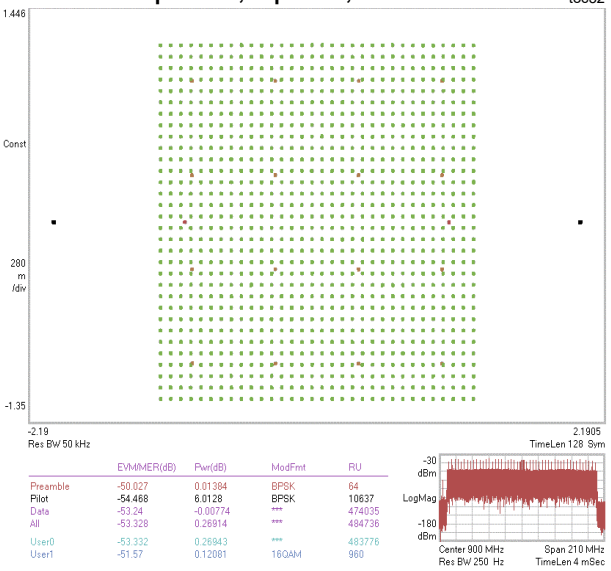
MER FOR 192MHz OFDM 1024QAM 50kHz SPACING
Ncp = 1024, Nrp = 192, CF = 600MHz

toc31



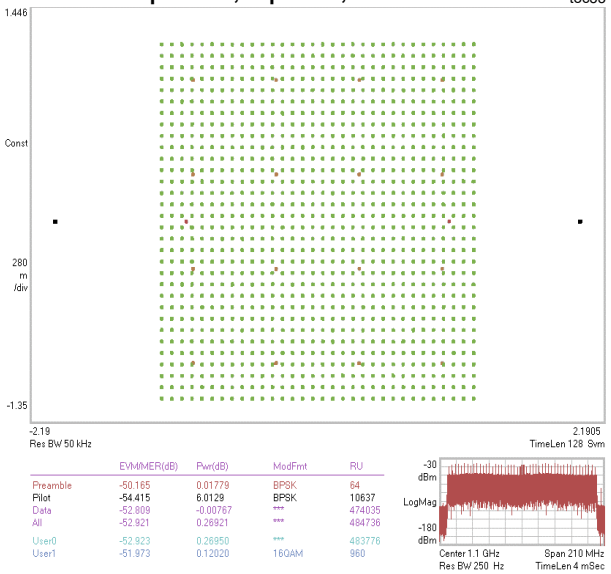
MER FOR 192MHz OFDM 1024QAM 50kHz SPACING
Ncp = 1024, Nrp = 192, CF = 900MHz

toc32



MER FOR 192MHz OFDM 1024QAM 50kHz SPACING
Ncp = 1024, Nrp = 192, CF = 1100MHz

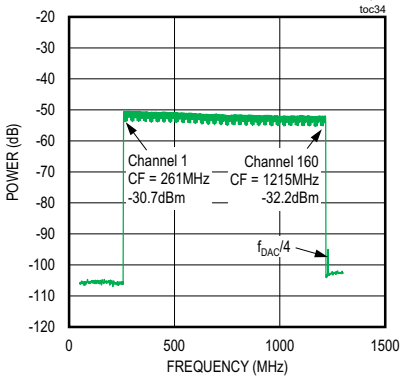
toc33



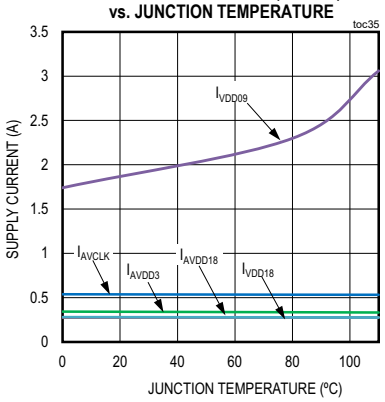
Typical Operating Characteristics (continued)

(Nominal supplies (V_{AVDD33} = 3.3V, V_{VDD18} = V_{AVDD18} = 1.8V, V_{AVCLK} = 1.85V, V_{VDD09} = 0.9V), T_A = +25°C, and DPD enabled, unless otherwise noted.)

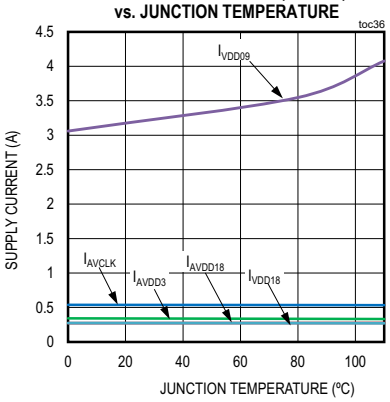
OUTPUT POWER FOR 160-CHANNEL 256QAM



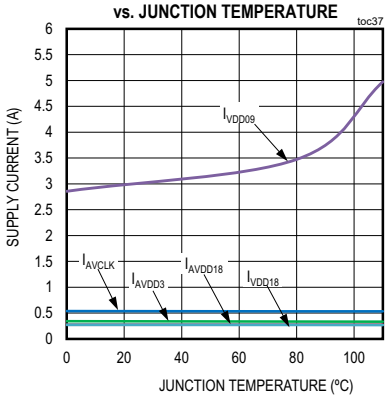
SUPPLY CURRENTS FOR 24 SCQAM AND 2OFDM (192MHz) vs. JUNCTION TEMPERATURE



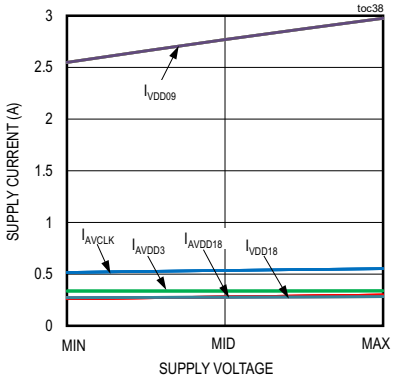
SUPPLY CURRENTS FOR 24 SCQAM AND 5OFDM (192MHz) vs. JUNCTION TEMPERATURE



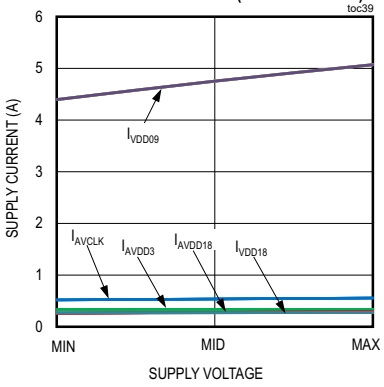
SUPPLY CURRENTS FOR 128 SCQAM AND 2OFDM (192MHz) vs. JUNCTION TEMPERATURE



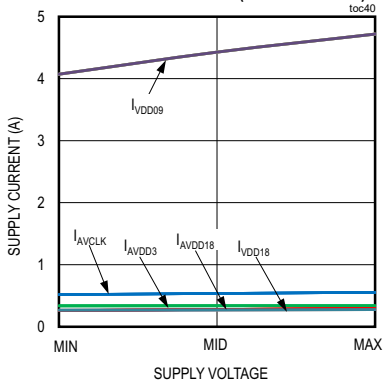
SUPPLY CURRENTS FOR 24 SCQAM AND 2OFDM (192MHz) at T_J = +80°C vs. SUPPLY VOLTAGE (MIN - MID - MAX)



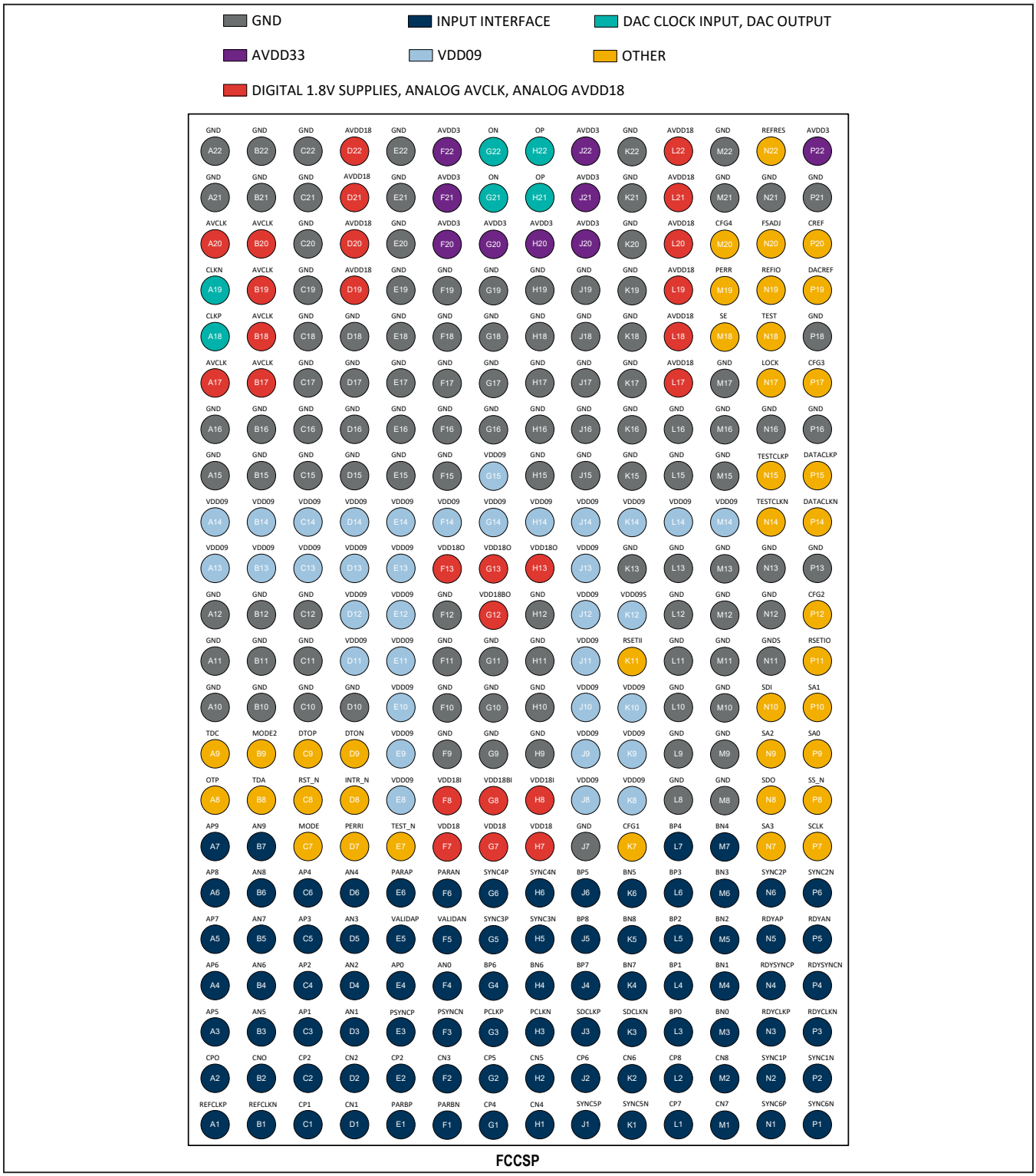
SUPPLY CURRENTS FOR 24 SCQAM AND 5OFDM (192MHz) at T_J = +80°C vs. SUPPLY VOLTAGE (MIN - MID - MAX)



SUPPLY CURRENTS FOR 128 SCQAM AND 2OFDM (192MHz) at T_J = +80°C vs. SUPPLY VOLTAGE (MIN - MID - MAX)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION	TYPE
A1	REFCLKP	OFDM Reference Clock Output (Positive)	LVDS/SSTL Output
A2	CP0	Port C Bit 0 (Positive) or OFDM Path 4 Bit 0 (Positive)	LVDS/SSTL Input
A3	AP5	SCQAM Symbol Port A Bit 5 (Positive)	LVDS/SSTL Input
A4	AP6	SCQAM Symbol Port A Bit 6 (Positive)	LVDS/SSTL Input
A5	AP7	SCQAM Symbol Port A Bit 7 (Positive)	LVDS/SSTL Input
A6	AP8	SCQAM Symbol Port A Bit 8 (Positive)	LVDS/SSTL Input
A7	AP9	SCQAM Symbol Port A Bit 9 (Positive)	LVDS/SSTL Input
A8	OTP	Manufacturing Test. Connect to ground.	Power
A9	TDC	DUC Temperature Diode Cathode. There is a 150Ω internal resistance to substrate. Connect to ground.	Analog
A10	GND		Ground
A11	GND		Ground
A12	GND		Ground
A13	VDD09	0.9V Digital Core Power Supply	Power
A14	VDD09	0.9V Digital Core Power Supply	Power
A15	GND		Ground
A16	GND		Ground
A17	AVCLK	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
A18	CLKP	Clock Input (Positive). There is an internal 100Ω termination resistor between CLKP and CLKN.	LVDS Input
A19	CLKN	Clock Input (Negative). There is an internal 100Ω termination resistor between CLKP and CLKN.	LVDS Input
A20	AVCLK	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
A21	GND		Ground
A22	GND		Ground
B1	REFCLKN	OFDM Reference Clock Output (Negative)	LVDS/SSTL Output
B2	CN0	Port C Bit 0 (Negative) or OFDM Path 4 Bit 0 (Negative)	LVDS/SSTL Input
B3	AN5	SCQAM Symbol Port A Bit 5 (Negative)	LVDS/SSTL Input
B4	AN6	SCQAM Symbol Port A Bit 6 (Negative)	LVDS/SSTL Input
B5	AN7	SCQAM Symbol Port A Bit 7 (Negative)	LVDS/SSTL Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
B6	AN8	SCQAM Symbol Port A Bit 8 (Negative)	LVDS/SSTL Input
B7	AN9	SCQAM Symbol Port A Bit 9 (Negative)	LVDS/SSTL Input
B8	TDA	DUC Temperature Diode Anode Connection	Analog
B9	MODE2	Synchronization and Test Signal	CMOS Input
B10	GND		Ground
B11	GND		Ground
B12	GND		Ground
B13	VDD09	0.9V Digital Core Power Supply	Power
B14	VDD09	0.9V Digital Core Power Supply	Power
B15	GND		Ground
B16	GND		Ground
B17	AVCLK	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
B18	AVCLK	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
B19	AVCLK	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
B20	AVCLK	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
B21	GND		Ground
B22	GND		Ground
C1	CP1	Port C Bit 1 (Positive) or OFDM Path 4 Bit 1 (Positive)	LVDS/SSTL Input
C2	CP2	Port C Bit 2 (Positive) or OFDM Path 4 Bit 2 (Positive)	LVDS/SSTL Input
C3	AP1	SCQAM Symbol Port A Bit 1 (Positive)	LVDS/SSTL Input
C4	AP2	SCQAM Symbol Port A Bit 2 (Positive)	LVDS/SSTL Input
C5	AP3	SCQAM Symbol Port A Bit 3 (Positive)	LVDS/SSTL Input
C6	AP4	SCQAM Symbol Port A Bit 4 (Positive)	LVDS/SSTL Input
C7	MODE	Manufacturing Test. Connect to 1.8V.	CMOS Input
C8	RST_N	Global Digital Reset (Active Low). Pulse RST_N low for a minimum of 100ns after each power-up.	CMOS Input
C9	DTOP	Digital Test Output (Positive)	LVDS/SSTL Output
C10	GND		Ground
C11	GND		Ground
C12	GND		Ground
C13	VDD09	0.9V Digital Core Power Supply	Power
C14	VDD09	0.9V Digital Core Power Supply	Power

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
C15	GND		Ground
C16	GND		Ground
C17	GND		Ground
C18	GND		Ground
C19	GND		Ground
C20	GND		Ground
C21	GND		Ground
C22	GND		Ground
D1	CN1	Port C Bit 1 (Negative) or OFDM Path 4 Bit 1 (Negative)	LVDS/SSTL Input
D2	CN2	Port C Bit 2 (Negative) or OFDM Path 4 Bit 2 (Negative)	LVDS/SSTL Input
D3	AN1	SCQAM Symbol Port A Bit 1 (Negative)	LVDS/SSTL Input
D4	AN2	SCQAM Symbol Port A Bit 2 (Negative)	LVDS/SSTL Input
D5	AN3	SCQAM Symbol Port A Bit 3 (Negative)	LVDS/SSTL Input
D6	AN4	SCQAM Symbol Port A Bit 4 (Negative)	LVDS/SSTL Input
D7	PERRI	Input Interface Parity Error Flag for Ports A, B, and C (Combined)	CMOS Output
D8	INTR_N	Interrupt Output (Active Low)	CMOS Output
D9	DTON	Digital Test Output (Negative)	LVDS/SSTL Output
D10	GND		Ground
D11	VDD09	0.9V Digital Core Power Supply	Power
D12	VDD09	0.9V Digital Core Power Supply	Power
D13	VDD09	0.9V Digital Core Power Supply	Power
D14	VDD09	0.9V Digital Core Power Supply	Power
D15	GND		Ground
D16	GND		Ground
D17	GND		Ground
D18	GND		Ground
D19	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
D20	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
D21	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
D22	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
E1	PARBCP	OFDM Symbol Port Parity Input (Positive). Parity input shared with port B and port C.	LVDS/SSTL Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
E2	CP3	Port C Bit 3 (Positive) or OFDM Path 5 Bit 0 (Positive)	LVDS/SSTL Input
E3	PSYNCP	SCQAM Symbol Port A SYNC Input (Positive)	LVDS/SSTL Input
E4	AP0	SCQAM Symbol Port A Bit 0 (Positive)	LVDS/SSTL Input
E5	VALIDAP	SCQAM Symbol Port A VALID Input (Positive)	LVDS/SSTL Input
E6	PARAP	SCQAM Symbol Port A Parity Input (Positive)	LVDS/SSTL Input
E7	TEST_N	Manufacturing Test. Connect to 1.8V	CMOS Input
E8	VDD09	0.9V Digital Core Power Supply	Power
E9	VDD09	0.9V Digital Core Power Supply	Power
E10	VDD09	0.9V Digital Core Power Supply	Power
E11	VDD09	0.9V Digital Core Power Supply	Power
E12	VDD09	0.9V Digital Core Power Supply	Power
E13	VDD09	0.9V Digital Core Power Supply	Power
E14	VDD09	0.9V Digital Core Power Supply	Power
E15	GND		Ground
E16	GND		Ground
E17	GND		Ground
E18	GND		Ground
E19	GND		Ground
E20	GND		Ground
E21	GND		Ground
E22	GND		Ground
F1	PARBCN	OFDM Symbol Port Parity Input (Negative). Parity input shared with port B and port C.	LVDS/SSTL Input
F2	CN3	Port C Bit 3 (Negative) or OFDM Path 5 Bit 0 (Negative)	LVDS/SSTL Input
F3	PSYNCN	SCQAM Symbol Port A SYNC Input (Negative)	LVDS/SSTL Input
F4	AN0	SCQAM Symbol Port A Bit 0 (Negative)	LVDS/SSTL Input
F5	VALIDAN	SCQAM Symbol Port A VALID Input (Negative)	LVDS/SSTL Input
F6	PARAN	SCQAM Symbol Port A Parity Input (Negative)	LVDS/SSTL Input
F7	VDD18	1.8V Power Supply	Power
F8	VDD18I	1.8V Power Supply	Power
F9	GND		Ground

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
F10	GND		Ground
F11	GND		Ground
F12	GND		Ground
F13	VDD18O	1.8V Power Supply	Power
F14	VDD09	0.9V Digital Core Power Supply	Power
F15	GND		Ground
F16	GND		Ground
F17	GND		Ground
F18	GND		Ground
F19	GND		Ground
F20	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power
F21	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power
F22	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power
G1	CP4	Port C Bit 4 (Positive) or OFDM Path 5 Bit 1 (Positive)	LVDS/SSTL Input
G2	CP5	Port C Bit 5 (Positive) or OFDM Path 5 Bit 2 (Positive)	LVDS/SSTL Input
G3	PCLKP	SCQAM Symbol Port CLK Input (Positive)	LVDS/SSTL Input
G4	BP6	Port B Bit 6 (Positive) or OFDM Path 3 Bit 0 (Positive)	LVDS/SSTL Input
G5	SYNC3P	OFDM Path 3 SYNC Input (Positive)	LVDS/SSTL Input
G6	SYNC4P	OFDM Path 4/Bypass Path 2 SYNC input (Positive)	LVDS/SSTL Input
G7	VDD18	1.8V Power Supply	Power
G8	VDD18BI	1.8V Power Supply	Power
G9	GND		Ground
G10	GND		Ground
G11	GND		Ground
G12	VDD18BO	1.8V Power Supply	Power
G13	VDD18O	1.8V Power Supply	Power
G14	VDD09	0.9V Digital Core Power Supply	Power
G15	VDD09	0.9V Digital Core Power Supply	Power
G16	GND		Ground
G17	GND		Ground
G18	GND		Ground
G19	GND		Ground
G20	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
G21	ON	RF DAC Output (Negative)	Differential Analog Output
G22	ON	RF DAC Output (Negative)	Differential Analog Output
H1	CN4	Port C Bit 4 (Negative) or OFDM Path 5 Bit 1 (Negative)	LVDS/SSTL Input
H2	CN5	Port C Bit 5 (Negative) or OFDM Path 5 Bit 2 (Negative)	LVDS/SSTL Input
H3	PCLKN	SCQAM Symbol Port CLK Input (Negative)	LVDS/SSTL Input
H4	BN6	Port B Bit 6 (Negative) or OFDM Path 3 Bit 0 (Negative)	LVDS/SSTL Input
H5	SYNC3N	OFDM Path 3 SYNC input	LVDS/SSTL Input
H6	SYNC4N	OFDM Path 4/Bypass Path 2 SYNC input (Negative)	LVDS/SSTL Input
H7	VDD18	1.8V Power Supply	Power
H8	VDD18I	1.8V Power Supply	Power
H9	GND		Ground
H10	GND		Ground
H11	GND		Ground
H12	GND		Ground
H13	VDD18O	1.8V Power Supply	Power
H14	VDD09	0.9V Digital Core Power Supply	Power
H15	GND		Ground
H16	GND		Ground
H17	GND		Ground
H18	GND		Ground
H19	GND		Ground
H20	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power
H21	OP	RF DAC Output (Positive)	Differential Analog Output
H22	OP	RF DAC Output (Positive)	Differential Analog Output
J1	SYNC5P	OFDM Path 5 SYNC Input (Positive)	LVDS/SSTL Input
J2	CP6	Port C Bit 6 (Positive) or OFDM Path 6 Bit 0 (Positive)	LVDS/SSTL Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
J3	SDCLKP	OFDM Path Clock Input (Positive)	LVDS/SSTL Input
J4	BP7	Port B Bit 7 (Positive) or OFDM Path 3 Bit 1 (Positive)	LVDS/SSTL Input
J5	BP8	Port B Bit 8 (Positive) or OFDM Path 3 Bit 2 (Positive)	LVDS/SSTL Input
J6	BP5	Port B Bit 5 (Positive) or OFDM Path 2 Bit 2 (Positive)	LVDS/SSTL Input
J7	GND		Ground
J8	VDD09	0.9V Digital Core Power Supply	Power
J9	VDD09	0.9V Digital Core Power Supply	Power
J10	VDD09	0.9V Digital Core Power Supply	Power
J11	VDD09	0.9V Digital Core Power Supply	Power
J12	VDD09	0.9V Digital Core Power Supply	Power
J13	VDD09	0.9V Digital Core Power Supply	Power
J14	VDD09	0.9V Digital Core Power Supply	Power
J15	GND		Ground
J16	GND		Ground
J17	GND		Ground
J18	GND		Ground
J19	GND		Ground
J20	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power
J21	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power
J22	AVDD3	3.3V Analog Power Supply. Bypass with 47nF capacitor to ground	Power
K1	SYNC5N	OFDM Path 5 SYNC Input (Negative)	LVDS/SSTL Input
K2	CN6	Port C Bit 6 (Negative) or OFDM Path 6 Bit 0 (Negative)	LVDS/SSTL Input
K3	SDCLKN	OFDM Path Clock Input (Negative)	LVDS/SSTL Input
K4	BN7	Port B Bit 7 (Negative) or OFDM Path 3 Bit 1 (Negative)	LVDS/SSTL Input
K5	BN8	Port B Bit 8 (Negative) or OFDM Path 3 Bit 2 (Negative)	LVDS/SSTL Input
K6	BN5	Port B Bit 5 (Negative) or OFDM Path 2 Bit 2 (Negative)	LVDS/SSTL Input
K7	CFG1	Hardware Block Power Configuration. Configure for desired block power up state.	CMOS Input
K8	VDD09	0.9V Digital Core Power Supply	Power
K9	VDD09	0.9V Digital Core Power Supply	Power
K10	VDD09	0.9V Digital Core Power Supply	Power
K11	RSETII	Manufacturing Test. Connect to ground.	Analog Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
K12	VDD09S	0.9V Digital Core Power Supply Sense	Power
K13	GND		Ground
K14	VDD09	0.9V Digital Core Power Supply	Power
K15	GND		Ground
K16	GND		Ground
K17	GND		Ground
K18	GND		Ground
K19	GND		Ground
K20	GND		Ground
K21	GND		Ground
K22	GND		Ground
L1	CP7	Port C Bit 7 (Positive) or OFDM Path 6 Bit 1 (Positive)	LVDS/SSTL Input
L2	CP8	Port C Bit 8 (Positive) or OFDM Path 6 Bit 2 (Positive)	LVDS/SSTL Input
L3	BP0	Port B Bit 0 (Positive) or OFDM Path 1 Bit 0 (Positive)	LVDS/SSTL Input
L4	BP1	Port B Bit 1 (Positive) or OFDM Path 1 Bit 1 (Positive)	LVDS/SSTL Input
L5	BP2	Port B Bit 2 (Positive) or OFDM Path 1 Bit 2 (Positive)	LVDS/SSTL Input
L6	BP3	Port B Bit 3 (Positive) or OFDM Path 2 Bit 0 (Positive)	LVDS/SSTL Input
L7	BP4	Port B Bit 4 (Positive) or OFDM Path 2 Bit 1 (Positive)	LVDS/SSTL Input
L8	GND		Ground
L9	GND		Ground
L10	GND		Ground
L11	GND		Ground
L12	GND		Ground
L13	GND		Ground
L14	VDD09	0.9V Digital Core Power Supply	Power
L15	GND		Ground
L16	GND		Ground
L17	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
L18	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
L19	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
L20	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
L21	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power
L22	AVDD18	1.8V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
M1	CN7	Port C Bit 7 (Negative) or OFDM Path 6 Bit 1 (Negative)	LVDS/SSTL Input
M2	CN8	Port C Bit 8 (Negative) or OFDM Path 6 Bit 2 (Negative)	LVDS/SSTL Input
M3	BN0	SCQAM Symbol Port B Bit 0 (Negative)	LVDS/SSTL Input
M4	BN1	SCQAM Symbol Port B Bit 1 (Negative)	LVDS/SSTL Input
M5	BN2	SCQAM Symbol Port B Bit 2 (Negative)	LVDS/SSTL Input
M6	BN3	SCQAM Symbol Port B Bit 3 (Negative)	LVDS/SSTL Input
M7	BN4	SCQAM Symbol Port B Bit 4 (Negative)	LVDS/SSTL Input
M8	GND		Ground
M9	GND		Ground
M10	GND		Ground
M11	GND		Ground
M12	GND		Ground
M13	GND		Ground
M14	VDD09	0.9V Digital Core Power Supply	Power
M15	GND		Ground
M16	GND		Ground
M17	GND		Ground
M18	SE	Manufacturing Test. Normally connected to ground.	CMOS Input
M19	PERR	Internal DUC-RFDAC Interface Parity Error Flag. When high, indicates an internal interface parity error by pulsing for a long period. (May briefly pulse high before DLL lock occurs.)	CMOS Output
M20	CFG4	Hardware Block Power Configuration. Configure for desired block power-up state.	CMOS Input
M21	GND		Ground
M22	GND		Ground
N1	SYNC6P	OFDM Path 6 SYNC Input (Positive)	LVDS/SSTL Input
N2	SYNC1P	OFDM Path 1/Bypass Path 1 SYNC Input (Positive)	LVDS/SSTL Input
N3	RDYCLKP	SCQAM Symbol Port READY Clock Output (Positive)	LVDS/SSTL Output
N4	RDYSYNCP	SCQAM Symbol Port READY SYNC Output (Positive)	LVDS/SSTL Output
N5	RDYAP	SCQAM Symbol Port A READY Output (Positive)	LVDS/SSTL Output

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
N6	SYNC2P	OFDM Path 2 SYNC Input (Positive)	LVDS/SSTL Input
N7	SA3	SPI Hardwired Package Address Bit 3	CMOS Input
N8	SDO	SPI Serial Data Output	CMOS 3-state Output
N9	SA2	SPI Hardwired Package Address Bit 2	CMOS Input
N10	SDI	SPI Serial Data Input	CMOS Input
N11	GNDS	Ground Sense (Periphery of the DUC)	Ground Sense
N12	GND		Ground
N13	GND		Ground
N14	TESTCLKN	Manufacturing Test Pin (Negative). Connect to ground	LVDS/SSTL Input
N15	TESTCLKP	Manufacturing Test Pin (Positive). Connect to ground	LVDS/SSTL Input
N16	GND		Ground
N17	LOCK	DLL Lock Indicator Output	CMOS Output
N18	TEST	Manufacturing Test Pin. Connect to ground	Analog
N19	REFIO	Reference Input/Output. Output pin for the internal 1.2V-bandgap reference. REFIO has a 10kΩ series resistance and can be driven using an external reference. Connect a 1µF capacitor between REFIO and DACREF.	Analog Input
N20	FSADJ	Full-Scale Adjust Input. Sets the full-scale output current of the DAC. For 80mA full-scale output current connect a 2kΩ resistor between FSADJ and DACREF. Do not connect to ground.	Analog
N21	GND		Ground
N22	REFRES	Connect a 500Ω resistor between REFRES and AVDD3	Analog
P1	SYNC6N	OFDM Path 6 SYNC Input (Negative)	LVDS/SSTL Input
P2	SYNC1N	OFDM Path 1/Bypass Path 1 SYNC Input (Negative)	LVDS/SSTL Input
P3	RDYCLKN	SCQAM Symbol Port READY Output (Negative)	LVDS/SSTL Output
P4	RDYSYNCN	SCQAM Symbol Port READY SYNC Output (Negative)	LVDS/SSTL Output
P5	RDYAN	SCQAM Symbol Port A READY Output (Negative)	LVDS/SSTL Output
P6	SYNC2N	OFDM Path 2 SYNC Input (Negative)	LVDS/SSTL Input
P7	SCLK	SPI SCLK Input	CMOS Input
P8	SS_N	SPI Select Input (Active Low)	CMOS Input
P9	SA0	SPI Hardwired Package Address Bit 0	CMOS Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
P10	SA1	SPI Hardwired Package Address Bit 1	CMOS Input
P11	RSETIO	Manufacturing Test Pin. Connect to ground.	Analog
P12	CFG2	Hardware Block Power Configuration. Configure for desired block power-up state.	CMOS Input
P13	GND		Ground
P14	DATACLKN	Internal DUC Master Clock (Negative). Leave unconnected or connect optional LC filter	LVDS/SSTL Input
P15	DATACLKP	Internal DUC Master Clock (Positive). Leave unconnected or connect optional LC filter.	LVDS/SSTL Input
P16	GND		Ground
P17	CFG3	Hardware Block Power Configuration. Configure for desired block power-up state.	CMOS Input
P18	GND		Ground
P19	DACREF	Current-Set Resistor Return Path. For 80mA full-scale output current connect a 2kΩ resistor between FSADJ and DACREF. DACREF is internally connected to ground. DO NOT CONNECT TO EXTERNAL GROUND.	Analog
P20	CREF	Noise Bypass Pin. A 1µF capacitor between the CREF and DACREF band limits the RF DAC phase noise.	Analog
P21	GND		Ground
P22	AVDD3	3.3V Analog Power Supply. Bypass with a 47nF capacitor to ground.	Power

Detailed Description

The MAX5861 (Figure 1) integrates a high-performance digital up-converter (featuring scalable 6 channels of IFFT-processed OFDM and 160 single-channel QAM channels) plus a 14-bit, 4.9152Gsps RF-DAC for direct RF synthesis of multicarrier quadrature amplitude modulation (QAM) signals in cable modem termination systems (CMTS) and edge QAM (EQAM) devices. The device combines Maxim Integrated's industry-proven DUC and RF-DAC technology in a single package to provide a compact, 12mm x 18mm, QAM modulation solution with logical system partitioning. The MAX5861 features excellent spurious, noise, and adjacent channel power (ACP) performance and can directly synthesize carriers to fill the 43MHz to 1218MHz cable downstream band as defined by the Data-Over-Cable Service Interface Specification (DOCSIS 3.0 and DOCSIS 3.1). The MAX5861 can operate with a clock rate (f_{CLK}) of up to 2.4576GHz. Since the output is updated on both rising and falling clock edges, a 2.4576GHz clock results in a DAC sample rate (f_{DAC}) of 4.9152Gsps.

The MAX5861 is compatible with DOCSIS 3.1 using differential input ports B and C. Each of the two DDR ports support three 192MHz OFDM channels using 12-bit (6-bit I and 6-bit Q)-wide IFFT-processing or one 192MHz channel in bypass mode. In bypass mode, the MAX5861 will support "any" user-created modulation of up to 192MHz bandwidth using 18-bit I/Q samples as input data.

The MAX5861 is also compatible with legacy DOCSIS (3.0 and prior) and performs SCQAM mapping, pulse shaping, and digital RF up-conversion of FEC encoded data with full agility. It accepts Forward Error Correction (FEC)-encoded differential data on a time-interleaved 10-bit differential input port with integrated parity checking. This 10-bit DDR input port A uses 5 bits for I and Q, and with the use of an offset bias bit, allows QAM mapped signals up to 1024QAM.

The MAX5861 SCQAM mapper supports all QAM constellations defined in ITU-T J.83. It performs pulse shaping, re-sampling, interpolation, and quadrature modulation of input data, supporting all data rates defined in DOCSIS. A cascade of interpolation filters, complex modulators,

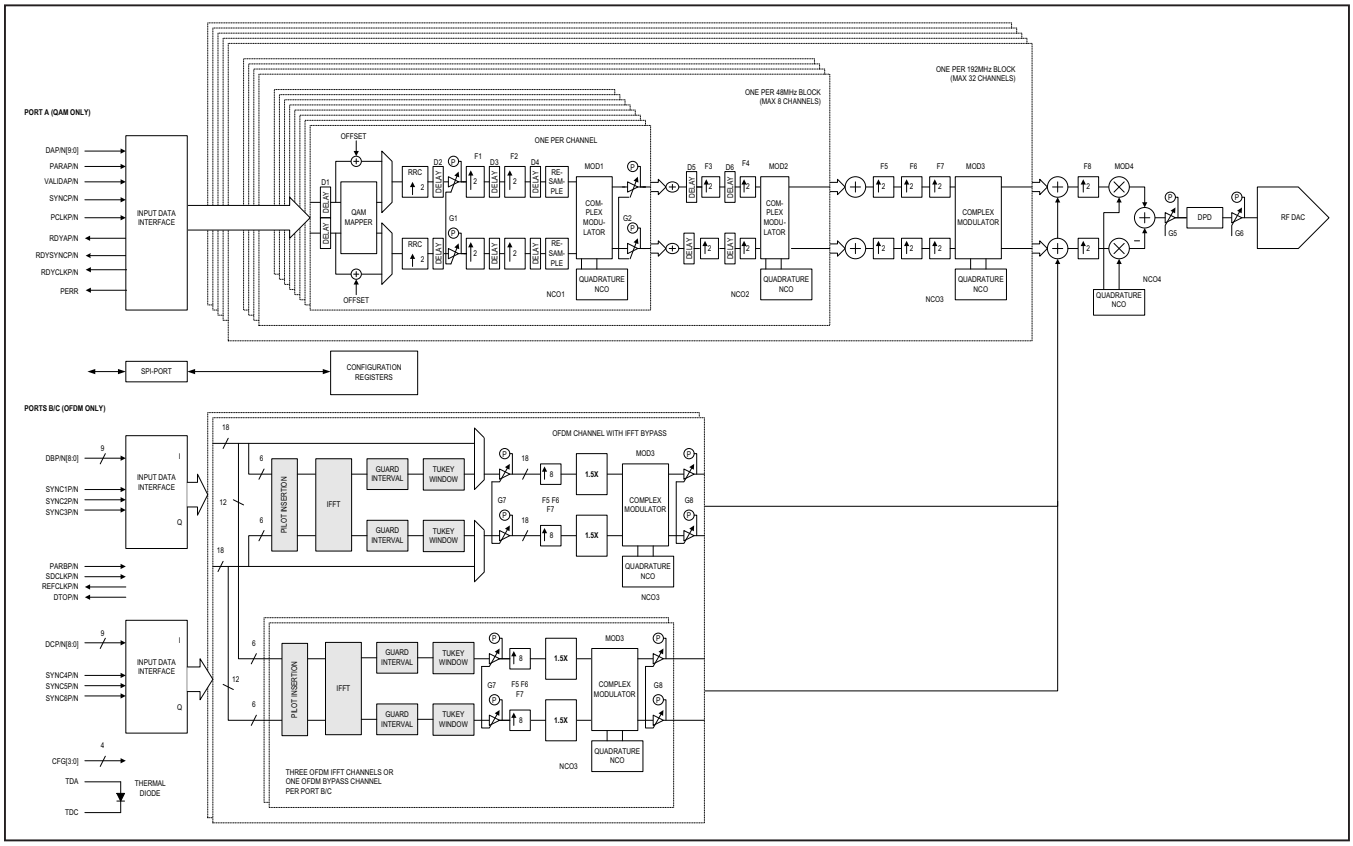


Figure 1. MAX5861 Block Diagram

and channel combiners allow modulation of the signal to any frequency in the band from 45MHz to 1218MHz. Integrated Direct Digital Frequency Synthesizers (DDFS) allow positioning of the carrier blocks with a resolution of 2.29Hz. The interpolation filters and resampler have linear phase, and excellent gain flatness. Output data from the last modulator is fed to a Digital Pre-Distortion (DPD) block to eliminate distortion performance limitations in the DAC and output amplifiers.

Up to four 20-bit I/Q RRC-bypass channels can be configured throughout the spectrum to allow legacy communication to older generation devices at up to 2.5Msym/sec. The four bypass channels can be selected from the first four channels of each of the twenty 8-channel combiners.

The MAX5861 has the digital modulation capability to modulate up to eleven blocks of 192MHz (5 x 192MHz of SCQAM and 6 x 192MHz of OFDM IFFT-processing). A combination of up to 6 blocks can be powered on at any one time. A block is defined by either a 32-channel combiner block (that can contain either 32 x 6MHz SCQAM blocks or 24 x 8MHz SCQAM blocks) or an OFDM block (up to 192MHz). This block definition is consistent with the definition in the PWR_CFG2 register (bits 10 down to 0). Unused blocks of the MAX5861 can be switched off to conserve power while limiting frequency agility.

The MAX5861 contains a current-steering DAC with an integrated 50Ω differential output termination to ensure optimum dynamic performance. Operating from 3.3V, 1.8V, and 0.9V power supplies, the MAX5861 dissipates 5.9W at 2.4576GHz. The device operates from an ambient temperature of -40°C to a junction temperature of up to +110°C and is offered in a 308-ball LFBGA package.

An interrupt pin signals when a system error condition has occurred. The 32-bit SPI port allows full configuration and debug capability.

Differential I/O Description

Differential I/O on the MAX5861 is configurable for operation using LVDS, SSTL15 (1.5V), and SSTL12 (1.2V) logic levels. The input buffer group (all differential inputs) may be configured for a logic-level and the output buffer group (all differential outputs) may be configured for the same or a different logic level. The individual input and output buffers have skew correction (variable delay circuits) capability.

SCQAM Modulation and Up-Conversion Description

Symbol Interface Description

SCQAM digital data streams interface to the MAX5861 through the port A channel multiplexer using a clock (PCLK) and sync (PSYNC) signal. Each active PCLK clock edge marks a time slot. The device loads parallel input data (up to 10 bits width) on each active edge of the clock signal. The periodic PSYNC signal is asserted high for one clock period every N clocks to indicate which clock period (time slot) is slot 1. The value N starts at 16. Each channel utilizes a configuration register that defines the assigned time slot from which the channel receives data.

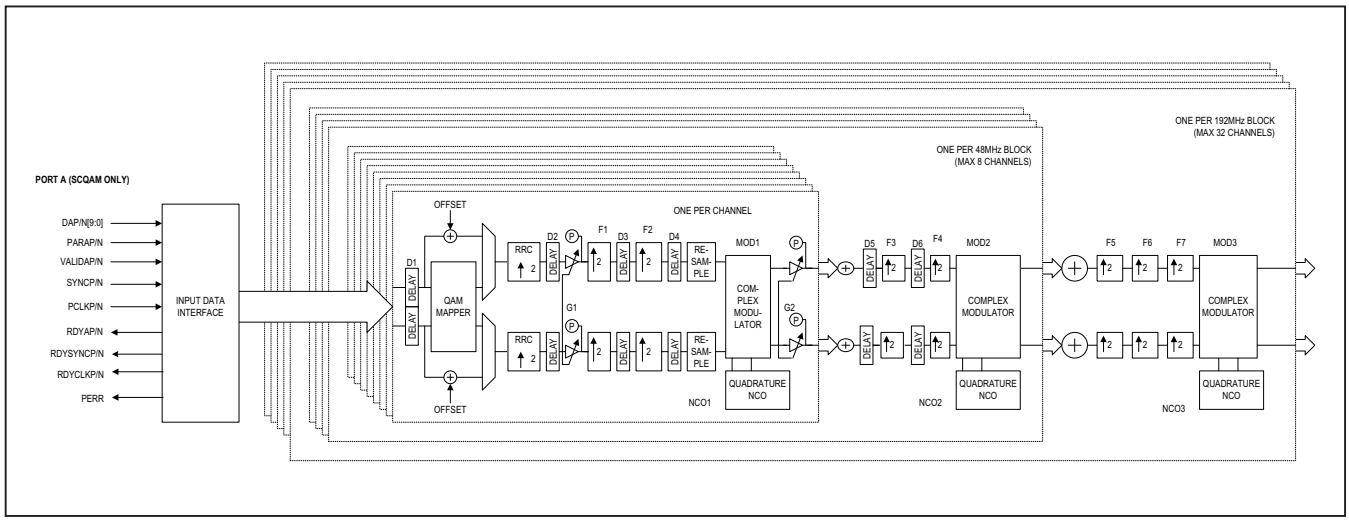


Figure 2. Single-Channel QAM Diagram

This configuration information is referred to as the time slot. The time slot state machine accepts the clock and sync signals and generates the slot-tagging information for port A. The *Port A Input Timing* section describes the timing of a time slot. The input port consists of a 10-bit DDR data input bus, a VALID input signal, and a RDY output signal. Use 6-bit wide data for 64-QAM mapping, 8-bit wide data for 256-QAM mapping, or bypass the QAM mapper and use an I/Q word width of up to 10 bits wide (12 bits wide with internal offset register). For 12-bit I/Q data, the internal offset register, which is shared by I and Q, can be set through the SPI channel configuration register. The input word in QAM mapper bypass mode is presented with the Q bits as the MSBs and the I bits as the LSBs. An active-high VALID signal indicates that valid data is being presented to the input that is loaded into the FIFO.

The RDY output indicates that the channel FIFO is ready to accept data. Each channel features a 16-word deep input FIFO to buffer the data stream from the user clock domain to the channel's symbol clock domain. The RDY signal for a time slot originates from a channel's FIFO and is routed to the appropriate time slot. RDY asserts high when the FIFO is ready to accept data, and asserts low when the channel FIFO is half-full (8 symbols) or greater. The FIFO continues to load data as long as the VALID signal is high. Drive valid low to block a FIFO load. Continuous writes could eventually result in a FIFO overflow and loss of data. The channel-overflow flag bit is saved in the corresponding FIFO overflow error register and is cleared after a register write. A FIFO underflow error is generated when the resampler initiates a read on an empty FIFO.

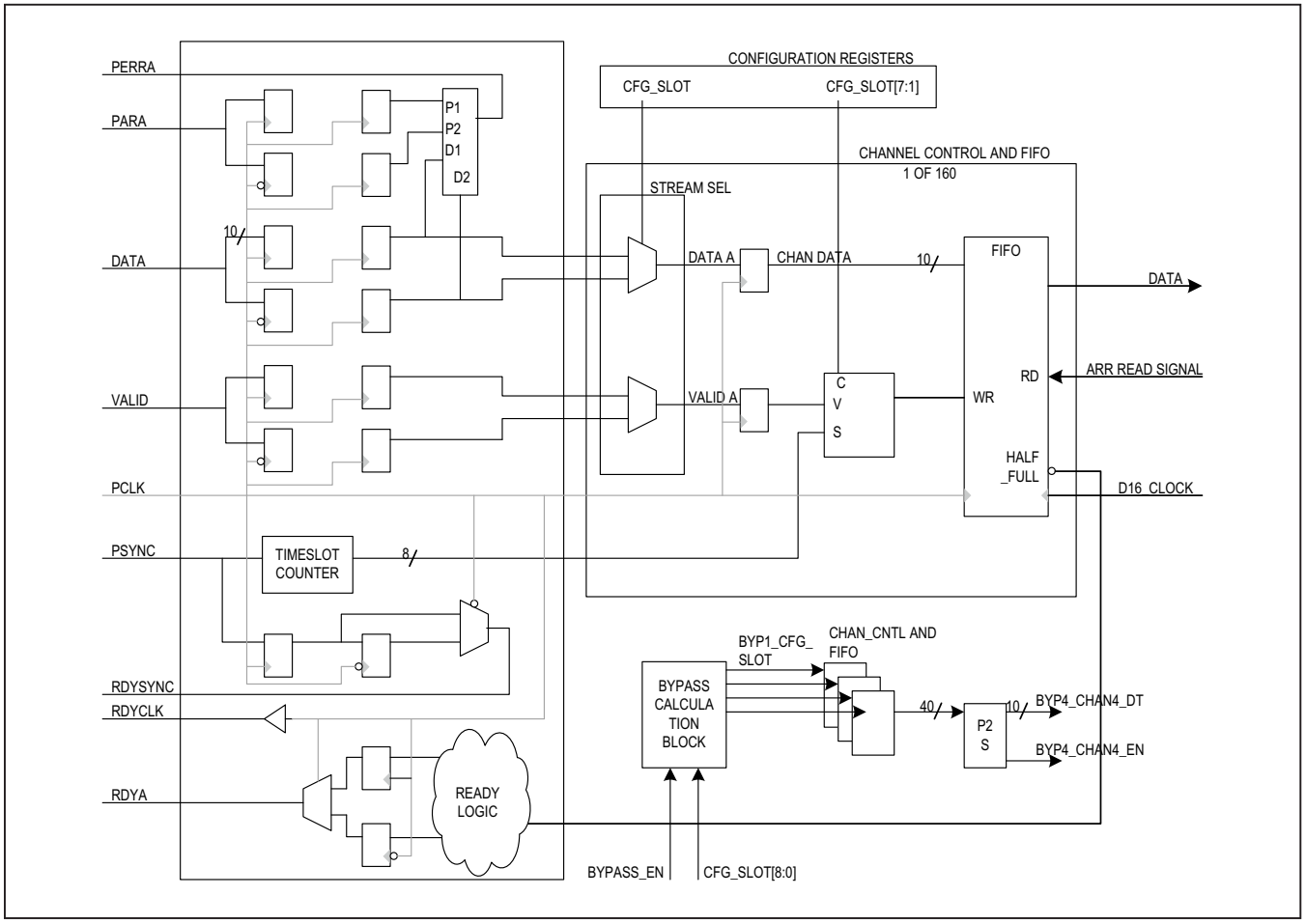


Figure 3. Symbol Interface Port Block Diagram

An underflow error indicates that the channel has missed a symbol, and this condition is signaled by the assertion (active-low) of the interrupt flag. The channel-underflow flag bit is saved in the corresponding FIFO underflow error register and is cleared after a register read. After an underflow occurs, the FIFO must fill halfway (8 words) before the FIFO will allow data transfer to resume again. A FIFO underflow cannot be generated until after the FIFO has started operation (filled to half-full and symbol transfer has started). A channel can be unmuted and sit idle (when its FIFO is not being loaded with data or before the FIFO has 8 symbols loaded) without generating an underflow flag. The device's flexible configuration permits configuring the port to accept an arbitrary amount of data by specifying the number of time slots, by adjusting the PCLK and PSYNC signals. A single data stream requires the slot count be set to 16 with only one slot containing user data. To maintain proper symbol flow to the channels and proper FIFO operation, the minimum port clock speed must be greater than or equal to the number of time slots multiplied by the maximum symbol rate. Ensure a 50% port clock duty cycle.

Port A Input Timing

The SCQAM input port provides a flexible time-multiplexed method of accepting multiple digital data streams, as shown in Figure 3. The port accepts a minimum of 16 data streams and up to a total limited by the max PCLK frequency. The PCLK and PSYNC signals control the time-division-multiplexing feature of the device. RDY and VALID signals provide FIFO handshaking for each channel and the interrupt-flag signals channel FIFO error conditions.

Figure 4 describes the expected symbol interface timing requirements (without any on-chip delay compensation). The input PCLK is required to be shifted by 90° (1/4 phase) with respect to the data. Each symbol port signal has 3 bits of delay compensation available to correct for circuit board or FPGA timing skews.

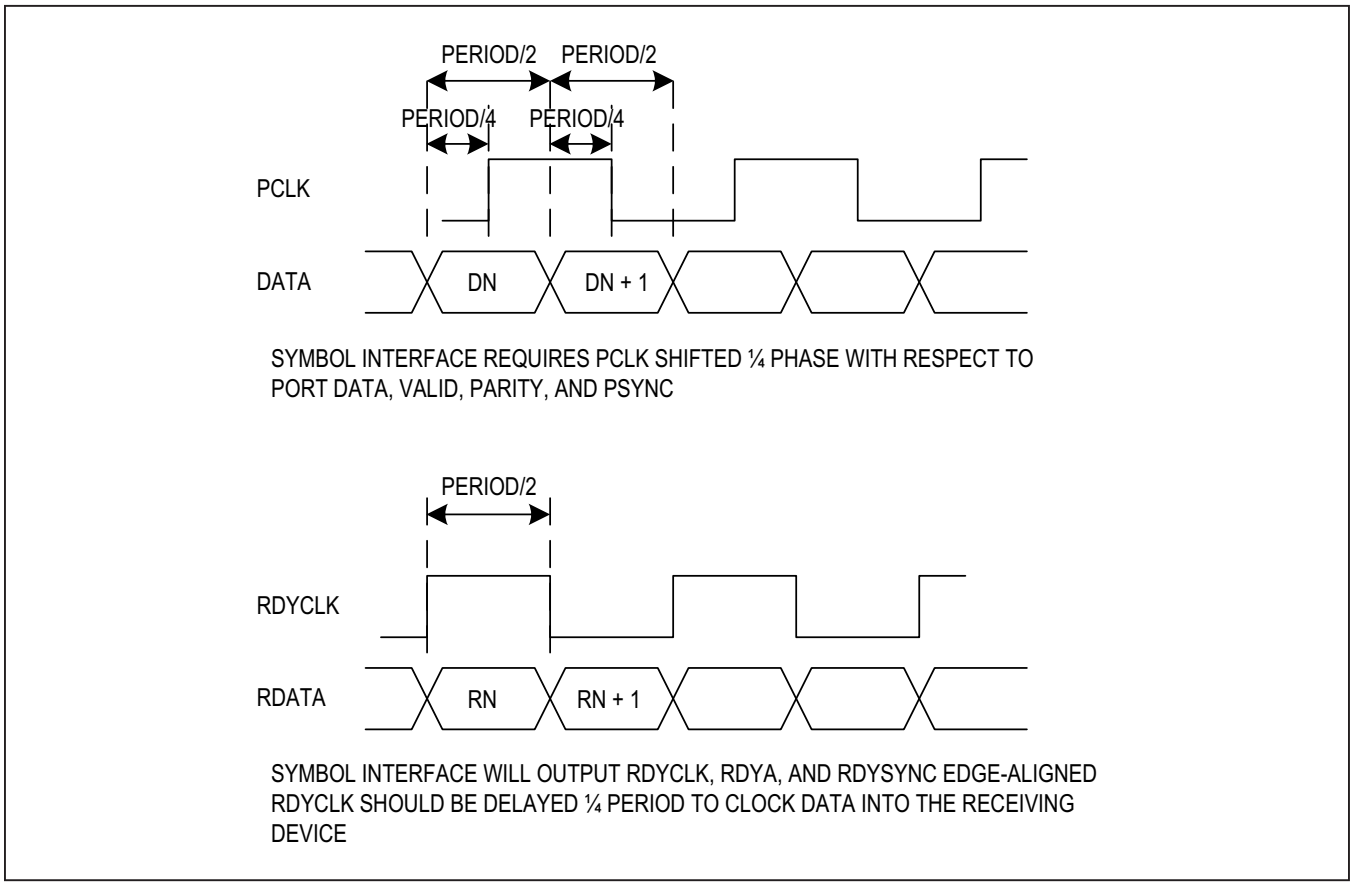


Figure 4. External Symbol Interface Timing

Handshaking

The two FIFO handshaking signals for each time slot are VALID (input signal) and RDY (output signal). VALID is asserted high along with the incoming data word to indicate that the data is loaded into the FIFO. If VALID is asserted low, then a FIFO write will not occur and the data word cannot be loaded into the FIFO. RDY is an output from the FIFO circuitry to indicate the FIFO fill status. RDY is asserted high if the FIFO is less than eight words from being full, thus allowing for an 8-word write buffer. If RDY is asserted low and VALID is asserted high, a FIFO data write still occurs. Should FIFO writes continue (VALID asserted high) when the FIFO RDY signal is asserted low, a FIFO overflow condition would eventually occur once the 8-word buffer space was consumed with resulting data loss. When a FIFO underflow occurs, data loss has occurred for the channel and the FIFO must fill at least halfway before normal FIFO operation begins. For the highest safety margin, RDY should be detected on the current cycle and VALID asserted appropriately on the following cycle. The FIFO RDY signal is expected to toggle during normal operation. To avoid a persistent underflow-interrupt condition after a global reset, FIFO reset, or FIFO underflow condition, the FIFO read pointer logic resets and the FIFO fills to half capacity (eight words) before data begins to be read and transferred to the DSP circuits. Time slots for data transfer are numbered starting from 1. Time slot 0 does not transfer data since it represents a mute condition for an enabled channel (no data, no handshaking).

Port Clock

The frequency of the common port clock can be synchronous or asynchronous to the output symbol rate. The port clock signal must be continuous (non-gapped) with a maximum frequency of 633MHz. Calculate the frequency of the port clock and input mode using the following formula:

$$PCLK\_freq \geq (\text{fastest symbol rate of any channel}) \times (\#\ \text{of time slots})/2$$

DDR port timing mode is always used. Clocking this interface slightly faster ensures that the DUC FIFOs do not empty (monitoring the VALID and RDY handshake signals ensures that the DUC FIFOs do not overflow).

PSYNC and Sync Counter

The PSYNC signal marks the beginning of the symbol transfer cycle (time-slot #1). PSYNC is used to reset and synchronize the internal sync counter. PSYNC is active-high for one clock period each N clocks, where N represents ½ the number of available time-slots in DDR mode. PSYNC is required to pulse once in the beginning (after configuration of the sync counter) to establish the frame start timing and PSYNC toggling is recommended to cease until frame retiming is required; however, PSYNC may be a periodic signal occurring once per frame. There will always be an even number of time slots due to operating in DDR mode. It is optional that each time slot contain valid symbol data. PSYNC is not required to be periodic after the initial input pulse has been applied.

The RDYSYNC output will toggle based on the programmed sync counter value and will automatically start once the sync counter value is programmed. Sync counter values may range from 16 to 172 in increments of four time slots only (16, 20, 24, etc.). The minimum sync counter value is required to be 16. Time-slots may be left empty (unused), so if 4 channels of data are required for operation then the sync counter must be set to any valid counter value at or above 16 timeslots.

The programmed sync counter value and the application of the PSYNC pulse should agree (i.e. PSYNC should be applied every 24 clocks or a multiple of every 24 clocks if the sync counter value is 48 timeslots to avoid possible port signal sensitivity). To avoid undesirable effects, the sync counter must not be constantly short-cycled by the PSYNC pulse.

Input Timing Diagram

The periodic port sync signal (PSYNC) is active-high for one half of a clock period each N clocks, where N is the number of time slots. The MAX5861 input port operates in DDR mode. The rising edge of PSYNC marks slot 1 on each transfer. Port sync is sampled on the rising edge of port clock. A repetitive (continuous) PSYNC signal is not required. There is always an even number of time slots due to operation in DDR mode.

The port timing diagram is shown in Figure 5. The port clock is a continuous signal that must not be stopped (gapped). PSYNC is active for one half of a clock period and is captured on the rising edge of port clock inside the DUC. DATA, and VALID signals captured on this same edge are defined as slot 1 DATA and VALID. Slot 2 DATA and VALID are captured on the same cycle but on the falling edge. The slot count continues to increment until the internal sync counter rolls over, or another sync signal occurs. A PSYNC signal must occur at least once at the beginning of data transfers to the port. The PSYNC input pulse is not required to be periodic after the initial input pulse has been applied. The RDYSYNC pulse repeats, based on the programmed PSYNC counter value. PSYNC counter values can start at 16 in even-value increments of 4 clocks (i.e., 16, 20, 24, etc.).

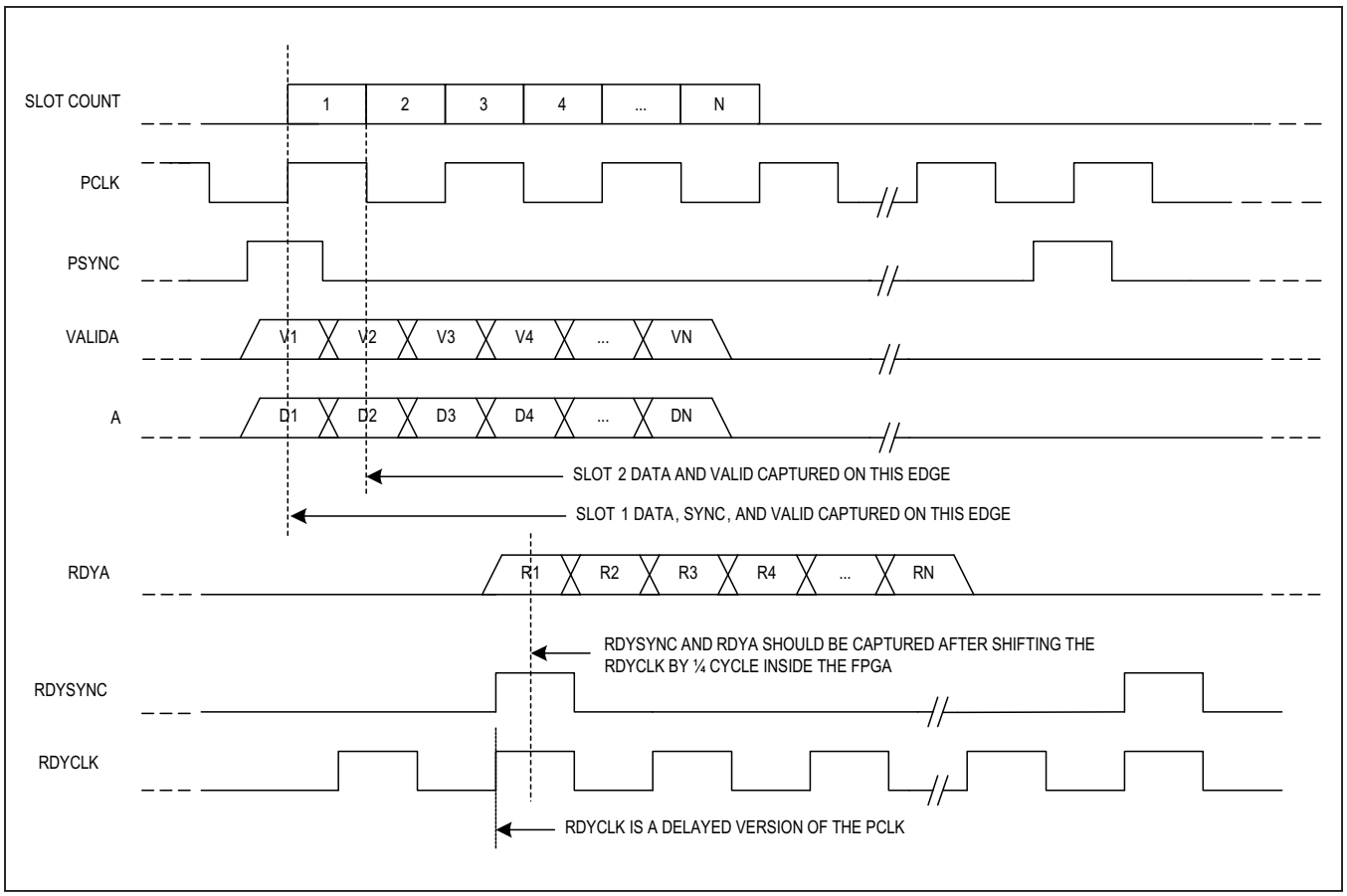


Figure 5. Input Port Timing Diagram

Configurable Input Parity

The input source may optionally include parity check bits for a configurable number of input signals (including VALID) for the parity inputs. Parity calculation is maskable from all bits plus VALID (11 bits total) to just one bit. Even parity is transmitted in on PARA and checked in the symbol port logic prior to de-muxing. The results of this parity checking can result in a parity error flag by stretching the error detection to 32 PCLK clock periods in width. Parity errors can optionally trigger an interrupt.

The VALID signal itself can be included in the parity checks as if it were a data bit by using a configuration bit or valid (when equal to 0) may be used to disable parity for that data. By using another configuration bit, parity checks can be disabled for the data whenever the VALID is low, but the checks will be performed when the VALID is high.

The parity detection can be delayed with respect to data by a clock cycle after the parity calculation. By enabling a configuration bit, the MAX5861 will account for this one clock lag (delay) between data and the corresponding parity bit.

Output Training Pattern

A training sequence pattern may be optionally enabled on port A to stimulate the ready and ready sync outputs. The repeating sequence of 101100… is applied before the final output flip-flops, which are clocked by the ready clock (RDYCLK) as in normal operation. SPI bit[17] in register 0x080 enables/disables the training sequence independent of the port input signals and data path. This training mode does not interfere with the normal operation of the port other than by sending the training sequence rather than normal interface signals. Figure 6 shows the training sequence waveform. RDYCLK continues to operate normally (as a buffered/time-delayed version of PCLK) .

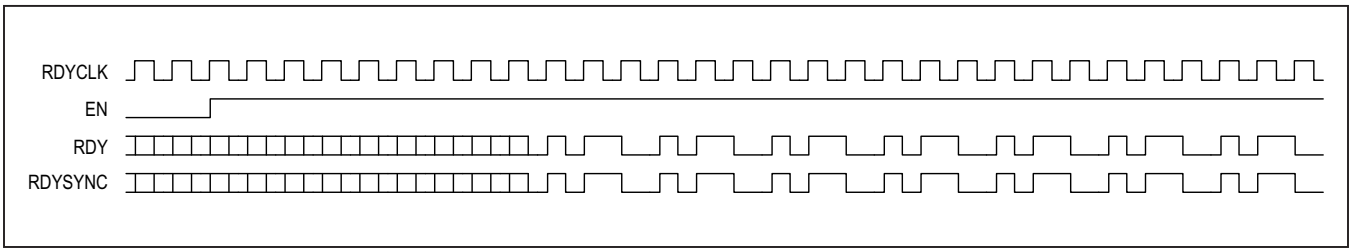


Figure 6. Port A Training Pattern Waveform

Channel FIFO Operation

Each channel features a 16-word deep FIFO for buffering the incoming asynchronous symbol data. The input FIFO (one per channel) is the only elastic memory in the data path. After global (hardware) reset, the FIFO content is set to all zeros.

After global reset or an underflow condition, the FIFO read pointer is reset and held at location 0. The FIFO must fill to 7 symbols before the FIFO read counter increments. While a channel is unmuted and before the FIFO pointer is allowed to increment, symbol data continues to be sampled from FIFO location 0. After global reset or underflow, the first input symbol word to be loaded into the FIFO is loaded at location 0.

The FIFO is clocked by the asynchronous port clock signal, which is not required to have any particular relationship to symbol rate or the DATACLK frequency. If the port clock frequency is higher than the required symbol “feed” rate for a channel, the FIFO absorbs the differences. The FIFO handshaking signals are used to avoid overflow or underflow. Should a channel FIFO underflow, the FIFO contents are set to zero and the associated QAM mapper output is zero (no symbol) until normal FIFO operation resumes again. An interrupt is not generated for the initial underflow condition (after reset) and only one interrupt is generated for each FIFO underflow thereafter if interrupt mode is “event” (continuous interrupts would be generated in “real time” mode). FIFO soft-reset is accomplished by toggling the FIFO reset bit for the channel of interest through an SPI command. While the FIFO reset bit is logic 1, the FIFO pointer is reset to location 0, overflow/underflow indicators are cleared, FIFO ready is inactive (logic 0), and FIFO writes are stopped (the previous contents of the FIFO are not zeroed).

When the FIFO reset bit is released (set to logic 0), the FIFO ready signal is asserted logic 1, which indicates that the FIFO is ready to accept data. The FIFO disallows data reads from the channel (ARR) until the pointer is at eight words.

A FIFO reset for a particular channel can be performed using one of three ways:

1) Set the local FIFO reset pulse bit in the channel configuration register (CHAN_x).

2) Enable the “use global reset” bit in the channel configuration register (CHAN_x), then set the self-clearing GBL_FIFO reset register bit in the global configuration (GBL_CFG) register section.

3) Enable the “use global reset” bit in the channel configuration register and set the “use external input for FIFO reset” (M2_SYNC_FIFO) bit in the global external sync register (GBL_CFG), then apply a pulse at the MODE2 input to reset the FIFO.

SCQAM DSP Path

The DSP path performs QAM mapping, pulse shaping, resampling, interpolation, and modulation of the incoming data. Up to 160 channels with a symbol rate up to 5.360537Msym/s, or up to 120 channels with a symbol rate up to 7.14Msym/s are synthesized into one digital RF signal, driving the integrated RF DAC at 4.9152Gsps. Incoming data can be premapped data or QAM-mapped data. Bytes should be QAM-mapped using the QAM mapper at the input of the DSP path. The QAM mapper supports 16-QAM, 32-QAM, 64-QAM, 128-QAM, and 256-QAM constellations, as defined in ITU-T J.83 [1] and DVB-C [3]. QAM-mapped data is first pulse-shaped using a root-raised cosine (RRC) filter. Each RRC filter has a configurable excess bandwidth factor of 0.12, 0.13, 0.15, or 0.18, meeting the requirements in J.83 Annex A, B, and C. [1]

As shown in Figure 1, at the first stage of multiplexing, 160 channels are divided into up to 20 blocks of up to 8 channels each. In each octal-channel combiner, up to 8 individual channels are frequency-translated and combined, forming a baseband block with a bandwidth of up to 48MHz. In the next stage, four of these blocks are frequency translated and combined into a larger baseband block with a maximum bandwidth of 192MHz.

Next, up to five of these blocks are frequency-translated and combined into a block with a maximum bandwidth of 1218MHz. This block is passed through a final 2x interpolation filter and the block is frequency translated to the desired output frequency using a quadrature modulator.

Spurious emissions and noise comply with DOCSIS requirements (Tables 7-36, 7-37, and 7-38) in CM-SP-PHYv3.1-I03-140610[2]. Internal digital predistortion (DPD) is required to improve out-of-band image attenuation above 1.218GHz. The MAX5861's RF-DAC has an attenuated f_{OUT} image located at $f_{DAC}/2 - f_{OUT}$, this image attenuation above 1.218GHz is limited by the DAC to approximately 40dB. Further image attenuation can be achieved using the $f_{DAC}/2 - f_{OUT}$ DPD branch.

Octal Channel Combiner (48MHz Block)

A block diagram of the octal-channel combiner is shown in Figure 7 (For simplicity, only one channel is shown). Seven more identical channels are added together in the adder (S1), forming a sub-block. 5-bit baseband I and Q data is received. The programmable delay block (D1) allows modifying the delay of each channel individually from 0 to 12 symbol periods in steps of 1 symbol period. The data can be passed through or bypass a QAM mapper. If the bypass function is used, an offset of 1/2 LSB can be set via SPI bit to allow representation of mapped 1024 QAM symbols. QAM-mapped data is pulse shaped using an RRC filter. The RRC filter interpolates the symbol rate by a factor of 2. Each RRC filter can be individually set to any of the J.83 standard excess bandwidth factor a equal to 0.12, 0.13, 0.15, or 0.18. The programmable delay block following the RRC filter allows delaying the RRC filter output by 0 or 1/2 symbol periods. A programmable gain block (G1) allows setting the gain with 11-bit resolution for leveling and equalization purposes. The sample rate is increased by a factor of 8 from the symbol rate using the RRC filter, the F1 and F2 half-band filters. Interpolated data is resampled with an arbitrary sample rate using an ARR. Each channel is frequency translated within the ±24MHz channel before being combined using an adder network. All channels can be delayed the same amount in up to 3/8 symbol periods with 1/8 symbol period resolution using delays D3 and D4. Configure the QAM mapper for 16-/32-/64-/128-/256-QAM modulation. QAM constellations are defined in ITU-T J.83 [1] and EN 300 429 V1.2.1 [3]. The QAM mapper can be bypassed. If the QAM mapper is bypassed, an adjustable offset is provided to allow representation of a 1024-QAM-mapped signal using only 10 bits. The SPI interface register contains an offset bit that moves the constellation off zero.

The arbitrary-rate resampler (ARR) is a Farrow filter that allows transitioning the sample rate from the symbol rate synchronous domain to the DAC clock synchronous domain. Sample rates must always be selected such that the resampler has a higher output data rate than the input data rate. Both the symbol clock and the DAC clock are derived from the same 10.24MHz DTI clock (DTI-I04-061222 [4]). Their frequencies are derived as f_{DAC} = M1/N1 x 10.24MHz and f_{Sym} = M2/N2 x 10.24MHz, where M1, M2, N1, and N2 are positive 16-bit integers. M2 and N2 can be different for different modulation schemes and standards. Because their frequencies are derived from the same 10.24MHz clock, the phase relationship between the two clocks is exactly known and can be calculated using 2-phase accumulators. While the DAC clock must run continuously, with very low jitter, symbol information can be transmitted with several samples of jitter, to be absorbed in FIFOs before the octal-channel combiner and at the input of the resampler. The resampler requests a new sample when needed to maintain the programmed,

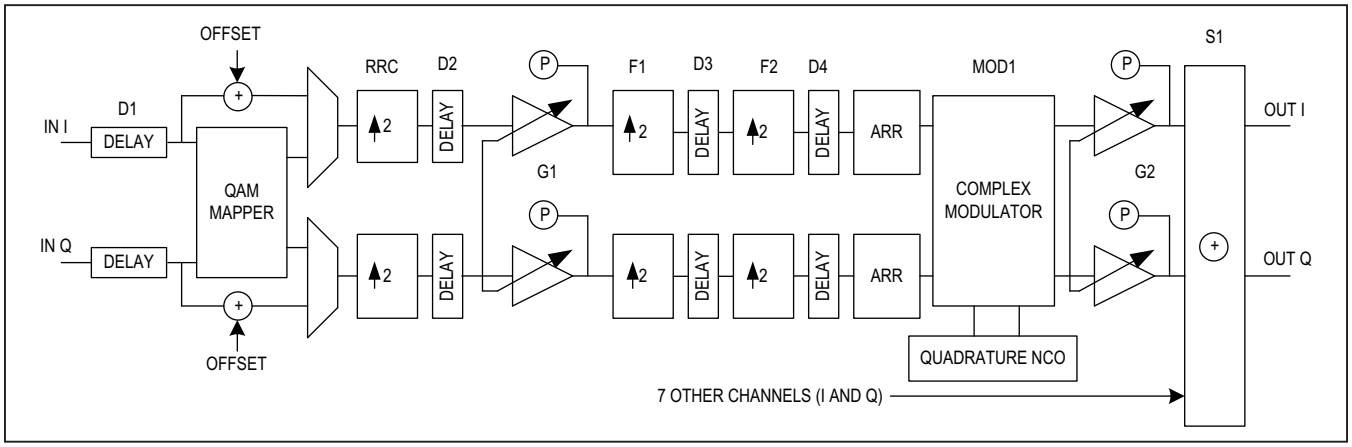


Figure 7. Octal Channel Combiner

constant output rate. The output of the resampler thereafter operates from a clock that is divided down from the DAC update rate by a factor of 64. A more detailed description of the ARR is given in the *Arbitrary Rate Resampler (ARR)* section. The complex modulator with its associated NCO is used to frequency-translate the channels within the block. The frequency tuning word for the NCO is defined with 19-bit resolution. All programmable parameters are programmed through the SPI interface.

Block Combiners and Digital Up-Conversion

The octal-channel combiners are followed by two stages of block combiners and a quadrature modulator, as shown in Figure 8. The sample rate of each sub-block of 8 channels is interpolated up by a factor of 4 before four sub-blocks are combined into one block of a maximum 32 channels.

The sample rate of each one of these blocks is further interpolated up by a factor of 8 and combined into a final output of up to 160 channels with a maximum bandwidth of 960MHz. Finally, the sample rate is interpolated up by another factor of 2 and the output is frequency translated using a digital quadrature modulator. The gain with 9-bit resolution using gain stage G5. The latency of the entire data path can be changed in steps of 32 DAC update periods, using programmable delay registers D5 and D6. All D5 registers have a common control bit and all D6 registers have a common control bit.

QAM Mapper

The QAM mapper performs SCQAM mapping of input data. There is a separate QAM mapper for each channel and all QAM mappers are configured independently. The QAM mapper supports the following constellations:

- ITU-T J.83 Annex A: 16-QAM, 32-QAM, 64-QAM, 128-QAM, and 256-QAM
- ITU-T J.83 Annex B: 64-QAM and 256-QAM
- ITU-T J.83 Annex C: 64-QAM and 256-QAM

See the following Notes 1, 2 and 3 and Table 1 for QAM constellations.

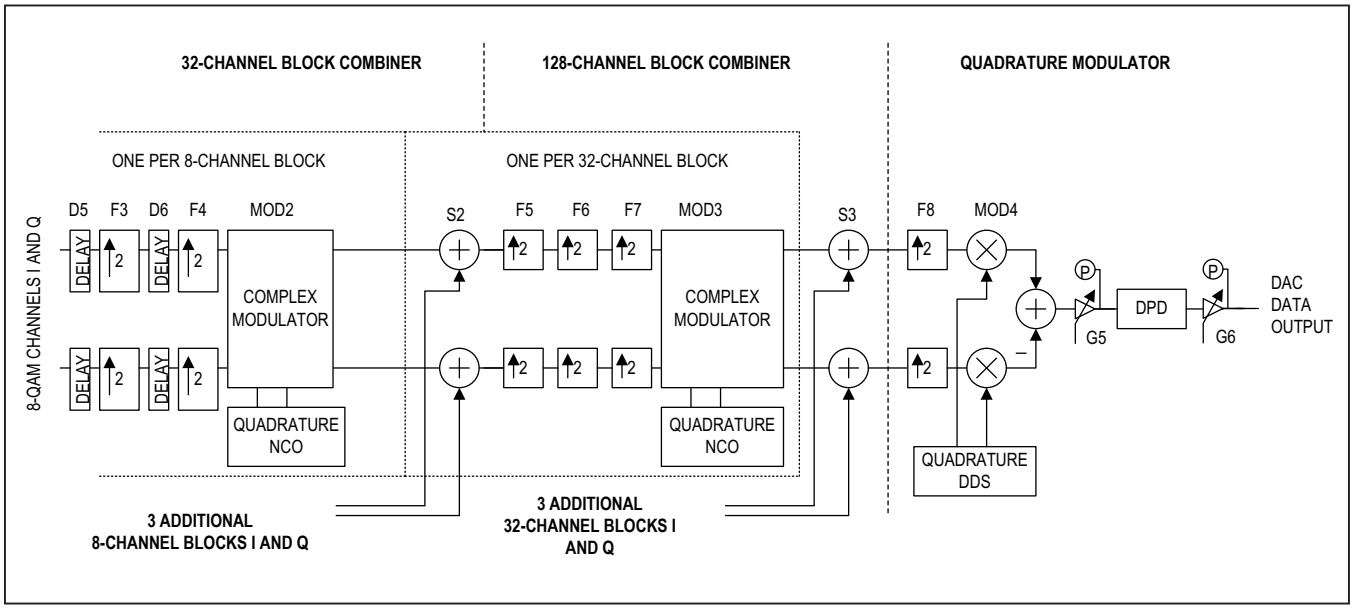


Figure 8. Channel Combiners and Interpolation/Modulation

Table 1 explains the QAM options for the internal mapper. Each of the input ports to the device is 10 bits in width. The QAM mapper is not available in RRC-bypass mode.

The bypass mode option allows the input of a constellation choice. The bypass mode option also allows the addition of an internal LSB static bit value (same for I and Q buses) to expand the effective bus width to 12 bits for 1024-QAM operation. This offset bit is set through an SPI register for each channel. The complex symbol data input in bypass mode is assumed to be (I + j Q) and the data input format is two's complement.

Table 2 shows the calculated RMS values for each modulation at the RRC filter input, calculated as the average vector length for all symbols. When using the bypass mode, all inputs expect two's complement formatted data.

In case of mapped data being applied in bypass mode, the user would place 5 bits of I data in bits [9:5] and 5 bits of Q data in bits [4:0] on the bus. Since there is a 10-bit data bus, the I/Q data can be represented by a minimum of 5 bits. The I/Q symbols are all odd numbers. Internally the 5 bits of I/Q are multiplied by 2 and an optional 1/2 LSB can be added.

Table 1. Internal QAM Mapper Options

SELECTION	TYPE	BUS BIT WIDTH	INPUT PORT BUS PARTITIONING	MSB
000	TCM 256-QAM (Note 15)	8	Bits [7:4] are I Bits [3:0] are Q	Bit 7 is MSB - I Bit 3 is MSB - Q
001	TCM 64-QAM	6	Bits [5:3] are I Bits [2:0] are Q	Bit 5 is MSB - I Bit 2 is MSB - Q
010	Diff Grey 16-QAM	4	Bits [3:0] used	Bit 3 is MSB
011	Diff Grey 32-QAM	5	Bits [4:0] used	Bit 4 is MSB
100	Diff Grey 64-QAM (Note 16)	6	Bits [5:0] used	Bit 5 is MSB
101	Diff Grey 128-QAM	7	Bits [6:0] used	Bit 6 is MSB
110	Diff Grey 256-QAM	8	Bits [7:0] used	Bit 7 is MSB
111	10-Bit Bypass Mode with Offset Register (Notes 17,18)	10	Bits [9:5] are I Bits [4:0] are Q	Bit 9 is MSB - I Bit 4 is MSB - Q

Note 15: The constellation mapping is as described in the Figure B.19 of the ITU J.83 standard document. Input bits are C7 to C0.

Note 16: The constellation mapping is as described in the Figure A.7 of the ITU J.83 standard document.

Note 17: Constellation mapping is outside the MAX5861. The complex symbol data input in bypass mode is (I + j Q) and the data input format is two's complement. Operation is y = 2x + b, where x is the 5-bit I or Q at the input and b is the LSB set by the register. For 64-QAM or 256-QAM, b = 0, for 1024-QAM, b = 1.

Note 18: An internal LSB offset register (same bit for I and Q) is provided to expand the bus to effectively be 12 bits with the LSB offset bit enabled.

Table 2. SCQAM Mapper Symbol Levels

QAM TYPE	VALUES ASSIGNED TO SYMBOLS	VALUES SEEN AT THE INPUT OF THE RRC FILTER	LEVELS SCALED TO ±1
256-QAM	± 1, 3, 5, 7, 9, 11, 13, 15	± 2, 6, 10, 14, 18, 22, 26, 30	± 0.0625 to 0.9375
128-QAM	± 1, 3, 5, 7, 9, 11	± 2, 6, 10, 14, 18, 22	± 0.0625 to 0.6875
64-QAM	± 1, 3, 5, 7	± 4, 12, 20, 28	± 0.125 to 0.875
32-QAM	± 1, 3, 5	± 4, 12, 20	± 0.125 to 0.625
16-QAM	± 1, 3	± 8, 24	± 0.25 to 0.75
Bypass mode with offset	-32, -30, -28 … -2, 0, 2 … 30	± 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	± 0.03125 to 0.96875
Bypass mode without offset	-32, -30, -28, … -2, 0, 2 … 30	-32, -30 … -2, 0, 2 … 30	-1.0 to 0.9375

Table 3. Resampling Ration Recommendations

SUPPORTED SYMBOL RATE (MSYM/S)	ITU-T J.83 ANNEX	C, MHZ) (FC, MHZ)	MODULATION (QAM)	M	N	M ÷ N
5.056941	B	6	64	401	812	0.4938423645
5.360537	B	6	256	78	149	0.5234899329
6.952	A	8	64	869	1280	0.6789062500
6.952	A	8	256	869	1280	0.6789062500
5.309734	C	6	64	1889	3643	0.5185286851
5.309734	C	6	256	1889	3643	0.5185286851

Spectral Inversion of Channel Data

Each channel offers three ways to internally invert IQ data after the QAM mapper via the SYMIF register. The SYMIF register for each channel has three bits available for spectral inversion:

- SWAP_IQ – Swaps the I and Q data.
- I_INV – Inverts (negates) the I data
- Q_INV – Inverts (negates) the Q data

Spectral inversion bits are not available in RRC-bypass mode.

RRC Filter

The RRC filter performs pulse shaping of the input symbols. The RRC filter excess bandwidth, passband flatness, stopband attenuation, and impulse response shape conform to ITU-T J.83 [1]. The RRC filter interpolates the symbol rate by a factor of 2. Use the SPI port to configure the excess bandwidth of each individual RRC filter. In RRC-bypass mode, data is inserted into the DSP chain after the RRC filter.

RRC Filter Bypass Mode

The first four channels of each 8 channel SCQAM combiner (up to a maximum of 4 channels) of the MAX5861 are capable of operating in “RRC-bypass mode” to allow legacy communications with older devices. Channels 1-4, 9-12, 17-20, 25-28, 33-36, 41-44, 49-52, 57-60, 65-68, 73-76, 81-84, 89-92, 97-100, 105-108, 113-116, 121-124, 129-132, 137-140, 145-148, and 153-156 have RRC-bypass capability (see the Channel and Block Combiner Numbering Reference figure for the channel numbering reference). The maximum symbol rate for RRC-bypass data is ~2.5M symbols per second since the RRC 2x interpolator pulse shaping is bypassed in this mode (Figure 10). The maximum symbol rate should be less than 6MHz/2 or 8MHz/2 as appropriate.

The 40 bit symbol data (2’s complement format) for a RRC-bypassed channel is transferred in four consecutive time-slots at a configurable position in the symbol transfer cycle. The 20 bits of I data (MSB first) are passed in two 10 bit words followed by the 20 bits of Q data (MSB first) passed in two 10 bit words. Bit order for the four time slots is: I[19:10], I[9:0], Q[19;10], Q[9:0]. For example, if a RRC-bypass channel is configured to begin in time-slot 51, then bits I[19:10] are passed in time-slot 51, bits I[9:0] are passed in time-slot 52, bits Q[19:10] are passed in time-slot 53, and bits Q[9:0] are passed in time-slot 54. Data is passed directly to the interpolation filters. The sample rate is 2 times input sample rate of a channel having the same symbol rate with pulse shaping enabled so the KF/LF value must be calculated appropriately. The sample rate will be 2 x 40 bits/symbol or 40 bits/sample at the MAX5861 port A input. To get the best dynamic performance, the peak value of the sample should be aligned with the MSB of the data.

Four 10 bit-wide FIFOs are combined to form a 40 bit-wide FIFO for a RRC-bypass channel’s data. This 40 bit-wide FIFO is 16 words deep. Each RRC-bypass channel data must have all four VALID signals high to load valid data into the FIFOs. All four RDY signals must be identical (high or low) for bypass channel time slots. Before switching a RRC-bypass channel to another channel allocation, the current RRC-bypass channel should have the VALID signals set low before configuring and switching to the new channel.

The RRC-bypass channel time slot(s) in the symbol transfer cycle is flexible but it may be desirable to place RRC-bypass channels at the end of the assigned time slots after normal channel assignments. RRC-bypass channels should start with a time slot which is a multiple of four plus one (i.e. 1, 5, 45, 81, etc.). Bit[13] of the SYMIF register enables RRC filter bypass mode. Once RRC bypass is enabled for a channel, the QAM mapper and the PRBS functions are no longer available. Data enters the DSP path before the G1 gain control, so G1 is available to control signal power. The spectral inversion bits are not available in RRC-bypass mode.

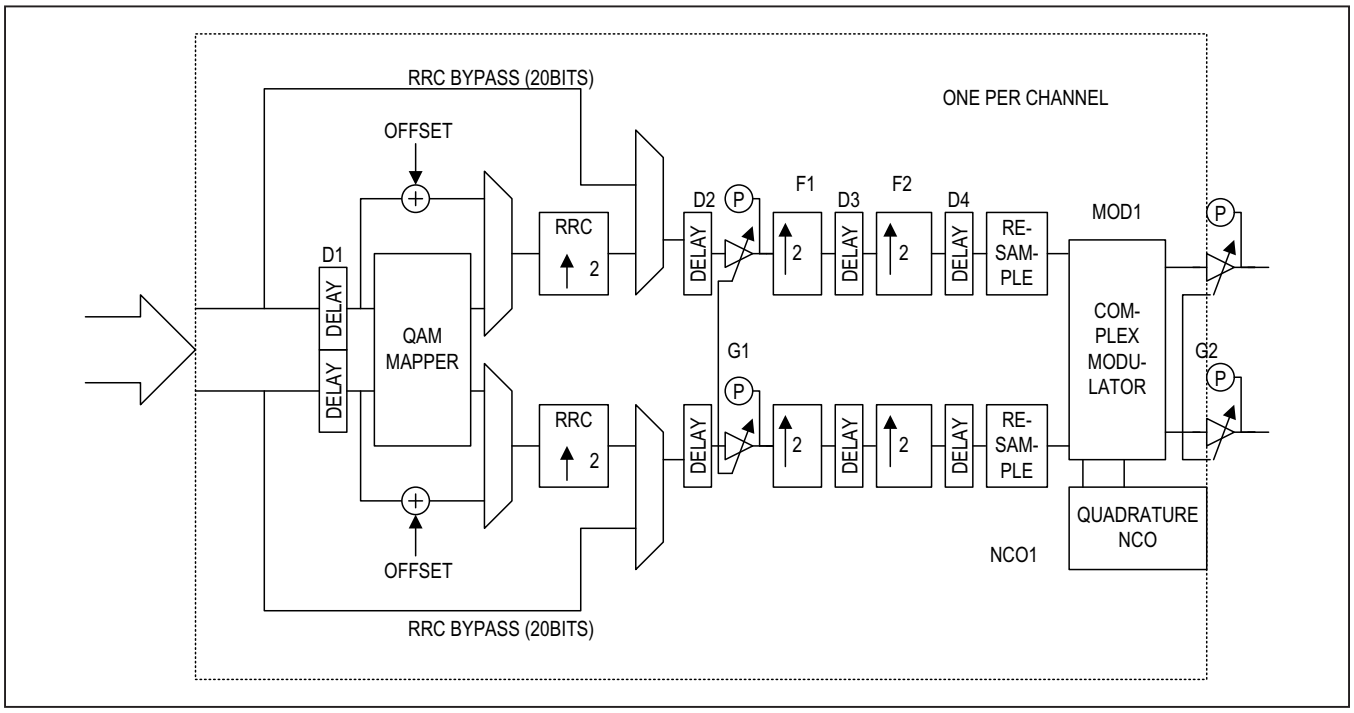


Figure 9. Channel Diagram Showing RRC Filter Bypass

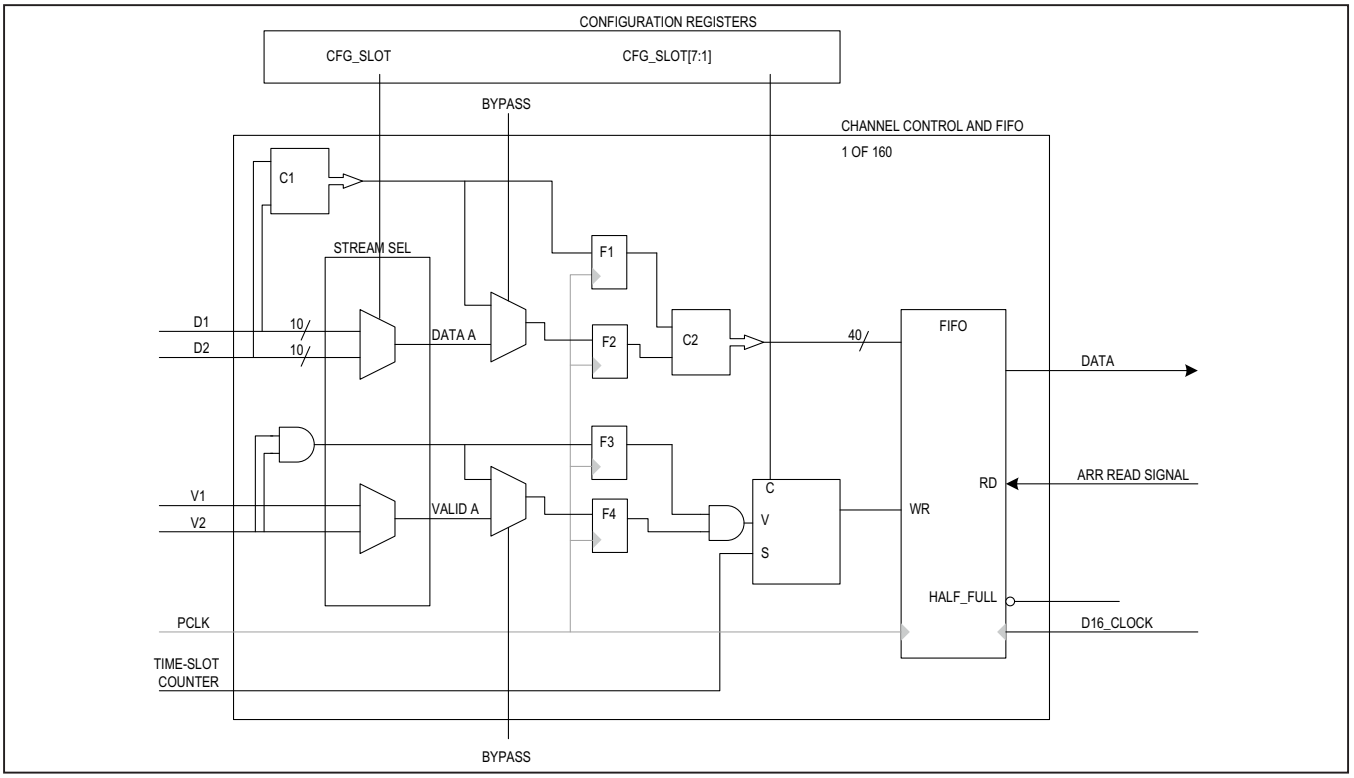


Figure 10. Channel Control Block Configured for RRC-Bypass Mode

Arbitrary Rate Resampler

The ARR converts the sample rate of the input symbols to a clock rate that is an integer division of the DAC clock rate. Both the symbol rate and the DAC update rate maintain a rational relationship to the 10.24MHz DTI clock. The symbol clock is related to the DTI clock as M/N x 10.24MHz, where M and N are integers. According to DOCSIS 3.0, these integers should be 16-bit integers. No M and N are published for Annex C. Table 3 shows the calculated M/N that meets the required symbol rate within 1ppm. To meet this accuracy, 16-bit numbers are needed, as indicated.

Choose sample rates such that the ARR output rate is higher than the input rate. The output rate of the ARR equals $f_{DAC}/64$. The RF DAC update rate is higher than 4096Msps when all streams have a symbol rate lower than 8MSym/s.

The ARR is configured by the KF and LF parameters.

The DAC update rate can be calculated as:

$$f_{DAC} = 8 \times 64 \times LF/KF \times (f_{Sym})$$

where f_{DAC} is the DAC update rate and f_{Sym} is the symbol rate; LF and KF are represented using 27-bit integers.

Modulators

Complex modulators are used for frequency translation of the carriers within the SCQAM channel combiners (Figure 11). The complex modulators allow both positive- and negative-frequency translation of the input signal. A quadrature modulator (MOD4) is used for frequency translation of the final block.

Power Adjustment and Power Probes

The gain-adjustment blocks in the block diagram can be programmed using the SPI interface. A clipping monitor is also associated with the gain adjustment. A clipping measurement is initiated as follows: a threshold, the number of samples to be measured over, and the count reset are set in registers. The number of times the signal exceeds the set threshold during the measurement is written to a register. By performing a number of these measurements, the amplitude distribution of the signal can be derived, and power, PAPR, and clipping probability can be estimated using an external microprocessor.

In addition to adjusting the gain, the power-adjustment blocks can also be used to mute channels. A channel can be configured without affecting the channels that are already online. For this reason, the gain adjustment at the output of the device is adjustable in fine steps (< 0.1dB) to allow for slowly ramping down the gain when adding additional channels.

OFDM Modulation and IFFT Processing Description

OFDM Path Features

- Up to three 192MHz DOCSIS 3.1-compatible OFDM blocks with IFFT processing or one 192MHz bypass channel per OFDM port
- Multiplexed 9-bit LVDS/SSTL compatible data interface at 409.6MHz DDR
- Baseband input data sample rate of 204.8Msps for each OFDM channel

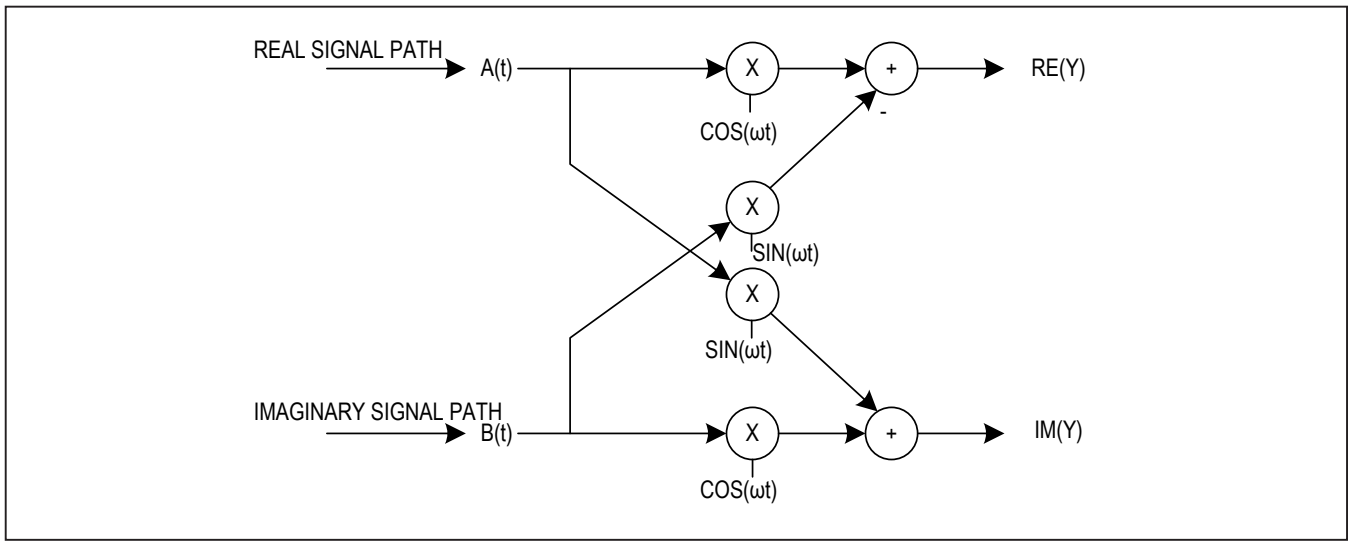


Figure 11. Complex Modulator Block Diagram

- OFDM block interpolation by 24x to support a DAC sample rate of 4.9152Gsps
- Integrated pilot insertion, IFFT, guard interval (GI) and windowing functionality
- IFFT supports OFDM bandwidths of 24MHz to 192MHz wide
- Capable of bypassing the pilot insertion function
- Capable of bypassing the IFFT, GI and Windowing function
- Each OFDM block can be placed anywhere in the downstream spectrum
- Per subcarrier gain control for all modulation profiles
- Pilot insertion with level and gain controls, with up to 6dB gain boosting
- Static gain equalization via SPI for each channel

Functional Description

The MAX5861 supports DOCSIS 3.1-standard OFDM channels. Differential input ports B and C offer a source-synchronous input for OFDM data using a fixed 204.8Msps sample rate. Ports B and C are identical in functionality and each supports a source-synchronous 9-bit data interface at 819.2Mbps (409.6MHz DDR) together with three SYNC pairs. Either of the two ports can be used to supply 3 x 192MHz wide OFDM blocks (6-bit I and 6-bit Q data) with the use of integrated pilot insertion, IFFT, guard interval and windowing functionality which allows up to six OFDM blocks. These functions can be bypassed to feed the interpolators directly with 18-bit I and 18-bit Q data words. The bypass option will require the entire data bandwidth of each 9-bit input Port B or C at 819.6Mbps (409.6MHz DDR). Thus using this IFFT bypass option, only one 192MHz block on each of the ports B or C can be used.

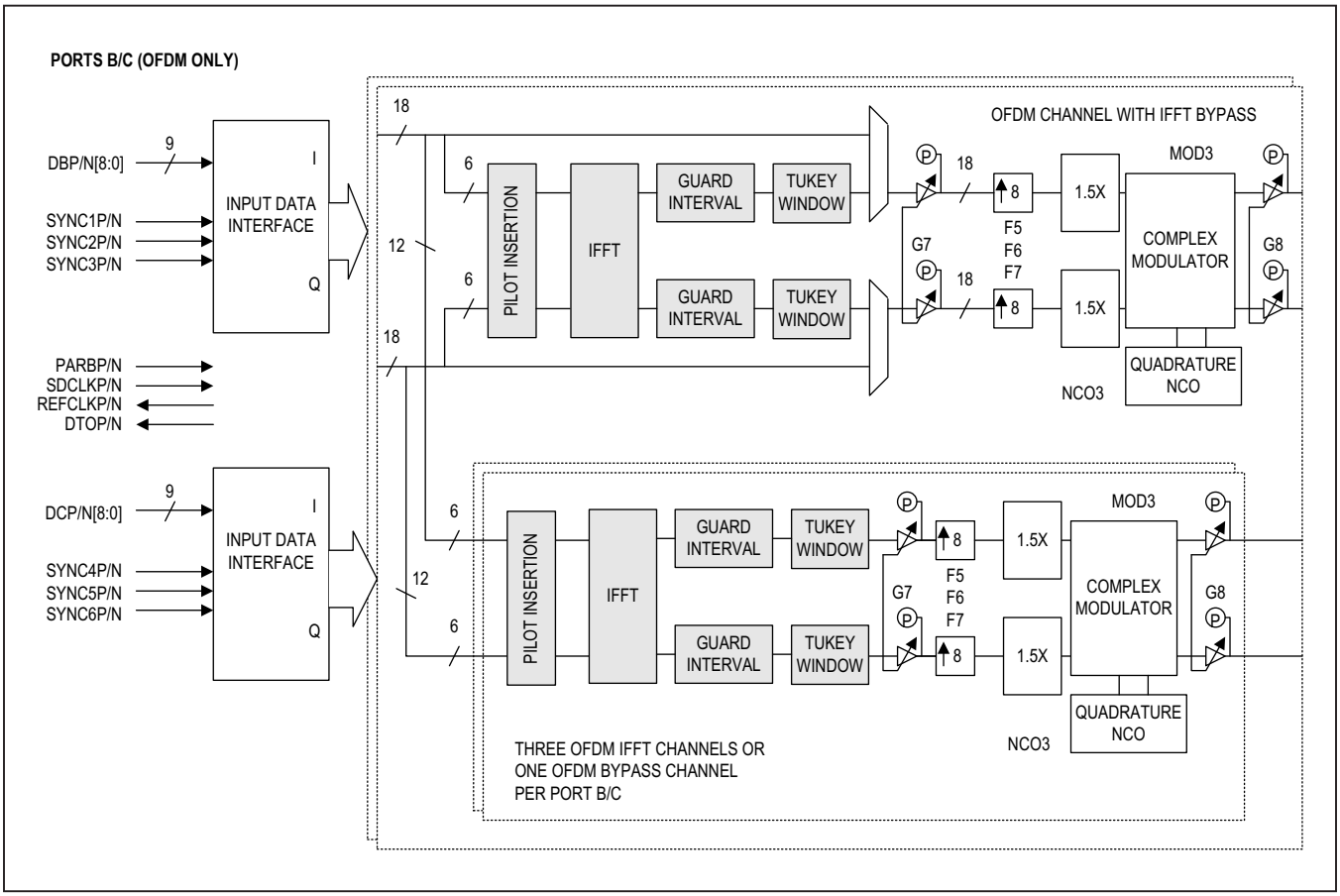


Figure 12. OFDM Section Block Diagram

The OFDM block's data is upsampled using half-band interpolation filters (F5, F6, F7) and 3/2 resampler allows the integrated MAX5882 RF DAC to be used at 4915.2Msps. An additional digital complex modulator MOD3 for each OFDM block is used to place the OFDM block anywhere in the downstream spectrum, and provides complete agility. Gain control G7/G8 are used to adjust the power level of the OFDM block relative to the QAM channels, along with the associated power monitors for checking the signal power levels. Port B and port C inputs are LVDS/SSTL compatible.

OFDM Input Data Interface

The DOCSIS 3.1 OFDM PHY functions of FEC Codeword building, QAM mapping and frequency/time interleaving are expected to be performed before being input to the MAX5861. The MAX5861 receives OFDM data, pilot's subcarrier indexes, subcarrier muting and gain information from the FPGA via Port B and/or Port C. The input data to MAX5861 for each of the six OFDM channels is QAM mapped in the FPGA, and at most 13 different mapping options are possible. The FPGA conveys the information to MAX5861 using a SYNC and 3 bits of serialized DATA operating at four times the 204.8MHz symbol rate for each channel. The mapping of Port B and Port C's DATA and SYNC signals is shown as Dn3 = I[5:3], Dn2 = I[2:0], Dn1 = Q[5:3], and Dn0 = Q[2:0] with even parity.

Figure 13 shows an example of the input port data interface timings for the MAX5861 for OFDM mode, where SDCLK is the input DDR clock and pins DCP/N[8:0] are shared by three OFDM channels: i.e. pins [8:6] Ch3, [5:3] Ch2, [2:0] Ch1. The SYNC[1:6]P/N signal is used to define the symbol boundary and carry the bit loading index information. The SYNC signal is high during the last 2 sample cycles of the cyclic prefix period.

If a channel is not being used, it can be disabled using the SPI interface (mute bit or power-down bit), or its corresponding SYNC being low while asserting logic 0 on the unused port pins. The SYNC symbol start indication triggers the IDFT processing. If SYNC is held low, all subcarriers are effectively muted, muting the entire 192MHz block. Under the normal operating conditions, SYNC (after symbol boundary has been identified) will be indicated periodically with the period of N+CP samples. The MAX5861 will be expecting SYNC to appear once in every symbol period at same location within the symbol period. If SYNC is not found at the expected location, all the following symbol period's IFFT payload will be sent as 0s, effectively muting the entire 192MHz block.

Configure the OFDM channel while muted. The channel can be reconfigured while the 192MHz block is muted by using SYNC and restarting normal operation by sending the new SYNC signal (which indicates the new symbol boundary).

Table 4. Port/Pin Mapping for Each OFDM Channel

PIN NAMES	FUNCTION	ASSOCIATED DATA	OFDM CHANNEL INDEXING
OFDM mode			
SYNC1P/N	Ch#1 frame sync & gain ctrl	Port#B DCP/N[2:0]	OFDM Ch#1
SYNC2P/N	Ch#2 frame sync & gain ctrl	Port#B DCP/N[5:3]	OFDM Ch#2
SYNC3P/N	Ch#3 frame sync & gain ctrl	Port#B DCP/N[8:6]	OFDM Ch#3
SYNC4P/N	Ch#4 frame sync & gain ctrl	Port#C DCP/N[2:0]	OFDM Ch#4
SYNC5P/N	Ch#5 frame sync & gain ctrl	Port#C DCP/N[5:3]	OFDM Ch#5
SYNC6P/N	Ch#6 frame sync & gain ctrl	Port#C DCP/N[8:6]	OFDM Ch#6
Bypass mode			
SYNC1P/N	Port B valid/sync port	Port#B DCP/N[8:0]	Bypass Mode Port#B
SYNC4P/N	Port C valid/sync port	Port#C DCP/N[8:0]	Bypass Mode Port#C

The incoming data stream indicates the symbol period boundary and gain information for each subcarrier using SYNC (via the SYNC input pins for the corresponding channel). Each of the 4096/8192 subcarrier's data is sent to MAX5861 using 3-bit wide data, while the associated subcarrier gain index value or pilot gain index value, per sample, is indicated by reusing the SYNC pin as shown in the timing diagram below.

As shown in the Figure 13, the symbol boundary is indicated by the SYNC pin as transition of 0 to 1 and staying logic 1 for eight clock transitions (two 204.8MHz sample widths), the DDR cycle immediately following this pattern defines the symbol boundary and the subcarrier index 0 data (Dn3, Dn2, Dn1, Dn0) is present in current and next 3 DDR cycles. At the same time SYNC carries the bit loading information (Bi3, Bi2, Bi1, Bi0) in the 4 DDR cycles for the corresponding sub carrier. The table below shows the bit loading information. The different gain values used for different QAM mapping type are programmed in a 14 x 8 register array using the SPI interface. This programmed gain value is fetched and applied based on the bit loading information received during the symbol reception. To increase the resolution of the constellation map and to make the constellation diagram symmetric, a 2x+L operation is performed on the each incoming data byte x, where L = 2n-1 and value of n can be programmed similar to the gain values for different QAM mapping type. The valid value of n can be programmed between 0-7 as 4K/2K-QAM n=1, 1K/512-QAM n=2, 256/128-QAM n=3, 64/32-QAM n=4, 16-QAM n=5, and QPSK n=6. The programmed value of n is ignored for the bit loading values of 0, 8 and 15 as shown in Table 10.

The input clock (SDCLK) is to be applied to the port shifted 90 degrees from the port B and port C input data as shown in Figure 13.

The incoming bit loading information indicates the pilot location to the MAX5861 by choosing the value of 8, and the MAX5861 performs the pilot insertion by replacing the received data value with the mapped LFSR output, and applying the appropriate gain. After applying the spectrum equalization gain (via SPI settings for the 128 or a programmable subcarrier groups) on the received data stream and pilot data, the incoming data is stored in the 16-word-deep input FIFO. This input FIFO is used to remove the clock phase offsets. The output from this FIFO is fed into the IFFT processing block, where the data for a complete symbol period i.e. 8192 x 28 bits is stored.

Each OFDM channel is independently capable of supporting different IDFT points and various possible guard interval lengths. The MAX5861 supports 4K/8K points IDFT (TU) and guard interval length (TG) of 192 to 1024 samples configured into both the FPGA and the MAX5861. Out of the total samples TG+TU received by the device, the meaningful samples which carry the data (TU), and the remaining sample slots can be considered as idle periods.

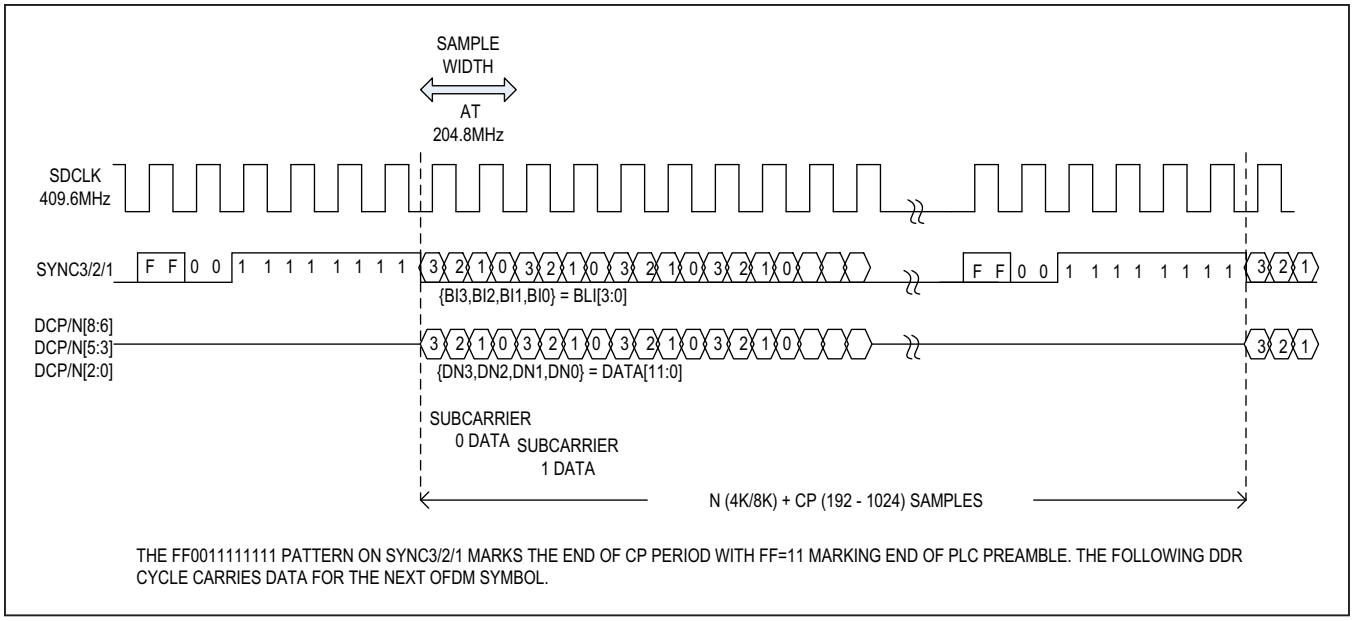


Figure 13. OFDM Channel Input Interface Timing

Figure 14 shows the detailed block diagram of the input data interface. The LVDS/SSTL interface receives DDR-pulsed input data, captures it on both transitions of SDCLK, and converts the data to full SDCLK clock cycle wide signals. This data is then captured by the LVDS/SSTL input demux and converted into a 12-bit bus. This input demux is a high-speed interface block that converts the serialized 3-bit data per OFDM channel, received on the data inputs (DP/N) in two clock periods of SDCLK, into 12 bits of parallel data in one clock cycle of SDCLK_D2 (divide-by-2 of SDCLK).

Subcarrier Gain Control

Within the same OFDM symbol, there can be different QAM modulation depths for each subcarrier, and it will be required to adjust the power levels for different subcarrier's data information for best dynamic range. Each OFDM sample can have power level adjustment using the 4-bits of gain select via the alternate use of the SYNC pins. An SPI-programmable 14 x 8 lookup table will be used to select one of fourteen 8-bit gain values for each subcarrier. A 6-bit gain value can be used and is sufficient to balance the average QAM power level to within 0.1dB for all the data subcarriers.

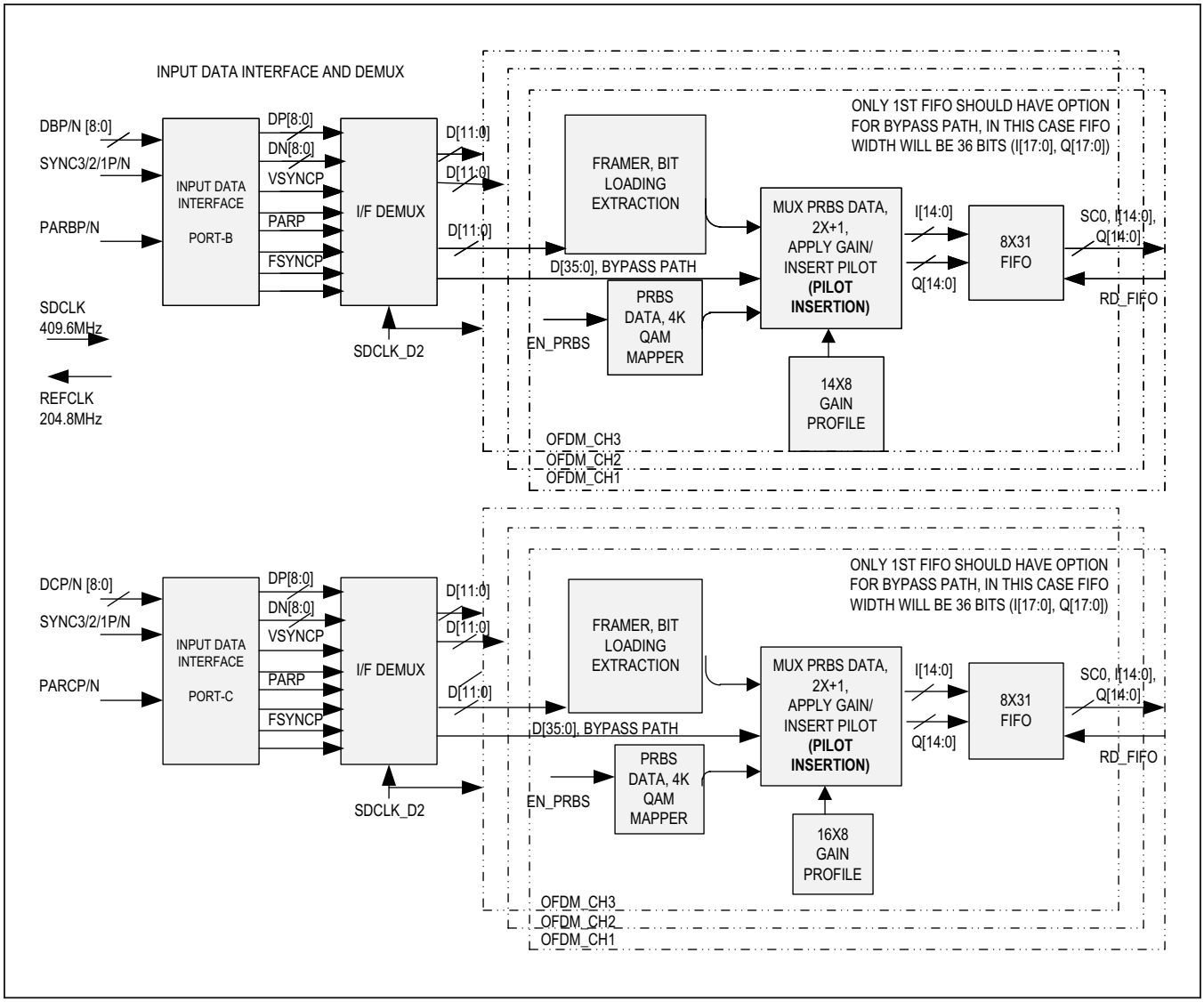


Figure 14. Input Data Interface Detailed Block Diagram

If the current subcarrier is indicated as pilot ('n'=8), then pilot insertion and pilot boosting is performed. The gain for continuous and scattered pilots, its level selection (-1/+1, +1/-1, 0/+1 or +1/0) will be programmed using the SPI configuration bits.

The MAX5861 uses a lookup table for a 4-bit bit loading index which maps to an 8-bit gain value configured through SPI. Table 5 shows the subcarrier and pilot gain analysis using a 6-bit gain for the average subcarrier power balanced to within 0.09dB.

Data in Table 5 is calculated based on the assumption that the input data being sent for each QAM mode will be aligned to MSB bits of each 6 bits of I and Q data. By default, the following is performed on each subcarrier:

1) Apply the amount of half LSB addition to the input data received.
2) If current subcarrier is indicated as pilot, replace the input data with a mapped LFSR output.
3) Apply the gain on data received or pilot data, gain can also mute the current subcarrier.
4) Perform static gain equalization from the SPI configuration.

Table 5. Calculated Subcarrier and Pilot Gain

MODULATION	RMS	VALUE	AFTER GAIN	REAL GAIN	BINARY GAIN	DATA POWER
4KQAM	104.4988	78	8150.9067	77.965483	01001110	6.063750188
2KQAM	72.7186	112	8144.4872	112.038676	01110000	6.070593707
1KQAM	104.4605	78	8147.9205	77.994057	01001110	6.066932998
512QAM	72.6636	112	8138.3242	112.123522	01110000	6.077168946
256QAM	104.3072	78	8135.9646	78.108670	01001110	6.079687618
128QAM	72.4431	112	8113.6251	112.464842	01110000	6.103569908
64QAM	103.6919	79	8191.6562	78.572227	01001111	6.020434242
32QAM	71.5542	114	8157.1760	113.861974	01110010	6.057071989
16QAM	101.1929	81	8196.6237	80.512574	01010001	6.015168681
QPSK	101.8234	80	8145.8701	80.014040	01010000	6.069119
BPSK pilot	127	129	16383.0000			
BPSK, zbl	104	78	8112.0000	78.339420	01001110	6.105309785
				Max QAM offset using 6-bit gain value (4 distinct values)	0.09	dB
	6dB Pilot boosting gain value				128.056669	10000001

Note: Assumes even distribution of the QAM symbols

Note: Pilot boosting =128*10^(-1*(6+20*LOG10(104.4988/127))/20)

Table 6 describes the I/Q values expected out of the constellation map, based on the values received from the FPGA on the input data pins. The 6-bit I/Q input is internally converted to 7 bits for better resolution by adding the half LSB to each input I/Q data. The gain data received in the OFDM channel's associated SYNC input will be applied to the internal 7-bit I/Q bus, before calculating the Inverse Fourier Transform of the input data stream.

An additional static gain stage in the MAX5861 is used to equalize 128 (or a programmed number) subcarrier groups. This gain stage is useful to correct for rolloff channel characteristics. The sub carrier group size (120-128) along with the 13 bits starting frequency index which defines the start of the first subgroup is programmed. A constant gain value stored in the lookup table is applied over the entire group, and a total of 32 different values can be programmed. The subcarrier group size automatically doubles if 8K IDFT option is used. Table 7 below shows the index used for each of the look up table (32x8) values. In the Table LE is a 13-bit programmed lower band edge index, and SGS is an 8-bit subcarrier group size.

Table 6. Input Data Mapping for Different QAM Modes

QAM MODE	MAPPED I/Q VALUE (TWO'S COMPLEMENT FORMAT)	MSB ALIGNED ON INPUT BUS	INTERNALLY CONVERTED TO 7 BITS FOR BETTER RESOLUTION
4K	-32 to 31	-32 to 31	-63, -61, -59, …, -1, 1, …, 59, 61, 63
2K	-24 to 23	-24 to 23	-47, -45, …, -1, 1, …, 45, 47
1K	-16 to 15	-32 to 30	-62, -58, …, -2, 2, …, 58, 62
512	-12 to 11	-24 to 22	-46, -42, …, -6, -2, 2, 6, …, 42, 46
256	-8 to 7	-32 to 28	-60, -52, …, -12, -4, 4, 12, …, 52, 60
128	-6 to 5	-24 to 20	-44, -36, …, -12, -4, 4, 12, …, 36, 44
64	-4 to 3	-32 to 24	-56, -40, -24, -8, 8, 24, 40, 56
32	-3 to 2	-24 to 16	-40, -24, -8, 8, 24, 40
16	-2 to 1	-32 to 16	-48, -16, 16, 48
4	-1 and 0	-32 and 0	-32, 32
2	-1 and 0 (Q=0)	-26 and 26 (Q=0)	-52, 52

Table 7. Static Subcarrier Gain Configuration

LOWER FREQUENCY INDEX OF BAND	UPPER FREQUENCY INDEX OF BAND	GAIN FROM LOOKUP TABLE
LE	LE+SGS-1	LT_gain(0)
LE+SGS	LS+2*SGS-1	LT_gain(1)
LE+2*SGS	LS+3*SGS-1	LT_gain(2)
...	...	
LE+31*SGS	LS+32*SGS-1	LT_gain(31)

Pilot Modulation

There are two modes for pilot modulation. The first mode (default) includes only a frequency domain LFSR for the modulation. The second mode includes an additional time domain LFSR which requires indication of the PLC Preamble location. This additional Time Domain LFSR's output XORing with the frequency domain LFSR's output can be disabled using a configuration bit, which enables switching between the two modes.

The pseudo-random sequence along the frequency axis is generated using a 13-bit linear feedback shift register, shown in Figure 15 with polynomial ($x^{13} + x^{12} + x^{11} + x^8 + 1$).

This linear feedback shift register is initialized to all ones, that is, 0x1FFF, for the k=0 index of the 4K or 8K discrete Fourier transform defining the OFDM signal. The initialized value of the rightmost bit BF of the shift register is used for the subcarrier at *k=0*. The shift register is clocked only after this subcarrier. That is, the rightmost bit BF of the first clocked version of the LFSR is used for the subcarrier *k=1*. After that the LFSR is clocked once after each subcarrier and is reinitialized for the next OFDM symbol.

A 7-bit linear feedback shift register defined by the polynomial ($x^7 + x^3 + 1$) is used along the time axis.

This is initialized to 0x7F just before the first symbol after the PLC preamble. It is then clocked after every complete OFDM symbol. Hence, the first OFDM symbol following the PLC preamble uses the initialized bit B_T of the 7-bit LFSR.

So for every OFDM symbol the 7-bit LFSR generates a pseudo-random binary bit B_T. For every subcarrier the 13-bit LFSR generates a pseudo-random binary bit B_F. Based on these the MAX5861 generates a pseudo-random binary bit B for every subcarrier of every OFDM symbol using the following equation:

$$B = B_T + B_F$$

It is an exclusive-OR operation of the two binary bits B_F and B_T. The exclusive-OR operation of B_T with B_F is configurable, and when DIS_TIME_LFSR is set (default), the above equation becomes:

$$B = B_F$$

If this subcarrier is a continual or scattered pilot, the MAX5861 will BPSK modulate that carrier with the value B as defined below:

For both pilot modulation modes, the following mapping is used (BPSK_LVL=2).

B = 0: Subcarrier value = (1 + j * 0)
B = 1: Subcarrier value = (-1 + j * 0)

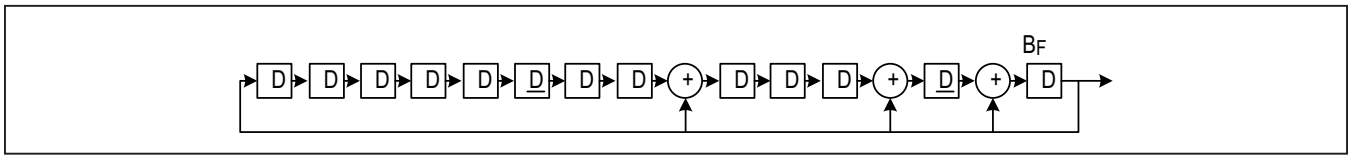


Figure 15. Frequency Axis 13-Bit Linear Feedback Shift Register for the Pilot Modulation

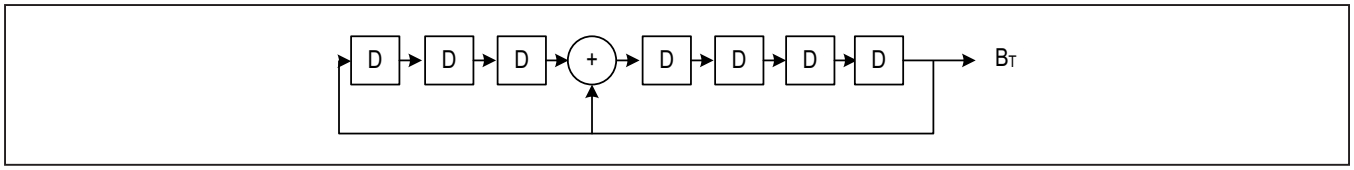


Figure 16. Time Axis 7-Bit Linear Feedback Shift Register for Pilot Modulation

Table 8. BPSK_LVL_SL[2:0] Mappings

LSFR OUTPUT	BPSK_LVL_SL=0	BPSK_LVL_SL =1	BPSK_LVL_SL =2	BPSK_LVL_SL =3
0	I=-1, Q=-1	I=+1, Q=+1	I=+1, Q=0	I=-1, Q=0
1	I=+1, Q=+1	I=-1, Q=-1	I=-1, Q=0	I=+1, Q=0

The MAX5861 pilot modulation function requires frame boundary indication for the second mode which requires the input interface protocol as shown in Figure 17. The additional F-bits in the diagram below (added F-bits on SYNCn pins) result in a FF0011111111 pattern to mark the end of an OFDM symbol. The two-dimensional LFSR requires alignment to PLC preamble and so the symbols need to be marked. FF=11 indicates the start of a frame (the frame structure is fixed and a frame start occurs every 128 symbols) and FF=00 indicates the continuation of a frame (a frame is composed of multiple symbols totaling 128). When the first mode of pilot modulation (using a single frequency domain LFSR only) is used, the FF bits are ignored.

Port B/C Bypass Mode

Port B and port C may each operate in bypass mode with one bypass channel of up to 192MHz (real bandwidth) without mapping or IFFT processing. Bypass mode uses 18 bits of I/Q data (four 9-bit DDR transfers) at 409.6MHz as shown in Figure 18. The input data transfer requirement for a bypass channel consumes all of the available bandwidth for a port. Since bypass mode receives raw data which is generated off-chip, any user-generated modulation scheme may be used as input (including but not limited to OFDM, DVB-C and DVB-C2).

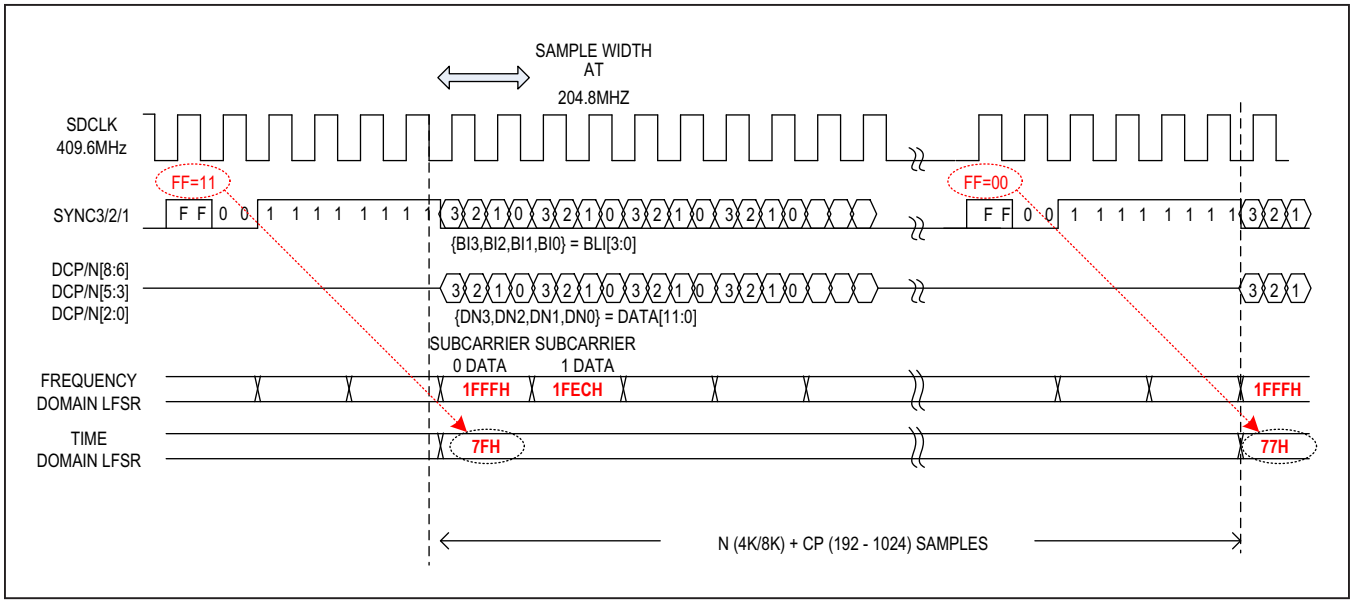


Figure 17. OFDM Channel Input Interface Timing Including PLC Preamble Boundary

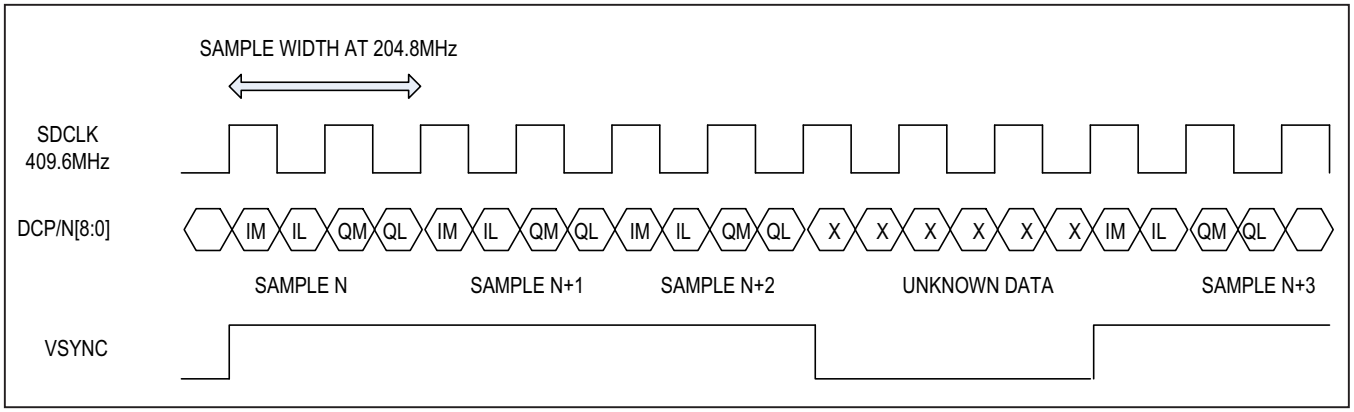


Figure 18. OFDM Bypass Mode Waveform

Port B would utilize OFDM channel signal processing path 1 and port C would utilize OFDM channel signal processing path 4 (as shown in Figure 12). The unused DSP of paths 2 and 3 and/or paths 5 and 6 would be powered-off.

The VSYNC signal, as shown in Figure 18, acts both as a sync marker and a data valid signal. The rising edge of VSYNC is edge-detected and used as the marker for the first data word transfer and VSYNC remains continuously high while the incoming data words are valid. VSYNC for port B maps to SYNC1 while VSYNC for port C maps to SYNC4.

PRBS

Individual PRBS (PRBS23) generators are available for use on each of the 6 OFDM channels (including bypass mode).

OFDM Configuration

The 14x8 table array is loaded via SPI using sets of seven registers GAIN_BAL_1_# through GAIN_BAL_7_# (where # is replaced by the appropriate channel number 1–6) starting at addresses 0x744, 0x752, 0x760, 0x76F, 0x77D, and 0x789. There is a 14x8 table array for each of the six OFDM channels.

Table 9. Bit Loading Index Decoding

{BI3,BI2,BI1,BI0} BIT LOADING INDEX ON SYNC PIN	DESCRIPTION	GAIN AND CONSTELLATION OFFSET SOURCE
0	Mute	—
1-7	Modulation type for any mapped data subcarrier, PLC, NCP MB	14x8 table Gain and constellation offset
8	Pilot	14x8 table Gain only
9-14	Modulation type for any mapped data subcarrier, PLC, NCP MB	14x8 table Gain and constellation offset
15	Reserved for determining frame boundary	—
Programmed ‘n'	Modified I value	Modified Q value
0	2X+1	2X
1-6	2X+L (L=2n-1)	2X+L (L=2n-1)
7	2X	2X

Table 10. Suggested 14x8 Table Gain and Offset

CONSTELLATION	I/Q (MSB ALIGNED)	SUGGESTED TABLE VALUES		
		8-Bit Gain (binary)	Constellation Offset (‘n’)	Notes
4KQAM	-32, -31, … , 30, 31	01001110	1	
2KQAM	-24, -23, … , 22, 23	01110000	1	
1KQAM	-32, -30, … , 28, 30	01001110	2	
512QAM	-24, -22, … , 20, 22	01110000	2	
256QAM	-32, -28, … , 24, 28	01001110	3	
128QAM	-24, -20, … , 16, 20	01110000	3	
64QAM	-32, -24, … , 16, 24	01001110	4	
32QAM	-24, -16, … , 8, 16	01110010	4	
16QAM	-32, -16, 0, 16	01010000	5	
QPSK	-32 and 0	01011010	6	
BPSK	-26 and 26 (Q=0)	01001110	7	(Zero bit-loaded subcarriers)
BPSK(pilot)	-26 and 26 (Q=0)	01001110	7	(if pilot modulation bypassed)
BPSK(pilot)	Ignored	10000001	Ignored	(if pilot modulation used)

A static gain stage is used to equalize programmed subcarrier groups and to correct for rolloff channel characteristics. The registers GAINEQ_ADD_* and GAINEQ_DAT_* are associated with the programming of 32 different 8-bit gain values which will be applied for each programmed GAINEQ_ADD_*. SGS subcarriers group starting from GAINEQ_ADD_*.GESE.

For example: if a g0, g1, … g31 on each 6MHz bandwidth channel starting with subcarrier index F=128 (F=0-4095 for 4K point IFFT or 0-8192 for 8K point IFFT) then GAINEQ_ADD and GAINEQ_DAT registers will be programmed in the following way:

1) For both 4k IFFT and 8k IFFT, the subcarrier group size (SGS) should be set to 120 (0x78).
2) Starting index of the gain balance band, GESE = 128(0x80).
3) The register GAINEQ_DAT_* is written multiple times to program the gain array. To program the 8x4 gain array (g0 ... g31), write the base address to GAINEQ_DAT_*.A [2:0]. Each read/write thereafter auto-increments the internal address.

The following SPI commands would be used:

```
0x742 0x000_80780          #GAINEQ_ADD_1 {7'h0,GESE,SGS,1'b0,A}
0x743 0x{g3,g2,g1,g0}      #GAINEQ_DAT_1
0x743 0x{g7,g6,g5,g4}      #GAINEQ_DAT_1
0x743 0x{g11,g10,g9,g8}    #GAINEQ_DAT_1
0x743 0x{g15,g14,g13,g12}  #GAINEQ_DAT_1
0x743 0x{g19,g18,g17,g16}  #GAINEQ_DAT_1
0x743 0x{g23,g22,g21,g20}  #GAINEQ_DAT_1
0x743 0x{g27,g26,g25,g24}  #GAINEQ_DAT_1
0x743 0x{g31,g30,g29,g28}  #GAINEQ_DAT_1
```

Note that reading/writing to 0x743 multiple times auto-increments the internal address register (in this case starting at address 0). The address can be set directly by writing to GAINEQ_ADD_# [2:0]. Table 11 describes the internal address assignments.

Table 11. Subcarrier Group Gain Equalization Assignments

GAINEQ_ADD_# [2:0]	GAINEQ_DAT_# [31:24]	GAINEQ_DAT_# [23:16]	GAINEQ_DAT_# [15:8]	GAINEQ_DAT_# [7:0]
0	G3	G2	G1	G0
1	G7	G6	G5	G4
2	G11	G10	G9	G8
3	G15	G14	G13	G12
4	G19	G18	G17	G16
5	G23	G22	G21	G20
6	G27	G26	G25	G24
7	G31	G30	G29	G28

$$w\left(\frac{N+N_{CP}+N_{RP}}{2}+i\right)=1.0,\quad \text{for } i=0,1,\ldots,\left(\frac{N+N_{CP}-N_{RP}}{2}-1\right)$$

$$w\left(i+\frac{N+N_{CP}+N_{RP}}{2}\right)=\frac{1}{2}\left(1-\sin\left(\frac{\pi}{\alpha\,(N+N_{CP})}\left(i-\frac{N+N_{CP}}{2}+1/2\right)\right)\right),$$

$$\text{for } i=\left(\frac{N+N_{CP}-N_{RP}}{2}\right),\ldots,\left(\frac{N+N_{CP}+N_{RP}}{2}-1\right)$$

$$\text{Here,}\quad \alpha=\frac{N_{RP}}{N+N_{CP}}$$

Figure 19. CM-SP-PHYv3.1-103-140610 OFDM Windowing Function

Windowing Function

The MAX5861 has hard-wired logic to generate the OFDM windowing function as well as a user-configurable lookup table in SRAM. Referring to CM-SP-PHYv3.1-I03-140610.pdf (Page No 77), the OFDM windowing function is described as shown in Figure 19.

Note: The final "1/2" term of the formula which is shown circled in red is not implemented in the MAX5861 hardware-logic. Analysis has shown that the missing "1/2" term does not affect ACP numbers. If we compare the hardware-implemented windowing function to the windowing function as specified in the standard (Wstd) we see the results plotted in Figure 20.

Figure 20 indicates that the maximum difference between the W_{IMP} and W_{STD} windowing functions is 0.01227 for N_{RP} = 64. The difference error minimizes as the length of the N_{RP} increases. From a real-world perspective, the difference between W_{IMP} and W_{STD} may not be detected.

However, full programmability of the windowing function is present in the MAX5861. Programmable registers are available to restore the windowing function to the exact specification of the standard or to any user-specified windowing configuration. The windowing function is stored in a 128 x 30 programmable lookup table which is implemented in SPI-accessible SRAM.

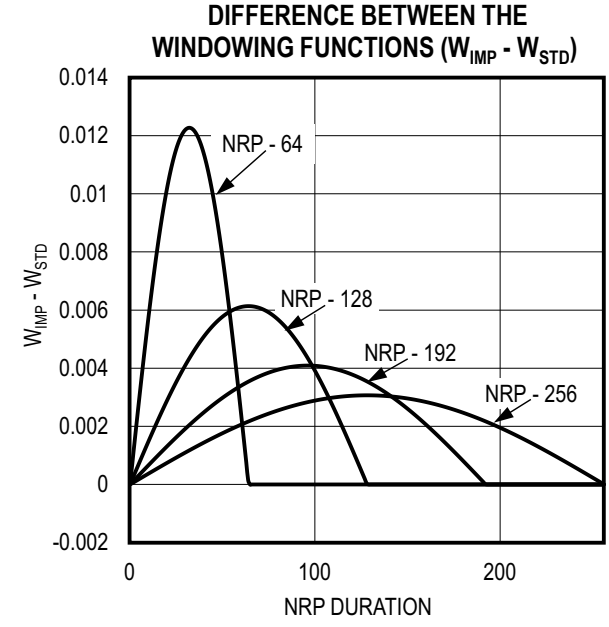


Figure 20. Effect Analysis of the Hardware Implementation (W_{IMP} - W_{STD})

Digital Predistortion (DPD)

DPD Function

The DPD block allows optimization of RF performance by correcting for distortion in the RF-DAC and the following RF amplifier chain. DPD is capable of correcting third-harmonic distortion (HD3), second-harmonic distortion (HD2), second- and third-order intermodulation products of the DAC and power amplifier, ($f_{DAC}/2$) - $2f_{OUT}$ spur in the RF DAC as well as the DAC interleaving errors. Figure 21 shows the top-level block diagram of the DPD.

- DAC Interleaving-Error Compensation: Since the DAC is updating on both clock edges, every other sample has an error resulting from the clock duty cycle being different by 50%. The DAC can also have a gain error in every other sample. The DAC interleaving compensation can correct for these two errors. By optimizing for these errors, the $f_{DAC}/2$ - f_{OUT} image is minimized. The block diagram of the DAC interleaving-error compensation block is shown in Figure 22.

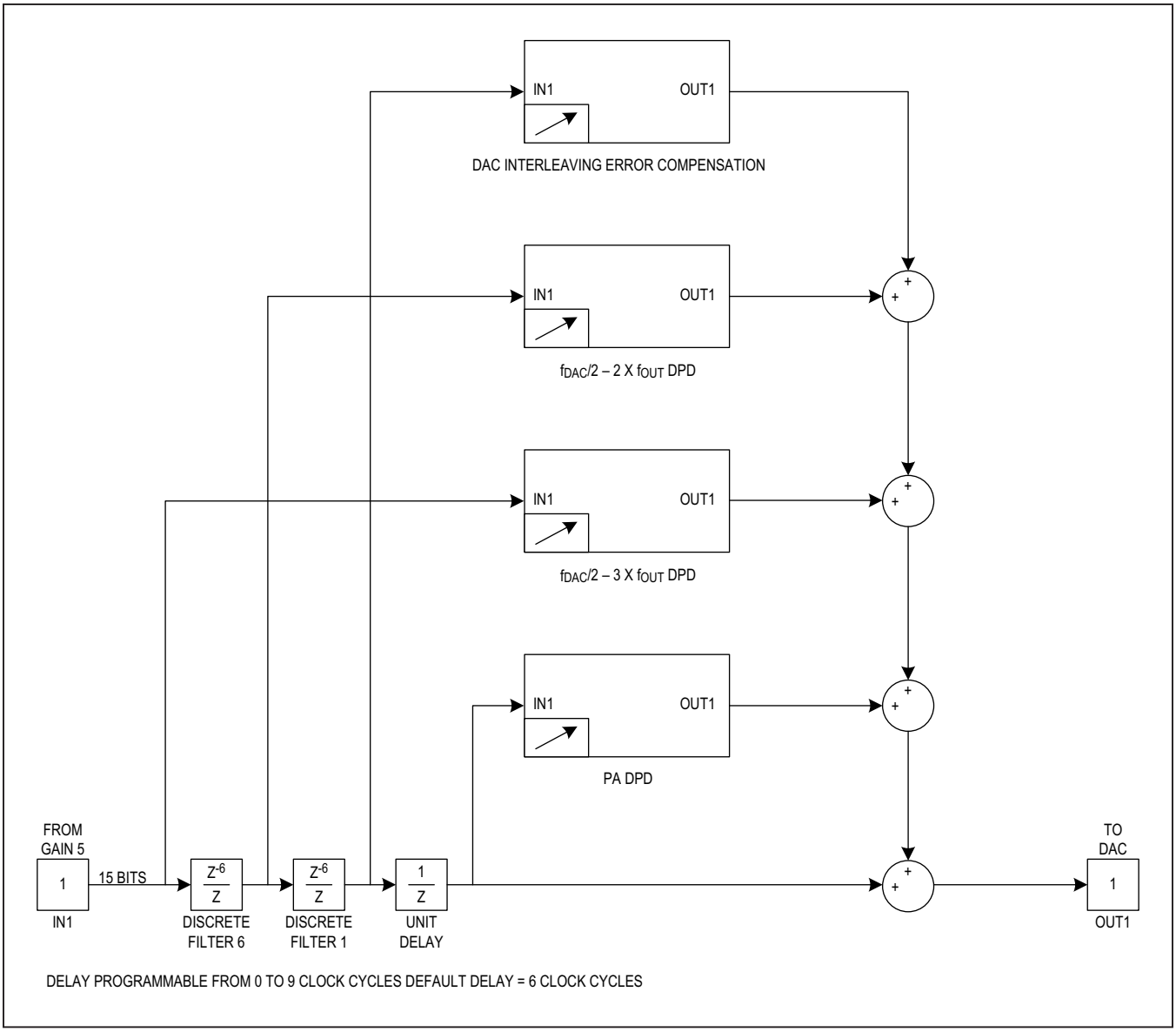


Figure 21. DPD—Top Level Block Diagram

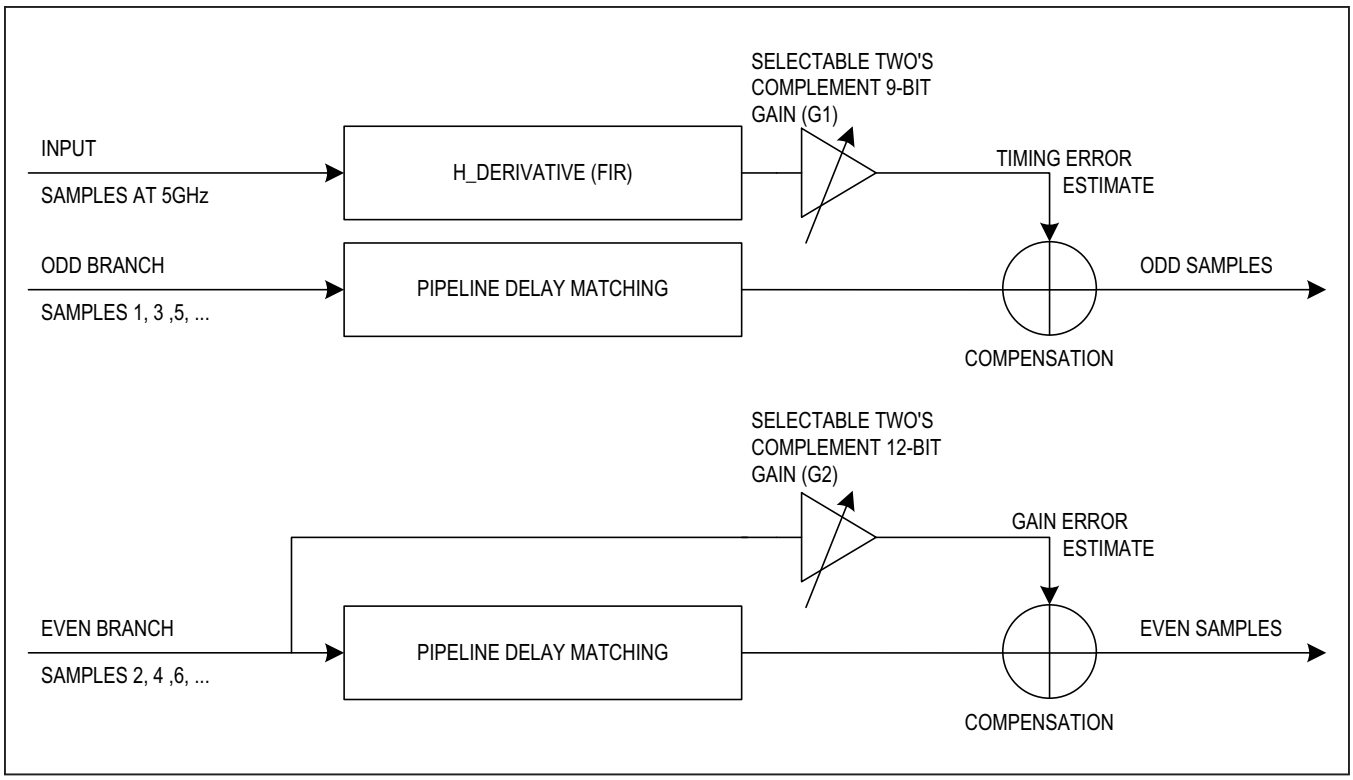


Figure 22. $f_{DAC/2}$ - f_{OUT} Correction Block

- PA DPD: This block allows correction for HD2, IM2, HD3, and IM3 that can be represented with the diagonal kernel of a third-order Volterra series. This is intended for correction of "classical" second- and third-order nonlinearities in the DAC and the following amplifiers. The block diagram of this block is shown in Figure 23.
- $f_{DAC}/2 - 2f_{OUT}$ DPD: This block allows for the correction of $f_{DAC}/2 - 2f_{OUT}$ spur. The block diagram of this section is shown in Figure 24.
- Static linearity correction: Corrects for deterministic gain error in 9 LSBs. Improves ACP by 1dB to 1.5dB and improves the DAC wideband noise floor by 2dB to 3dB. See Figure 25.

Using the SPI interface, program the gain for all DPD paths and delays for the paths as indicated in the previous block diagrams. Table 12 provides a summary of the programmable parameters, ranges, and resolution. Review the Register Descriptions section for programming information. The DAC interleaving compensation shown in Figure 22 contains two paths. Interleaving compensation adjusts for gain errors of every other sample, caused by either actual DC gain error or by clock duty-cycle error. The uppermost data path in this figure corrects for clock duty-cycle error. A duty-cycle error causes an error in the boundary between two samples that is proportional to the step size. In the uppermost data path, the step size is extracted and then every other step is extracted and scaled. The phase-correction filter aligns the phase of the correction signal with the transition between two adjacent samples. The lowermost data path extracts every other sample of the input signal and scales the input signal using the Gain 1 parameter. When added into the signal path, a gain adjustment for every other sample results.

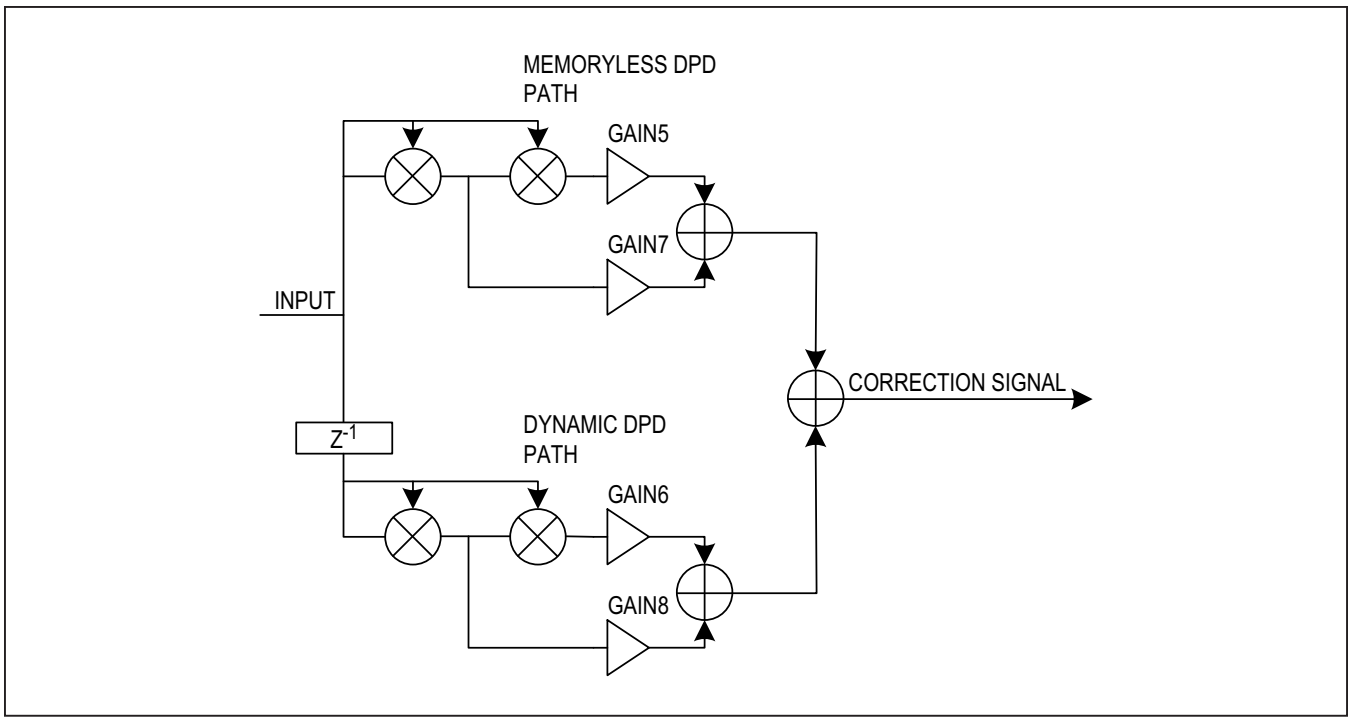


Figure 23. Correction for HD2/IM2, HD3/IM3 with Memory Effect

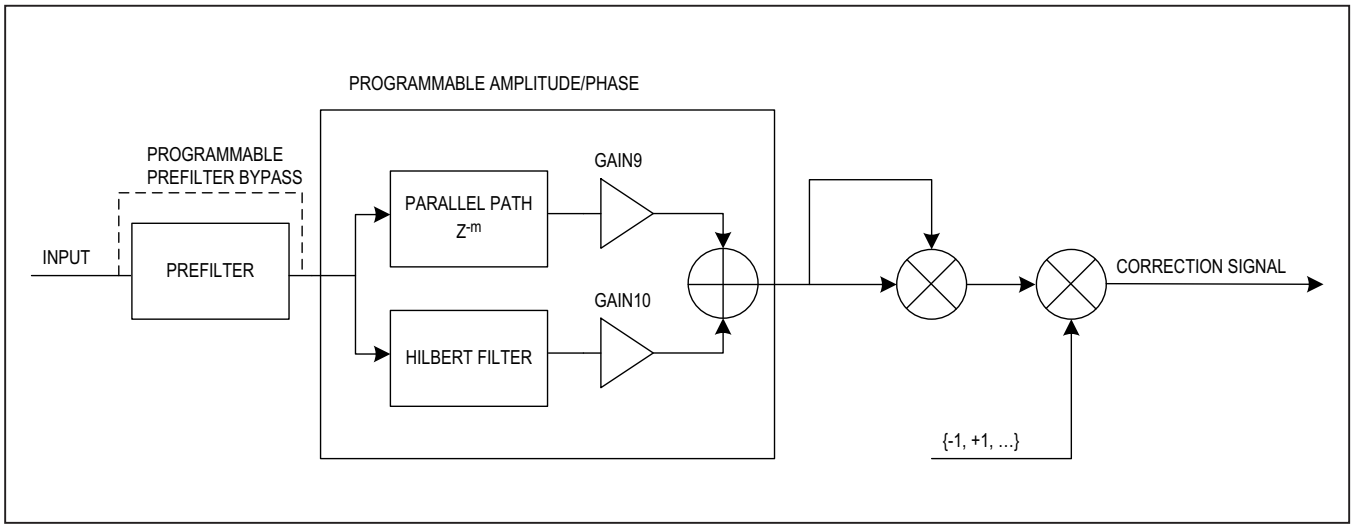


Figure 24. $f_{DAC}/2 - 2f_{OUT}$ DAC DPD

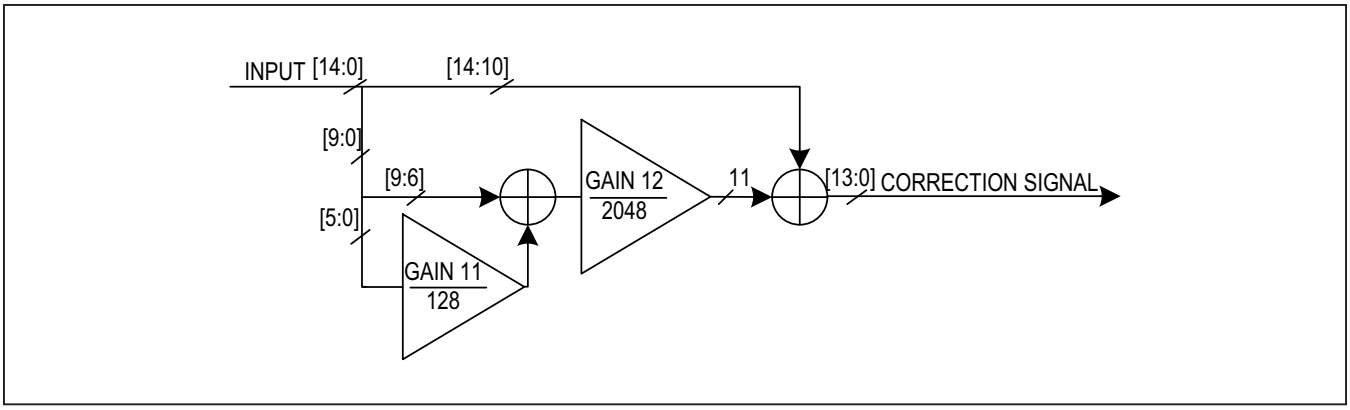


Figure 25. Static Linearity Correction Block

Table 12. DPD Parameters Range and Resolution

PARAMETER	RANGE	RESOLUTION	MIN TO MAX	UNSIGNED
Delay 1	0-15	1 DAC Sample	0 to 15	Signed
Delay 2	0-15	1 DAC Sample	0 to 15	Signed
Delay 3	0-9	1 DAC Sample	0 to 9	Signed
Gain 1	±1	9 Bits	-256 to +255	Signed
Gain 2	±1/8	12 Bits	-256 to +255	Signed
Gain 3	±1/512	12 Bits	-2048 to +2047	Signed
Gain 4	±1/512	12 Bits	-2048 to +2047	Signed
Gain 5	±1/32	12 Bits	-2048 to +2047	Signed
Gain 6	±1/32	12 Bits	-2048 to +2047	Signed
Gain 7	±1/32	12 Bits	-2048 to +2047	Signed
Gain 8	±1/32	12 Bits	-2048 to +2047	Signed
Gain 9	±1/32	8 Bits	-128 to 127	Signed
Gain 10	±1/32	8 Bits	-128 to 127	Signed
Gain 11	0.75-1.125	8 Bits	96 to 144	Unsigned
Gain 12	0.9375-1.06	12 Bits	1920 to 2172	Unsigned

Note: Gain 1-10 registers in the DPD use two's complement data format

Gain can be programmed through the SPI interface for all digital predistortion paths and delays for some paths as indicated in the block diagrams above. Table 12 provides a summary of the programmable parameters, their range and resolution. Review the register descriptions section for programming information.

The $f_{DAC}/2 - 2f_{OUT}$ DPD block (Figure 24) includes a bypassable pre-filter with a nonlinear phase response that approximates the characteristics of the MAX5861's RF DAC spur. The pre-filter output feeds a Hilbert filter and a parallel path, which produce -90N and 0N phase shifts, respectively. A weighted sum of these two is squared and modulated with Q1 to calculate the block's DPD out-put. The modulation pattern is programmable and can start with either +1 or -1 for the first output sample, and alternates for the rest of the seven output samples from the DPD. The Hilbert filter is scaled by the gain coefficient Gain 10, and the parallel path with 0 N phase shift is scaled by the gain coefficient Gain 9.

The static linearity correction block is shown in Figure 25. This block sits on the output of the DPD and directly drives the RF DAC. The algorithm has two user-programmable gains to adjust the LSB to MID segment boundary and the MID/LSB to MSB segment boundary. Gain 11 has a programmable range from 96 to 144 (<register value>/128, 128±16, reset value 128) and gain 12 has a programmable range from 1920 to 2176 (<register value>/2048, 2048±128, reset value 2048). Gain 11 and Gain 12 have registers for storing the user defined values.

When the DPD block is in normal functional mode, the latency is Delay 3 clock cycles longer than when the block is in functional bypass mode.

By default after global reset, all gains (Gain 1 - Gain 10) default to zero, Gain 11 defaults to 128 and Gain 12 defaults 2048. The DPD block takes 15-bit input signals and removes the LSB to form a 14-bit-wide signal. Gains (Gain 1 - Gain 10) need to be configured for the DPD to begin calculations. After reset, Delay 1 = 1, Delay 2 = 12, and Delay 3 = 6. Program these delay registers to the appropriate values if needed. The Delay 3 value is used as it is for $f_{DAC}/2$ - 2 x f_{OUT} DPD block. (Delay 3 + 6) value is used for interleaving compensation DAC DPD. (Delay 3 + 6 + 1) is used for both PA DPD and undistorted signal passing to the output. The maximum value of Delay 3 that can be programmed is 9; any higher number defaults to 9.

Digital-To-Analog Converter

Synthesizable Bandwidth vs. Clock Rate

The DSP receives a clock from the DAC with frequency f_{DSP} equal to 1/2 of f_{CLK}. The bandwidths stated elsewhere in this data sheet can be synthesized with a clock frequency of 1024MHz or higher. The bandwidth of all the filters behind the resampler is proportional to the clock rate. A clock rate higher than 1024MHz results in a higher synthesizable bandwidth. The synthesizable bandwidths, taking the clock rate into account, are:

- Octal-channel SCQAM combiner: 48MHz x f_{DSP}/1024MHz
- 32-channel SCQAM combiner: 192MHz x f_{DSP}/1024MHz
- Continuous bandwidth that SCQAM channels can be placed in: 768MHz x f_{DSP}/1024MHz
- Maximum bandwidth that SCQAM channels can be placed in: 960MHz x f_{DSP}/1024MHz

Reference System

The MAX5861 supports operation with the on-chip 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source or as the internal reference output if the DAC is operating with the internal reference. For stable operation with the internal reference, decouple REFIO to DACREF with a 1µF capacitor. Since REFIO has a 10kΩ series resistance, buffer REFIO with an external amplifier to drive external loads.

The MAX5861's reference circuit (Figure 26) employs a control amplifier, designed to regulate the full-scale current (I_{OUT}) for the differential current outputs of the DAC. The bandwidth of the control amplifier is typically less than 100kHz. The DAC full-scale output current can be calculated as follows:

$$I_{OUT} = 128 \times I_{REF} \times 16383/16384$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$) and I_{OUT} is the full-scale output current of the DAC. With an external reference voltage of 1.25V, R_{SET} is typically set to 2kΩ, resulting in a full-scale current of 80mA and maximum 9.46dBm output power for a continuous wave (CW) signal. Generally, the dynamic performance of the DAC improves with increasing full-scale current.

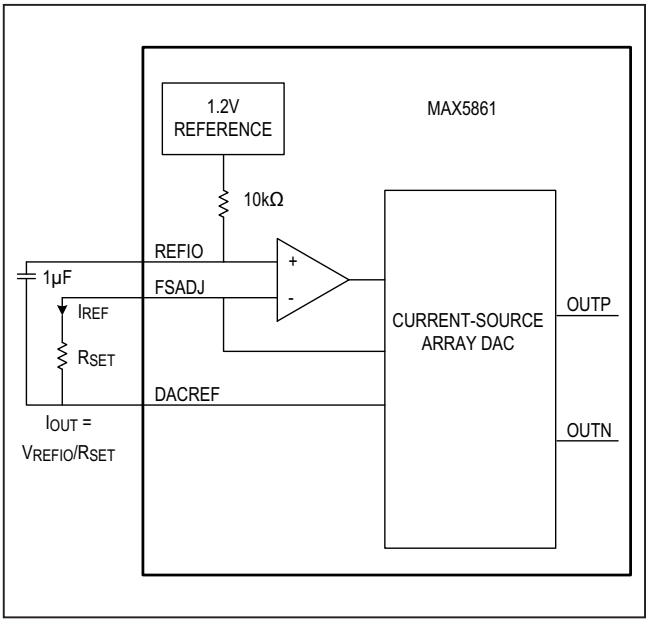


Figure 26. Reference System Architecture

Analog Output

The MAX5861 contains a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to AVDD3 providing a 50Ω differential output resistance. In addition to the signal current, a constant 40mA current sink is connected to each DAC output. Figure 27 shows an equivalent circuit of the internal output structure of the MAX5861. The circuit has some resistive, capacitive, and inductive elements. The output uses a resistive differential 50Ω load.

The outputs need to be pulled up externally to AVDD3. It is recommended that inductors be used for this purpose as shown in Figure 28. The use of discrete inductors and capacitors allows for near perfect symmetry in the output circuit layout. An external 50Ω differential load is also required to avoid excessive voltage swings at the DAC output pins.

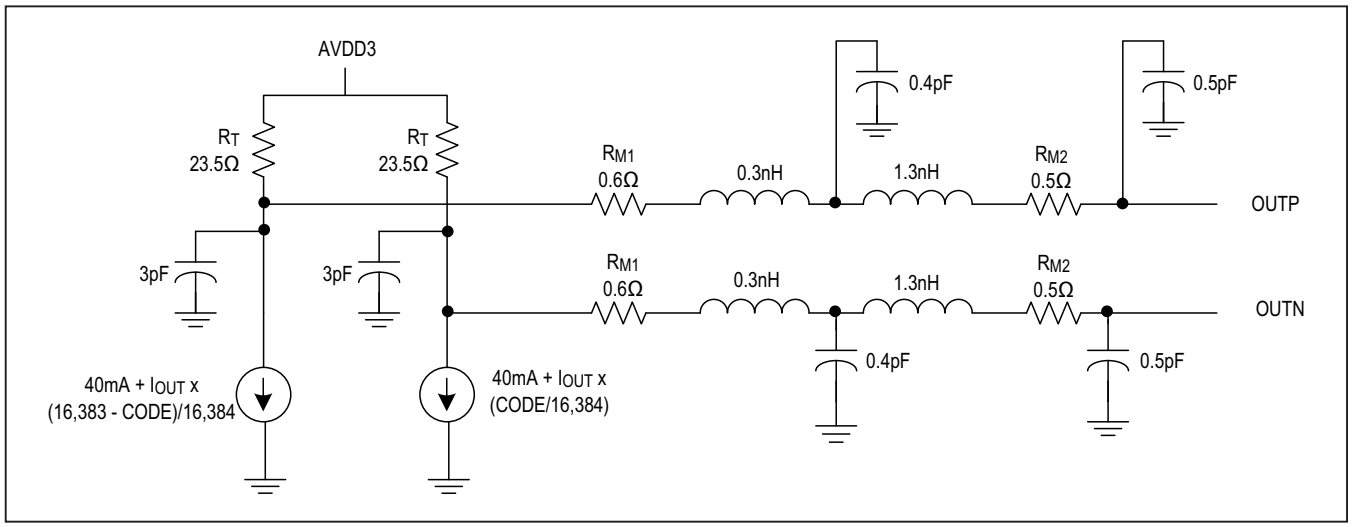


Figure 27. Equivalent Output Circuit

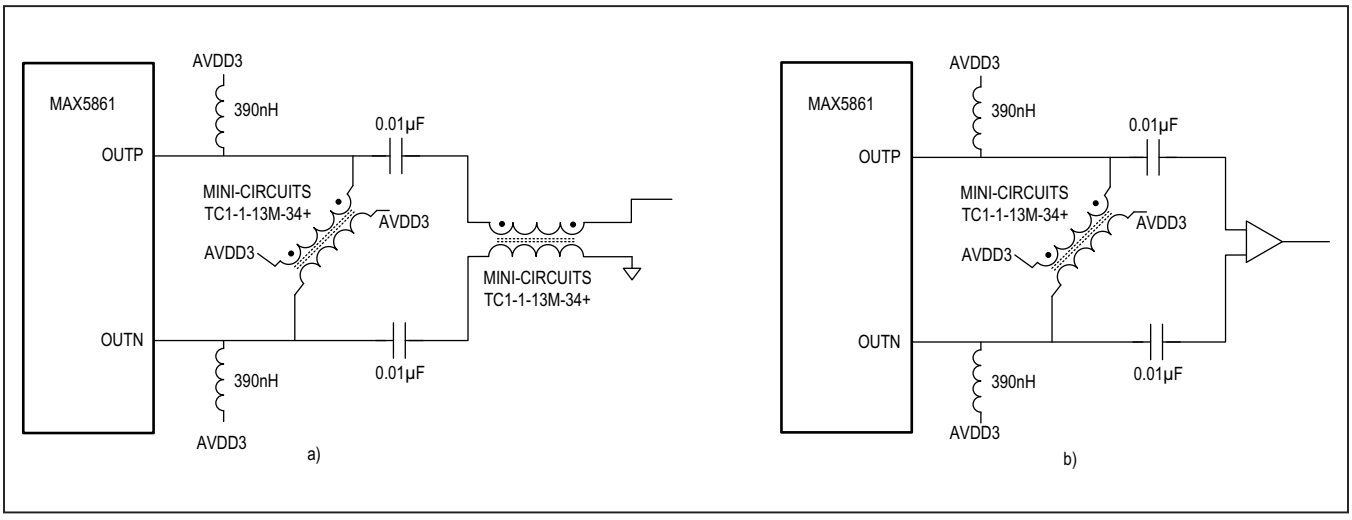


Figure 28. Balun Transformer Output (a) and Amplified Output Configuration (b)

Clock Inputs

The MAX5861 has a universal, differential clock input (CLKP, CLKN) operating from a separate power supply (AVCLK) to achieve the best possible jitter performance. The two clock inputs should be driven from a differential clock source. A sine wave or a square-wave signal can be used.

Each clock pin is internally DC-biased to 1/3 the supply voltage AVCLK. A sinusoidal clock that is AC-coupled to the DAC clock inputs should be used. See the *Clock Duty Cycle* section for important design requirements. The clock input has an internal 100Ω differential termination resistor. For 50Ω (differential) termination at high clock frequencies, an additional external termination resistor is required between CLKP and CLKN. The balanced input should be AC-coupled unless the common-mode of the clock source is within the specifications for the MAX5861's RF-DAC clock input (CLKP/CLKN). An example of a well-balanced single-ended to differential application circuit using three baluns is shown in Figure 29.

Clock Duty Cycle

The MAX5861 input clock is supplied at a frequency (f_{CLK}) that is one half the DAC update rate (f_{DAC}). The DAC output updates on both edges of the clock. Deviation from a balanced duty-cycle will contribute to images in the output spectrum. The magnitude of the images is dependent on the absolute value of the deviation from an ideal 50% duty cycle. These artifacts will occur at the following frequencies:

$$f_{IMAGE} = (f_{DAC}/2) \pm f_{OUT}$$

To minimize the image at $f_{DAC}/2 - f_{OUT}$, the clock duty-cycle should be close to 50%. A filtered sine wave will have this characteristic. An offset voltage at the input of the clock input buffer will cause a duty-cycle change. The duty-cycle change in percent is approximately (100%) x V_{OFS}/Ampl where V_{OFS} is the offset voltage and Ampl is the peak clock input amplitude.

With a clock amplitude of 1V peak (differential), an offset of 3.14mV would shift the duty cycle from 50.0% to 50.1/49.9%. Alternatively, the amplitude of the odd and even input data channels can be adjusted to remove the $f_{DAC}/2 - f_{OUT}$ component. For example, the gain of the digital data into channels A and C can be slightly adjusted up or down to remove the $f_{DAC}/2 - f_{OUT}$ image, see the *Digital Predistortion (DPD)* section.

LOCK Signal

The LOCK pin is an output signal. When SE is logic-low (0V), the LOCK signal indicates the lock condition of the DLL circuit; LOCK is logic-high (1.8V) when the DLL is locked. The LOCK can be a logic-low level even if the DLL is locked, as it will be triggered when the DLL if required to shift more than a set amount. A better indicator of the health of the DLL and data alignment and interface is the PERR signal.

SPI Interface

The MAX5861 contains a slave SPI interface. Data transfers are initiated by the master, which generates the SCLK and SS signals. The MAX5861 receives serial data on SDI and transmits serial data on SDO. Since SDO remains in high impedance except when the MAX5861 is transmitting data to the bus master, SDI and SDO may be tied together to form a three-wire interface if desired.

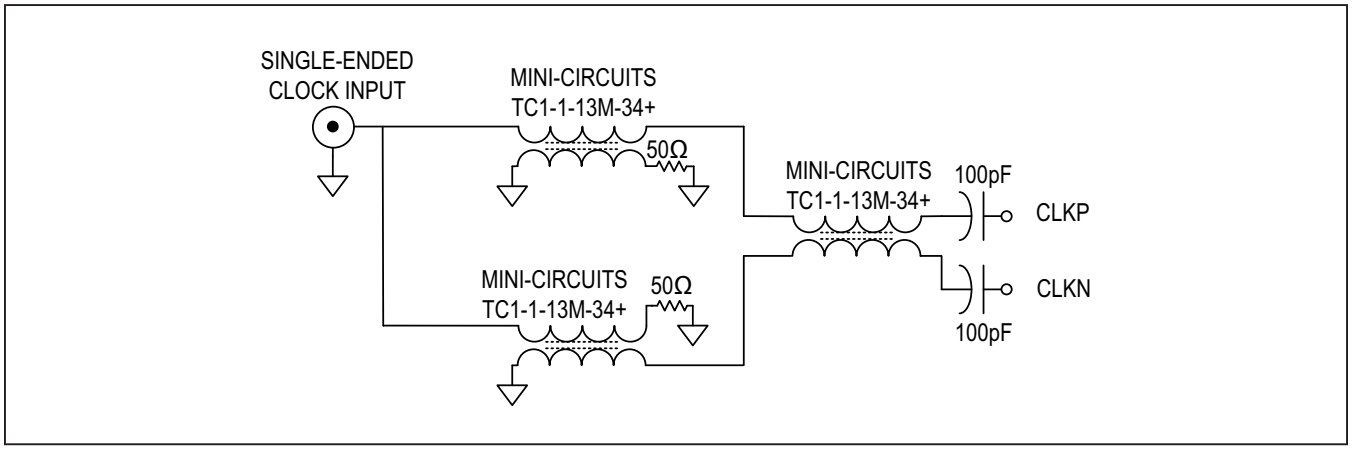


Figure 29. Balanced RF DAC Clock Interface Circuit for MAX5861

The addressing of the SPI port is accomplished using the SS select signal. Drive SS high between SPI commands. SCLK can be discontinuous. Timing for the SPI interface is shown in Figure 30.

SPI Command Format

The basic SPI command consists of 56 bits:

- read/write bit
- multi_adr_flag
- 3 idle bits
- 4 bit hardwired package address
- 11-bit address field
- 2 idle bits
- 32-bit data field
- 2 to 8 termination bits

The read/write bit is set to logic 1 for reads and logic 0 for writes. The multi_adr_flag is 0 for a single address read/write, and 1 for a multi-address (burst) mode read/write. The idle and termination bits are not decoded so they can be set to either 0 or 1. Drive SS to logic 0 (select) at the beginning of a frame, and it must be set to logic 1 (deselect) at the end of the frame. A read or write data word is always 32 bits wide. The SPI command may be extended using burst mode.

Hardwired Package Address

Each MAX5861 package is assigned a 4-bit hardware address by setting logic values on the hardwired package address balls (SA3-SA0). This allows multiple devices to be paralleled on the SPI bus. It is recommended that if this feature is not desired, the SA pins may be connected to ground and zeros be sent in the SPI command header for the hardwired address.

Write Command

Set the read/write bit to logic 0 and set multi-adr_flag to logic 0 for a single address write. Figure 31 shows the write command waveform. SDO maintains a high-impedance state during write operations.

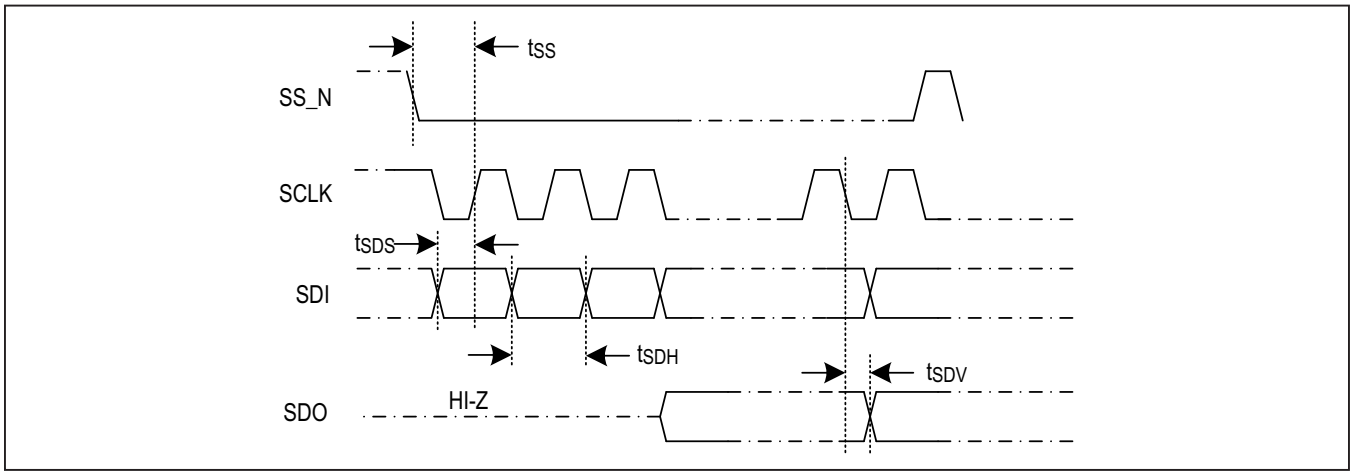


Figure 30. SPI Timing Diagram

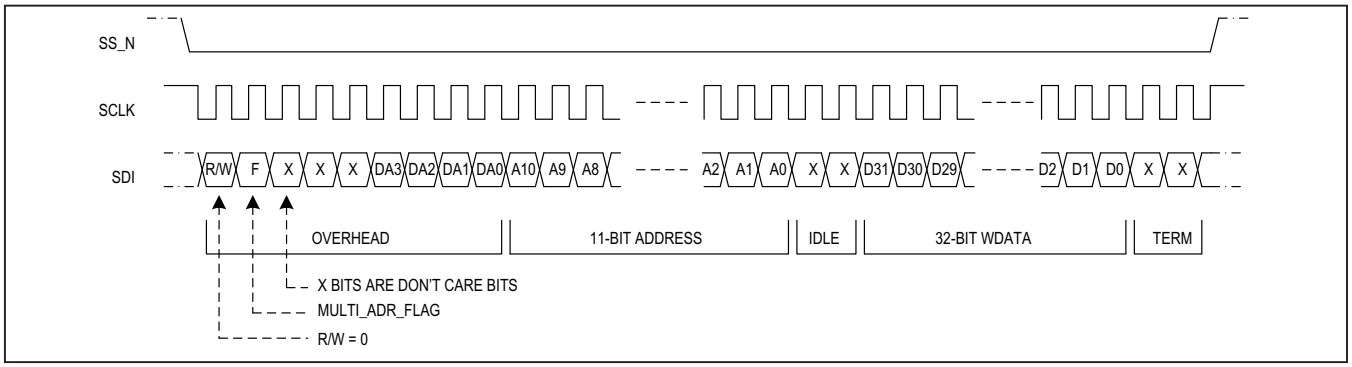


Figure 31. SPI Write Waveform

Read Command

Set the read/write bit to logic 1 for an SPI read and set multi-adr_flag to logic 0 for a single address read. Figure 32 shows the read command waveform. After receiving the address, SDO switches from a high-impedance state to outputting the requested 32-bit data. SDI and SDO can be connected together if a 3-wire interface is desired.

SPI Burst Mode Write Command

The time required to configure the MAX5861 can be significantly shortened by using SPI burst mode. Burst mode, which auto-increments the write addresses, is activated by setting the multi_adr_flag to 1. In burst mode, the basic 56-bit SPI command sets the initial address and data word, and every 32-bit data word which follows while SS remains low (active) auto-increments the write or read address.

There is not a limit to the number WDATA words being sent. If at least the first 2 clocks are received in the final write data (WDATA+n) word, then the previous write data word (WDATA+n-1) will be written; if less than 32 bits are received for WDATA+n and/or it is not terminated by at least 2 TERM bits, then WDATA+n will not be written.

Figure 33 describes burst-mode operation for writes using terminology as established in Figure 31. In Figure 33, the basic 56-bit SPI write command is shown as the leading 56 bits on the command (the bits from OVERHEAD through IDLE). The initial write address is established by ADDRESS. Additional 32-bit write data words follow the IDLE bits, each consecutive WDATA word being sequentially written to ADDRESS+1, ADDRESS+2,… ADDRESS+n addresses. The TERM bits, which end the burst mode sequence, can be 2 to 8 bits in length.

SPI Burst Mode Read Command

Burst mode, which auto-increments the read addresses, is activated by setting the multi_adr_flag to 1. Figure 34 describes burst-mode operation for reads using terminology as established in Figure 32. In Figure 34, the basic 56-bit SPI read command is shown as the leading 56 bits on the command (the bits from OVERHEAD through IDLE). The initial read address is established by ADDRESS. Additional 32 bit read data words follow the IDLE bits, each consecutive RDATA word being sequentially read from ADDRESS+1, ADDRESS+2,…

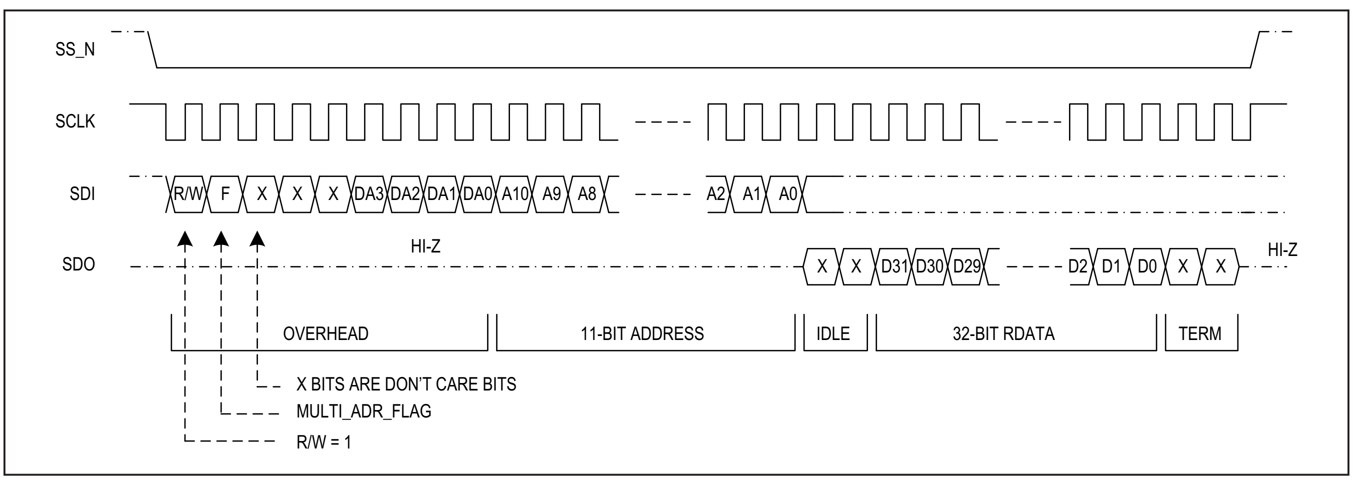


Figure 32. SPI Read Waveform

SDI: OVERHEAD – ADDRESS – IDLE – WDATA – IDLE – WDATA – WDATA – WDATA - … – WDATA - TERM

Figure 33. Burst Mode Write

SDI: OVERHEAD – ADDRESS –

SDO: – – – – – – – – – – – – – – IDLE – RDATA – IDLE – RDATA – RDATA – RDATA - … – RDATA - TERM

Figure 34. Burst Mode Read

ADDRESS+n addresses. The TERM bits, which end the burst-mode sequence, can be 2 to 8 bits in length. There is not a limit to the number RDATA words which can be received. SDO switches from high impedance to logical output immediately after the read address is received. The first read data word is prefixed by two IDLE bits which are ignored.

SPI Burst Mode Debug Registers

To help debug the large packets which may be generated during burst mode, two debug registers are provided. These registers are updated during burst mode (multi_adr_flag=1 and for data after the first 56 bits) but are left unchanged during single address mode (multi_adr_flag=0). Therefore, to read the debug registers, follow the multi-address burst-mode write or read by single address mode (multi_adr_flag=0) register read of these registers.

The SPI burst-mode checksum register (SPI_BM_CHKSUM address 0x007) provides a checksum (32 LSB sum) of the WDATA words starting from WDATA+1 onwards (i.e. not including the first data in the first 56 bits). This would be the checksum of all the WDATA words following the IDLE bits as shown in Figure 33. Checksum example: Summing data words 0xF6501100, 0xF010F600, 0xCC010000, 0xBC000012 yields a checksum of 0x6E620712.

The SPI burst-mode debug counters register (SPI_BM_CNTS address 0x006) provides access to two counters. The address increment counter (ADD_INC) counts the number of addresses which were auto-incremented, and the SCLK positive edge counter (SCK_EDGE) counts the number of SCLK rising edges. These counters operate after the first 56 bits of a burst command.

It is always recommended that a few registers (especially at the end of the address range) be read to confirm the correct data.

SPI 3-Wire Mode

SDI and SDO can be connected together if a 3-wire interface is desired. SDO is normally in a high-impedance state until after receiving the address, then SDO switches from a high-impedance state to outputting the requested 32-bit data. SDO maintains a high-impedance state during write operations.

In read mode, SDO switches from high-impedance to a driven state during the idle period after the address. To avoid contention in 3-wire mode, data should cease being driven after the address is sent and specifically during the idle bit period to allow the chip to start driving the output.

Global Reset

The external global reset input RST_N asynchronously clears all registers and flip-flops in the design. The external global reset signal may be applied and removed asynchronously. Internally, reset is asynchronously applied to all flip-flops in the design and it is synchronously removed by use of the CLK and SDCLK (OFDM) clock signals. Global reset should be applied at each power-up.

SDCLK is required to synchronously remove reset from the OFDM input port logic. SDCLK should be applied a few clocks early (when the clock is stable) before port B or port C SYNC and symbol data are input.

Global G1 and G2 Gain Settings

Gain G1 [7:0] and G2 [10:0] global write operation is available by writing the GBL_G1_WRITE or GBL_G2_WRITE resisters. By writing one of these registers, the corresponding gain value for all 160 channels is simultaneously updated (overwritten). G1 or G2 gain values may be written to individual channels at any time after the global write.

Symbol Pattern Match Test

The SYMBOL_TEST register allows a programmable symbol value to be detected at the FIFO output of one of the 160 channels. This is useful to trace a symbol through the symbol input interface. The compare results are available in an SPI register or the DTO output.

The 10-bit expected symbol (EXP_SYM) can be configured to be detected at a selected channel (CHANNEL) FIFO output. An interrupt can be configured to signal when the symbol match is detected. The real-time status can be read (CMP_RT) or the latched event status (CMP_LAT). The real-time result of the symbol compare may also be observed at the DTO pin by setting the OEM_TEST register DSEL bits to 0x05.

Interrupts

All interrupt functions are enabled after reset by default; however, disabling the interrupt bit disables all interrupts. The interrupt flag is active-low. The interrupt flag is for information purposes only and does not otherwise affect the operation of the device. Interrupt sources can be individually disabled but interrupts cannot be disabled for individual channels. In normal operation, the interrupt flag remains at logic 1 (inactive).

Most interrupt sources signal a condition of degraded performance of the system. Following the detection of logic 0 on the interrupt output, read the interrupt source register to determine the source. Interrupt mode is selectable to be either event-detect (edge-detect) or real-time (level detect) for all interrupt sources. If the interrupt mode is event-detect, the interrupt source must be cleared before it will signal the next interrupt condition. Interrupt sources are cleared by writing a 0 to the appropriate bit location in the interrupt control register.

FIFO Overflow

Each of the 160 channels features a 16-word-deep FIFO. The channel RDY signal asserts high when the FIFO is accepting data, and asserts low to signify when the port stops writing data. The RDY signal asserts high when the FIFO count indicates that fewer than seven register locations are available. As a system-timing buffer, data writes are accepted by the FIFO when the RDY signal is low. When the FIFO is full and a write occurs, the interrupt bit of this channel is set and the interrupt flag is asserted logic 0 to signify the loss of data.

Each channel has an individual bit to signify an overflow condition. Muted channels cannot set a channel FIFO overflow flag bit.

FIFO Underflow

Each of the 160 channels features a 16-word-deep FIFO. The channel accepts data from the FIFO as needed at a rate commensurate with the symbol rate for that specific channel. When a channel is ready for the next symbol, it issues a read to the FIFO. When the FIFO stored word count is 0 and a read occurs, the interrupt bit for this channel is set and the interrupt flag is asserted low to signify a symbol is unavailable when requested by the channel. Each channel has an individual bit to signify an underflow condition. Muted channels cannot set a channel FIFO underflow flag bit.

Channel Capacity Exceeded (CCE)

The device is available with factory-set channel SCQAM capacities of 160 channels or less. Logic present on the input multiplexer limits the number of data channels to the factory-set channel capacity. Activating more than the factory-set number of QAM channels in the device causes the additional channel(s) not to activate and the CCE interrupt bit to be set.

Channels are activated one at a time by setting the channel mute bit to logic 0 through the SPI port. The CCE bit is set when the first channel activation over the channel-capacity limit is attempted. To clear the CCE bit, reduce the number of active channels to lower than or equal to the factory-set number (or default configuration, whichever is higher).

Phase Error

The phase error interrupt indicates that the relationship between the PSYNC and PCLK has changed. PSYNC is always captured with the positive edge of the PCLK if this capturing is violated, then it will be indicated by phase error, if associated interrupt enable bit is set high. This interrupt flag can be cleared by writing 0 at the bit location in the interrupt control register.

DAC Parity Error

The DAC parity error indicates a parity error occurred at the DUC and DAC data interface. This error is flagged when the parity value received from DUC did not match with the calculated value in the DAC. This interrupt flag can be cleared by writing 0 at the bit location in the interrupt control register.

DAC Lock

This interrupt indicates that the DLL has locked. This interrupt flag can be cleared by writing 0 at the bit location in the interrupt control register.

Symbol Port A Parity Error

When parity checking on symbol Port A is enabled, this interrupt indicates a parity error has occurred on port A. Even parity is calculated on the incoming symbol data and compared against the incoming parity value. This interrupt flag can be cleared by writing 0 at the bit location in the interrupt control register.

Symbol Port B/C Parity Error

When parity checking on symbol port B/ port C is enabled, this interrupt indicates a parity error has occurred on port B/ port C. Even parity is calculated on the incoming symbol data and compared against the incoming parity value. This interrupt flag can be cleared by writing 0 at the bit location in the interrupt control register.

Output Test Mode

This interrupt is set when the MAX5861 is put into output test mode (a manufacturing test mode). This interrupt flag can be cleared by writing 0 at the bit location in the interrupt control register.

Power Monitor Timer

The power-monitor block contains a counter that times the interval over which data collection occurs. An interrupt is generated once the counter counts down to zero. At that time the power-monitor registers can be read through the SPI interface. One power monitor timer is used by all power monitors.

Interrupt Tree

Figure 35 shows the device interrupt tree. The interrupt-flag enable bit is located as part of the global configuration register. System interrupts are FIFO overflow, FIFO underflow, output test mode enabled, power-monitor timer, and maximum channel capacity exceeded.

CFG Pin Usage

The CFG[4:1] pins provide a power-up hardware default to setting 192MHz block power-up configuration. The hardware default may be overwritten by SPI command. CFG4 is the MSB and CFG1 is the LSB. This configuration does not supersede the factory power-up configuration for product variants.

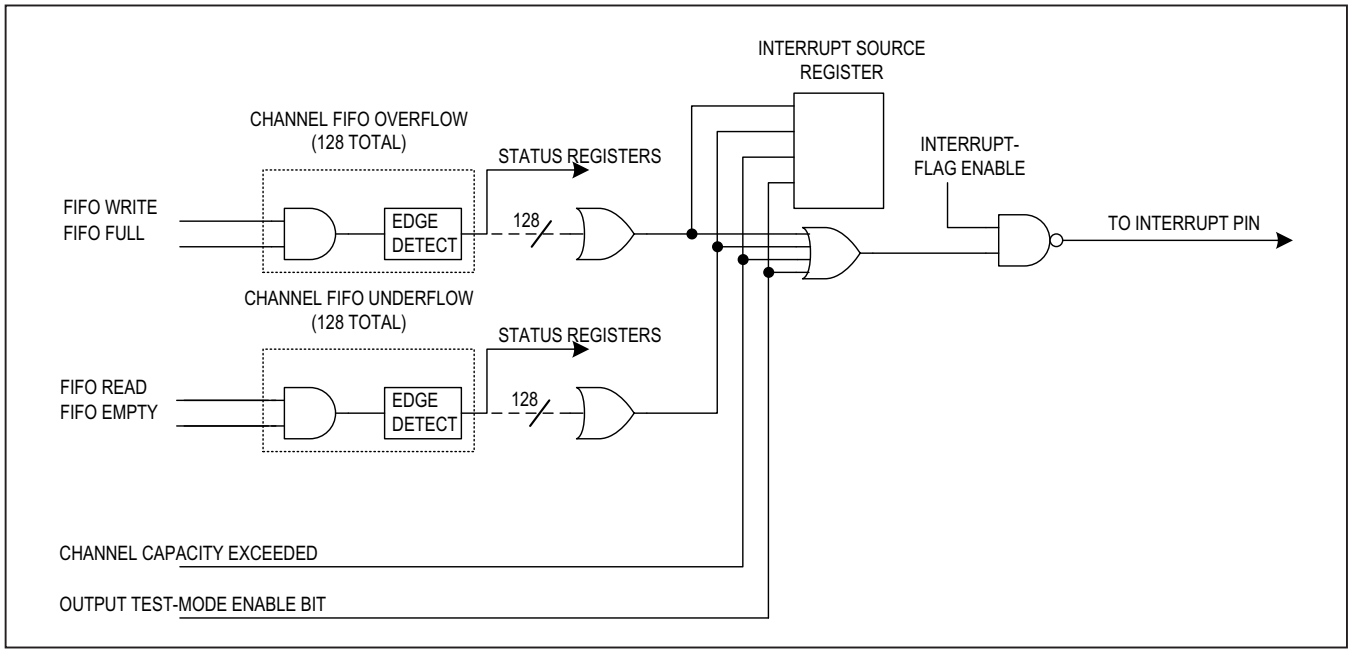


Figure 35. Interrupt Tree Diagram

Table 13. CFG Pin Usage

4 BIT CONFIG CFG [4:1]	SCQAM 32-CH COMB 1	SCQAM 32-CH COMB 2	SCQAM 32-CH COMB 3	SCQAM 32-CH COMB 4	SCQAM 32-CH COMB 5	OFDM CH 1	OFDM CH 2	OFDM CH 3	OFDM CH 4	OFDM CH 5	OFDM CH 6	NOTE
0	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	DEFAULT FOR 160SCQAM(43-1003MHz) + 2OFDM, PORT B
1	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	128SCQAM(43-811MHz) + 2OFDM, PORT B
2	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	128SCQAM(235-1003MHz) + 2OFDM, PORT B
3	ON	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	OFF	160SCQAM(43-1003MHz) + 2OFDM, PORT C
4	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	128SCQAM(43-811MHz) + 2OFDM, PORT C
5	OFF	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	OFF	128SCQAM(235-1003MHz) + 2OFDM, PORT C
6	ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	128SCQAM(GAP 2) + 2OFDM, PORT B
7	ON	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	128SCQAM(GAP 3) + 2OFDM, PORT B
8	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	128SCQAM(GAP 4) + 2OFDM, PORT B
9	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	OFF	128SCQAM + 3OFDM, PORT B
10	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	128SCQAM + 3OFDM, PORT C
11	ON	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	96SCQAM + 4OFDM
12	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	64SCQAM + 5OFDM
13	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	32SCQAM + 5OFDM
14	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ALL ON
15	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ALL OFF

Applications Information

Channel Initialization - Register Programming Order

The optimal order of operation for the system with the MAX5861 receiving data from an FPGA is the following:

1) Configure the MAX5861 for the SCQAM and/or OFDM channel.
2) Program the FPGA to send data to the MAX5861 channel.
3) With data flowing from the FPGA to the MAX5861, clear the status registers of the MAX5861 of the startup condition triggers (FIFO, parity, saturation, etc).
4) Monitor MAX5861 for health as needed.

For the initial configuration of the device, the optimal order of operation for the registers within the MAX5861 is the following:

1) Set the Gain5/Gain6 to zero (GAIN56 register).
2) Power up the blocks (GBL_CFG2).
3) Program channel(s) to include all NCO load pulses.
4) Set Gain5/Gain6 to desired values.

To program another channel when the device is already configured, program in the order defined:

1) Make sure the channel is muted (CHAN_x_x for SCQAM and OFDM_CFG_x for OFDM).
2) Power up the additional block(s) (GBL_CFG2).
3) Set the Gain1/Gain2 (G1G2_x) for SCQAM or Gain7/Gain8 (GAIN_x) for OFDM of the added channels to zero.
4) Unmute the additional channel(s).
5) Program the channel(s) to include all NCO load pulses (if using OFDM, this includes the GAIN_x register for the NCO3 load, while keeping Gain7/Gain 8 at zero).
6) Set Gain1/Gain2 or Gain7/Gain8 to the desired gain values.

This procedure should ensure that the channels come up cleanly in the spectrum.

Grounding, Bypassing, Power-Supply, and Board Layout Considerations

Grounding and power-supply decoupling can strongly influence the performance of the MAX5861. Unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections, affecting dynamic performance. Proper grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed. This reduces EMI and internal crosstalk that can significantly affect the dynamic performance of the MAX5861.

Use of a multilayer PCB with separate ground and power-supply planes is required. It is recommended that the analog output and the clock input are run as controlled-impedance micro-strip lines on the top layer of the board, directly above a ground plane, and that no vias are used for the clock input (CLKP, CLKN) and the analog output (OUTP, OUTN) signals. Depending on the length of the traces, and the operating condition, a low-loss dielectric material (such as ROGERS RO4003) as the top layer dielectric may be advisable. Design guidelines for high-speed design should be followed. The analog output (OUTP, OUTN) signals should have well-balanced routing.

The MAX5861 high-speed DAC section supports three separate power-supply inputs for analog 3.3V (AVDD3), switching (VDD18), and clock (AVCLK) circuits. The DUC section supports multiple 1.8V supplies (VDD18, VDD18I, VDD18O, VDD18BI and VDD18BO) and a core 0.9V (VDD09) supply. Each supply input should at least be decoupled with a separate 47nF capacitor as close to the input as possible and their opposite ends with the shortest possible connection to the corresponding ground plane, to minimize loop inductance. All three power-supply voltages should also be decoupled at the point they enter the PC board with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance. Each supply should be routed to support the current requirements for the supply. The VDD09 plane should be under the DUC section of the die, and not under the DAC section.

Output Coupling

The differential voltage between OUTP and OUTN can be converted to a single-ended voltage using a transformer or a differential amplifier configuration. The DAC outputs should be pulled up to AVDD3. It is recommended to use bias tees built from discrete inductors and capacitors for the pullups. Two recommended output circuit configurations are shown in Figure 28. To achieve the maximum bandwidth, minimize the inductance in the ground lead on the secondary side of the transformer. Use a very short trace and multiple vias for the connection to the ground plane.

NCO Characteristics

There are 160 NCO1 oscillators (one per SCQAM channel), 20 NCO2 oscillators (one per octal QAM channel combiner), 11 NCO3 oscillators (one in each of the 192MHz QAM modulation paths and one in each of the six OFDM modulation channels), and one NCO4 oscillator. The NCO3 frequency control words may be 30 bits [29:0] in high-resolution mode (2.29Hz frequency resolution) or 21 bits [20:0] in low-resolution mode (1171Hz frequency resolution) depending on the state of bits [16:15] in register address 0x008. Utilizing all of the NCOs, the smallest frequency resolution at f_{DAC} = 4915.2MHz is either 2.29Hz or 146Hz based on the NCO3 resolution mode setting.

DAC Sample Rate Selection

The 4915.2Msps maximum sample rate of the MAX5861 allows flexibility in system design. Several trade-offs exist in terms of sample rate versus performance or circuit complexity, and these should be considered when selecting the DAC sample rate for SCQAM mode functionality. If using the OFDM branch for DOCSIS OFDM, the rate is dictated by the standard to be 4915.2Msps.

DAC Control Bits Via SPI

Control signals for the DAC are internally generated. There are 5 control bits for the RF DAC which are controlled by SPI bits.

DACPOR_EN

DACPOR_EN

1: Enable automatic DLLOFF toggle (reset pulse) after SOFT_RESET (default)

0: Disable automatic DLLOFF toggle (reset pulse) after SOFT_RESET

The global reset pin will always generate a DAC reset (DLLOFF) pulse.

GDELAY[1:0] and GDLLOFF[1:0] (DLL Controls)

GDELAY and GDLLOFF are the DAC DLL clock mode controls. These are internal 4-state drivers with the equivalent functionality shown in Table 15.

Settings of GDELAY and GDLLOFF for the operation of the DLL are shown in Table 16. It is recommended that the DLL be enabled for normal operation.

Table 14. NCO Output Frequency Table

TYPE	FREQ RESOLUTION (Hz)	CONTROL WORD SIZE	OUTPUT FREQUENCY RANGE (Hz) (SMALLER OF THOSE LISTED)
NCO1	$f_{DAC}/(2^{25})$	19 bits	$\pm f_{DAC}/128$ ±(0.5 x 48MHz - 0.5 x Channel BW)
NCO2	$f_{DAC}/(2^{25})$	21 bits	$\pm f_{DAC}/32$ ±(0.5 x 192MHz - 0.5 x 48MHz)
NCO3	Selectable $f_{DAC}/(2^{22})$ or $f_{DAC}/(2^{31})$	Selectable 21 or 30 bits	$\pm f_{DAC}/4$ ±(0.5 x 960MHz - 0.5 x 192MHz)
NCO4	$f_{DAC}/(2^{22})$	22 bits	$\pm f_{DAC}/4$

Table 15. Four-State Driver Equivalent Functionality

GDLLOFF[1:0] OR GDELAY[1:0]	INTERNAL RESULT
00	Float (open)
01	Weak resistor to ground
10	Logic 0
11	Logic 1

Table 16. GDELAY/GDLLOFF Operation

GDLLOFF[1:0]	GDELAY[1:0]	FCLK(MHZ)	OPERATION
10	11	2150-2457.6	DLL enabled
10	00	1900-2150	DLL enabled
11	10	10-2304	DLL disabled (no delay)

Harmonic Distortion

The MAX5861 features low harmonic distortion. Second harmonic distortion (HD2) and third harmonic distortion (HD3) are usually the dominant harmonics, and they increase with increasing output frequency. The frequency of HD2 is below 1200MHz for frequencies below 600MHz and the frequency of HD3 is below 1200MHz for output frequencies lower than 400MHz.

Harmonics of Images Around the Clock Frequency

The MAX5861 has a spur at $f_{DAC}/2 - 2f_{OUT}$. This spur is lower than the DOCSIS limit for channel counts greater than 8 but may violate DOCSIS for lower channel counts and high output frequencies. This spur is coincident with f_{OUT} for $f_{OUT} = f_{DAC}/6$. This spur is correctable with the use of the internal DPD.

Latency

SCQAM Path Latency

The device symbol latency is variable due to the fact that the CLK frequency is not required to be frequency-locked to the symbol rate. Achieving the proper symbol rate in the device causes the ratio of KF/LF to be a non-integer value, which in turn forces the device to make periodic adjustments to average the KF/LF rate. This adjustment appears every certain number of symbol clocks as one CLK_D16 clock difference in the symbol rate (relatively either +1 or -1 CLK_D16). One CLK_D16 is 32 CLK periods.

For example, in the case of KF/LF = 869/1000, four symbols have one latency value and the next five symbols have a one CLK_D16 latency value difference. This relative sequence is cyclic and would continue to repeat.

The total latency through the device depends on the many parameters (i.e., the maximum time-slot value programmed for the input interface, time-slot selection for each channel, the port clock, KF and LF values, and individual programmable delay stage parameters). The input interface uses an asynchronous clock for capturing the input data and for FIFO loading. It is impossible to define an equation to calculate the latency through the input block. Latency is therefore defined from the point a symbol is read by the ARR to the output of the device. Since symbols are upsampled as many as 512 times by the device during processing, the center sample at the output is taken as the reference point for this calculation. The following equation defines the latency through the device in terms of CLK clock periods:

$$Latency_{SCQAM} = [((lat\_sym \times 512) + lat\_cc +/- 512) + lat\_DAC] * t_{DAC}$$

where:

lat_sym = (12480 + (256 x D1) + (128 x D2) + (64 x D3) + D4)/(KF/LF)

lat_cc = 19986 + (512 x D5) + (256 x D6) + DPD_D3

lat_DAC = 11

t_{DAC} = period of DAC CLK

D1 through D6 are the user-selectable delay values for the channel-combiner path.

DPD_D3 is the programmable delay for DPD (default value of 6 which is equivalent to 192 CLKs).

The parameter lat_unc is the uncertainty due to the division by LF in the ARR and is equal to one CLK_D16 (16 DATACLK cycles or 32 CLK periods). When a symbol's sampling rate is changed from the symbol rate to the internal MAX5861 output sampling rate, an adjustment to the data read rate from the FIFO to the ARR occurs dynamically to maintain the target symbol rate (LF and KF values). This uncertainty would be reduced to zero if the 1/(LF/KF) ratio became an integer value.

Parameter lat_DAC is the latency through the high-speed DAC.

OFDM Path Latency

The latency through the OFDM path is dependent on the parameters of the OFDM channel.

$$Latency_{OFDM} = (38 \times t_{SDCLK}) + (NIFFT \times 18 + IFFT\ processing\ delay + 2092 + 24 \times NCP) \times t_{DAC}$$

where:

NIFFT is the IFFT points of 4096 or 8192

IFFT Processing delay is 88,464 for 4096 IFFT and 174,144 for 8192 IFFT

NCP is the programmed Cyclic Prefix selection value of 192, 256, 768 or 1024

$t_{SDCLK}$is the period of the SDCLK (2.44ns = 1/409.6MHz)

t_{DAC} is the DAC CLK period (203.45ps = 1/4915.2MHz)

In the case of OFDM latency has been calculated from SYNC rising edge capture to the first subcarrier in the final spectrum, after removing the NCP period.

User-Configurable Delays

User-configurable delays are present in the design. Each individual SCQAM channel block (of which there are 160) has three configurable delays:

- D1: 0 to 12 symbol periods (selectable)
- D2: 0 or ½ symbol period
- D3: 0 or ¼ symbol period

Each 8-channel combiner (of which there are 20) has two user-configurable delays:

- D5: 0 or 1 DATACLK/16 clock period
- D6: 0 or 1 DATACLK/8 clock period

The DPD has three user-configurable delays:

- D1: 0 to 15 DATACLK/2 periods (default 1)
- D2: 0 to 15 DATACLK/2 periods (default 12)
- D3: 0 to 15 DATACLK/2 periods (default 6)

One DATACLK = 2 CLK periods.

Symbol Timing Alignment (Synchronization)

Aligning Multiple SCQAM Channels within a Single MAX5861

The MAX5861 allows symbols in groups of multiple (same symbol rate) SCQAM channels to be exactly time-aligned. Within an individual MAX5861, timing alignment of SCQAM channels requires no external FPGA and will have zero skew. No internal mechanism is provided to allow byte order alignment of data; however, it is possible for the user to byte-align data by careful manipulation of input port timing and the transfer of data. If channels are muted after synchronizing, synchronization is lost; therefore, it is recommended that the channel gain be set to 0 after synchronization rather than muting a channel.

A group of FIFOs can be configured via SPI commands and by using the MODE2 pin to release read pointers and synchronize reads at exactly the same time. Without using this configuration method, a group of unsynchronized FIFOs could spread their symbols across two symbol time slots.

It may be desirable to synchronize all of the channels in one operation at startup. The unused channels would have their G1/G2 gains set to zero. G1 and G2 are channel gains for the specific channel. When removing channels, these gains would also be set to zero. This allows all of the channels to maintain exact synchronization. Figure 36 indicates the use of the MODE2 pin for synchronization.

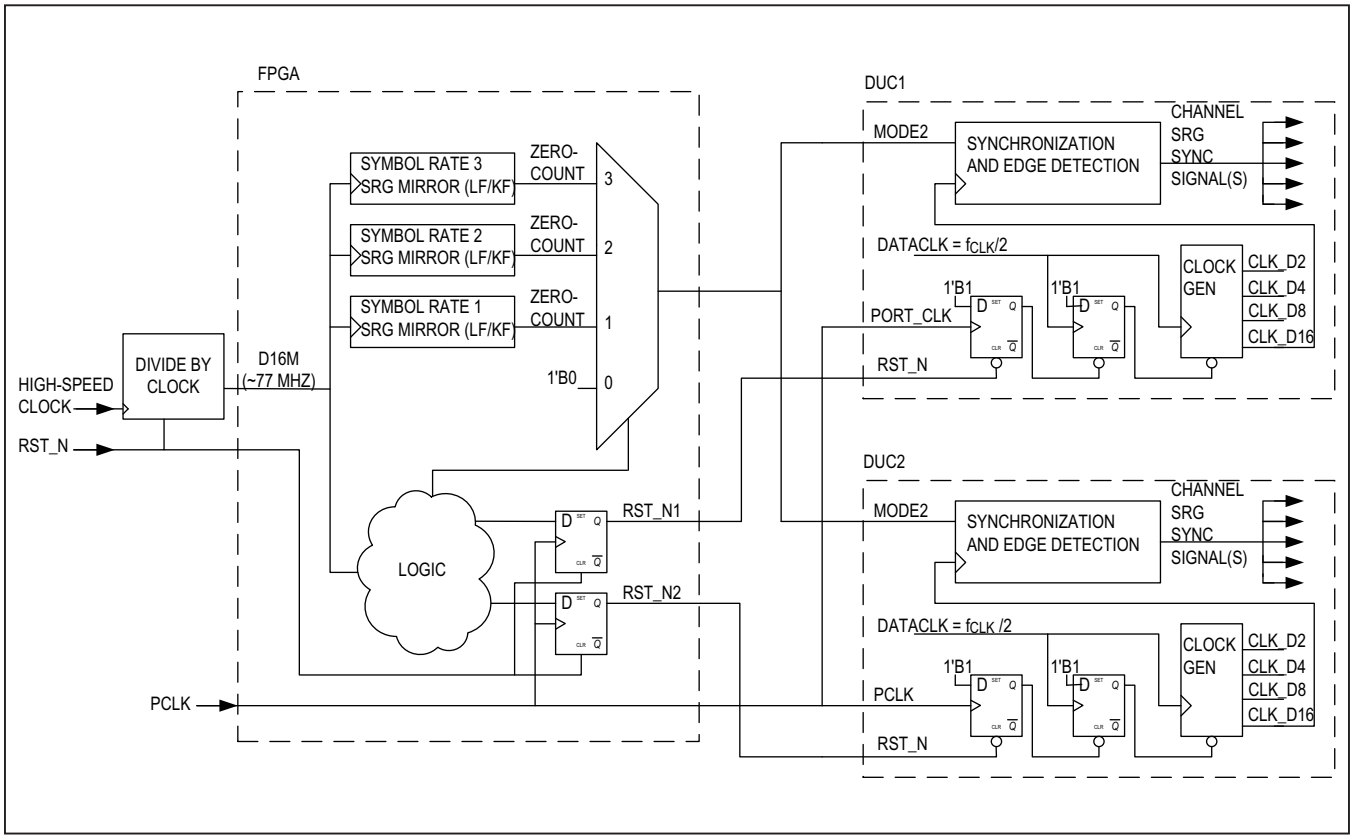


Figure 36. Symbol Time-Alignment Functional Block Diagram

Aligning SCQAM Channels across Multiple MAX5861 Devices

Multiple symbol rate groups can also be time-aligned within a tolerance across separate MAX5861 devices. Timing alignment over multiple devices is achieved by use of external logic. The MAX5861 does not source time-alignment signals, but rather it responds to input control signals. This configuration avoids the complexity of a master-slave system and avoids reliability issues.

Figure 36 is an example of a symbol time-alignment implementation for multiple MAX5861 devices. The FPGA sources the timing-alignment control signals for the channel symbol groups and multiple devices. There are no feedback signals from the MAX5861 to the FPGA. DUC1 would be an operational MAX5861 and DUC2 would be the MAX5861 being brought online and into synchronization.

The FPGA contains mirrors of the MAX5861 KF/LF symbol rate generators which are driven by the d16m signal. The accuracy of the synchronization depends on how closely the d16m signal mirrors the MAX5861 internal clk_d16 clock. The phase and frequency of the d16m clock is dependent upon the quality of the input high speed clock, the best choice being the DAC clock (DATACLK). Timing alignment is possible with less than two clk_d16 clocks skew (~30 ns or less) when using a quality clock.

There would be a symbol rate (KF/LF) generator in the FPGA for each symbol rate being aligned in the MAX5861 devices. The zero-count signals from the generators would be muxed via logic to the desired MAX5861 at the appropriate times.

The reset signals from the FPGA (RST_N1 and RST_N2) attaches to the global reset (RST_N). The global reset aligns the skew and phase of the internal clocks of the MAX5861 device being brought online. An already-operational MAX5861 would not have its global reset toggled, as all configuration registers would be cleared.

The MODE2 input receives the zero-count signal. MODE2 is synchronized and rising-edge detected using the internal clk_d16 clock. Alignment of symbol rate generators to the MODE2 input is selectively configured via SPI commands.

A general setup procedure for a MAX5861 being brought into alignment would be:

1) Power up the MAX5861 being brought online. Start clocks (PCLK, DATACLK).
2) FPGA provides new MAX5861 with hardware reset.
3) Configure the MAX5861:
   - Turn on gated clocks at 32 channel block level.
   - Un-mute channels
   - Configure each channel (port, slot, mute, lf, kf....)
   - Configure frequency map.
   - Enable selected channels for synchronization.
4) Configure FPGA:
   - Configure internal symbol rate generator (LF/KF).
   - Turn off data to the MAX5861 (force port valid low).
   - Generate sync pulse to align FPGA SRGs and MAX5861 SRGs.
   - Pulse MODE2 aligned to the d16m clock domain. (The NCOs, global LF/KF network and FIFO reset network will be aligned by reset.)
   - Wait a few clocks for the reset pulse to propagate.
   - Enable PSYNC, data, and port valid signals to DUC. Send at least 8 words consecutively to all channels during the next 8 symbol periods to ready the FIFOs.
   - Send symbol data as required based on MAX5861 handshaking signals.
5) Configure DUC
   - Disable global FIFO reset enables.
6) Let the MODE2 sync pulse free run.
7) Configure some other symbol rate (LF/KF).
   - repeat step 4 and 5 for those channels.

Power Reduction

Significant power reduction can be achieved if a smaller number of channels are used and frequency agility is limited.

Lowest Standby Power

The lowest standby power for the MAX5861 may be achieved by toggling the external global reset input RST_N at logic 0 (active) and setting the configuration state to power down all of the blocks. Since the MAX5861 configuration registers are cleared by RST_N, the device must be re-configured after global reset is removed.

The absolute lowest standby power can be achieved by powering down the five 192MHz QAM blocks and the six OFDM blocks. This removes dynamic and leakage power as well.

Channel Muting

Power may be reduced by muting unused SCQAM channels. When a channel is muted, the clock is turned off to symbol interface block. This includes the circuitry from the D1_delay block to the MOD1 block.

Another way to minimize channel power is to set individual channel gain controls 1 and 2 to zero. This reduces data toggling power to zero but the associated clocks will remain active.

Block Shutdown of 8 SCQAM Channel Combiners

The MUTE_8CC register allows the twenty 8 SCQAM channel combiners to be individually muted. Muting an 8-channel combiner disables clocks for the combiner and the 8 channels that feed it. Shutting down an 8-channel combiner will remove an output frequency block of 48MHz.

Block Shutdown of 32 SCQAM Channel Combiners

The MAX5861 has five 32 SCQAM channel block combiners, each of which may be configured to be turned off for significant power savings using bits in the CFG_CC32MUTE register. The 32-channel combiner block includes 32 input channels, the associated four 8-channel combiners, and logic in the 32-channel combiner itself. Shutting down a 32-channel combiner will remove an output frequency block of 192MHz.

Low-Current Differential Inputs

About a quarter watt of 1.8V power can be saved by setting the LVDS driver to low-current (low swing) mode. Set the CUR_MODE_O bit (LVDS_TRIM[24]) to 0 to reduce internal LVDS power.

For additional power savings, set the CUR_MODE_I bit (LVDS_TRIM register[23]) to 0 to reduce input LVDS driver power. Test this mode with the input symbol port FPGA to assure compatibility.

Individual DPD Branch Shutdown

Each branch of the DPD is active (clocking) after reset. Unused branches of the DPD can be deactivated (remove clocking) to minimize power (register 0x038 bits [8:4]). Deactivating all four branches of the DPD can save about 250mW.

Removing Power from Selected 192MHz Blocks

The PWR_CFG2 register allows power-switching of selected 192MHz blocks to remove dynamic and leakage power via SPI. This achieves the lowest dynamic and standby power but with reduced frequency agility.

The CFG pins may also be used to program the default power-up/reset conditions of these blocks. All 192MHz blocks will be powered-on while global reset is being applied. After release of global reset, the status of the CFG pins will be read and loaded into the SPI register if the device clock (CLKP/N) is active. The SPI register write will overwrite the default CFG pin power configuration allowing the user full power-on/-off control of the blocks regardless of the hardwired state of the CFG pins.

Interfacing to an External Temperature Sensor

The user is required to monitor and maintain the proper die junction temperature (< 110°C) to avoid thermal damage. The MAX5861 has a built-in thermal diode junction that interfaces to external dual current temperature sensors, such as the MAX6654. This sensor allows the user to monitor the die temperature of the MAX5861 and it can also output an overtemperature warning signal. The interface circuit is shown in Figure 37. For board layout recommendations, please refer to the MAX6654 data sheet. Always ground the TDC pin to eliminate the small potential created by its internal connection to substrate via a small resistance.

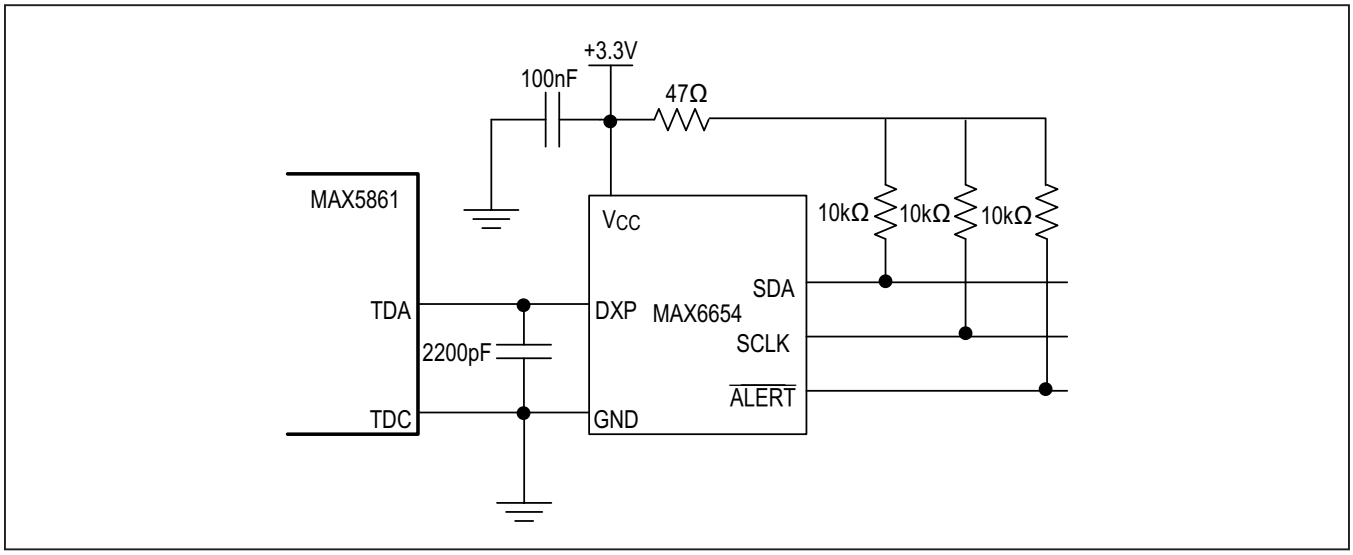


Figure 37. Interfacing to the MAX6654 Temperature Sensor

Differential I/O Data Skew PCB Compensation

Matching signal skews is important to allow the largest signal eye and highest operational speed. The preliminary skew offsets listed in Table 17 represent intrinsic signal delay skews from silicon to the package balls. They are calculated across all foundry PVT corners using static timing analysis methods. Three timing-related signal groups are indicated: the Port A input group, the Port A output group, and the Port B/C group. It is important that these signal groups are routed on the PCB such that they are the same length ± compensation in order to have the greatest data eye opening.

The following tables indicate delta delay compensation for the Port A input group, the Port A output group, and the Port B and C input group.

Signal A5 has the largest skew for the Port A input group and the remaining skews represent the additional routing delay for each signal the PCB would incorporate to make the skews equivalent (i.e. VALIDA would require 20ps of additional PCB routing delay than the A5 routing delay in order to have matching skews). Signal C3 has the largest skew for the Ports B and C group.

Table 17. Differential I/O PCB Skew Compensation

PORT A INPUT GROUP			PORTS B AND C GROUP				
Signal Name	MAX5861 Compensation (ps)		Signal Name	MAX5861 Compensation (ps)		Signal Name	MAX5861 Compensation (ps)
PCLKN	21		SDCLK	9		PARB	8
A0	16		B0	67		C0	25
A1	6		B1	69		C1	30
A2	22		B2	29		C2	31
A3	22		B3	22		C3	0**
A4	18		B4	13		C4	13
A5	0*		B5	97		C5	18
A6	19		B6	95		C6	71
A7	25		B7	97		C7	68
A8	3		B8	94		C8	62
A9	2		SYNC1	25		SYNC4	3
PARA	18		SYNC2	30		SYNC5	16
PSYNC	34		SYNC3	35		SYNC6	31
VALIDA	20						

PORT A OUTPUT GROUP	
Signal Name	MAX5861 Compensation (ps)
RDYA	0***
RDYSYNC	0***
RDYCLK	0***

*A5 has the longest silicon + package delay in the Port A group.

**C3 has the longest silicon + package delay in the Port B/Port C group.

***All Port A outputs are ≤ 20ps of each other – no compensation required.

The Port A output group (RDYA, RDYSYNC, and RDYCLK) are already adequately skew-compensated (being within 20ps of each other) so no compensation is given. However, they would be expected to each have the same PCB route length (timing skew) so that the three signals would arrive (reasonably) simultaneously at the FPGA. RDYCLK is expected to be shifted ¼ cycle (90°) internally in the FPGA and be used to capture RDYA and RDYSYNC. Silicon+package delay skew is reasonably equal for these output signals, but simulations show that the rise/fall rates for these differential outputs vary significantly over PVT (foundry library corners -40°C to +125°C) and add up to about 172ps. This is why RDYCLK is recommended to be shifted 90° to capture RDYA and RDYSYNC. Figure 38 below shows this relationship.

It is desirable to have the PCB designed to accommodate these three signal timing groups by managing the signal routing lengths. SPI-configurable on-chip delay compensation is available for each differential input and output in the range of 0 to 240ps (typical) in ~30ps steps (3 bits) if required using registers (IOL_CFG1- IOL_CFG5).

PRBS Operation

Two PRBS modes are configurable in the MAX5861. Both PRBS modes provide flat response for all modulation types. PRBS23 is the preferred mode of operation. The first channel of each 8-channel combiner may be optionally programmed to have its seed reloaded (short-cycled) after N clocks (N in the range of 1 to 2^{16}).

PRBS23 Mode Operation

The standard PRBS23 mode generates a maximally long sequence. It has more than 200 programmable taps to provide independent sequences for each of the 160 channels. The PRBS23 sequence always starts at zero.

A fixed seed of 0x000001 is loaded when PRBS23 is enabled or its sequence repeats. The 13-bit XOR taps (in addition to the MSB) are selected from the following configuration bits:

- Address 0x108 for Channel 1, Address 0x110 for Channel 2 etc.
- XOR taps from concatenation of symif_*.prbs_shft[0], symif_*.d1[3:0], symif_*.prbs_seed[7:0]
- symif_*.prbs_shft[2:1] are not used in this mode

PRBS enable is taken from from symif_*.prbs = 1

PRBS23 mode select is taken from from symif_*.prbs_type = 0 (default)

The channel QAM mode is used to determine number of bits to be used from the PRBS23 stream and therefore a loss of bits is avoided.

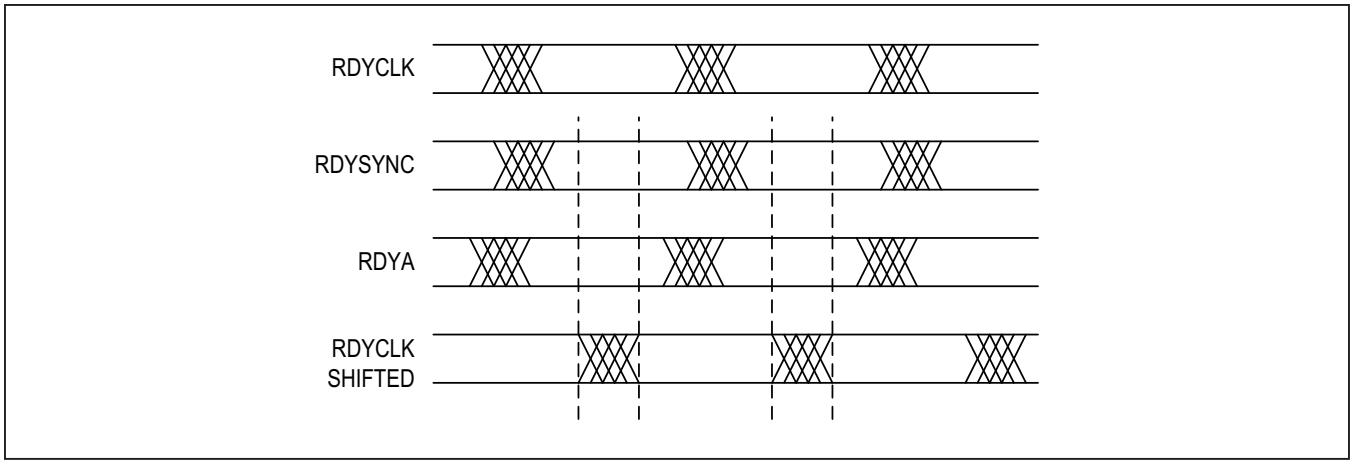


Figure 38. Port A Output Rise/Fall Differences

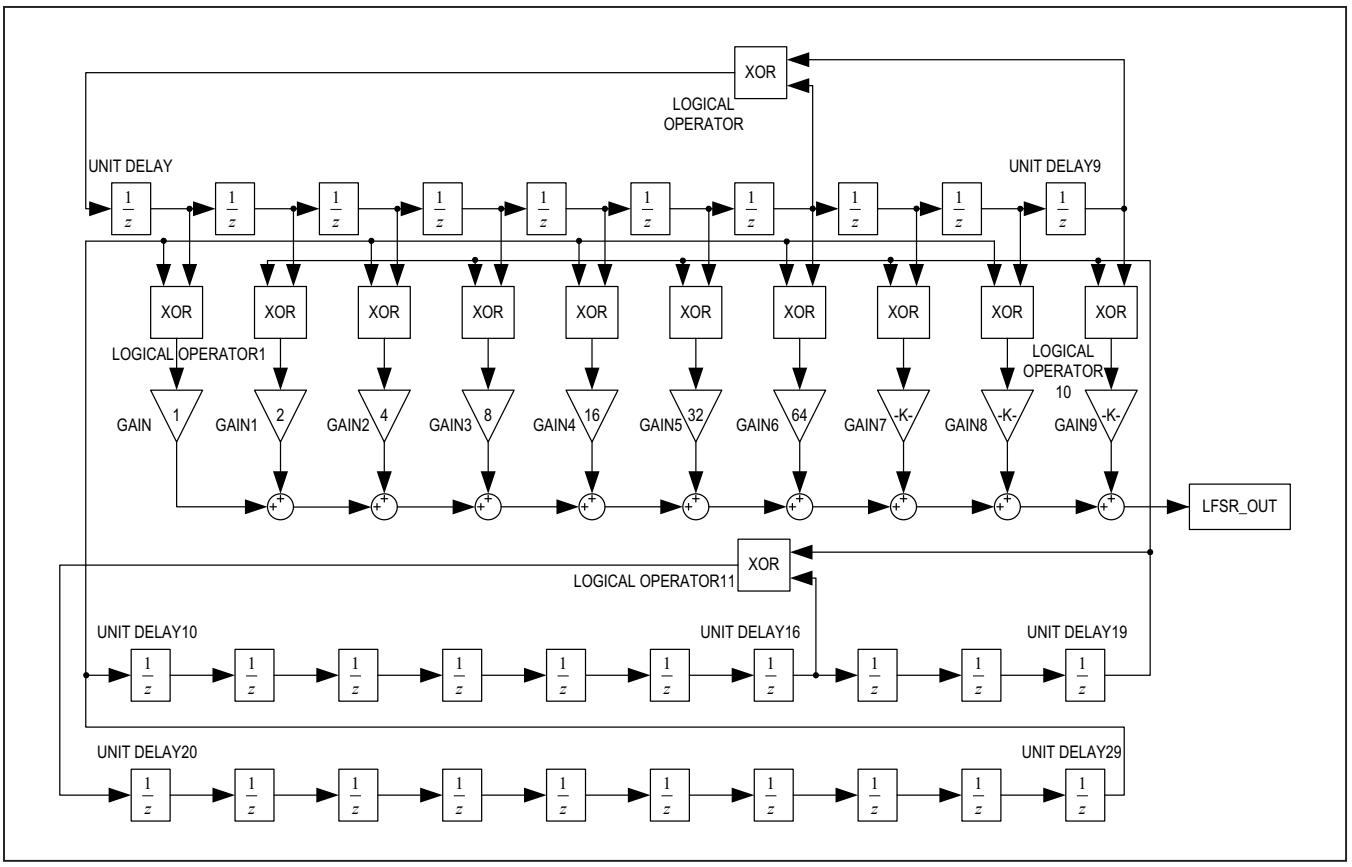


Figure 39. LFSR Block Diagram

Dual 10/20 LFSR PRBS Mode Operation

This PRBS is used in the MAX5880 and the MAX5860. The block diagram of the dual 10/20 LSFR PRBS generator is shown in Figure 39. The generator consists of two LFSRs. The top LFSR is 10 bits long and it is used to generate a uniformly distributed sequence of 10-bit values. The bottom LFSR is 20 bits long and it is used to decorrelate the sequence generated by the first LFSR. The output of the 20-bit LFSR drives the inputs of the XOR gates controlling the polarity of the sequence generated by the first LFSR. The feedback taps in both LFSRs are selected such that they generate maximum length sequences, and there is no need to make the taps programmable.

However, the seed values have to be programmable in both LFSRs. The seed word is 10 bits long for the top LFSR and 12 bits long for the bottom LFSR. The 12-bit seed value should be aligned with the MSBs of the LFSR. This is shown in Figure 40.

The output sequence of the PRBS generator should have a uniform amplitude distribution and a spectral characteristic of white noise.

Figure 40 diagrams the LFSR seeding operation. In picking a seed, the user need only set the 4 d1 select bits (register SYMIF, one per channel) and the 8 bits of the appropriate SEEDA or SEEDB value (PRBS register) so they combine to a unique value for each channel. During PRBS operation, the d1_delay function is not operational.

Detailed operation of the LFSR is now described. To create the seeds internally, the d1 delay register bits (1 set of 4 per channel) are utilized along with the appropriate 8-bit PRBS seeds for each channel.

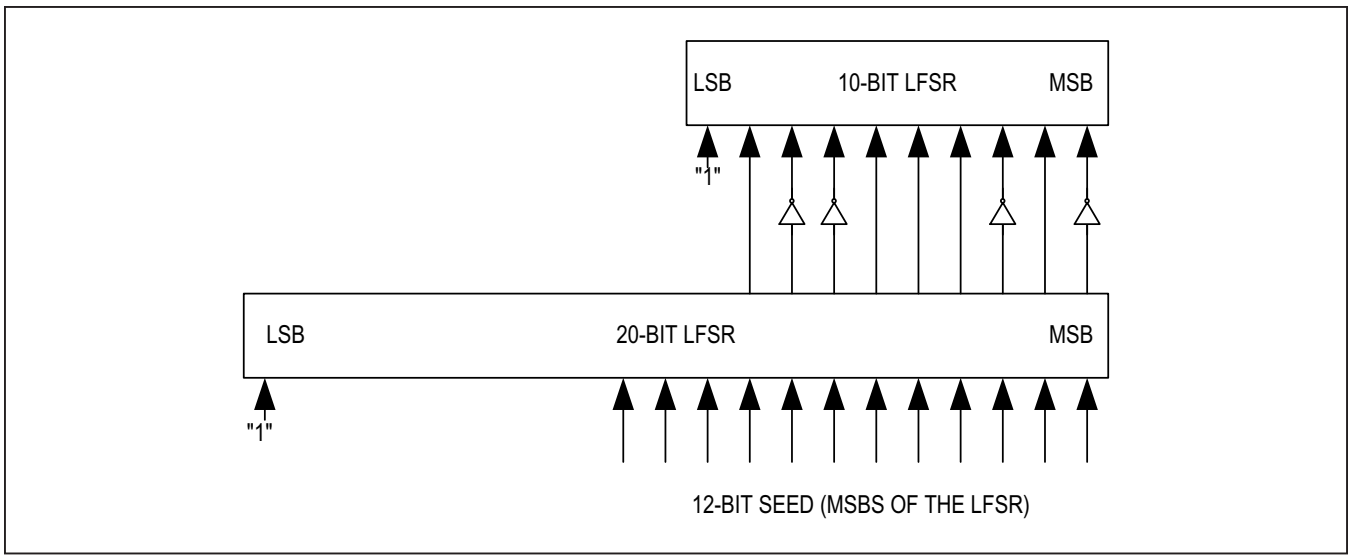


Figure 40. LFSR Seeds

The seed for the upper 10 bit LFSR is formed according to the following equation:

seed10 = {~d1_select[3], d1_select[2], ~d1_select[1], d1_select[0], seed[7], seed[6],~seed[5], ~seed[4], seed[3], 1'b1 } where seed[] refers to the appropriate SEEDA or SEEDB register.

The seed for the lower 20-bit LFSR is formed according to the following equation:

seed20 = { d1_select[3:0], SEEDA[7:0] or SEEDB[7:0], 8'b1 }

PRBS Short-Cycle Feature

The first channel of each 8-channel combiner may be optionally programmed to have its seed reloaded (short-cycled) after N clocks (N in the range of 1 to 216). This feature can be used with either PRBS mode.

The PRBS cycle restarts by reloading the seed value. For PRBS23 mode, this means reloading the 0x000001 seed. For 10/20 LFSR PRBS mode, the programmable seed value is reloaded.

The following control registers are used for this feature

- Address 0x10F for Channel 1, Address 0x15F for Channel 9 etc.
- prbs_*.rep_ctl[16] enables the repetition mode
- prbs_*.rep_ctl[15:0] set the repetition cycle counter (1 to 216)

DTO (Digital Test Output) Configuration

DTO (Digital Test Output) is a differential output used to monitor/examine various internal signals. It can select one of a number of internal nodes for observation. Its operation is configured by bits in the OEM_TEST register. The use of DTO is not required for normal operation.

The OEM_TEST register (0x002) has 6 bits (DSEL[13:8]) as a level 1 select plus 7 bits (lvds_sel[20:14]) as a level 2 select to select specific internal signals to be output on the DTO. The default state for the DTOP/N output LVDS drive. The channel FIFO read signals are available for every ninth channel. These FIFO read signals may aid the user in determining the actual channel synchronization.

Table 18. DTO Level 1 Select Options

OEMTEST: DSEL[13:8]	SIGNAL	FUNCTION
0x00		Output disabled.
0x01	clk_d16	DATACLK/16
0x02	pulse_ff	Global FIFO reset pulse
0x03	mode2_in	MODE2 sync'd to clk_d16
0x04	misr_sample	MISR sample signal
0x05	sym_det_out	Input LVDS symbol detect
0x09	lvds_observe	Selected by bits lvds_sel[21:16]
0x0a	test_vin	CMOS VIL/VIH observe
0x0b	mode2_enable	Observe d32 or d64 enable
0x0c	rd_1	Channel 1 FIFO read signal
0x0d	rd_9	Channel 9 FIFO read signal
0x0e	rd_17	Channel 17 FIFO read signal
0x0f	rd_25	Channel 25 FIFO read signal
0x10	rd_33	Channel 33 FIFO read signal
0x11	rd_41	Channel 41 FIFO read signa
0x12	rd_49	Channel 49 FIFO read signal
0x13	rd_57	Channel 57 FIFO read signal
0x14	rd_65	Channel 65 FIFO read signal
0x15	rd_73	Channel 73 FIFO read signal
0x16	rd_81	Channel 81 FIFO read signal
0x17	rd_89	Channel 89 FIFO read signal
0x18	rd_97	Channel 97 FIFO read signal
0x19	rd_105	Channel 105 FIFO read signal
0x1a	rd_113	Channel 113 FIFO read signal
0x1b	rd_121	Channel 121 FIFO read signal
0x1c	rd_129	Channel 129 FIFO read signal
0x1d	rd_137	Channel 137 FIFO read signal
0x1e	rd_145	Channel 145 FIFO read signal
0x1f	rd_153	Channel 153 FIFO read signal

The setup/hold limits for the LVDS data inputs to the symbol input ports may be observed by selecting the lvds_observe DTO selection and the desired test_dout signal via the control bits lvds_sel [20:14].

Table 19. DTO Level 2 Select Options

OEMTEST: LVDS_SEL[20:14]	SIGNAL	FUNCTION
0x00	0x00	No signals observed/output
0x01	test_dout_r[0]	Rising edge capture of PSYNC
0x02	test_dout_r[1]	Rising edge capture of PARA
0x03	test_dout_r[2]	Rising edge capture of VALIDA
0x04	test_dout_r[3]	Rising edge capture of A0
0x05	test_dout_r[4]	Rising edge capture of A1
0x06	test_dout_r[5]	Rising edge capture of A2
0x07	test_dout_r[6]	Rising edge capture of A3
0x08	test_dout_r[7]	Rising edge capture of A4
0x09	test_dout_r[8]	Rising edge capture of A5
0x0A	test_dout_r[9]	Rising edge capture of A6
0x0B	test_dout_r[10]	Rising edge capture of A7
0x0C	test_dout_r[11]	Rising edge capture of A8
0x0D	test_dout_r[12]	Rising edge capture of A9
0x0E	|test_dout_r	Logical OR of the rising edge captures
0x0F	test_dout_f[0]	Falling edge capture of PSYNC
0x10	test_dout_f[1]	Falling edge capture of PARA
0x11	test_dout_f[2]	Falling edge capture of VALIDA
0x12	test_dout_f[3]	Falling edge capture of A0
0x13	test_dout_f[4]	Falling edge capture of A1
0x14	test_dout_f[5]	Falling edge capture of A2
0x15	test_dout_f[6]	Falling edge capture of A3
0x16	test_dout_f[7]	Falling edge capture of A4
0x17	test_dout_f[8]	Falling edge capture of A5
0x18	test_dout_f[9]	Falling edge capture of A6
0x19	test_dout_f[10]	Falling edge capture of A7
0x1A	test_dout_f[11]	Falling edge capture of A8
0x1B	test_dout_f[12]	Falling edge capture of A9
0x1C	0x00	No signals observed
0x1D	| test_dout_f	Logical OR of the falling edge captures
0x1E	|test_dout_f || |test_dout_r	Logical OR of PORTA captures
0x1F	|test_dout_f || |test_dout_r	Logical OR of PORTA captures
0x20	PORT BC test_dout_r[0];	Rising edge capture of SYNC6
0x21	PORT BC test_dout_r[1];	Rising edge capture of SYNC5
0x22	PORT BC test_dout_r[2];	Rising edge capture of SYNC4
0x23	PORT BC test_dout_r[3];	Rising edge capture of C0
0x24	PORT BC test_dout_r[4];	Rising edge capture of C1
0x25	PORT BC test_dout_r[5];	Rising edge capture of C2
0x26	PORT BC test_dout_r[6];	Rising edge capture of C3

Table 19. DTO Level 2 Select Options (continued)

0x27	PORT BC test_dout_r[7];	Rising edge capture of C4
0x28	PORT BC test_dout_r[8];	Rising edge capture of C5
0x29	PORT BC test_dout_r[9];	Rising edge capture of C6
0x2A	PORT BC test_dout_r[10]	Rising edge capture of C7
0x2B	PORT BC test_dout_r[11]	Rising edge capture of C8
0x2C	PORT BC test_dout_r[12]	Rising edge capture of SYNC3
0x2D	PORT BC test_dout_r[13]	Rising edge capture of SYNC2
0x2E	PORT BC test_dout_r[14]	Rising edge capture of SYNC1
0x2F	PORT BC test_dout_r[15]	Rising edge capture of PARB
0x30	PORT BC test_dout_r[16]	Rising edge capture of B0
0x31	PORT BC test_dout_r[17]	Rising edge capture of B1
0x32	PORT BC test_dout_r[18]	Rising edge capture of B2
0x33	PORT BC test_dout_r[19]	Rising edge capture of B3
0x34	PORT BC test_dout_r[20]	Rising edge capture of B4
0x35	PORT BC test_dout_r[21]	Rising edge capture of B5
0x36	PORT BC test_dout_r[22]	Rising edge capture of B6
0x37	PORT BC test_dout_r[23]	Rising edge capture of B7
0x38	PORT BC test_dout_r[24]	Rising edge capture of B8
0x39	|PORT BC test_dout_r	Logical OR of the rising edge PORT BC captures
0x40	PORT BC test_dout_f[0];	Falling edge capture of SYNC6
0X41	PORT BC test_dout_f[1];	Falling edge capture of SYNC5
0X42	PORT BC test_dout_f[2];	Falling edge capture of SYNC4
0X43	PORT BC test_dout_f[3];	Falling edge capture of C0
0X44	PORT BC test_dout_f[4];	Falling edge capture of C1
0X45	PORT BC test_dout_f[5];	Falling edge capture of C2
0X46	PORT BC test_dout_f[6];	Falling edge capture of C3
0X47	PORT BC test_dout_f[7];	Falling edge capture of C4
0X48	PORT BC test_dout_f[8];	Falling edge capture of C5
0X49	PORT BC test_dout_f[9];	Falling edge capture of C6
0X4A	PORT BC test_dout_f[10]	Falling edge capture of C7
0X4B	PORT BC test_dout_f[11]	Falling edge capture of C8
0X4C	PORT BC test_dout_f[12]	Falling edge capture of SYNC3
0X4D	PORT BC test_dout_f[13]	Falling edge capture of SYNC2
0X4E	PORT BC test_dout_f[14]	Falling edge capture of SYNC1
0X4F	PORT BC test_dout_f[15]	Falling edge capture of PARB
0X50	PORT BC test_dout_f[16]	Falling edge capture of B0
0X51	PORT BC test_dout_f[17]	Falling edge capture of B1
0X52	PORT BC test_dout_f[18]	Falling edge capture of B2
0X53	PORT BC test_dout_f[19]	Falling edge capture of B3

Table 19. DTO Level 2 Select Options (continued)

0X54	PORT BC test_dout_f[20]	Falling edge capture of B4
0X55	PORT BC test_dout_f[21]	Falling edge capture of B5
0X56	PORT BC test_dout_f[22]	Falling edge capture of B6
0X57	PORT BC test_dout_f[23]	Falling edge capture of B7
0X58	PORT BC test_dout_f[24]	Falling edge capture of B8
0x59	|PORT BC test_dout_f	Logical OR of the falling edge PORT BC captures
0x5A	|PORT BC test_dout_f || |PORT BC test_dout_f	Logical OR PORT BC captures

Manufacturing Test Pins

For end-user applications, the following signal connection rules apply:

- TEST_n and MODE must always be asserted logic 1 (1.8V)
- RSETI is connected directly to ground.

Static Performance Parameter Definitions

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes, with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the specified accuracy.

Noise-Spectral Density

The DAC output noise is the sum of the quantization noise and other noise sources. Noise spectral density is the noise power in a 1Hz bandwidth.

Two-/Four-Tone Intermodulation Distortion (IMD)

The two-/four-tone IMD is the ratio expressed in dBc (or dBFS) of the worst third-order (or higher) IMD products to any output tone.

Adjacent Channel Power (ACP)

Adjacent channel power is commonly used in combination with DOCSIS-compliant QAM signals. ACP is the ratio in dB between the power in a channel at a specified frequency offset from the edge of the transmitted channel block, and power in the lowest frequency channel of the transmitted block. ACP provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

References

[1] ITU-T J.83, Digital multiprogram systems for television, sound, and data services for cable distribution (12/2007), download from www.itu.org

[2] Data-Over-Cable Service Interface Specifications, Physical Layer Specification CM-SP-PHYv3.1-I03-140610, download from www.cablelabs.com

[3] DVB-C standard: EN 300 429 V1.2.1 (1998-04) Digital Video Broadcasting (DVB); Framing Structure, channel coding and modulation for cable systems, download from www.etsi.org

[4] Data-Over-Cable Service Interface Specifications, Modular CMTS, DOCSIS Timing Interface Specification, CM-SP-DTI-I04-061222, download from www.cablelabs.com

Register Definition and Description

REGISTER MAP

The MAX5861 contains 1492 registers, each 32 bits wide, for a total of approximately 37900 programmable bits. These registers are described by the 96 unique-function register descriptions which follow in this section. Zeros should be written to reserved bit locations.

Each register table contains the following information:

- Address: Either a single address or a formula if multiple occurrences.
- Register Name: Abbreviated register designation.
- Occurrences: Number of times this register appears in the memory map.
- Description: General description of the register function.
- Bit # (in two rows): Bit position from 31 to 16 and 15 to 0.
- Default bit value (in two rows): Logical bit value after reset and before any SPI writes.
  - Self-clearing (pulse-generation) bits are denoted by *
  - Clear-on-register-write bits are denoted by **

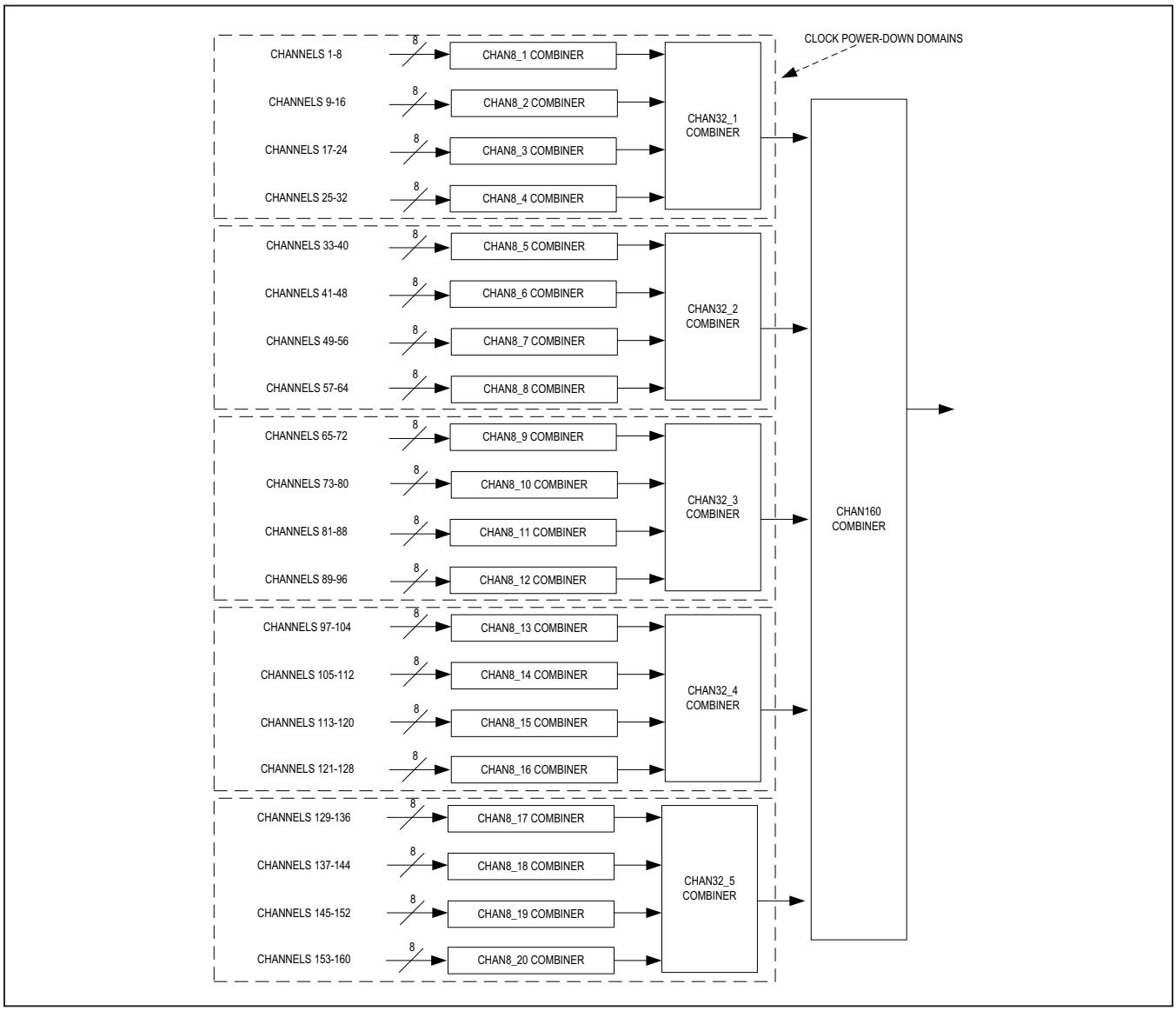


Figure 41. Channel A and B Block Combiner Reference

ID

Address 0x000

Register Name ID

Occurrences 1

Description Identification Register

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	R	R	R	R	V	V	V	V	V	V	V	V

[31:24]	ID	ID code (always 27 decimal)
[11:8]	REV	4-bit silicon revision code
[7:0]	VAR	Product variant code

GBL_CFG

Address 0x001

Register Name GBL_CFG

Occurrences 1

Description Global Configuration

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

[31]	SOFT_RESET_N	Resets all data path except config registers (active low) 0: Soft reset asserted 1: Soft reset deasserted
[30]	MV_DCLK_DIVS	If 1, dclk divides will be delayed by one dclk
[29]	MV_SDCLK_D2	If 1, sdclk_d2 will be delayed by one sdclk
[28]	EN_M2_DCLK	If 1, MODE2 pin pulsed re-starts DUC clock divide counter
[27]	GBL_CLK	If 1, re-loads all the DUC clock divide counters
[26]	DACPOR_EN	If 1, enable DLLOFF to DAC to follow RST_N at power on reset
[25:24]	GDELAY	GDELAY output value [1:0]
[23:22]	GDLLOFF	GDLLOFF output value [1:0]
[21:16]	RSVD	Reserved bits [5:0]
[15:14]	SPARE	Spare bits [1:0]
[13:12]	M2_SEL	MODE2 sync clock select, 00 or 01: clk_d16 selected 10: clk_d32 selected 11: clk_64 selected
[11]	D6	If 1, Add DCLK/8 period delay in the signal chain
[10]	D5	If 1, Add DCLK/16 period delay in the signal chain

[9]	D4	If 1, Add SYMBOL Period/8 period delay in the signal chain
[8]	D3	If 1, Add SYMBOL Period/4 period delay in the signal chain
[7]	M2_SYNC_PRBS	Enable MODE2 pin to re-start all PRBS generators
[6]	M2_SYNC_FIFO	Enable MODE2 pin to reset all the FIFOs
[5]	M2_SYNC_LF	Enable MODE2 pin to re-load all the KF/LF data
[4]	M2_SYNC_NCO	Enable MODE2 pin to re-load all the NCOs
[3]	GBL_PRBS	Generates re-load pulse for all PRBS generators *
[2]	GBL_FIFO	Reset all the FIFOs in the input data interface *
[1]	GBL_KFLF	Re-loads all the KF/LF data to counters in ARR *
[0]	GBL_FCW	Re-loads all the NCOs with Frequency Control Word *

*Denotes self-clearing bit. A pulse is generated when asserted logic 1.

OEM_TEST

Address 0x002

Register Name OEM_TEST

Occurrences 1

Description DTO and manufacturing test enable bits

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:23]	RSVD	Reserved bits [8:0]
[22:21]	TEST_REF	Manufacturing test bits 00 or 01: normal REFCLK 10: assert REFCLK output low 11: assert REFCLK output high.
[20:14]	LVDS_SEL	Input LVDS select value for DTO observation [6:0]
[13:8]	DSEL	Set DTO pin function [5:0] (See section 9.14 for configuration details) 0: High Z state (Default) 1: DCLK/16 clock output in DTO pin 2: Global Fifo reset derived from mode2 3: Registered MODE2 signal 4: MISR sample pulse 5: Symbol detect compare value 9: Input LVDS observation control 10: CMOS NAND tree for VIL/VIH testing 11: MODE2 d32/d64 enable pulse 12-31: FIFO read signal from each 8 channel combiner 32 On signal for 32 channel combiner 1. 33 On signal for 32 OFDM BLK 1.

[7:4]	RSVD	Reserved bits [3:0]
[3:0]	CW	Control Word: Set to 1101 to enable OEM_TEST function. [3:0] In OEM mode bypass channels which cannot be configured.

GBL_G2_WRITE

Address 0x003

Register Name GBL_G2_WRITE

Occurrences 1

Description Global write of G2 gain for all active channels

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:24]	RSVD	Reserved bits [7:0]
[23:16]	G2	Global G2 gain value [7:0]

GBL_G1_WRITE

Address 0x004

Register Name GBL_G1_WRITE

Occurrences 1

Description Global write of G1 gain for all active channels

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:11]	RSVD	Reserved bits [20:0]
[10:0]	G1	Global G1 gain value [10:0]

IO_TRIM

Address 0x005

Register Name IO_TRIM

Occurrences 1

Description Differential I/O options and trim

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:25]	RSVD	Reserved bits [6:0]
[24]	CUR_MODE_O	Enable low current mode LVDS tx DAC side (default low)
[23]	CUR_MODE_I	Enable low current mode LVDS tx FPGA side (default high)
[22]	BIASI_EN	Enable RSETII output

[21]	BIASO_EN	Enable RSETIO output
[20]	SPISRC	Selects source of the BIAS generator trim bits (1=SPI)
[19:15]	TCTRIM_I	Input LVDS bias generator, temp compensation trim [4:0]
[14:10]	CTRL_I	Input LVDS bias generator, current level controls [4:0]
[9:5]	TCTRIM_O	DAC LVDS bias generator, temp compensation trim [4:0]
[4:0]	CTRL_O	DAC LVDS bias generator, current level controls [4:0]

SPI_BM_CNTS

Address 0x006

Register Name SPI_BM_CNTS

Occurrences 1

Description SPI Burst mode debug counters

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:16]	ADD_INC	Address increment count in SPI burst mode [15:0]
[15:0]	SCK_EDGE	SCLK positive edge count in SPI burst mode [15:0]

SPI_BM_CHKSUM

Address 0x007

Register Name SPI_BM_CHKSUM

Occurrences 1

Description SPI Burst mode checksum

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:0]	VAL	Checksum status value (SPI burst write mode) [31:0]

MASTER_KEY_1

Address 0x010

Register Name MASTER_KEY_1

Occurrences 1

Description Master key bits [31:0] (32 LSBs)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:0]	MKEY	Master Key register, 32 LSBs of 56 bits key [31:0]

MASTER_KEY_2

Address 0x011

Register Name MASTER_KEY_2

Occurrences 1

Description Master key bits [55:32] (24 MSBs)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:24]	RSVD	Reserved bits [7:0]
[23:0]	MKEY	Master Key register, 24 MSBs of 56 bits key [23:0]

CAPACITY_STATUS

Address 0x014

Register Name CAPACITY_STATUS

Occurrences 1

Description Channel capacity status.

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:16]	RSVD	Reserved bits [15:0]
[15:8]	FCAP	Factory programmed capacity, bits [7:0]
[7:5]	RSVD	Reserved bits [2:0]
[4:0]	CCAP	Current capacity [4:0]

IOL_INV

Address 0x020

Register Name IOL_INV

Occurrences 1

Description Invert the IO output data polarity

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:20]	RSVD	Reserved bits [11:0]
[19:10]	IADT	1: Invert the polarity of Port A data bits [9:0]
[9]	RSVD	Reserved bit
[8]	IAVLD	1: Invert the polarity of Port A Valid
[7]	IBPAR	1: Invert the polarity of Port B/C Parity
[6]	IAPAR	1: Invert the polarity of Port A Parity
[5]	IBRDY	1: Invert the polarity of Port B RDY
[4]	IARDY	1: Invert the polarity of Port A RDY
[3]	IPSYNC	1: Invert the polarity of PSYNC
[2]	IRSYNC	1: Invert the polarity of RDYSYNC
[1]	IPCLK	1: Invert the polarity of PCLK
[0]	IRCLK	1: Invert the polarity of RDY-CLK

IOL_CFG1

Address 0x021

Register Name IOL_CFG1

Occurrences 1

Description IO skew control registers

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	RSVD	Reserved bits [1:0]
[29:27]	A9	A9 skew adjustment [2:0]
[26:24]	A8	A8 skew adjustment [2:0]
[23:21]	A7	A7 skew adjustment [2:0]
[20:18]	A6	A6 skew adjustment [2:0]
[17:15]	A5	A5 skew adjustment [2:0]
[14:12]	A4	A4 skew adjustment [2:0]
[11:9]	A3	A3 skew adjustment [2:0]
[8:6]	A2	A2 skew adjustment [2:0]
[5:3]	A1	A1 skew adjustment [2:0]
[2:0]	A0	A0 skew adjustment [2:0]

IOL_CFG2

Address	0x022
Register Name	IOL_CFG2
Occurrences	1
Description	IO skew control registers

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	RSVD	Reserved bits [1:0]
[29:27]	SYNC5	SYNC5 skew adjustment [2:0]
[26:24]	B8	B8 skew adjustment [2:0]
[23:21]	B7	B7 skew adjustment [2:0]
[20:18]	B6	B6 skew adjustment [2:0]
[17:15]	B5	B5 skew adjustment [2:0]
[14:12]	B4	B4 skew adjustment [2:0]
[11:9]	B3	B3 skew adjustment [2:0]
[8:6]	B2	B2 skew adjustment [2:0]
[5:3]	B1	B1 skew adjustment [2:0]
[2:0]	B0	B0 skew adjustment [2:0]

IOL_CFG3

Address	0x023
Register Name	IOL_CFG3
Occurrences	1
Description	IO skew control registers

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	RSVD	Reserved bits [1:0]
[29:27]	SYNC4	SYNC4 skew adjustment [2:0]
[26:24]	SDCLK	SDCLK skew adjustment [2:0]
[23:21]	SYNC3	SYNC3 skew adjustment [2:0]
[20:18]	SYNC2	SYNC2 skew adjustment [2:0]
[17:15]	VALIDA	VALIBA skew adjustment [2:0]
[14:12]	SYNC1	SYNC1 skew adjustment [2:0]
[11:9]	PARA	PARA skew adjustment [2:0]
[8:6]	PARB	PARB skew adjustment [2:0]
[5:3]	SYNC	PSYNC skew adjustment [2:0]
[2:0]	RSVD	Reserved bits [2:0]

IOL_CFG4

Address 0x024

Register Name IOL_CFG4

Occurrences 1

Description IO skew control registers

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:15]	RSVD	Reserved bits [16:0]
[14:12]	DTO	DTO skew adjustment [2:0]
[11:9]	RDYCLK	RDYCLK skew adjustment [2:0]
[8:6]	RDYSYNC	RDYSYNC skew adjustment [2:0]
[5:3]	REF_CLK	REF_CLK skew adjustment [2:0]
[2:0]	RDYA	RDYA skew adjustment [2:0]

IOL_CFG5

Address 0x025

Register Name IOL_CFG5

Occurrences 1

Description IO skew control registers

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	RSVD	Reserved bits [1:0]
[29:27]	SYNC6	SYNC6 skew adjustment [2:0]
[26:24]	C8	C8 skew adjustment [2:0]
[23:21]	C7	C7 skew adjustment [2:0]
[20:18]	C6	C6 skew adjustment [2:0]
[17:15]	C5	C5 skew adjustment [2:0]
[14:12]	C4	C4 skew adjustment [2:0]
[11:9]	C3	C3 skew adjustment [2:0]
[8:6]	C2	C2 skew adjustment [2:0]
[5:3]	C1	C1 skew adjustment [2:0]
[2:0]	C0	C0 skew adjustment [2:0]

IOL_CFG6

Address 0x026

Register Name IOL_CFG6

Occurrences 1

Description IO General config

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

[31:20]	RSVD	Reserved bits [11:0]
[19]	CMFB_ENABLE	Output Common mode feedback level set 0: SSTL (off) 1: LVDS (on)
[18]	LOCM	Output common mode level control 0: LVDS 1: SSTL
[17]	PRE_EMPH	Output Pre-emphasis control: 0: no high frequency boost 1: 9dB boost at Nyquist frequency
[16]	SSTL_MODE_O	Set SSTL Output Level 0: SSTL12 1: SSTL15
[15:5]	RSVD	Reserved bits [10:0]
[4:3]	RADJ	Input resistor trim bits [1:0] 00: increased nominal termination value 01: nominal termination value 10: decreased nominal termination value 11: termination disabled
[2]	TERM_DIS	Termination control 0: terminations active 1: terminations disabled.
[1]	S15EN	Set SSTL Input Level 0: SSTL12 1: SSTL15
[0]	SSTL_MODE	Differential input level: 0: LVDS 1: SSTL

Bits 0-4 configure the receivers on the FPGA interface.

Bits 16-19 configure the output drivers on the FPGA interface.

(IO_TRIM register 0x005 bit 23 enables hi-current LVDS output drive if required.)

IOL_INV_OFDM

Address 0x027

Register Name IOL_INV_OFDM

Occurrences 1

Description Invert the IO LVDS OFDM port data polarity

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:27]	RSVD	Reserved bits [4:0]
[26]	SEO	1: swap even/odd captured data
[25]	ISYNC6	1: Invert the polarity of SYNC6
[24]	ISYNC5	1: Invert the polarity of SYNC5
[23]	ISYNC4	1: Invert the polarity of SYNC4
[22]	ISYNC3	1: Invert the polarity of SYNC3
[21]	ISYNC2	1: Invert the polarity of SYNC2
[20]	ISYNC1	1: Invert the polarity of SYNC1
[19]	IPARB	1: Invert the polarity of OFDM Parity
[18]	ISDCLK	1: Invert the polarity of SDCLK
[17:9]	ICDT	1: Invert the polarity of Port_C data bits [8:0]
[8:0]	IBDT	1: Invert the polarity of Port_B data bits [8:0]

SKEW_QA_1

Address 0x048

Register Name SKEW_QA_1

Occurrences 1

Description DUC to DAC interface output bit skew config register for QA bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	SPARE	Spare [1:0]
[29:27]	QA9	Qa9 skew adjustment [2:0]
[26:24]	QA8	Qa8 skew adjustment [2:0]
[23:21]	QA7	Qa7 skew adjustment [2:0]
[20:18]	QA6	Qa6 skew adjustment [2:0]
[17:15]	QA5	Qa5 skew adjustment [2:0]
[14:12]	QA4	Qa4 skew adjustment [2:0]
[11:9]	QA3	Qa3 skew adjustment [2:0]
[8:6]	QA2	Qa2 skew adjustment [2:0]
[5:3]	QA1	Qa1 skew adjustment [2:0]
[2:0]	QA0	Qa0 skew adjustment [2:0]

SKEW_QA_2

Address 0x049

Register Name SKEW_QA_2

Occurrences 1

Description DUC to DAC interface output bit skew config register for QA bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:15]	RSVD	Reserved bits [16:0]
[14:12]	SPARE	Spare [2:0]
[11:9]	QA13	Qa13 skew adjustment [2:0]
[8:6]	QA12	Qa12 skew adjustment [2:0]
[5:3]	QA11	Qa11 skew adjustment [2:0]
[2:0]	QA10	Qa10 skew adjustment [2:0]

SKEW_QB_1

Address 0x04A

Register Name SKEW_QB_1

Occurrences 1

Description DUC to DAC interface output bit skew config register for QB bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	SPARE	Spare [1:0]
[29:27]	QB9	Qb9 skew adjustment [2:0]
[26:24]	QB8	Qb8 skew adjustment [2:0]
[23:21]	QB7	Qb7 skew adjustment [2:0]
[20:18]	QB6	Qb6 skew adjustment [2:0]
[17:15]	QB5	Qb5 skew adjustment [2:0]
[14:12]	QB4	Qb4 skew adjustment [2:0]
[11:9]	QB3	Qb3 skew adjustment [2:0]
[8:6]	QB2	Qb2 skew adjustment [2:0]
[5:3]	QB1	Qb1 skew adjustment [2:0]
[2:0]	QB0	Qb0 skew adjustment [2:0]

SKEW_QB_2

Address 0x04B

Register Name SKEW_QB_2

Occurrences 1

Description DUC to DAC interface output bit skew config register for QB bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:15]	RSVD	Reserved bits [16:0]
[14:12]	SPARE	Spare1 [2:0]
[11:9]	QB13	Qb13 skew adjustment [2:0]
[8:6]	QB12	Qb12 skew adjustment [2:0]
[5:3]	QB11	Qb11 skew adjustment [2:0]
[2:0]	QB10	Qb10 skew adjustment [2:0]

SKEW_QC_1

Address 0x04C

Register Name SKEW_QC_1

Occurrences 1

Description DUC to DAC interface output bit skew config register for QC bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	SPARE	Spare [1:0]
[29:27]	QC9	Qc9 skew adjustment [2:0]
[26:24]	QC8	Qc8 skew adjustment [2:0]
[23:21]	QC7	Qc7 skew adjustment [2:0]
[20:18]	QC6	Qc6 skew adjustment [2:0]
[17:15]	QC5	Qc5 skew adjustment [2:0]
[14:12]	QC4	Qc4 skew adjustment [2:0]
[11:9]	QC3	Qc3 skew adjustment [2:0]
[8:6]	QC2	Qc2 skew adjustment [2:0]
[5:3]	QC1	Qc1 skew adjustment [2:0]
[2:0]	QC0	Qc0 skew adjustment [2:0]

SKEW_QC_2

Address 0x04D

Register Name SKEW_QC_2

Occurrences 1

Description DUC to DAC interface output bit skew config register for QC bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:15]	RSVD	Reserved bits [16:0]
[14:12]	SPARE	Spare1 [2:0]
[11:9]	QC13	Qc13 skew adjustment [2:0]
[8:6]	QC12	Qc12 skew adjustment [2:0]
[5:3]	QC11	Qc11 skew adjustment [2:0]
[2:0]	QC10	Qc10 skew adjustment [2:0]

SKEW_QD_1

Address 0x04E

Register Name SKEW_QD_1

Occurrences 1

Description DUC to DAC interface output bit skew config register for QD bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	SPARE	Spare [1:0]
[29:27]	QD9	Qd9 skew adjustment [2:0]
[26:24]	QD8	Qd8 skew adjustment [2:0]
[23:21]	QD7	Qd7 skew adjustment [2:0]
[20:18]	QD6	Qd6 skew adjustment [2:0]
[17:15]	QD5	Qd5 skew adjustment [2:0]
[14:12]	QD4	Qd4 skew adjustment [2:0]
[11:9]	QD3	Qd3 skew adjustment [2:0]
[8:6]	QD2	Qd2 skew adjustment [2:0]
[5:3]	QD1	Qd1 skew adjustment [2:0]
[2:0]	QD0	Qd0 skew adjustment [2:0]

SKEW_QD_2

Address 0x04F

Register Name SKEW_QD_2

Occurrences 1

Description DUC to DAC interface output bit skew config register for QD bus

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:24]	RSVD	Reserved bits [7:0]
[23:21]	DATACLK	Dataclk skew adjustment [2:0]
[20:18]	PAR	Parity skew adjustment [2:0]
[17:15]	XOR	XOR skew adjustment [2:0]
[14:12]	SYNC	SYNC skew adjustment [2:0]
[11:9]	QD13	Qd13 skew adjustment [2:0]
[8:6]	QD12	Qd12 skew adjustment [2:0]
[5:3]	QD11	Qd11 skew adjustment [2:0]
[2:0]	QD10	Qd10 skew adjustment [2:0]

DPDCFG

Address 0x038

Register Name DPDCFG

Occurrences 1

Description DPD Configuration

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:9]	RSVD	Reserved bits [22:0]
[8]	DPDG1G2_EN	Enable DPD G1 and DPD G2 branch
[7]	FDAC_2_3F_ON	DPD fdac_by2_3fout clk gating
[6]	HD3_HD2_ON	DPD hd3 & hd2 clk gating
[5]	INTER_DAC_ON	DPD interleaving err comp clk gating
[4]	FDAC_2_2F_ON	DPD fdac_by2_2fout dac clk gating
[3]	SIGN_2_2FOUT	Sign bit for fDAC/2-2fOUT
[2]	PREFILT_BYPASS	When ‘1’, pre-filter for fDAC/2-2fOUT branch is bypassed

[1]	DAC_EVEN_SAMPL	Default '0' indicates odd sample programmability. Value of '1' indicates even sampling to the DPD for nullifying 3RD order IMD and $f_{DAC}/2-3f_{OUT}$
[0]	BYPASS	DPD bypass

DPD_DEL

Address 0x039

Register Name DPD_DEL

Occurrences 1

Description DPD Delay 1

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0

[31:20]	RSVD	Reserved bits [11:0]
[19:16]	D1	DPD Delay 1 [3:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:8]	D2	DPD Delay 2 [3:0]
[7:4]	RSVD	Reserved bits [3:0]
[3:0]	D3	DPD Delay 3 [3:0]

DPD_GAIN1

Address 0x03A

Register Name DPD_GAIN1

Occurrences 1

Description DPD gain 1

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:25]	RSVD	Reserved bits [6:0]
[24:16]	G1	DPD gain 1 [8:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	G2	DPD gain 2 [11:0]

DPD_GAIN2

Address 0x03B

Register Name DPD_GAIN2

Occurrences 1

Description DPD gain 2

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27:16]	G3	DPD gain 3 [11:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	G4	DPD gain 4 [11:0]

DPD_GAIN3

Address 0x03C

Register Name DPD_GAIN3

Occurrences 1

Description DPD gain 3

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27:16]	G5	DPD gain 5 [11:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	G6	DPD gain 6 [11:0]

DPD_GAIN4

Address 0x03D

Register Name DPD_GAIN4

Occurrences 1

Description DPD gain 4

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27:16]	G7	DPD gain 7 [11:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	G8	DPD gain 8 [11:0]

DPD_GAIN5

Address 0x03E

Register Name DPD_GAIN5

Occurrences 1

Description DPD gain 5

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:24]	RSVD	Reserved bits [7:0]
[23:16]	G9	DPD fdac/2-2fout gain 9 [7:0]
[15:8]	RSVD	Reserved bits [7:0]
[7:0]	G10	DPD fdac/2-2fout gain 10 [7:0]

DPD_GAIN6

Address 0x03F

Register Name DPD_GAIN6

Occurrences 1

Description DPD gain 6

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

[31:24]	RSVD	Reserved bits [7:0]
[23:16]	G11	DPD sawtooth lower lsb gain 11 [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	G12	DPD sawtooth upper lsb gain 12 [11:0]

HS_CFG

Address 0x040

Register Name HS_CFG

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

[31:14]	RSVD	Reserved bits [17:0]
[13]	MODE2_EN	Allow MODE2 to load SYNC and XOR LFSR.
[12]	RSVD	Reserved bit
[11:8]	SPARE	Spare [3:0]
[7]	RSVD	Reserved bit
[6]	A_C_LVDS_OFF	Switch OFF pair of A and C LVDS
[5]	B_D_LVDS_OFF	Switch OFF pair of B and D LVDS
[4]	MOD_BD	Complement B and D outputs.
[3]	ENXCLK	Enable XOR clk output
[2]	XOR	Enable modulating data outputs with LSFR pattern
[1]	SYNC	Enable LSFR pattern on SYNC pin
[0]	DDS4_CW_LD	Load Modulator 4 frequency control word *

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

NCO4

Address 0x041

Register Name NCO4

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:22]	RSVD	Reserved bits [9:0]
[21:0]	FCW	Modulator 4 frequency control word [21:0]

GAIN56

Address 0x042

Register Name GAIN56

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

[31:25]	RSVD	Reserved bits [6:0]
[24:16]	G6	G6 gain value [8:0]
[15:9]	RSVD	Reserved bits [6:0]
[8:0]	G5	G5 gain value [8:0]

G56_PWR

Address 0x043

Register Name G56_PWR

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	DPD_SAT	DPD saturate **
[30]	MOD_SAT	M4 saturate **
[29]	ADDQ_SAT	ADD filter saturate **
[28]	F8Q_SAT	F8 filter saturate **
[27:16]	P6	P6 Power monitor threshold count [11:0]
[15:14]	RSVD	Reserved bits [1:0]
[13]	ADDI_SAT	ADD filter saturate **
[12]	F8I_SAT	F8 filter saturate **
[11:0]	P5	P5 Power monitor threshold count [11:0]

* * Denotes clear on write bit. A register write will clear the status.

PWRMON_CFG

Address 0x044

Register Name PWRMON_CFG

Occurrences 1

Description Power monitor control register

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:16]	RSVD	Reserved bits [15:0]
[15:8]	THLD	Power monitor threshold value in twos complement format [7:0]
[7:3]	RSVD	Reserved bits [4:0]
[2]	PM	Enable power monitor data collection
[1]	MODE	Selects above threshold (1) or below threshold (0)
[0]	RESET	Reset counters *

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

PWRMON

Address 0x045

Register Name PWRMON

Occurrences 2

Description Power monitor 48 bit timer register (32 LSBs)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:0]	COUNT	32 LSBs of 48 bits Power monitor start count [31:0]

PWRMON_2

Address 0x046

Register Name PWRMON

Occurrences 2

Description Power monitor 48 bit timer register (16 MSBs)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

31:16 : RSVD

[15:0]	COUNT	16 MSBs of 48 bits Power monitor start count [47:32]

LSFR_CFG

Address 0x047

Register Name LSFR_CFG

Occurrences 1

Description SYNC/XOR LSFR tap select register

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0

[31:16]	XOR	Enable feedback from LSFR MSB to low order bit positions [15:0]
[15:0]	SYNC	Enable feedback from LSFR MSB to low order bit positions [15:0]

One set of three registers is assigned to each of the five 32-channel combiners.

CC32_CFG

Address 0x05C + (CC32# * 0x004), where CC32# = 1 to 5

Register Name CC32_CFG

Occurrences 5

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:20]	RSVD	Reserved bits [11:0]
[19:17]	SPARE	Spare bit [2:0]
[16:1]	RSVD	Reserved bits [15:0]
[0]	DDS3_CW_LD	Load Modulator 3 frequency control word *

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

NCO3

Address 0x05D + (CC32# * 0x004), where CC32# = 1 to 5

Register Name NCO3

Occurrences 5

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:21]	RSVD	Reserved bits [10:0]
[29:0]	FCW3	Modulator 3 frequency control word [29:0]

C32_SAT

Address 0x05E + (CC32# * 0x004), where CC32# = 1 to 5

Register Name C32_SAT

Occurrences 5

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:9]	RSVD	Reserved bits [22:0]
[8]	MOD_SAT	M3 saturate **
[7]	ADDQ_SAT	ADD filter saturate **
[6]	F7Q_SAT	F7 filter saturate **
[5]	F6Q_SAT	F6 filter saturate **
[4]	F5Q_SAT	F5 filter saturate **
[3]	ADDI_SAT	ADD filter saturate **
[2]	F7I_SAT	F7 filter saturate **
[1]	F6I_SAT	F5 filter saturate **
[0]	F5I_SAT	F6 filter saturate **

* * Denotes clear--on--write bit. The bit must be written in order to clear the status.

CFG_CC-32MUTE

Address 0x080

Register Name CFG_CC32MUTE

Occurrences 1

Description configuration and 32 channel combiner mute bits

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	1	0	0	0	0	0	1	0	1	1	1	1	1

[31:18]	RSVD	Reserved bits [13:0]
[17]	TRNG	Enables Port A training sequence
[16]	LEVEL_DET	interrupts- 0: event triggered, 1: real-time (level detect)
[15:8]	MAX_SLOTS	Rollover value for slot counter [7:0] (min=16)
[7]	RSVD	Reserved bit
[6]	RSYNC	1: Enables internal ready sync generation for proper operation
[5]	RSVD	Reserved bit

[4]	MUTE32_E	1: Mute 32 block channel combiner #5, clocks are gated off
[3]	MUTE32_D	1: Mute 32 block channel combiner #4, clocks are gated off
[2]	MUTE32_C	1: Mute 32 block channel combiner #3, clocks are gated off
[1]	MUTE32_B	1: Mute 32 block channel combiner #2, clocks are gated off
[0]	MUTE32_A	1: Mute 32 block channel combiner #1, clocks are gated off

PWR_CFG2

Address 0x008

Register Name PWR_CFG2

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:17]	RSVD	Reserved bits [14:0]
[16]	NCO3Q_HR	SCQAM NCO3 control word width- 1:30 bits, 0:21 bits
[15]	NCO3O_HR	OFDM NCO3 control word width- 1:30 bits, 0:21 bits
[14:13]	PAR_OUT_SEL	00 - OR'd Port A,B,C parity, 01 - Port A parity, 10 - Port B,C parity [1:0]
[12:11]	RSVD	Reserved bits [1:0]
[10]	CC32_5	Power Down mode bit for 32 channel combiner block
[9]	CC32_4	Power Down mode bit for 32 channel combiner block
[8]	CC32_3	Power Down mode bit for 32 channel combiner block
[7]	CC32_2	Power Down mode bit for 32 channel combiner block
[6]	CC32_1	Power Down mode bit for 32 channel combiner block
[5]	OFDM_6	Power Down mode bit for OFDM block
[4]	OFDM_5	Power Down mode bit for OFDM block
[3]	OFDM_4	Power Down mode bit for OFDM block
[2]	OFDM_3	Power Down mode bit for OFDM block
[1]	OFDM_2	Power Down mode bit for OFDM block
[0]	OFDM_1	Power Down mode bit for OFDM block

These bits power-switch the selected 192MHz blocks and they will overwrite the CFG pin default (reset) settings.

Blocks may be permanently powered-down by factory configuration.

GLB_PWR_STATUS

Address 0x009

Register Name GLB_PWR_STATUS

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:11]	RSVD	Reserved bits [20:0]
[10]	CC32_5_ON	Power on status bit for 32 channel combiner
[9]	CC32_4_ON	Power on status bit for 32 channel combiner
[8]	CC32_3_ON	Power on status bit for 32 channel combiner
[7]	CC32_2_ON	Power on status bit for 32 channel combiner
[6]	CC32_1_ON	Power on status bit for 32 channel combiner
[5]	OFDM_6_ON	Power on status bit for OFDM block
[4]	OFDM_5_ON	Power on status bit for OFDM block
[3]	OFDM_4_ON	Power on status bit for OFDM block
[2]	OFDM_3_ON	Power on status bit for OFDM block
[1]	OFDM_2_ON	Power on status bit for OFDM block
[0]	OFDM_1_ON	Power on status bit for OFDM block

PWRDN

Address 0x00A

Register Name PWRDN

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

[31:19]	RSVD	Reserved bits [12:0]
[18]	C_PD	Port C LVDS power down control. 1-power down, 0 - powered on
[17]	B_PD	Port B LVDS power down control. 1-power down, 0 - powered on
[16]	A_PB	Port A LVDS power down control. 1-power down, 0 - powered on
[15:0]	SLP_DELAY	Counter to control sleep turn off/on rate. Min value 3. [15:0]

MUTE_8CC

Address 0x081

Register Name MUTE_8CC

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[31:20]	RSVD	Reserved bits [11:0]
[19]	MUTE8_20	Disables 20th 8 block channel combiner, clocks are gated off
[18]	MUTE8_19	Disables 19th 8 block channel combiner, clocks are gated off
[17]	MUTE8_18	Disables 18th 8 block channel combiner, clocks are gated off
[16]	MUTE8_17	Disables 17th 8 block channel combiner, clocks are gated off
[15]	MUTE8_16	Disables 16th 8 block channel combiner, clocks are gated off
[14]	MUTE8_15	Disables 15th 8 block channel combiner, clocks are gated off
[13]	MUTE8_14	Disables 14th 8 block channel combiner, clocks are gated off
[12]	MUTE8_13	Disables 13th 8 block channel combiner, clocks are gated off
[11]	MUTE8_12	Disables 12th 8 block channel combiner, clocks are gated off
[10]	MUTE8_11	Disables 11th 8 block channel combiner, clocks are gated off
[9]	MUTE8_10	Disables 10th 8 block channel combiner, clocks are gated off
[8]	MUTE8_9	Disables 9th 8 block channel combiner, clocks are gated off
[7]	MUTE8_8	Disables 8th 8 block channel combiner, clocks are gated off
[6]	MUTE8_7	Disables 7th 8 block channel combiner, clocks are gated off
[5]	MUTE8_6	Disables 6th 8 block channel combiner, clocks are gated off
[4]	MUTE8_5	Disables 5th 8 block channel combiner, clocks are gated off
[3]	MUTE8_4	Disables 4th 8 block channel combiner, clocks are gated off
[2]	MUTE8_3	Disables 3rd 8 block channel combiner, clocks are gated off
[1]	MUTE8_2	Disables 2nd 8 block channel combiner, clocks are gated off
[0]	MUTE8_1	Disables 1st 8 block channel combiner, clocks are gated off

PARITY_CFG

Address 0x082

Register Name PARITY_CFG

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

[31:26]	RSVD	Reserved bits [5:0]
[25]	SPARE	Spare register bit

[24]	EN_PAR_VALID	Enable parity calculation for time slots where valid=0
[23:22]	PARITY_DELAY	Define the delay of parity with resepect to the data [1:0] 0-3: Incoming parity bit is lagging by 0-3 clock periods
[21:11]	RSVD	Reserved bits [10:0]
[10]	PORTA_VALID_MASK	Mask valid bit for PortA parity calculation 0: mask the valid signal in parity calculation 1: use the valid signal in parity calculation
[9:0]	PORTA_MASK	Mask bits for parity calculation for PortA[9:0] data 0: ignore the corresponding data bit in parity calc 1: include the corresponding data bit in parity calc

CHAN_1

Address 0x088

Register Name CHAN_1

Occurrences 1

Description channel 1,2

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_2	Global FIFO reset enable
[26]	LCL_RST_2	Local FIFO reset pulse, self-clearing *
[25]	MUTE_2	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_2	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_1	Global FIFO reset enable
[10]	LCL_RST_1	Local FIFO reset pulse, self-clearing *
[9]	MUTE_1	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_1	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_3

Address 0x089

Register Name CHAN_3

Occurrences 1

Description channel 3,4

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_4	Global FIFO reset enable
[26]	LCL_RST_4	Local FIFO reset pulse, self-clearing *
[25]	MUTE_4	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_4	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_3	Global FIFO reset enable
[10]	LCL_RST_3	Local FIFO reset pulse, self-clearing *
[9]	MUTE_3	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_3	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_5

Address 0x08A

Register Name CHAN_5

Occurrences 1

Description channel 5,6

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_6	Global FIFO reset enable
[26]	LCL_RST_6	Local FIFO reset pulse, self-clearing *
[25]	MUTE_6	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_6	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_5	Global FIFO reset enable
[10]	LCL_RST_5	Local FIFO reset pulse, self-clearing *

[9]	MUTE_5	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_5	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_7

Address 0x08B

Register Name CHAN_7

Occurrences 1

Description channel 7,8

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_8	Global FIFO reset enable
[26]	LCL_RST_8	Local FIFO reset pulse, self-clearing *
[25]	MUTE_8	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_8	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_7	Global FIFO reset enable
[10]	LCL_RST_7	Local FIFO reset pulse, self-clearing *
[9]	MUTE_7	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_7	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_9

Address 0x08C

Register Name CHAN_9

Occurrences 1

Description channel 9,10

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_10	Global FIFO reset enable
[26]	LCL_RST_10	Local FIFO reset pulse, self-clearing *
[25]	MUTE_10	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_10	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_9	Global FIFO reset enable
[10]	LCL_RST_9	Local FIFO reset pulse, self-clearing *
[9]	MUTE_9	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_9	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_11

Address 0x08D

Register Name CHAN_11

Occurrences 1

Description channel 11,12

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_12	Global FIFO reset enable
[26]	LCL_RST_12	Local FIFO reset pulse, self-clearing *
[25]	MUTE_12	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_12	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_11	Global FIFO reset enable
[10]	LCL_RST_11	Local FIFO reset pulse, self-clearing *
[9]	MUTE_11	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_11	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_13

Address 0x08E

Register Name CHAN_13

Occurrences 1

Description channel 13,14

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_14	Global FIFO reset enable
[26]	LCL_RST_14	Local FIFO reset pulse, self-clearing *
[25]	MUTE_14	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_14	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_13	Global FIFO reset enable
[10]	LCL_RST_13	Local FIFO reset pulse, self-clearing *
[9]	MUTE_13	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_13	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_15

Address 0x08F

Register Name CHAN_15

Occurrences 1

Description channel 15,16

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_16	Global FIFO reset enable
[26]	LCL_RST_16	Local FIFO reset pulse, self-clearing *
[25]	MUTE_16	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_16	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_15	Global FIFO reset enable
[10]	LCL_RST_15	Local FIFO reset pulse, self-clearing *

[9]	MUTE_15	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_15	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_17

Address 0x090

Register Name CHAN_17

Occurrences 1

Description channel 17,18

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_18	Global FIFO reset enable
[26]	LCL_RST_18	Local FIFO reset pulse, self-clearing *
[25]	MUTE_18	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_18	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_17	Global FIFO reset enable
[10]	LCL_RST_17	Local FIFO reset pulse, self-clearing *
[9]	MUTE_17	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_17	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_19

Address 0x091

Register Name CHAN_19

Occurrences 1

Description channel 19,20

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_20	Global FIFO reset enable

[26]	LCL_RST_20	Local FIFO reset pulse, self-clearing *
[25]	MUTE_20	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_20	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_19	Global FIFO reset enable
[10]	LCL_RST_19	Local FIFO reset pulse, self-clearing *
[9]	MUTE_19	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_19	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_21

Address 0x092

Register Name CHAN_21

Occurrences 1

Description channel 21,22

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_22	Global FIFO reset enable
[26]	LCL_RST_22	Local FIFO reset pulse, self-clearing *
[25]	MUTE_22	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_22	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_21	Global FIFO reset enable
[10]	LCL_RST_21	Local FIFO reset pulse, self-clearing *
[9]	MUTE_21	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_21	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_23

Address 0x093

Register Name CHAN_23

Occurrences 1

Description channel 23,24

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_24	Global FIFO reset enable
[26]	LCL_RST_24	Local FIFO reset pulse, self-clearing *
[25]	MUTE_24	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_24	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_23	Global FIFO reset enable
[10]	LCL_RST_23	Local FIFO reset pulse, self-clearing *
[9]	MUTE_23	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_23	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_25

Address 0x094

Register Name CHAN_25

Occurrences 1

Description channel 25,26

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_26	Global FIFO reset enable
[26]	LCL_RST_26	Local FIFO reset pulse, self-clearing *
[25]	MUTE_26	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_26	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_25	Global FIFO reset enable
[10]	LCL_RST_25	Local FIFO reset pulse, self-clearing *

[9]	MUTE_25	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_25	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_27

Address 0x095

Register Name CHAN_27

Occurrences 1

Description channel 27,28

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_28	Global FIFO reset enable
[26]	LCL_RST_28	Local FIFO reset pulse, self-clearing *
[25]	MUTE_28	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_28	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_27	Global FIFO reset enable
[10]	LCL_RST_27	Local FIFO reset pulse, self-clearing *
[9]	MUTE_27	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_27	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_29

Address 0x096

Register Name CHAN_29

Occurrences 1

Description channel 29,30

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_30	Global FIFO reset enable
[26]	LCL_RST_30	Local FIFO reset pulse, self-clearing *
[25]	MUTE_30	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_30	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_29	Global FIFO reset enable
[10]	LCL_RST_29	Local FIFO reset pulse, self-clearing *
[9]	MUTE_29	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_29	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_31

Address 0x097

Register Name CHAN_31

Occurrences 1

Description channel 31,32

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_32	Global FIFO reset enable
[26]	LCL_RST_32	Local FIFO reset pulse, self-clearing *
[25]	MUTE_32	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_32	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_31	Global FIFO reset enable
[10]	LCL_RST_31	Local FIFO reset pulse, self-clearing *
[9]	MUTE_31	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_31	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_33

Address 0x098

Register Name CHAN_33

Occurrences 1

Description channel 33,34

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_34	Global FIFO reset enable
[26]	LCL_RST_34	Local FIFO reset pulse, self-clearing *
[25]	MUTE_34	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_34	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_33	Global FIFO reset enable
[10]	LCL_RST_33	Local FIFO reset pulse, self-clearing *
[9]	MUTE_33	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_33	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_35

Address 0x099

Register Name CHAN_35

Occurrences 1

Description channel 35,36

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_36	Global FIFO reset enable
[26]	LCL_RST_36	Local FIFO reset pulse, self-clearing *
[25]	MUTE_36	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_36	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_35	Global FIFO reset enable
[10]	LCL_RST_35	Local FIFO reset pulse, self-clearing *

[9]	MUTE_35	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_35	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_37

Address 0x09A

Register Name CHAN_37

Occurrences 1

Description channel 37,38

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_38	Global FIFO reset enable
[26]	LCL_RST_38	Local FIFO reset pulse, self-clearing *
[25]	MUTE_38	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_38	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_37	Global FIFO reset enable
[10]	LCL_RST_37	Local FIFO reset pulse, self-clearing *
[9]	MUTE_37	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_37	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_39

Address 0x09B

Register Name CHAN_39

Occurrences 1

Description channel 39,40

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_40	Global FIFO reset enable
[26]	LCL_RST_40	Local FIFO reset pulse, self-clearing *
[25]	MUTE_40	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_40	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_39	Global FIFO reset enable
[10]	LCL_RST_39	Local FIFO reset pulse, self-clearing *
[9]	MUTE_39	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_39	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_41

Address 0x09C

Register Name CHAN_41

Occurrences 1

Description channel 41,42

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_42	Global FIFO reset enable
[26]	LCL_RST_42	Local FIFO reset pulse, self-clearing *
[25]	MUTE_42	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_42	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_41	Global FIFO reset enable
[10]	LCL_RST_41	Local FIFO reset pulse, self-clearing *
[9]	MUTE_41	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_41	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_43

Address 0x09D

Register Name CHAN_43

Occurrences 1

Description channel 43,44

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_44	Global FIFO reset enable
[26]	LCL_RST_44	Local FIFO reset pulse, self-clearing *
[25]	MUTE_44	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_44	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_43	Global FIFO reset enable
[10]	LCL_RST_43	Local FIFO reset pulse, self-clearing *
[9]	MUTE_43	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_43	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_45

Address 0x09E

Register Name CHAN_45

Occurrences 1

Description channel 45,46

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_46	Global FIFO reset enable
[26]	LCL_RST_46	Local FIFO reset pulse, self-clearing *
[25]	MUTE_46	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_46	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_45	Global FIFO reset enable
[10]	LCL_RST_45	Local FIFO reset pulse, self-clearing *

[9]	MUTE_45	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_45	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_47

Address 0x09F

Register Name CHAN_47

Occurrences 1

Description channel 47,48

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_48	Global FIFO reset enable
[26]	LCL_RST_48	Local FIFO reset pulse, self-clearing *
[25]	MUTE_48	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_48	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_47	Global FIFO reset enable
[10]	LCL_RST_47	Local FIFO reset pulse, self-clearing *
[9]	MUTE_47	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_47	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_49

Address 0x0A0

Register Name CHAN_49

Occurrences 1

Description channel 49,50

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_50	Global FIFO reset enable
[26]	LCL_RST_50	Local FIFO reset pulse, self-clearing *
[25]	MUTE_50	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_50	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_49	Global FIFO reset enable
[10]	LCL_RST_49	Local FIFO reset pulse, self-clearing *
[9]	MUTE_49	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_49	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_51

Address 0x0A1

Register Name CHAN_51

Occurrences 1

Description channel 51,52

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_52	Global FIFO reset enable
[26]	LCL_RST_52	Local FIFO reset pulse, self-clearing *
[25]	MUTE_52	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_52	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_51	Global FIFO reset enable
[10]	LCL_RST_51	Local FIFO reset pulse, self-clearing *
[9]	MUTE_51	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_51	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_53

Address 0x0A2

Register Name CHAN_53

Occurrences 1

Description channel 53,54

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_54	Global FIFO reset enable
[26]	LCL_RST_54	Local FIFO reset pulse, self-clearing *
[25]	MUTE_54	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_54	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_53	Global FIFO reset enable
[10]	LCL_RST_53	Local FIFO reset pulse, self-clearing *
[9]	MUTE_53	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_53	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_55

Address 0x0A3

Register Name CHAN_55

Occurrences 1

Description channel 55,56

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_56	Global FIFO reset enable
[26]	LCL_RST_56	Local FIFO reset pulse, self-clearing *
[25]	MUTE_56	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_56	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_55	Global FIFO reset enable
[10]	LCL_RST_55	Local FIFO reset pulse, self-clearing *

[9]	MUTE_55	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_55	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_57

Address 0x0A4

Register Name CHAN_57

Occurrences 1

Description channel 57,58

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_58	Global FIFO reset enable
[26]	LCL_RST_58	Local FIFO reset pulse, self-clearing *
[25]	MUTE_58	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_58	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_57	Global FIFO reset enable
[10]	LCL_RST_57	Local FIFO reset pulse, self-clearing *
[9]	MUTE_57	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_57	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_59

Address 0x0A5

Register Name CHAN_59

Occurrences 1

Description channel 59,60

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_60	Global FIFO reset enable
[26]	LCL_RST_60	Local FIFO reset pulse, self-clearing *
[25]	MUTE_60	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_60	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_59	Global FIFO reset enable
[10]	LCL_RST_59	Local FIFO reset pulse, self-clearing *
[9]	MUTE_59	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_59	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_61

Address 0x0A6

Register Name CHAN_61

Occurrences 1

Description channel 61,62

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_62	Global FIFO reset enable
[26]	LCL_RST_62	Local FIFO reset pulse, self-clearing *
[25]	MUTE_62	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_62	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_61	Global FIFO reset enable
[10]	LCL_RST_61	Local FIFO reset pulse, self-clearing *
[9]	MUTE_61	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_61	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_63

Address 0x0A7

Register Name CHAN_63

Occurrences 1

Description channel 63,64

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_64	Global FIFO reset enable
[26]	LCL_RST_64	Local FIFO reset pulse, self-clearing *
[25]	MUTE_64	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_64	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_63	Global FIFO reset enable
[10]	LCL_RST_63	Local FIFO reset pulse, self-clearing *
[9]	MUTE_63	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_63	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_65

Address 0x0A8

Register Name CHAN_65

Occurrences 1

Description channel 65,66

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_66	Global FIFO reset enable
[26]	LCL_RST_66	Local FIFO reset pulse, self-clearing *
[25]	MUTE_66	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_66	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_65	Global FIFO reset enable
[10]	LCL_RST_65	Local FIFO reset pulse, self-clearing *

[9]	MUTE_65	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_65	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_67

Address 0x0A9

Register Name CHAN_67

Occurrences 1

Description channel 67,68

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_68	Global FIFO reset enable
[26]	LCL_RST_68	Local FIFO reset pulse, self-clearing *
[25]	MUTE_68	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_68	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_67	Global FIFO reset enable
[10]	LCL_RST_67	Local FIFO reset pulse, self-clearing *
[9]	MUTE_67	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_67	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_69

Address 0x0AA

Register Name CHAN_69

Occurrences 1

Description channel 69,70

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_70	Global FIFO reset enable
[26]	LCL_RST_70	Local FIFO reset pulse, self-clearing *
[25]	MUTE_70	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_70	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_69	Global FIFO reset enable
[10]	LCL_RST_69	Local FIFO reset pulse, self-clearing *
[9]	MUTE_69	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_69	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_71

Address 0x0AB

Register Name CHAN_71

Occurrences 1

Description channel 71,72

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_72	Global FIFO reset enable
[26]	LCL_RST_72	Local FIFO reset pulse, self-clearing *
[25]	MUTE_72	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_72	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_71	Global FIFO reset enable
[10]	LCL_RST_71	Local FIFO reset pulse, self-clearing *
[9]	MUTE_71	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_71	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_73

Address 0x0AC

Register Name CHAN_73

Occurrences 1

Description channel 73,74

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_74	Global FIFO reset enable
[26]	LCL_RST_74	Local FIFO reset pulse, self-clearing *
[25]	MUTE_74	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_74	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_73	Global FIFO reset enable
[10]	LCL_RST_73	Local FIFO reset pulse, self-clearing *
[9]	MUTE_73	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_73	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_75

Address 0x0AD

Register Name CHAN_75

Occurrences 1

Description channel 75,76

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_76	Global FIFO reset enable
[26]	LCL_RST_76	Local FIFO reset pulse, self-clearing *
[25]	MUTE_76	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_76	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_75	Global FIFO reset enable
[10]	LCL_RST_75	Local FIFO reset pulse, self-clearing *

[9]	MUTE_75	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_75	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_77

Address 0x0AE

Register Name CHAN_77

Occurrences 1

Description channel 77,78

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_78	Global FIFO reset enable
[26]	LCL_RST_78	Local FIFO reset pulse, self-clearing *
[25]	MUTE_78	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_78	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_77	Global FIFO reset enable
[10]	LCL_RST_77	Local FIFO reset pulse, self-clearing *
[9]	MUTE_77	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_77	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_79

Address 0x0AF

Register Name CHAN_79

Occurrences 1

Description channel 79,80

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_80	Global FIFO reset enable
[26]	LCL_RST_80	Local FIFO reset pulse, self-clearing *
[25]	MUTE_80	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_80	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_79	Global FIFO reset enable
[10]	LCL_RST_79	Local FIFO reset pulse, self-clearing *
[9]	MUTE_79	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_79	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_81

Address 0x0B0

Register Name CHAN_81

Occurrences 1

Description channel 81,82

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_82	Global FIFO reset enable
[26]	LCL_RST_82	Local FIFO reset pulse, self-clearing *
[25]	MUTE_82	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_82	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_81	Global FIFO reset enable
[10]	LCL_RST_81	Local FIFO reset pulse, self-clearing *
[9]	MUTE_81	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_81	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_83

Address 0x0B1

Register Name CHAN_83

Occurrences 1

Description channel 83,84

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_84	Global FIFO reset enable
[26]	LCL_RST_84	Local FIFO reset pulse, self-clearing *
[25]	MUTE_84	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_84	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_83	Global FIFO reset enable
[10]	LCL_RST_83	Local FIFO reset pulse, self-clearing *
[9]	MUTE_83	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_83	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_85

Address 0x0B2

Register Name CHAN_85

Occurrences 1

Description channel 85,86

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_86	Global FIFO reset enable
[26]	LCL_RST_86	Local FIFO reset pulse, self-clearing *
[25]	MUTE_86	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_86	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_85	Global FIFO reset enable
[10]	LCL_RST_85	Local FIFO reset pulse, self-clearing *

[9]	MUTE_85	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_85	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_87

Address 0x0B3

Register Name CHAN_87

Occurrences 1

Description channel 87,88

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_88	Global FIFO reset enable
[26]	LCL_RST_88	Local FIFO reset pulse, self-clearing *
[25]	MUTE_88	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_88	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_87	Global FIFO reset enable
[10]	LCL_RST_87	Local FIFO reset pulse, self-clearing *
[9]	MUTE_87	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_87	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_89

Address 0x0B4

Register Name CHAN_89

Occurrences 1

Description channel 89,90

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_90	Global FIFO reset enable
[26]	LCL_RST_90	Local FIFO reset pulse, self-clearing *
[25]	MUTE_90	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_90	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_89	Global FIFO reset enable
[10]	LCL_RST_89	Local FIFO reset pulse, self-clearing *
[9]	MUTE_89	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_89	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_91

Address 0x0B5

Register Name CHAN_91

Occurrences 1

Description channel 91,92

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_92	Global FIFO reset enable
[26]	LCL_RST_92	Local FIFO reset pulse, self-clearing *
[25]	MUTE_92	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_92	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_91	Global FIFO reset enable
[10]	LCL_RST_91	Local FIFO reset pulse, self-clearing *
[9]	MUTE_91	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_91	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_93

Address 0x0B6

Register Name CHAN_93

Occurrences 1

Description channel 93,94

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_94	Global FIFO reset enable
[26]	LCL_RST_94	Local FIFO reset pulse, self-clearing *
[25]	MUTE_94	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_94	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_93	Global FIFO reset enable
[10]	LCL_RST_93	Local FIFO reset pulse, self-clearing *
[9]	MUTE_93	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_93	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_95

Address 0x0B7

Register Name CHAN_95

Occurrences 1

Description channel 95,96

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_96	Global FIFO reset enable
[26]	LCL_RST_96	Local FIFO reset pulse, self-clearing *
[25]	MUTE_96	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_96	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_95	Global FIFO reset enable
[10]	LCL_RST_95	Local FIFO reset pulse, self-clearing *

[9]	MUTE_95	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_95	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_97

Address 0x0B8

Register Name CHAN_97

Occurrences 1

Description channel 97,98

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_98	Global FIFO reset enable
[26]	LCL_RST_98	Local FIFO reset pulse, self-clearing *
[25]	MUTE_98	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_98	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_97	Global FIFO reset enable
[10]	LCL_RST_97	Local FIFO reset pulse, self-clearing *
[9]	MUTE_97	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_97	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_99

Address 0x0B9

Register Name CHAN_99

Occurrences 1

Description channel 99,100

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_100	Global FIFO reset enable
[26]	LCL_RST_100	Local FIFO reset pulse, self-clearing *
[25]	MUTE_100	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_100	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_99	Global FIFO reset enable
[10]	LCL_RST_99	Local FIFO reset pulse, self-clearing *
[9]	MUTE_99	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_99	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_101

Address 0x0BA

Register Name CHAN_101

Occurrences 1

Description channel 101,102

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_102	Global FIFO reset enable
[26]	LCL_RST_102	Local FIFO reset pulse, self-clearing *
[25]	MUTE_102	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_102	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_101	Global FIFO reset enable
[10]	LCL_RST_101	Local FIFO reset pulse, self-clearing *
[9]	MUTE_101	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_101	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_103

Address 0x0BB

Register Name CHAN_103

Occurrences 1

Description channel 103,104

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_104	Global FIFO reset enable
[26]	LCL_RST_104	Local FIFO reset pulse, self-clearing *
[25]	MUTE_104	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_104	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_103	Global FIFO reset enable
[10]	LCL_RST_103	Local FIFO reset pulse, self-clearing *
[9]	MUTE_103	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_103	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_105

Address 0x0BC

Register Name CHAN_105

Occurrences 1

Description channel 105,106

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_106	Global FIFO reset enable
[26]	LCL_RST_106	Local FIFO reset pulse, self-clearing *
[25]	MUTE_106	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_106	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_105	Global FIFO reset enable
[10]	LCL_RST_105	Local FIFO reset pulse, self-clearing *

[9]	MUTE_105	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_105	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_107

Address 0x0BD

Register Name CHAN_107

Occurrences 1

Description channel 107,108

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_108	Global FIFO reset enable
[26]	LCL_RST_108	Local FIFO reset pulse, self-clearing *
[25]	MUTE_108	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_108	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_107	Global FIFO reset enable
[10]	LCL_RST_107	Local FIFO reset pulse, self-clearing *
[9]	MUTE_107	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_107	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_109

Address 0x0BE

Register Name CHAN_109

Occurrences 1

Description channel 109,110

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_110	Global FIFO reset enable
[26]	LCL_RST_110	Local FIFO reset pulse, self-clearing *
[25]	MUTE_110	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_110	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_109	Global FIFO reset enable
[10]	LCL_RST_109	Local FIFO reset pulse, self-clearing *
[9]	MUTE_109	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_109	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_111

Address 0x0BF

Register Name CHAN_111

Occurrences 1

Description channel 111,112

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_112	Global FIFO reset enable
[26]	LCL_RST_112	Local FIFO reset pulse, self-clearing *
[25]	MUTE_112	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_112	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_111	Global FIFO reset enable
[10]	LCL_RST_111	Local FIFO reset pulse, self-clearing *
[9]	MUTE_111	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_111	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_113

Address 0x0C0

Register Name CHAN_113

Occurrences 1

Description channel 113,114

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_114	Global FIFO reset enable
[26]	LCL_RST_114	Local FIFO reset pulse, self-clearing *
[25]	MUTE_114	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_114	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_113	Global FIFO reset enable
[10]	LCL_RST_113	Local FIFO reset pulse, self-clearing *
[9]	MUTE_113	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_113	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_115

Address 0x0C1

Register Name CHAN_115

Occurrences 1

Description channel 115,116

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_116	Global FIFO reset enable
[26]	LCL_RST_116	Local FIFO reset pulse, self-clearing *
[25]	MUTE_116	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_116	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_115	Global FIFO reset enable
[10]	LCL_RST_115	Local FIFO reset pulse, self-clearing *

[9]	MUTE_115	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_115	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_117

Address 0x0C2

Register Name CHAN_117

Occurrences 1

Description channel 117,118

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_118	Global FIFO reset enable
[26]	LCL_RST_118	Local FIFO reset pulse, self-clearing *
[25]	MUTE_118	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_118	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_117	Global FIFO reset enable
[10]	LCL_RST_117	Local FIFO reset pulse, self-clearing *
[9]	MUTE_117	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_117	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_119

Address 0x0C3

Register Name CHAN_119

Occurrences 1

Description channel 119,120

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_120	Global FIFO reset enable
[26]	LCL_RST_120	Local FIFO reset pulse, self-clearing *
[25]	MUTE_120	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_120	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_119	Global FIFO reset enable
[10]	LCL_RST_119	Local FIFO reset pulse, self-clearing *
[9]	MUTE_119	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_119	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_121

Address 0x0C4

Register Name CHAN_121

Occurrences 1

Description channel 121,122

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_122	Global FIFO reset enable
[26]	LCL_RST_122	Local FIFO reset pulse, self-clearing *
[25]	MUTE_122	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_122	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_121	Global FIFO reset enable
[10]	LCL_RST_121	Local FIFO reset pulse, self-clearing *
[9]	MUTE_121	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_121	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_123

Address 0x0C5

Register Name CHAN_123

Occurrences 1

Description channel 123,124

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_124	Global FIFO reset enable
[26]	LCL_RST_124	Local FIFO reset pulse, self-clearing *
[25]	MUTE_124	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_124	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_123	Global FIFO reset enable
[10]	LCL_RST_123	Local FIFO reset pulse, self-clearing *
[9]	MUTE_123	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_123	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_125

Address 0x0C6

Register Name CHAN_125

Occurrences 1

Description channel 125,126

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_126	Global FIFO reset enable
[26]	LCL_RST_126	Local FIFO reset pulse, self-clearing *
[25]	MUTE_126	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_126	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_125	Global FIFO reset enable
[10]	LCL_RST_125	Local FIFO reset pulse, self-clearing *

[9]	MUTE_125	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_125	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_127

Address 0x0C7

Register Name CHAN_127

Occurrences 1

Description channel 127,128

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_128	Global FIFO reset enable
[26]	LCL_RST_128	Local FIFO reset pulse, self-clearing *
[25]	MUTE_128	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_128	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_127	Global FIFO reset enable
[10]	LCL_RST_127	Local FIFO reset pulse, self-clearing *
[9]	MUTE_127	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_127	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_129

Address 0x0C8

Register Name CHAN_129

Occurrences 1

Description channel 129,130

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_130	Global FIFO reset enable
[26]	LCL_RST_130	Local FIFO reset pulse, self-clearing *
[25]	MUTE_130	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_130	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_129	Global FIFO reset enable
[10]	LCL_RST_129	Local FIFO reset pulse, self-clearing *
[9]	MUTE_129	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_129	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_131

Address 0x0C9

Register Name CHAN_131

Occurrences 1

Description channel 131,132

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_132	Global FIFO reset enable
[26]	LCL_RST_132	Local FIFO reset pulse, self-clearing *
[25]	MUTE_132	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_132	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_131	Global FIFO reset enable
[10]	LCL_RST_131	Local FIFO reset pulse, self-clearing *
[9]	MUTE_131	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_131	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_133

Address 0x0CA

Register Name CHAN_133

Occurrences 1

Description channel 133,134

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_134	Global FIFO reset enable
[26]	LCL_RST_134	Local FIFO reset pulse, self-clearing *
[25]	MUTE_134	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_134	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_133	Global FIFO reset enable
[10]	LCL_RST_133	Local FIFO reset pulse, self-clearing *
[9]	MUTE_133	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_133	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_135

Address 0x0CB

Register Name CHAN_135

Occurrences 1

Description channel 135,136

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_136	Global FIFO reset enable
[26]	LCL_RST_136	Local FIFO reset pulse, self-clearing *
[25]	MUTE_136	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_136	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_135	Global FIFO reset enable
[10]	LCL_RST_135	Local FIFO reset pulse, self-clearing *

[9]	MUTE_135	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_135	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_137

Address 0x0CC

Register Name CHAN_137

Occurrences 1

Description channel 137,138

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_138	Global FIFO reset enable
[26]	LCL_RST_138	Local FIFO reset pulse, self-clearing *
[25]	MUTE_138	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_138	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_137	Global FIFO reset enable
[10]	LCL_RST_137	Local FIFO reset pulse, self-clearing *
[9]	MUTE_137	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_137	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_139

Address 0x0CD

Register Name CHAN_139

Occurrences 1

Description channel 139,140

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_140	Global FIFO reset enable
[26]	LCL_RST_140	Local FIFO reset pulse, self-clearing *
[25]	MUTE_140	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_140	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_139	Global FIFO reset enable
[10]	LCL_RST_139	Local FIFO reset pulse, self-clearing *
[9]	MUTE_139	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_139	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_141

Address 0x0CE

Register Name CHAN_141

Occurrences 1

Description channel 141,142

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_142	Global FIFO reset enable
[26]	LCL_RST_142	Local FIFO reset pulse, self-clearing *
[25]	MUTE_142	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_142	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_141	Global FIFO reset enable
[10]	LCL_RST_141	Local FIFO reset pulse, self-clearing *
[9]	MUTE_141	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_141	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_143

Address 0x0CF

Register Name CHAN_143

Occurrences 1

Description channel 143,144

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_144	Global FIFO reset enable
[26]	LCL_RST_144	Local FIFO reset pulse, self-clearing *
[25]	MUTE_144	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_144	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_143	Global FIFO reset enable
[10]	LCL_RST_143	Local FIFO reset pulse, self-clearing *
[9]	MUTE_143	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_143	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_145

Address 0x0D0

Register Name CHAN_145

Occurrences 1

Description channel 145,146

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_146	Global FIFO reset enable
[26]	LCL_RST_146	Local FIFO reset pulse, self-clearing *
[25]	MUTE_146	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_146	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_145	Global FIFO reset enable
[10]	LCL_RST_145	Local FIFO reset pulse, self-clearing *

[9]	MUTE_145	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_145	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_147

Address 0x0D1

Register Name CHAN_147

Occurrences 1

Description channel 147,148

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_148	Global FIFO reset enable
[26]	LCL_RST_148	Local FIFO reset pulse, self-clearing *
[25]	MUTE_148	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_148	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_147	Global FIFO reset enable
[10]	LCL_RST_147	Local FIFO reset pulse, self-clearing *
[9]	MUTE_147	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_147	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_149

Address 0x0D2

Register Name CHAN_149

Occurrences 1

Description channel 149,150

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_150	Global FIFO reset enable
[26]	LCL_RST_150	Local FIFO reset pulse, self-clearing *
[25]	MUTE_150	Mute the channel, 1:channel off, 0: channel on

[24]	RSVD	Reserved bit
[23:16]	SLOT_150	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_149	Global FIFO reset enable
[10]	LCL_RST_149	Local FIFO reset pulse, self-clearing *
[9]	MUTE_149	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_149	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_151

Address 0x0D3

Register Name CHAN_151

Occurrences 1

Description channel 151,152

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_152	Global FIFO reset enable
[26]	LCL_RST_152	Local FIFO reset pulse, self-clearing *
[25]	MUTE_152	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_152	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_151	Global FIFO reset enable
[10]	LCL_RST_151	Local FIFO reset pulse, self-clearing *
[9]	MUTE_151	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_151	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_153

Address 0x0D4

Register Name CHAN_153

Occurrences 1

Description channel 153,154

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_154	Global FIFO reset enable
[26]	LCL_RST_154	Local FIFO reset pulse, self-clearing *
[25]	MUTE_154	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_154	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_153	Global FIFO reset enable
[10]	LCL_RST_153	Local FIFO reset pulse, self-clearing *
[9]	MUTE_153	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_153	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_155

Address 0x0D5

Register Name CHAN_155

Occurrences 1

Description channel 155,156

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_156	Global FIFO reset enable
[26]	LCL_RST_156	Local FIFO reset pulse, self-clearing *
[25]	MUTE_156	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_156	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_155	Global FIFO reset enable
[10]	LCL_RST_155	Local FIFO reset pulse, self-clearing *
[9]	MUTE_155	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_155	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_157

Address 0x0D6

Register Name CHAN_157

Occurrences 1

Description channel 157,158

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_158	Global FIFO reset enable
[26]	LCL_RST_158	Local FIFO reset pulse, self-clearing *
[25]	MUTE_158	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_158	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_157	Global FIFO reset enable
[10]	LCL_RST_157	Local FIFO reset pulse, self-clearing *
[9]	MUTE_157	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_157	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

CHAN_159

Address 0x0D7

Register Name CHAN_159

Occurrences 1

Description channel 159,160

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	GBL_RST_160	Global FIFO reset enable
[26]	LCL_RST_160	Local FIFO reset pulse, self-clearing *
[25]	MUTE_160	Mute the channel, 1:channel off, 0: channel on
[24]	RSVD	Reserved bit
[23:16]	SLOT_160	Defines the time slot value for this channel [7:0]
[15:12]	RSVD	Reserved bits [3:0]
[11]	GBL_RST_159	Global FIFO reset enable
[10]	LCL_RST_159	Local FIFO reset pulse, self-clearing *

[9]	MUTE_159	Mute the channel, 1:channel off, 0: channel on
[8]	RSVD	Reserved bit
[7:0]	SLOT_159	Defines the time slot value for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

INTERRUPT_CTRL

Address 0x0D8

Register Name INTERRUPT_CTRL

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	INTRP	Global interrupt enable
[30]	LOCK_EN	Selects lock condition for DAC_DLL_LOCK (bit 13) interrupt. 0 – enable “DLL locked”
[25]	OFIFO	Enable input FIFO overflow interrupt
[24]	UFIFO	Enable input FIFO underflow interrupt
[23]	PHERR	Enable Port D2 clock changed phase interrupt
[22]	DPERR	Enable DAC Parity Error interrupt
[21]	DDLOCK	Enable DAC DLL LOCK interrupt
[20]	PERRB	Enable parityB/C error interrupt
[19]	PERRA	Enable parityA error interrupt
[18]	PMON	Enable power monitor interrupt
[17]	OTEST	Enable output test mode interrupt
[16]	CAP	Enable channel count exceeded interrupt
[15]	PH_ERR_STAT	Port D2 clock changed phase real time
[14]	DAC_PERR_STAT	DAC Parity error real time status
[13]	DAC_DLL_LOCK	DAC DLL LOCK status When LOCK_EN (bit 30)=1, DLL is LOCKED when ‘1’. The status bit sets on the rising edge of the DAC indicator signal. When LOCK_EN=0, DLL is NOT LOCKED when ‘1’. The status bit sets on the falling edge of the DAC indicator.
[12]	PWR_MON	Power monitor period complete status
[11]	OUT_TEST	Output test mode status
[10]	MAX_CH	Channel count exceeded status
[9]	LAT_OFIFO	Any input FIFO overflow status
[8]	LAT_UFIFO	Any input FIFO underlow status

[7]	PORT_PH_ERR	Port D2 clock changed phase latched status **
[6]	DAC_PERR	LSR DAC Parity error latched status **
[5]	DAC_LOCK	LSR DAC DLL LOCK latched status **
[4]	PARITYB_ERR	Parity error latched status for Port B/C **
[3]	PARITYA_ERR	Parity error latched status for Port A **
[2]	PWR_MON_IN	Power monitor period complete latched status **
[1]	LAT_OTEST	Output test mode latched status **
[0]	LAT_MAX_CH	Channel count exceeded latched status **

* * Denotes clear on write bit. A register write will clear the status.

How to interpret the DLL lock condition:

Setting LOCK_EN == 0 enables the interrupt.

if (DAC_LOCK == 1 && DAC_DLL_LOCK == 1) Lock has been lost;

else if (DAC_LOCK == 1 && DAC_DLL_LOCK == 0) Locked now, but previously lost lock;

else if (DAC_LOCK == 0 && DAC_DLL_LOCK == 0) Locked;

else (DAC_LOCK == 0 && DAC_DLL_LOCK == 1) DLL was never locked;

INT_FIFO_SUM

Address 0x0D9

Register Name INT_FIFO_SUM

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:20]	RSVD	Reserved bits [11:0]
[19]	OFDMX	Interrup summary for Port B/C demux
[18:13]	IFFT	Interrup summary for OFMD channels 6-1 [5:0]
[12]	UFSUM_5	Underflow summary for channels 160-129
[11]	UFSUM_4	Underflow summary for channels 128-97
[10]	UFSUM_3	Underflow summary for channels 96-65
[9]	UFSUM_2	Underflow summary for channels 64-33
[8]	UFSUM_1	Underflow summary for channels 32-1
[7:5]	RSVD	Reserved bits [2:0]
[4]	OFSUM_5	Overflow summary for channels 160-129
[3]	OFSUM_4	Overflow summary for channels 128-97
[2]	OFSUM_3	Overflow summary for channels 96-65
[1]	OFSUM_2	Overflow summary for channels 64-33

[0]	OFSUM_1	Overflow summary for channels 32-1

OFLOW_1

Address 0x0DA

Register Name OFLOW_1

Occurrences 1

Description Overflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	OF_32	Input FIFO 32 overflow LSR **
[30]	OF_31	Input FIFO 31 overflow LSR **
[29]	OF_30	Input FIFO 30 overflow LSR **
[28]	OF_29	Input FIFO 29 overflow LSR **
[27]	OF_28	Input FIFO 28 overflow LSR **
[26]	OF_27	Input FIFO 27 overflow LSR **
[25]	OF_26	Input FIFO 26 overflow LSR **
[24]	OF_25	Input FIFO 25 overflow LSR **
[23]	OF_24	Input FIFO 24 overflow LSR **
[22]	OF_23	Input FIFO 23 overflow LSR **
[21]	OF_22	Input FIFO 22 overflow LSR **
[20]	OF_21	Input FIFO 21 overflow LSR **
[19]	OF_20	Input FIFO 20 overflow LSR **
[18]	OF_19	Input FIFO 19 overflow LSR **
[17]	OF_18	Input FIFO 18 overflow LSR **
[16]	OF_17	Input FIFO 17 overflow LSR **
[15]	OF_16	Input FIFO 16 overflow LSR **
[14]	OF_15	Input FIFO 15 overflow LSR **
[13]	OF_14	Input FIFO 14 overflow LSR **
[12]	OF_13	Input FIFO 13 overflow LSR **
[11]	OF_12	Input FIFO 12 overflow LSR **
[10]	OF_11	Input FIFO 11 overflow LSR **
[9]	OF_10	Input FIFO 10 overflow LSR **
[8]	OF_9	Input FIFO 9 overflow LSR **
[7]	OF_8	Input FIFO 8 overflow LSR **
[6]	OF_7	Input FIFO 7 overflow LSR **
[5]	OF_6	Input FIFO 6 overflow LSR **
[4]	OF_5	Input FIFO 5 overflow LSR **
[3]	OF_4	Input FIFO 4 overflow LSR **
[2]	OF_3	Input FIFO 3 overflow LSR **

[1]	OF_2	Input FIFO 2 overflow LSR **
[0]	OF_1	Input FIFO 1 overflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

OFLOW_2

Address	0x0DB
Register Name	OFLOW_2
Occurrences	1
Description	Overflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	OF_64	Input FIFO 64 overflow LSR **
[30]	OF_63	Input FIFO 63 overflow LSR **
[29]	OF_62	Input FIFO 62 overflow LSR **
[28]	OF_61	Input FIFO 61 overflow LSR **
[27]	OF_60	Input FIFO 60 overflow LSR **
[26]	OF_59	Input FIFO 59 overflow LSR **
[25]	OF_58	Input FIFO 58 overflow LSR **
[24]	OF_57	Input FIFO 57 overflow LSR **
[23]	OF_56	Input FIFO 56 overflow LSR **
[22]	OF_55	Input FIFO 55 overflow LSR **
[21]	OF_54	Input FIFO 54 overflow LSR **
[20]	OF_53	Input FIFO 53 overflow LSR **
[19]	OF_52	Input FIFO 52 overflow LSR **
[18]	OF_51	Input FIFO 51 overflow LSR **
[17]	OF_50	Input FIFO 50 overflow LSR **
[16]	OF_49	Input FIFO 49 overflow LSR **
[15]	OF_48	Input FIFO 48 overflow LSR **
[14]	OF_47	Input FIFO 47 overflow LSR **
[13]	OF_46	Input FIFO 46 overflow LSR **
[12]	OF_45	Input FIFO 45 overflow LSR **
[11]	OF_44	Input FIFO 44 overflow LSR **
[10]	OF_43	Input FIFO 43 overflow LSR **
[9]	OF_42	Input FIFO 42 overflow LSR **
[8]	OF_41	Input FIFO 41 overflow LSR **
[7]	OF_40	Input FIFO 40 overflow LSR **
[6]	OF_39	Input FIFO 39 overflow LSR **

[5]	OF_38	Input FIFO 38 overflow LSR **
[4]	OF_37	Input FIFO 37 overflow LSR **
[3]	OF_36	Input FIFO 36 overflow LSR **
[2]	OF_35	Input FIFO 35 overflow LSR **
[1]	OF_34	Input FIFO 34 overflow LSR **
[0]	OF_33	Input FIFO 33 overflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

OFLOW_3

Address 0x0DC

Register Name OFLOW_3

Occurrences 1

Description Overflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	OF_96	Input FIFO 96 overflow LSR **
[30]	OF_95	Input FIFO 95 overflow LSR **
[29]	OF_94	Input FIFO 94 overflow LSR **
[28]	OF_93	Input FIFO 93 overflow LSR **
[27]	OF_92	Input FIFO 92 overflow LSR **
[26]	OF_91	Input FIFO 91 overflow LSR **
[25]	OF_90	Input FIFO 90 overflow LSR **
[24]	OF_89	Input FIFO 89 overflow LSR **
[23]	OF_88	Input FIFO 88 overflow LSR **
[22]	OF_87	Input FIFO 87 overflow LSR **
[21]	OF_86	Input FIFO 86 overflow LSR **
[20]	OF_85	Input FIFO 85 overflow LSR **
[19]	OF_84	Input FIFO 84 overflow LSR **
[18]	OF_83	Input FIFO 83 overflow LSR **
[17]	OF_82	Input FIFO 82 overflow LSR **
[16]	OF_81	Input FIFO 81 overflow LSR **
[15]	OF_80	Input FIFO 80 overflow LSR **
[14]	OF_79	Input FIFO 79 overflow LSR **
[13]	OF_78	Input FIFO 78 overflow LSR **
[12]	OF_77	Input FIFO 77 overflow LSR **
[11]	OF_76	Input FIFO 76 overflow LSR **
[10]	OF_75	Input FIFO 75 overflow LSR **
[9]	OF_74	Input FIFO 74 overflow LSR **
[8]	OF_73	Input FIFO 73 overflow LSR **

[7]	OF_72	Input FIFO 72 overflow LSR **
[6]	OF_71	Input FIFO 71 overflow LSR **
[5]	OF_70	Input FIFO 70 overflow LSR **
[4]	OF_69	Input FIFO 69 overflow LSR **
[3]	OF_68	Input FIFO 68 overflow LSR **
[2]	OF_67	Input FIFO 67 overflow LSR **
[1]	OF_66	Input FIFO 66 overflow LSR **
[0]	OF_65	Input FIFO 65 overflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

OFLOW_4

Address 0x0DD

Register Name OFLOW_4

Occurrences 1

Description Overflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	OF_128	Input FIFO 128 overflow LSR **
[30]	OF_127	Input FIFO 127 overflow LSR **
[29]	OF_126	Input FIFO 126 overflow LSR **
[28]	OF_125	Input FIFO 125 overflow LSR **
[27]	OF_124	Input FIFO 124 overflow LSR **
[26]	OF_123	Input FIFO 123 overflow LSR **
[25]	OF_122	Input FIFO 122 overflow LSR **
[24]	OF_121	Input FIFO 121 overflow LSR **
[23]	OF_120	Input FIFO 120 overflow LSR **
[22]	OF_119	Input FIFO 119 overflow LSR **
[21]	OF_118	Input FIFO 118 overflow LSR **
[20]	OF_117	Input FIFO 117 overflow LSR **
[19]	OF_116	Input FIFO 116 overflow LSR **
[18]	OF_115	Input FIFO 115 overflow LSR **
[17]	OF_114	Input FIFO 114 overflow LSR **
[16]	OF_113	Input FIFO 113 overflow LSR **
[15]	OF_112	Input FIFO 112 overflow LSR **
[14]	OF_111	Input FIFO 111 overflow LSR **
[13]	OF_110	Input FIFO 110 overflow LSR **
[12]	OF_109	Input FIFO 109 overflow LSR **
[11]	OF_108	Input FIFO 108 overflow LSR **
[10]	OF_107	Input FIFO 107 overflow LSR **

[9]	OF_106	Input FIFO 106 overflow LSR **
[8]	OF_105	Input FIFO 105 overflow LSR **
[7]	OF_104	Input FIFO 104 overflow LSR **
[6]	OF_103	Input FIFO 103 overflow LSR **
[5]	OF_102	Input FIFO 102 overflow LSR **
[4]	OF_101	Input FIFO 101 overflow LSR **
[3]	OF_100	Input FIFO 100 overflow LSR **
[2]	OF_99	Input FIFO 99 overflow LSR **
[1]	OF_98	Input FIFO 98 overflow LSR **
[0]	OF_97	Input FIFO 97 overflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

OFLOW_5

Address	0x0DE
Register Name	OFLOW_5
Occurrences	1
Description	Overflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	OF_160	Input FIFO 160 overflow LSR **
[30]	OF_159	Input FIFO 159 overflow LSR **
[29]	OF_158	Input FIFO 158 overflow LSR **
[28]	OF_157	Input FIFO 157 overflow LSR **
[27]	OF_156	Input FIFO 156 overflow LSR **
[26]	OF_155	Input FIFO 155 overflow LSR **
[25]	OF_154	Input FIFO 154 overflow LSR **
[24]	OF_153	Input FIFO 153 overflow LSR **
[23]	OF_152	Input FIFO 152 overflow LSR **
[22]	OF_151	Input FIFO 151 overflow LSR **
[21]	OF_150	Input FIFO 150 overflow LSR **
[20]	OF_149	Input FIFO 149 overflow LSR **
[19]	OF_148	Input FIFO 148 overflow LSR **
[18]	OF_147	Input FIFO 147 overflow LSR **
[17]	OF_146	Input FIFO 146 overflow LSR **
[16]	OF_145	Input FIFO 145 overflow LSR **
[15]	OF_144	Input FIFO 144 overflow LSR **
[14]	OF_143	Input FIFO 143 overflow LSR **

[13]	OF_142	Input FIFO 142 overflow LSR **
[12]	OF_141	Input FIFO 141 overflow LSR **
[11]	OF_140	Input FIFO 140 overflow LSR **
[10]	OF_139	Input FIFO 139 overflow LSR **
[9]	OF_138	Input FIFO 138 overflow LSR **
[8]	OF_137	Input FIFO 137 overflow LSR **
[7]	OF_136	Input FIFO 136 overflow LSR **
[6]	OF_135	Input FIFO 135 overflow LSR **
[5]	OF_134	Input FIFO 134 overflow LSR **
[4]	OF_133	Input FIFO 133 overflow LSR **
[3]	OF_132	Input FIFO 132 overflow LSR **
[2]	OF_131	Input FIFO 131 overflow LSR **
[1]	OF_130	Input FIFO 130 overflow LSR **
[0]	OF_129	Input FIFO 129 overflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

UFLOW_1

Address	0x0DF
Register Name	UFLOW_1
Occurrences	1
Description	Underflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	UF_32	Input FIFO 32 underflow LSR **
[30]	UF_31	Input FIFO 31 underflow LSR **
[29]	UF_30	Input FIFO 30 underflow LSR **
[28]	UF_29	Input FIFO 29 underflow LSR **
[27]	UF_28	Input FIFO 28 underflow LSR **
[26]	UF_27	Input FIFO 27 underflow LSR **
[25]	UF_26	Input FIFO 26 underflow LSR **
[24]	UF_25	Input FIFO 25 underflow LSR **
[23]	UF_24	Input FIFO 24 underflow LSR **
[22]	UF_23	Input FIFO 23 underflow LSR **
[21]	UF_22	Input FIFO 22 underflow LSR **
[20]	UF_21	Input FIFO 21 underflow LSR **
[19]	UF_20	Input FIFO 20 underflow LSR **
[18]	UF_19	Input FIFO 19 underflow LSR **
[17]	UF_18	Input FIFO 18 underflow LSR **
[16]	UF_17	Input FIFO 17 underflow LSR **

[15]	UF_16	Input FIFO 16 underflow LSR **
[14]	UF_15	Input FIFO 15 underflow LSR **
[13]	UF_14	Input FIFO 14 underflow LSR **
[12]	UF_13	Input FIFO 13 underflow LSR **
[11]	UF_12	Input FIFO 12 underflow LSR **
[10]	UF_11	Input FIFO 11 underflow LSR **
[9]	UF_10	Input FIFO 10 underflow LSR **
[8]	UF_9	Input FIFO 9 underflow LSR **
[7]	UF_8	Input FIFO 8 underflow LSR **
[6]	UF_7	Input FIFO 7 underflow LSR **
[5]	UF_6	Input FIFO 6 underflow LSR **
[4]	UF_5	Input FIFO 5 underflow LSR **
[3]	UF_4	Input FIFO 4 underflow LSR **
[2]	UF_3	Input FIFO 3 underflow LSR **
[1]	UF_2	Input FIFO 2 underflow LSR **
[0]	UF_1	Input FIFO 1 underflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

UFLOW_2

Address 0x0E0

Register Name UFLOW_2

Occurrences 1

Description Underflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	UF_64	Input FIFO 64 underflow LSR **
[30]	UF_63	Input FIFO 63 underflow LSR **
[29]	UF_62	Input FIFO 62 underflow LSR **
[28]	UF_61	Input FIFO 61 underflow LSR **
[27]	UF_60	Input FIFO 60 underflow LSR **
[26]	UF_59	Input FIFO 59 underflow LSR **
[25]	UF_58	Input FIFO 58 underflow LSR **
[24]	UF_57	Input FIFO 57 underflow LSR **
[23]	UF_56	Input FIFO 56 underflow LSR **
[22]	UF_55	Input FIFO 55 underflow LSR **
[21]	UF_54	Input FIFO 54 underflow LSR **
[20]	UF_53	Input FIFO 53 underflow LSR **
[19]	UF_52	Input FIFO 52 underflow LSR **
[18]	UF_51	Input FIFO 51 underflow LSR **

[17]	UF_50	Input FIFO 50 underflow LSR **
[16]	UF_49	Input FIFO 49 underflow LSR **
[15]	UF_48	Input FIFO 48 underflow LSR **
[14]	UF_47	Input FIFO 47 underflow LSR **
[13]	UF_46	Input FIFO 46 underflow LSR **
[12]	UF_45	Input FIFO 45 underflow LSR **
[11]	UF_44	Input FIFO 44 underflow LSR **
[10]	UF_43	Input FIFO 43 underflow LSR **
[9]	UF_42	Input FIFO 42 underflow LSR **
[8]	UF_41	Input FIFO 41 underflow LSR **
[7]	UF_40	Input FIFO 40 underflow LSR **
[6]	UF_39	Input FIFO 39 underflow LSR **
[5]	UF_38	Input FIFO 38 underflow LSR **
[4]	UF_37	Input FIFO 37 underflow LSR **
[3]	UF_36	Input FIFO 36 underflow LSR **
[2]	UF_35	Input FIFO 35 underflow LSR **
[1]	UF_34	Input FIFO 34 underflow LSR **
[0]	UF_33	Input FIFO 33 underflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

UFLOW_3

Address	0x0E1
Register Name	UFLOW_3
Occurrences	1
Description	Underflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	UF_96	Input FIFO 96 underflow LSR **
[30]	UF_95	Input FIFO 95 underflow LSR **
[29]	UF_94	Input FIFO 94 underflow LSR **
[28]	UF_93	Input FIFO 93 underflow LSR **
[27]	UF_92	Input FIFO 92 underflow LSR **
[26]	UF_91	Input FIFO 91 underflow LSR **
[25]	UF_90	Input FIFO 90 underflow LSR **
[24]	UF_89	Input FIFO 89 underflow LSR **
[23]	UF_88	Input FIFO 88 underflow LSR **
[22]	UF_87	Input FIFO 87 underflow LSR **
[21]	UF_86	Input FIFO 86 underflow LSR **
[20]	UF_85	Input FIFO 85 underflow LSR **

[19]	UF_84	Input FIFO 84 underflow LSR **
[18]	UF_83	Input FIFO 83 underflow LSR **
[17]	UF_82	Input FIFO 82 underflow LSR **
[16]	UF_81	Input FIFO 81 underflow LSR **
[15]	UF_80	Input FIFO 80 underflow LSR **
[14]	UF_79	Input FIFO 79 underflow LSR **
[13]	UF_78	Input FIFO 78 underflow LSR **
[12]	UF_77	Input FIFO 77 underflow LSR **
[11]	UF_76	Input FIFO 76 underflow LSR **
[10]	UF_75	Input FIFO 75 underflow LSR **
[9]	UF_74	Input FIFO 74 underflow LSR **
[8]	UF_73	Input FIFO 73 underflow LSR **
[7]	UF_72	Input FIFO 72 underflow LSR **
[6]	UF_71	Input FIFO 71 underflow LSR **
[5]	UF_70	Input FIFO 70 underflow LSR **
[4]	UF_69	Input FIFO 69 underflow LSR **
[3]	UF_68	Input FIFO 68 underflow LSR **
[2]	UF_67	Input FIFO 67 underflow LSR **
[1]	UF_66	Input FIFO 66 underflow LSR **
[0]	UF_65	Input FIFO 65 underflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

UFLOW_4

Address 0x0E2

Register Name UFLOW_4

Occurrences 1

Description Underflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	UF_128	Input FIFO 128 underflow LSR **
[30]	UF_127	Input FIFO 127 underflow LSR **
[29]	UF_126	Input FIFO 126 underflow LSR **
[28]	UF_125	Input FIFO 125 underflow LSR **
[27]	UF_124	Input FIFO 124 underflow LSR **
[26]	UF_123	Input FIFO 123 underflow LSR **
[25]	UF_122	Input FIFO 122 underflow LSR **
[24]	UF_121	Input FIFO 121 underflow LSR **
[23]	UF_120	Input FIFO 120 underflow LSR **
[22]	UF_119	Input FIFO 119 underflow LSR **

[21]	UF_118	Input FIFO 118 underflow LSR **
[20]	UF_117	Input FIFO 117 underflow LSR **
[19]	UF_116	Input FIFO 116 underflow LSR **
[18]	UF_115	Input FIFO 115 underflow LSR **
[17]	UF_114	Input FIFO 114 underflow LSR **
[16]	UF_113	Input FIFO 113 underflow LSR **
[15]	UF_112	Input FIFO 112 underflow LSR **
[14]	UF_111	Input FIFO 111 underflow LSR **
[13]	UF_110	Input FIFO 110 underflow LSR **
[12]	UF_109	Input FIFO 109 underflow LSR **
[11]	UF_108	Input FIFO 108 underflow LSR **
[10]	UF_107	Input FIFO 107 underflow LSR **
[9]	UF_106	Input FIFO 106 underflow LSR **
[8]	UF_105	Input FIFO 105 underflow LSR **
[7]	UF_104	Input FIFO 104 underflow LSR **
[6]	UF_103	Input FIFO 103 underflow LSR **
[5]	UF_102	Input FIFO 102 underflow LSR **
[4]	UF_101	Input FIFO 101 underflow LSR **
[3]	UF_100	Input FIFO 100 underflow LSR **
[2]	UF_99	Input FIFO 99 underflow LSR **
[1]	UF_98	Input FIFO 98 underflow LSR **
[0]	UF_97	Input FIFO 97 underflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

UFLOW_5

Address	0x0E3
Register Name	UFLOW_5
Occurrences	1
Description	Underflow LSR (Latched Status Register)

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	UF_160	Input FIFO 160 underflow LSR **
[30]	UF_159	Input FIFO 159 underflow LSR **
[29]	UF_158	Input FIFO 158 underflow LSR **
[28]	UF_157	Input FIFO 157 underflow LSR **
[27]	UF_156	Input FIFO 156 underflow LSR **
[26]	UF_155	Input FIFO 155 underflow LSR **

[25]	UF_154	Input FIFO 154 underflow LSR **
[24]	UF_153	Input FIFO 153 underflow LSR **
[23]	UF_152	Input FIFO 152 underflow LSR **
[22]	UF_151	Input FIFO 151 underflow LSR **
[21]	UF_150	Input FIFO 150 underflow LSR **
[20]	UF_149	Input FIFO 149 underflow LSR **
[19]	UF_148	Input FIFO 148 underflow LSR **
[18]	UF_147	Input FIFO 147 underflow LSR **
[17]	UF_146	Input FIFO 146 underflow LSR **
[16]	UF_145	Input FIFO 145 underflow LSR **
[15]	UF_144	Input FIFO 144 underflow LSR **
[14]	UF_143	Input FIFO 143 underflow LSR **
[13]	UF_142	Input FIFO 142 underflow LSR **
[12]	UF_141	Input FIFO 141 underflow LSR **
[11]	UF_140	Input FIFO 140 underflow LSR **
[10]	UF_139	Input FIFO 139 underflow LSR **
[9]	UF_138	Input FIFO 138 underflow LSR **
[8]	UF_137	Input FIFO 137 underflow LSR **
[7]	UF_136	Input FIFO 136 underflow LSR **
[6]	UF_135	Input FIFO 135 underflow LSR **
[5]	UF_134	Input FIFO 134 underflow LSR **
[4]	UF_133	Input FIFO 133 underflow LSR **
[3]	UF_132	Input FIFO 132 underflow LSR **
[2]	UF_131	Input FIFO 131 underflow LSR **
[1]	UF_130	Input FIFO 130 underflow LSR **
[0]	UF_129	Input FIFO 129 underflow LSR **

* * Denotes clear on write bit. A register write will clear the status.

UNLOCK_CH_1

Address 0x0E4

Register Name UNLOCK_CH_1

Occurrences 1

Description Unlock channel status, associated with the device capacity and channel mutes

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	ST_32	Channel 32 unlock status
[30]	ST_31	Channel 31 unlock status
[29]	ST_30	Channel 30 unlock status
[28]	ST_29	Channel 29 unlock status

[27]	ST_28	Channel 28 unlock status
[26]	ST_27	Channel 27 unlock status
[25]	ST_26	Channel 26 unlock status
[24]	ST_25	Channel 25 unlock status
[23]	ST_24	Channel 24 unlock status
[22]	ST_23	Channel 23 unlock status
[21]	ST_22	Channel 22 unlock status
[20]	ST_21	Channel 21 unlock status
[19]	ST_20	Channel 20 unlock status
[18]	ST_19	Channel 19 unlock status
[17]	ST_18	Channel 18 unlock status
[16]	ST_17	Channel 17 unlock status
[15]	ST_16	Channel 16 unlock status
[14]	ST_15	Channel 15 unlock status
[13]	ST_14	Channel 14 unlock status
[12]	ST_13	Channel 13 unlock status
[11]	ST_12	Channel 12 unlock status
[10]	ST_11	Channel 11 unlock status
[9]	ST_10	Channel 10 unlock status
[8]	ST_9	Channel 9 unlock status
[7]	ST_8	Channel 8 unlock status
[6]	ST_7	Channel 7 unlock status
[5]	ST_6	Channel 6 unlock status
[4]	ST_5	Channel 5 unlock status
[3]	ST_4	Channel 4 unlock status
[2]	ST_3	Channel 3 unlock status
[1]	ST_2	Channel 2 unlock status
[0]	ST_1	Channel 1 unlock status

UNLOCK_CH_2

Address	0x0E5
Register Name	UNLOCK_CH_2
Occurrences	1
Description	Unlock channel status, associated with the device capacity and channel mutes

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	ST_64	Channel 64 unlock status
[30]	ST_63	Channel 63 unlock status

[29]	ST_62	Channel 62 unlock status
[28]	ST_61	Channel 61 unlock status
[27]	ST_60	Channel 60 unlock status
[26]	ST_59	Channel 59 unlock status
[25]	ST_58	Channel 58 unlock status
[24]	ST_57	Channel 57 unlock status
[23]	ST_56	Channel 56 unlock status
[22]	ST_55	Channel 55 unlock status
[21]	ST_54	Channel 54 unlock status
[20]	ST_53	Channel 53 unlock status
[19]	ST_52	Channel 52 unlock status
[18]	ST_51	Channel 51 unlock status
[17]	ST_50	Channel 50 unlock status
[16]	ST_49	Channel 49 unlock status
[15]	ST_48	Channel 48 unlock status
[14]	ST_47	Channel 47 unlock status
[13]	ST_46	Channel 46 unlock status
[12]	ST_45	Channel 45 unlock status
[11]	ST_44	Channel 44 unlock status
[10]	ST_43	Channel 43 unlock status
[9]	ST_42	Channel 42 unlock status
[8]	ST_41	Channel 41 unlock status
[7]	ST_40	Channel 40 unlock status
[6]	ST_39	Channel 39 unlock status
[5]	ST_38	Channel 38 unlock status
[4]	ST_37	Channel 37 unlock status
[3]	ST_36	Channel 36 unlock status
[2]	ST_35	Channel 35 unlock status
[1]	ST_34	Channel 34 unlock status
[0]	ST_33	Channel 33 unlock status

UNLOCK_CH_3

Address	0x0E6
Register Name	UNLOCK_CH_3
Occurrences	1
Description	Unlock channel status, associated with the device capacity and channel mutes

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	ST_96	Channel 96 unlock status
[30]	ST_95	Channel 95 unlock status

[29]	ST_94	Channel 94 unlock status
[28]	ST_93	Channel 93 unlock status
[27]	ST_92	Channel 92 unlock status
[26]	ST_91	Channel 91 unlock status
[25]	ST_90	Channel 90 unlock status
[24]	ST_89	Channel 89 unlock status
[23]	ST_88	Channel 88 unlock status
[22]	ST_87	Channel 87 unlock status
[21]	ST_86	Channel 86 unlock status
[20]	ST_85	Channel 85 unlock status
[19]	ST_84	Channel 84 unlock status
[18]	ST_83	Channel 83 unlock status
[17]	ST_82	Channel 82 unlock status
[16]	ST_81	Channel 81 unlock status
[15]	ST_80	Channel 80 unlock status
[14]	ST_79	Channel 79 unlock status
[13]	ST_78	Channel 78 unlock status
[12]	ST_77	Channel 77 unlock status
[11]	ST_76	Channel 76 unlock status
[10]	ST_75	Channel 75 unlock status
[9]	ST_74	Channel 74 unlock status
[8]	ST_73	Channel 73 unlock status
[7]	ST_72	Channel 72 unlock status
[6]	ST_71	Channel 71 unlock status
[5]	ST_70	Channel 70 unlock status
[4]	ST_69	Channel 69 unlock status
[3]	ST_68	Channel 68 unlock status
[2]	ST_67	Channel 67 unlock status
[1]	ST_66	Channel 66 unlock status
[0]	ST_65	Channel 65 unlock status

UNLOCK_CH_4

Address	0x0E7
Register Name	UNLOCK_CH_4
Occurrences	1
Description	Unlock channel status, associated with the device capacity and channel mutes

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	ST_128	Channel 128 unlock status
[30]	ST_127	Channel 127 unlock status

[29]	ST_126	Channel 126 unlock status
[28]	ST_125	Channel 125 unlock status
[27]	ST_124	Channel 124 unlock status
[26]	ST_123	Channel 123 unlock status
[25]	ST_122	Channel 122 unlock status
[24]	ST_121	Channel 121 unlock status
[23]	ST_120	Channel 120 unlock status
[22]	ST_119	Channel 119 unlock status
[21]	ST_118	Channel 118 unlock status
[20]	ST_117	Channel 117 unlock status
[19]	ST_116	Channel 116 unlock status
[18]	ST_115	Channel 115 unlock status
[17]	ST_114	Channel 114 unlock status
[16]	ST_113	Channel 113 unlock status
[15]	ST_112	Channel 112 unlock status
[14]	ST_111	Channel 111 unlock status
[13]	ST_110	Channel 110 unlock status
[12]	ST_109	Channel 109 unlock status
[11]	ST_108	Channel 108 unlock status
[10]	ST_107	Channel 107 unlock status
[9]	ST_106	Channel 106 unlock status
[8]	ST_105	Channel 105 unlock status
[7]	ST_104	Channel 104 unlock status
[6]	ST_103	Channel 103 unlock status
[5]	ST_102	Channel 102 unlock status
[4]	ST_101	Channel 101 unlock status
[3]	ST_100	Channel 100 unlock status
[2]	ST_99	Channel 99 unlock status
[1]	ST_98	Channel 98 unlock status
[0]	ST_97	Channel 97 unlock status

UNLOCK_CH_5

Address	0x0E8
Register Name	UNLOCK_CH_5
Occurrences	1
Description	Unlock channel status, associated with the device capacity and channel mutes

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	ST_160	Channel 160 unlock status
[30]	ST_159	Channel 159 unlock status
[29]	ST_158	Channel 158 unlock status
[28]	ST_157	Channel 157 unlock status
[27]	ST_156	Channel 156 unlock status
[26]	ST_155	Channel 155 unlock status
[25]	ST_154	Channel 154 unlock status
[24]	ST_153	Channel 153 unlock status
[23]	ST_152	Channel 152 unlock status
[22]	ST_151	Channel 151 unlock status
[21]	ST_150	Channel 150 unlock status
[20]	ST_149	Channel 149 unlock status
[19]	ST_148	Channel 148 unlock status
[18]	ST_147	Channel 147 unlock status
[17]	ST_146	Channel 146 unlock status
[16]	ST_145	Channel 145 unlock status
[15]	ST_144	Channel 144 unlock status
[14]	ST_143	Channel 143 unlock status
[13]	ST_142	Channel 142 unlock status
[12]	ST_141	Channel 141 unlock status
[11]	ST_140	Channel 140 unlock status
[10]	ST_139	Channel 139 unlock status
[9]	ST_138	Channel 138 unlock status
[8]	ST_137	Channel 137 unlock status
[7]	ST_136	Channel 136 unlock status
[6]	ST_135	Channel 135 unlock status
[5]	ST_134	Channel 134 unlock status
[4]	ST_133	Channel 133 unlock status
[3]	ST_132	Channel 132 unlock status
[2]	ST_131	Channel 131 unlock status
[1]	ST_130	Channel 130 unlock status
[0]	ST_129	Channel 129 unlock status

COMB8

Address 0x0B0 + (CC8# * 0x050), CC8# = 1 to 20

Register Name COMB8

Occurrences 20

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:10]	RSVD	Reserved bits [21:0]
[9:8]	SPARE	Spare bit [1:0]
[7:1]	RSVD	Reserved bits [6:0]
[0]	CW_LD	Frequency control word 2 load pulse (self-clearing), resets NCO2 *

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

NCO2

Address 0x0B1 + (CC8# * 0x050), CC8# = 1 to 20

Register Name NCO2

Occurrences 20

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:21]	RSVD	Reserved bits [10:0]
[20:0]	FCW2	Modulator 2 frequency control word [20:0]

CC8_SAT

Address 0x0B2 + (CC8# * 0x050), CC8# = 1 to 20

Register Name CC8_SAT

Occurrences 20

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:7]	RSVD	Reserved bits [24:0]
[6]	MOD2_SAT	MOD2 saturate **
[5]	ADDQ_SAT	8 Channel Adder saturate **
[4]	F4Q_SAT	F4 filter saturate **
[3]	F3Q_SAT	F3 filter saturate **

[2]	ADDI_SAT	8 Channel Adder saturate **
[1]	F4I_SAT	F4 filter saturate **
[0]	F3I_SAT	F3 filter saturate **

** Denotes clear on write bit. A register write will clear the status.

There is one set of seven registers for each channel (each of these registers occurs 160 times in the register map).

"(CH# - 1)/8" requires integer division to yield the proper value

(i.e. integer division yields 3 if CH# is 0x20 and 0 if CH# is 0x05).

SYMIF

Address 0x100 + (CH# * 8) + ((CH# - 1) / 8)* 0x10, CH# = 1 to 0xA0 (160)

Register Name SYMIF

Occurrences 160

Description Symbol Interface Configuration

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	PRBS_TYPE	PRBS type select, 0-PRBS23, 1-MAX5880 style PRBS
[30:28]	PRBS_SHFT	10/20 PRBS shift [2:0]
[27]	RSVD	Reserved bit
[26]	SWAP_IQ	Swap the i/q output of qam mapper
[25]	I_INV	Negate the value of I output
[24]	Q_INV	1:Enable Spectrum inversion for this channel
[23]	CW_LD	Channel_1 frequency control word load pulse local *
[22]	LD_KFLF	Lf/kf control word load pulse generated *
[21]	GLB_KFLF	Enable global lf/kf load
[20]	PRBS	Enable PRBS for this channel
[19:18]	ALPHA	RRC alpha select [1:0]
[17]	QOFF	Enable QAM qoff bit
[16:14]	QAM	QAM map select (default is bypass) [2:0]
[13]	BYPASS_CH	RRC-Bypass channel (only valid for channels 1, 2, 3, and 4)
[12]	D2	Enable half symbol delay, D2 delay
[11:8]	D1	Enable full symbol period delay [3:0]
[7:0]	PRBS_SEED	8 LSBs of the 12 bits PRBS seed for this channel [7:0]

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

KFA

Address 0x101 + (CH# * 8) + ((CH# - 1) / 8) * 0x10, CH# = 1 to 0xA0 (160)

Register Name KFA

Occurrences 160

Description KF Value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:27]	RSVD	Reserved bits [4:0]
[26:0]	KF	KF value for ARR [26:0]

LFA

Address 0x102 + (CH# * 8) + ((CH# - 1) / 8) * 0x10, CH# = 1 to 0xA0 (160)

Register Name LFA

Occurrences 160

Description LF Value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:27]	RSVD	Reserved bits [4:0]
[26:0]	LF	LF value for ARR, user need to Always use ld_kflf when LF gets updated. [26:0]

NCO1

Address 0x103 + (CH# * 8) + ((CH# - 1) / 8) * 0x10, CH# = 1 to 0xA0 (160)

Register Name NCO1

Occurrences 160

Description NCO1 Frequency Control Word

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:19]	RSVD	Reserved bits [12:0]
[18:0]	FCW1	Modulator 1 frequency control word [18:0]

G1G2

Address 0x104 + (CH# * 8) + ((CH# - 1) / 8) * 0x10, CH# = 1 to 0xA0 (160)

Register Name G1G2

Occurrences 160

Description G1 and G2 Gain

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:24]	RSVD	Reserved bits [7:0]
[23:16]	G2	G2 gain value [7:0]
[15:11]	RSVD	Reserved bits [4:0]
[10:0]	G1	G1 gain value [10:0]

G1_PWR-MON

Address 0x105 + (CH# * 8) + ((CH# - 1) / 8) * 0x10, CH# = 1 to 0xA0 (160)

Register Name G1_PWRMON

Occurrences 160

Description G1 Power Monitor

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	ARRQ_SAT	ARR filter saturate **
[30]	F2Q_SAT	F2 filter saturate **
[29]	F1Q_SAT	F1 filter saturate **
[28]	PCQ_SAT	PC filter saturate **
[27:16]	IPWR	P1 Power monitor threshold count, I path [11:0]
[15]	ARRI_SAT	ARR filter saturate **
[14]	F2I_SAT	F2 filter saturate **
[13]	F1I_SAT	F1 filter saturate **
[12]	PCI_SAT	PC filter saturate **
[11:0]	QPWR	P1 Power monitor threshold count, Q path [11:0]

* * Denotes clear on write bit. A register write will clear the status.

G2_PWR-MON

Address 0x106 + (CH# * 8) + ((CH# - 1) / 8) * 0x10, CH# = 1 to 0xA0 (160)

Register Name G2_PWRMON

Occurrences 160

Description G2 Power Monitor

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31]	MOD1_SAT	MOD1 saturate **
[30:28]	RSVD	Reserved bits [2:0]
[27:16]	IPWR	P2 Power monitor threshold count, I path [11:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	QPWR	P2 Power monitor threshold count, Q path [11:0]

* * Denotes clear on write bit. A register write will clear the status.

The first channel of each 8 channel combiner may be configured to have the PRBS generator repeat at a configurable length.

PRBS-23 always restarts its sequence with a zero data word output.

There are 20 instances of this register corresponding to channels 1, 9, 17, … , 153

PRBS_REPEAT

Address 0x0BF + (CC8# * 0x50), CC8# = 0x01 to 0x14 (20)

Register Name PRBS_REPEAT

Occurrences 20

Description PRBS short-cycle : first channel PRBS of each 8 channel group

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:17]	RSVD	Reserved bits [14:0]
[16:0]	REP_CTL	PRBS23 repeat count control, MSB as enable [16:0]

PAR_CFG_PORTB

Address 0x740

Register Name PAR_CFG_PORTB

Occurrences 1

Description OFDM Port B Configuration

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0

[31:18]	RSVD	Reserved bits [13:0]
[17]	DIS_TLFSR	Disables the Time Domain LFSR for pilots
[16]	DELAY	Define the delay of parity with respect to data.
[15:14]	BPSK_LVL_SL	Default value is 2 [1:0]

LSFR Output	BPSK_LVL_ SL=0	BPSK_LVL_ SL=1	BPSK_LVL_ SL=2	BPSK_LVL_ SL=3
0	I=-1, Q=-1	I=+1, Q=+1	I=+1, Q=0	I=-1, Q=0
1	I=+1, Q=+1	I=-1, Q=-1	I=-1, Q=0	I=+1, Q=0

[13]	RSVD	Reserved bit
[12:10]	FSYNC_MASK	FSYNC Parity Calculation Pin Masking Bits [2:0] Bit [2] is FSYNC3, bit [1] is FSYNC2, bit [0] is FSYNC1
[9:1]	DAT_MSK	Port B Parity Calculation Data Pin Masking Bits [8:0]
[0]	BYP	1: Bypass the OFDM path(IFFT and windowing)

PAR_CFG_PORTC

Address 0x76B

Register Name PAR_CFG_PORTC

Occurrences 1

Description OFDM Port C Configuration

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0

[31:13]	RSVD	Reserved bits [18:0]
[12:10]	FSYNC_MASK	FSYNC Parity Calculation Pin Masking Bits [2:0] Bit [2] is FSYNC6, bit [1] is FSYNC5, bit [0] is FSYNC4
[9:1]	DAT_MSK	Port C Parity Calculation Data Pin Masking Bits [8:0]
[0]	BYP	Bypass the OFDM path(IFFT and windowing)

The nomenclature “+ (OFDM_CH# > 3)?1:0” is defined as: if OFDM_CH# is greater than 3, then add 1. Otherwise add 0. OFDM_CH# range is from 1 to 6. The bypass channel for port B is OFDM channel 1. The bypass channel for port C is OFDM channel 4.

OFDM_CFG

Address 0x741 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name OFDM_CFG

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	1

[31:19]	RSVD	Reserved bits [12:0]
[18]	OF_ST	Overflow status
[17]	UF_ST	Underflow status
[16]	SAT_OCH	Gain Saturation bit of OFDM channel **
[15]	SYNC_DET	New Sync detected at new position SRL **
[14]	SYNC_MIS	Missed the Sync at the expected position SRL **
[13]	OF	Input FIFO overflow LSR **
[12]	UF	Input FIFO underflow LSR **
[11]	SYNC_DET_IE	Enable new sync detect interrupt
[10]	SYNC_MIS_IE	Enable missing sync interrupt
[9]	OF_IE	Enable input FIFO overflow interrupt
[8]	UF_IE	Enable input FIFO underflow interrupt
[7:6]	RSVD	Reserved bits [1:0]
[5]	SWAP_IQ	Swap the i/q output
[4]	Q_INV	Negate the value of q output
[3]	I_INV	Negate the value of i output
[2]	GBL_RST	Global FIFO reset enable
[1]	LCL_RST	Local FIFO reset pulse *
[0]	MUTE	Mute the channel

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

* * Denotes clear on write bit. A register write will clear the status.

GAINEQ_ADD

Address 0x742 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAINEQ_ADD

Occurrences 6

Description Gain Equalization

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

[24:12]	gese	Gain equalization Band Start Edge frequency Index
[11:4]	sgs	SGS subcarrier group for gain quantization. This value becomes 2x when 8K DFT is selected
[2:0]	a	Base address (range of 0 to 7) for gaineq_dat register- writing to the gaineq_dat register auto-increments this address. It is suggested that this register be written for each table load.[2:0]

GAINEQ_DAT

Address 0x743 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAINEQ_DAT

Occurrences 6

Description Subcarrier Gain Equalization Value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

[31:24]	ge3	G3/G7/G11/G15/G19/G23/G27/G31 gain equalization value [7:0]
[23:16]	ge2	G2/G6/G10/G14/G18/G22/G26/G30 gain equalization value [7:0]
[15:8]	ge1	G1/G5/G9/G13/G17/G21/G25/G29 gain equalization value [7:0]
[7:0]	ge0	G0/G4/G8/G12/G16/G20/G24/G28 gain equalization value [7:0]

GAIN_BAL_1

Address 0x744 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAIN_BAL_1

Occurrences 6

Description OFDM data path gain balancing value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[27:24]	n2	4 bit 'n' constellation offset table value, index 0x2 [3:0]
[23:16]	d2	8 bit gain table value, index 0x2 [7:0]
[11:8]	n1	4 bit 'n' constellation offset table value, index 0x1 [3:0]
[7:0]	d1	8 bit gain table value, index 0x1 [7:0]

14x8 Table (gain and offset), one for each OFDM channel.

Seven gain_bal registers are used to store fourteen 12 bit words.

The unsigned 12 bit value has a range of 0 to 1.99999 with two 12 bit gain values are stored in each register.

GAIN_BAL_2

Address 0x745 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAIN_BAL_2

Occurrences 6

Description OFDM data path gain balancing value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[27:24]	n4	4 bit 'n' constellation offset table value, index 0x4 [3:0]
[23:16]	d4	8 bit gain table value, index 0x4 [7:0]
[11:8]	n3	4 bit 'n' constellation offset table value, index 0x3 [3:0]
[7:0]	d3	8 bit gain table value, index 0x3 [7:0]

14x8 Table (gain and offset), one for each OFDM channel.

Seven gain_bal registers are used to store fourteen 12 bit words.

The unsigned 12 bit value has a range of 0 to 1.99999 with two 12 bit gain values are stored in each register.

GAIN_BAL_3

Address 0x746 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAIN_BAL_3

Occurrences 6

Description OFDM data path gain balancing value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[27:24]	n6	4 bit 'n' constellation offset table value, index 0x6 [3:0]
[23:16]	d6	8 bit gain table value, index 0x6 [7:0]
[11:8]	n5	4 bit 'n' constellation offset table value, index 0x5 [3:0]
[7:0]	d5	8 bit gain table value, index 0x5 [7:0]

14x8 Table (gain and offset), one for each OFDM channel.

Seven gain_bal registers are used to store fourteen 12 bit words.

The unsigned 12 bit value has a range of 0 to 1.99999 with two 12 bit gain values are stored in each register.

GAIN_BAL_4

Address 0x747 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAIN_BAL_4

Occurrences 6

Description OFDM data path gain balancing value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[27:24]	n8	4 bit 'n' constellation offset table value, index 0x8 [3:0]
[23:16]	d8	8 bit gain table value, index 0x8 [7:0]
[11:8]	n7	4 bit 'n' constellation offset table value, index 0x7 [3:0]
[7:0]	d7	8 bit gain table value, index 0x7 [7:0]

14x8 Table (gain and offset), one for each OFDM channel.

Seven gain_bal registers are used to store fourteen 12 bit words.

The unsigned 12 bit value has a range of 0 to 1.99999 with two 12 bit gain values are stored in each register.

GAIN_BAL_5

Address 0x748 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAIN_BAL_5

Occurrences 6

Description OFDM data path gain balancing value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[27:24]	nA	4 bit 'n' constellation offset table value, index 0xA [3:0]
[23:16]	dA	8 bit gain table value, index 0xA [7:0]
[11:8]	n9	4 bit 'n' constellation offset table value, index 0x9 [3:0]
[7:0]	d9	8 bit gain table value, index 0x9 [7:0]

14x8 Table (gain and offset), one for each OFDM channel.

Seven gain_bal registers are used to store fourteen 12 bit words.

The unsigned 12 bit value has a range of 0 to 1.99999 with two 12 bit gain values are stored in each register.

GAIN_BAL_6

Address 0x749 + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAIN_BAL_6

Occurrences 6

Description OFDM data path gain balancing value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[27:24]	nC	4 bit 'n' constellation offset table value, index 0xC [3:0]
[23:16]	dC	8 bit gain table value, index 0xC [7:0]
[11:8]	nB	4 bit 'n' constellation offset table value, index 0xB [3:0]
[7:0]	dB	8 bit gain table value, index 0xB [7:0]

14x8 Table (gain and offset), one for each OFDM channel.

Seven gain_bal registers are used to store fourteen 12 bit words.

The unsigned 12 bit value has a range of 0 to 1.99999 with two 12 bit gain values are stored in each register.

GAIN_BAL_7

Address 0x74A + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name GAIN_BAL_7

Occurrences 6

Description OFDM data path gain balancing value

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[27:24]	nE	4 bit 'n' constellation offset table value, index 0xE [3:0]
[23:16]	dE	8 bit gain table value, index 0xE [7:0]
[11:8]	nD	4 bit 'n' constellation offset table value, index 0xD [3:0]
[7:0]	dD	8 bit gain table value, index 0xD [7:0]

14x8 Table (gain and offset), one for each OFDM channel.

Seven gain_bal registers are used to store fourteen 12 bit words.

The unsigned 12 bit value has a range of 0 to 1.99999 with two 12 bit gain values are stored in each register.

PRBSMD

Address 0x74B + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name PRBSMD

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

[31]	RSVD	Reserved bit
[30:24]	INITLOC	Pilot's Initial Location [6:0]
[23:20]	RSVD	Reserved bits [3:0]
[19:16]	QAM	Selects the QAM type for OFDM QAM mapper [3:0] 0000:4k, 0001:2k, 0010:1k, 0011:512, 0100:256, 0101:128, 0110:64, 0111:32, 1000:16, 1001:bypass
[15]	RSVD	Reserved bit
[14:4]	SEED	11bits prbs seed value [10:0]
[3]	RSVD	Reserved bit
[2]	DIS_SCTPIL	Disables calculation of scattered pilot location in PRBS mode
[1]	DIS_PILINS	Disables Pilot insertions
[0]	EN	PRBS enable for this channel

PRBS_FRQBND

Address 0x74C + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name PRBS_FRQBND

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	1
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0

[31:26]	RSVD	Reserved bits [5:0]
[25:13]	UP	Upper edge Frequency index for PRBS mode [12:0]
[12:0]	LOW	Lower edge Frequency index for PRBS mode [12:0]

PRBS_LOOP

Address 0x74D + ((OFDM_CH#-1)*0xE) + (OFDM_CH#>3)?1:0, OFDM_CH# = 1 to 6

Register Name PRBS_LOOP

Occurrences 1

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:17]	RSVD	Reserved bits [14:0]
[16:0]	CNT	PRBS loop val count. This should be programmed for NIFFT+CP-1; bit [16] enables the counter [16:0]

IFFT_CFG

Address 0x7B0 + ((OFDM_CH#-1)*0xC), OFDM_CH# = 1 to 6

Register Name IFFT_CFG

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27]	TONE_GEN	Pass the NCO3 output as tone output, NCO4 should be zero
[26]	NRP_PRG_EN	Enable NRP and NCP prog enable for numerical settings instead of enumerated settings

[25]	FLP_RLOF	Flip rolloff curve. When set to 1, the rolloff coefficients are read in reverse order
[24:16]	NRP	9bits rolloff period interval max value - 256 [8:0] If NRP_PROG_EN is 0, only 3 LSB bits select 5 different options where 0=0, 1=64, 2=128, 3=192 and 4=256
[15:12]	RSVD	Reserved bits [3:0]
[11:1]	NCP	11 bits Cyclic prefix time interval max val - 1024[10:0] If NRP_PROG_EN=0, only 3 LSB bits select 5 different options where 0=192, 1=256, 2=512, 3=768 and 4=1024
[0]	SUBCR_MD	0:4096 with 50kHz spacing, 1:8192 with 25kHz spacing

NCO3_OFDM

Address 0x7B1 + ((OFDM_CH#-1)*0xC, OFDM_CH# = 1 to 6

Register Name NCO3_OFDM

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:21]	RSVD	Reserved bits [10:0]
[29:0]	FCW31	Modulator 3 frequency control word [29:0]

GAIN

Address 0x7B2 + ((OFDM_CH#-1)*0xC, OFDM_CH# = 1 to 6

Register Name GAIN

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

[31:17]	RSVD	Reserved bits [14:0]
[16]	CW_LD	Load Modulator 3 frequency control word *
[15:8]	G8	G8 gain value [7:0] Unsigned 8 bit value, range of 0 to 1.99999
[7:0]	G7	G7 gain value [7:0] Unsigned 8 bit value, range of 0 to 1.99999

* Denotes self-clearing bit. A pulse is generated when asserted logic 1.

RLOF_ADD

Address 0x7B3 + ((OFDM_CH#-1)*0xC), OFDM_CH# = 1 to 6

Register Name RLOF_ADD

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:7]	RSVD	Reserved bits [24:0]
[6:0]	A	128x30 internal array to store the rolloff coefficients.[6:0]

Sets the address the first rolloff coefficient.

RLOF_DAT

Address 0x7B4 + ((OFDM_CH#-1)*0xC), OFDM_CH# = 1 to 6

Register Name RLOF_DAT

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:30]	RSVD	Reserved bits [1:0]
[29:0]	D	30 bit data to store the rolloff coefficients [29:0]

IFFT_FIFO

Address 0x7B5 + ((OFDM_CH#-1)*0xC), OFDM_CH# = 1 to 6

Register Name IFFT_FIFO

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

[31:28]	RB1_WOFF	RBF1 read/write pointer offset adjustment [3:0]
[27:24]	RB2_WOFF	RBF2 read/write pointer offset adjustment [3:0]
[23:7]	RSVD	Reserved bits [16:0]
[6]	OP_VAL	1: IFFT o/p is valid, 0: invalid
[5]	PROC_STP	1: stops proc o/p is not valid **
[4]	IN_OF	Input FIFO overflow bit **

[3]	IN_UF	Input FIFO underflow bit **
[2]	STP_IE	Enable IFFT proc stop intr enable
[1]	OF_IE	Enable FIFO overflow interrupt
[0]	UF_IE	Enable FIFO underflow interrupt

* * Denotes clear on write bit. A register write will clear the status.

SAT

Address 0x7B6 + ((OFDM_CH#-1)*0xC), OFDM_CH# = 1 to 6

Register Name SAT

Occurrences 6

Description

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:14]	RSVD	Reserved bits [17:0]
[13]	G8_OF	G8 Overflow status **
[12]	G7_OF	G7 Overflow status **
[11]	MOD	Status M3 saturate **
[10]	F1P5Q	Status F1.5 filter saturate **
[9]	RSVD	Reserved bit
[8]	F7Q	Status F7 filter saturate **
[7]	F6Q	Status F6 filter saturate **
[6]	F5Q	Status F5 filter saturate **
[5]	F1P5I	Status F1.5 filter saturate **
[4]	RSVD	Reserved bit
[3]	F7I	Status F7 filter saturate **
[2]	F6I	Status F6 filter saturate **
[1]	F5I	Status F5 filter saturate **
[0]	IFFT	Status IFFT saturate **

* * Denotes clear on write bit. A register write will clear the status.

G7_PWR

Address 0x7B7 + ((OFDM_CH#-1)*0xC), OFDM_CH# = 1 to 6

Register Name G7_PWR

Occurrences 6

Description G7 Power monitor threshold count

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27:16]	IPWR	Power monitor threshold count, I path [11:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	QPWR	Power monitor threshold count, q path [11:0]

G8_PWR

Address 0x7B8 + ((OFDM_CH#-1)*0xC), OFDM_CH# = 1 to 6

Register Name G8_PWR

Occurrences 6

Description G8 Power monitor threshold count

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[31:28]	RSVD	Reserved bits [3:0]
[27:16]	IPWR	Power monitor threshold count, I path [11:0]
[15:12]	RSVD	Reserved bits [3:0]
[11:0]	QPWR	Power monitor threshold count, q path [11:0]

TST_REG

Register Name: TST_REG

Address: 0x0E9

Description: Test register for demux and symbol detect

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default Value	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0

[31:21]	RSVD	Reserved bits [10:0]
[20]	CMP_IE	Interrupt enable for the compare result
[19]	CMP_OP	Raw output of comparison
[18]	CMP_RES	Status of compare result, SRL <<clear--on--write>>
[17:10]	FADD	FIFO add with which these bytes should be compared [7:0]
[9:0]	SYM	Expected symbol value for trigger [9:0]

Ordering Information

PART NUMBER	FUNCTION CAPABILITY		TEMPERATURE RANGE	PIN-PACKAGE
	OFDM	SCQAM		
MAX5861TEXA+	6 x 192MHz OFDM	160 Channels	T_A = -40°C (Min) T_J = +110°C (Max)	308 LFBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—
1	9/15	Fixed errors in data sheet and added Thermal Characteristics section	8, 14, 15, 23, 26, 27, 33, 36, 38, 39, 43, 51, 53, 55, 57, 62, 69, 72, 74-76, 78, 92, 93, 95-100, 103, 108-110, 160, 172-176, 179, 185, 191, 194, 196, 197
2	8/18	Updated *Electrical Characteristics, Detailed Desciption, Applications Information*	9, 10, 15, 35, 50, 55, 56, 72, 76, 108