EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ
User Guide
UG-1284

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Evaluating the ADGS1408/ADGS1409 SPI Interface, 4 Ω R_{ON}, ±15 V/+12 V/±5 V, 1.8 V Logic Control, 8:1/Dual 4:1 Muxes

FEATURES

- SPI interface with error detection
- Includes CRC error detection, invalid read/write address detection, and SCLK count error detection
- Analog supply voltages
  - Dual supply: ±15 V
  - Single supply: 12 V
- PC control in conjunction with evaluation software

EVALUATION KIT CONTENTS

EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ

EQUIPMENT NEEDED

- SDP-B controller board (EVAL-SDP-CB1Z)
- ACE software with EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ plug-in
- DC voltage source
  - ±15 V for dual supply
  - 12 V for single supply
- Optional digital logic supply: 3.3 V
- Analog signal source
- Digital multimeter

DOCUMENTS NEEDED

ADGS1408/ADGS1409 data sheet

GENERAL DESCRIPTION

The EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ are the evaluation boards for the ADGS1408/ADGS1409. The ADGS1408/ADGS1409 are low R_{ON}, 8:1/dual 4:1 multiplexers controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read/write address detection, and serial clock (SCLK) count error detection. It is possible to daisy-chain multiple ADGS1408/ADGS1409 devices together to enable the configuration of multiple devices with a minimal amount of digital lines. The ADGS1408/ADGS1409 also support burst mode, which decreases the time between SPI commands.

Figure 1 and Figure 2 shows the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ board photographs. The EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ are controlled by the EVAL-SDP-CB1Z system demonstration platform (SDP), which connects to a PC via a USB port. The ADGS1408/ADGS1409 is on the center of the evaluation board, and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device and, if required, a fourth terminal provides users with a defined digital logic supply voltage. Alternatively, the digital logic supply voltage can be supplied from the SDP-B board.

Consult the ADGS1408/ADGS1409 data sheet (available from Analog Devices, Inc.) in conjunction with this user guide when working with the evaluation board.

The evaluation board interfaces to the USB port of a PC via the SDP-B board. The SDP-B controller board (EVAL-SDP-CB1Z) is available for order at www.analog.com/SDP-B.

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REVISION HISTORY

6/2018—Revision 0: Initial Version

EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ PHOTOGRAPHS

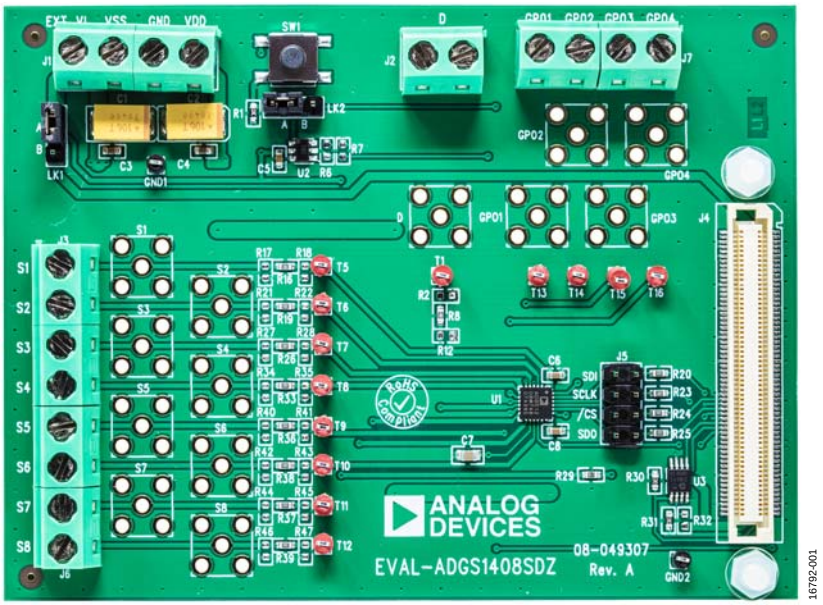

Figure 1. EVAL-ADGS1408SDZ Photograph

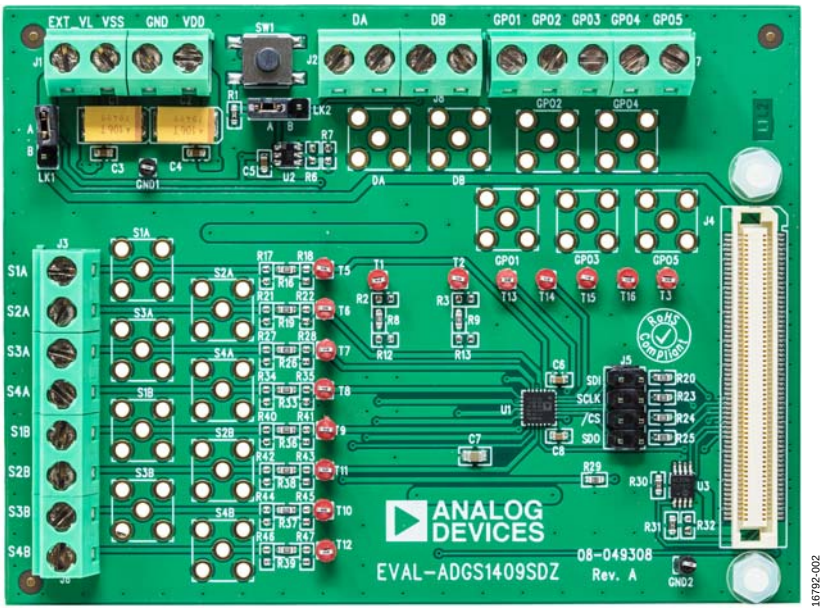

Figure 2. EVAL-ADGS1409SDZ Photograph

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Connector J1 provides access to the supply pins of the ADGS1408/ADGS1409. VDD, GND, and VSS on the J1 terminal block link to the appropriate pins on the ADGS1408/ADGS1409. For dual-supply voltages, the evaluation board can be powered from ±15 V. For single-supply voltages, the GND and VSS terminals must connect together and power the evaluation board from 12 V. Additionally, the SDP supplies 3.3 V to the $\overline{\text{RESET}}/V_L$ pin of the ADGS1408/ADGS1409 when Link LK1 is in Position B. When using a method other than the SDP to control the ADGS1408/ADGS1409, supply between 2.7 V and 5.5 V to the $\overline{\text{RESET}}/V_L$ pin of the ADGS1408/ADGS1409 via the EXT_VL screw terminal input on J1. LK1 must be in Position A.

INPUT SIGNALS

Screw connectors (J2, J3, and J6) are provided to connect to both the source and drain pins of the ADGS1408/ADGS1409. Additional Subminiature Version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain pins includes two sets of 0603 pads, which place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor, combined with the 0603 pads, creates a simple resistor-capacitor filter.

DIGITAL OUTPUTS

The GPOx digital output are accessible from the J7 screw connector, and there are additional SMB connector footprints available if extra connections are required.

LINK OPTIONS

The EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ evaluation boards provide several link options that must be set at the required operating conditions before use.

Table 1 shows the positioning of the links necessary for controlling the evaluation board via the SDP-B board using a PC and external power supplies. Table 2 shows the functions of these link options.

LK1 must be in Position B to avoid damaging the SDP-B when using it in conjunction with the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ.

Table 1. Link Options for SDP Control (Default)

Link Number	Option
LK1	B
LK2	B

Table 2. Link Functions

Link Number	Function
LK1	This link selects the source of the V_L voltage supplied to the ADGS1408/ADGS1409. Position A selects EXT_VL from J1. Position B selects the 3.3 V from the SDP-B.
LK2	This link selects how a hardware reset is performed. Position A indicates the SW1 push-button can perform a hardware reset. Position B indicates the SDP-B can perform a hardware reset.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE SOFTWARE

The EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ evaluation boards use the Analog Devices Analysis, Control, Evaluation (ACE) software. ACE is a desktop software application that facilitates the control and evaluation of multiple evaluation systems.

ACE installs the required SDP drivers and .NET Framework 4 by default. Install ACE before connecting the SDP-B board to the PC. The ACE software and comprehensive instructions on its installation and use are available at www.analog.com/ACE.

After the installation is finished, the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ evaluation board plug-ins appear when ACE is opened.

INITIAL SETUP

To set up the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ evaluation boards, complete the following steps:

1. Connect the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ evaluation boards to the SDP-B board, and connect the SDP-B board to the PC via a USB cable.
2. Turn on the evaluation board as described in the Power Supplies section.
3. Run the **ACE** application. The EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ boards plug-ins appear in the attached hardware section of the **Start** tab.
4. Double-click the **ADGS1408/ADGS1409SDZ Board** plug-in to open the evaluation board view shown in Figure 3. This figure shows the basic functionality and main functions of the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ evaluation boards.

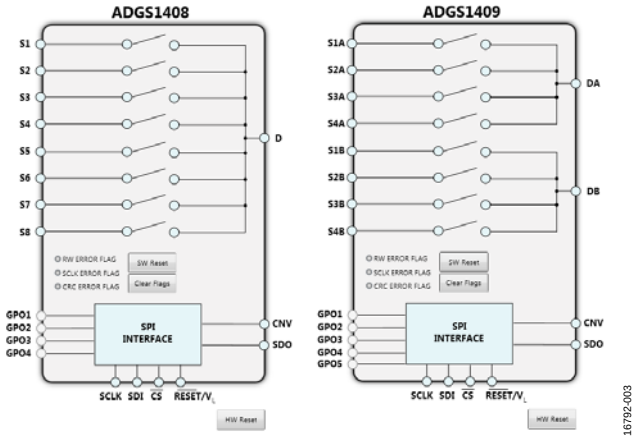

Figure 3. Evaluation Board View of the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ

BLOCK DIAGRAM AND DESCRIPTION

The similar appearance of the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ software to the functional block diagram of the ADGS1408/ADGS1409 data sheet renders it easy to correlate the board functions of the EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ with the description of the functional block diagram in the data sheet. The ADGS1408/ADGS1409 data sheet provides comprehensive descriptions for each function, block, register, and setting.

Table 3 describes the blocks and their functions pertaining to the evaluation board. The full screen block diagram shown in Figure 4 shows the functionality of each block.

MEMORY MAP

Click **Memory Map** to access all the registers, which can be edited at the bit level (see Figure 5 and Figure 6). Bits shaded in dark gray are read only bits and inaccessible from ACE. All other bits are toggled. Click **Apply Changes** to transfer data modifications to the device.

All changes to the memory map correspond to the block diagram. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. Bolded bits or registers represent modified values that have not been transferred to the evaluation board. After clicking **Apply Changes**, the data is transferred to the evaluation board and no longer appears as bolded.

Table 3. Block Diagram Functions (see Figure 4)

Label	Function
A	The switch icons configure which channel is selected.
B	The **Detect Invalid Read/Write**, **Detect Invalid SCLK Count**, and **Detect Invalid CRC** check boxes enable or disable the error detection features on the SPI interface.
C	The **Enable Burst Mode** check box enables or disables burst mode.
D	The **RW ERROR FLAG**, **SCLK ERROR FLAG**, and **CRC ERROR FLAG** indicators illuminate red when the relevant error flags are asserted in the error flags register.
E	The **Clear Flags** button clears the error flags register.
F	The **Apply Changes** button applies all modified values to the devices.
G	The **SW Reset** button causes the device to perform a software reset.
H	The **GPO1**, **GPO2**, **GPO3**, and **GPO4** buttons select whether the corresponding GPO is on or off.

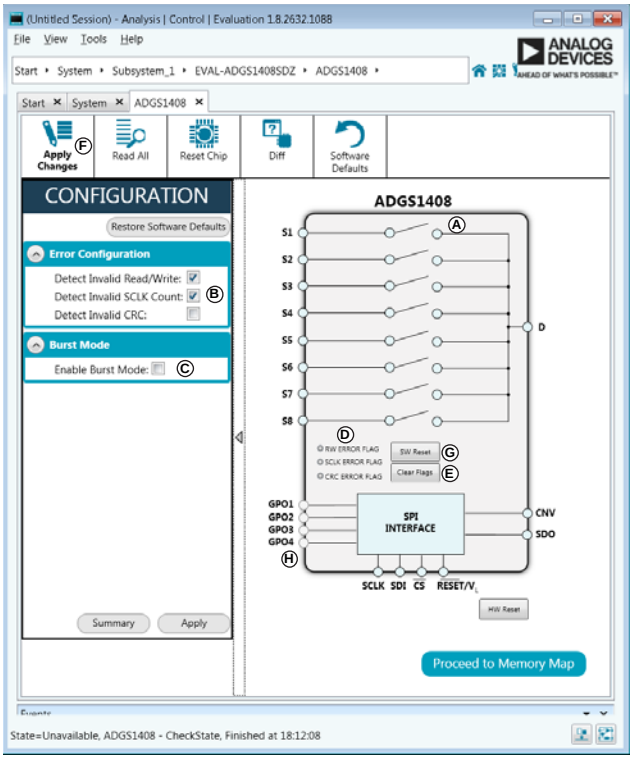

Figure 4. EVAL-ADGS1408SDZ/EVAL-ADGS1409SDZ Block Diagram with Labels

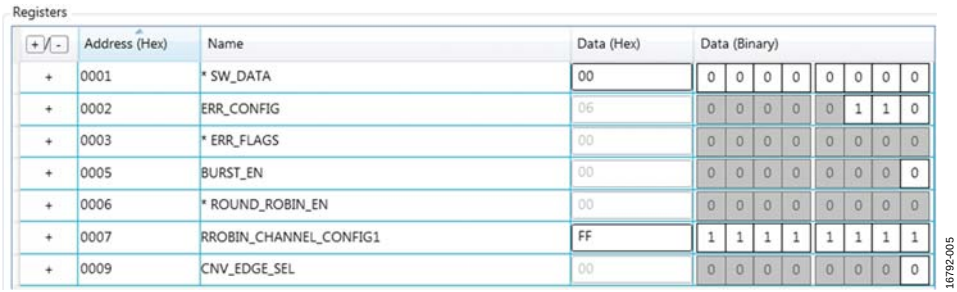

Figure 5. ADGS1408/ADGS1409 Memory Map

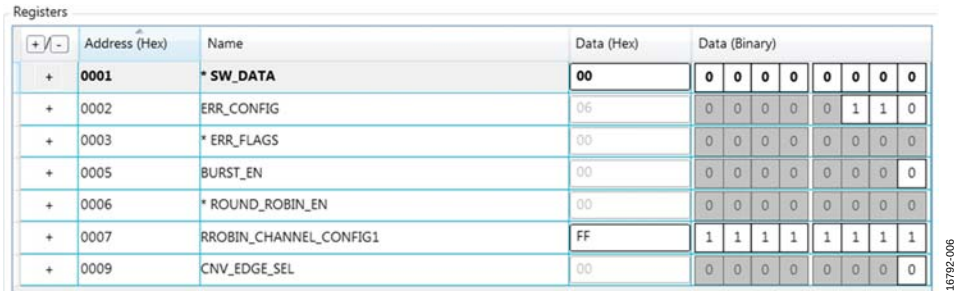

Figure 6. ADGS1408/ADGS1409 Memory Map with Unapplied Changes in the SW_DATA Register

EVALUATION BOARD SCHEMATICS AND ARTWORK

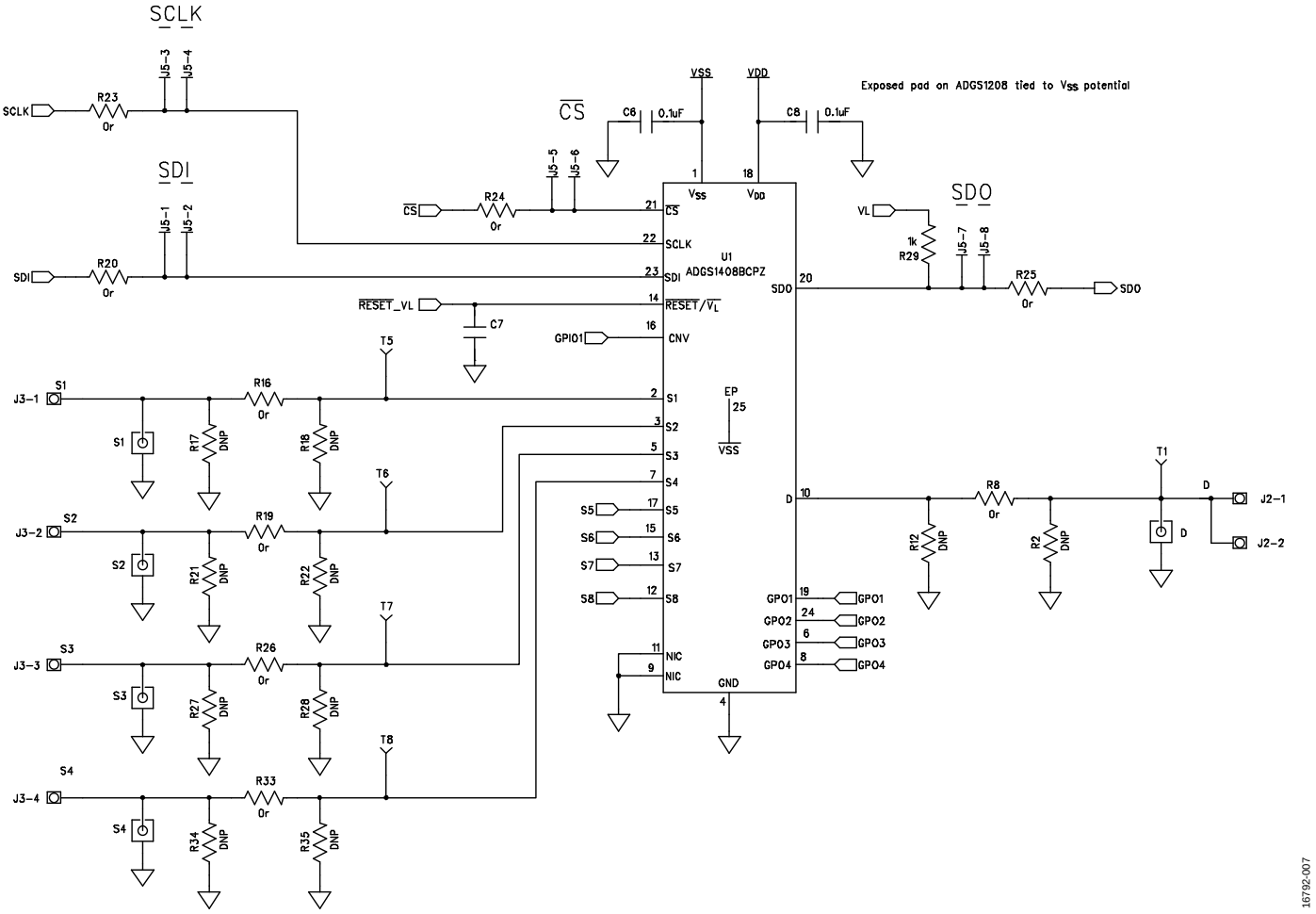

Figure 7. EVAL-ADGS1408SDZ Schematic—Main Device

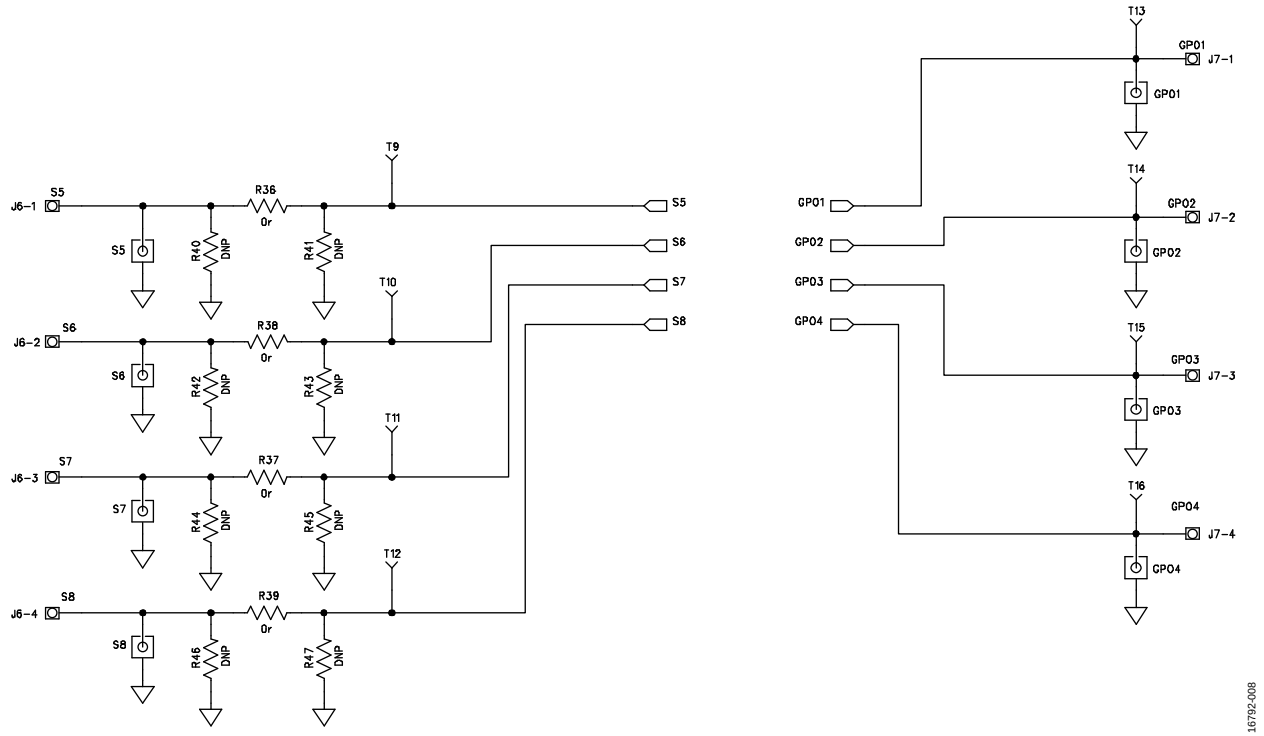

Figure 8. EVAL-ADGS1408SDZ—Main Device, Continued

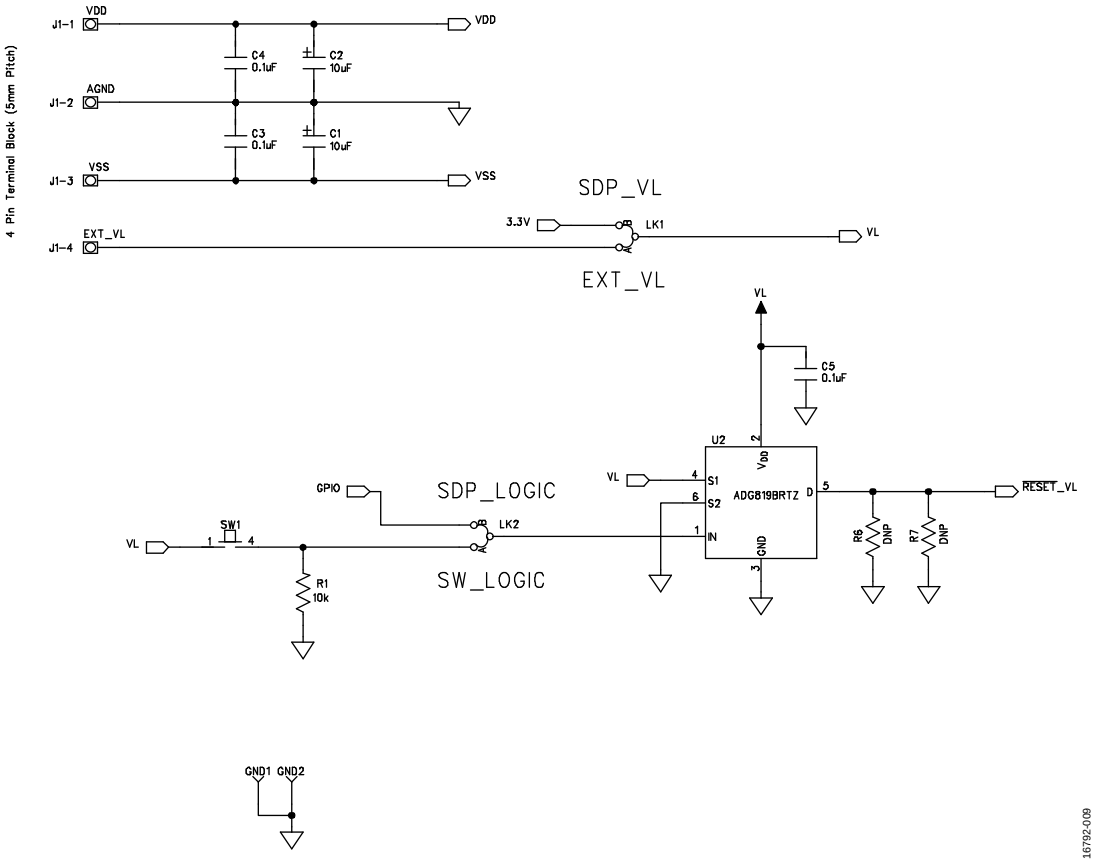

Figure 9. EVAL-ADGS1408SDZ—Power and Hardware Reset

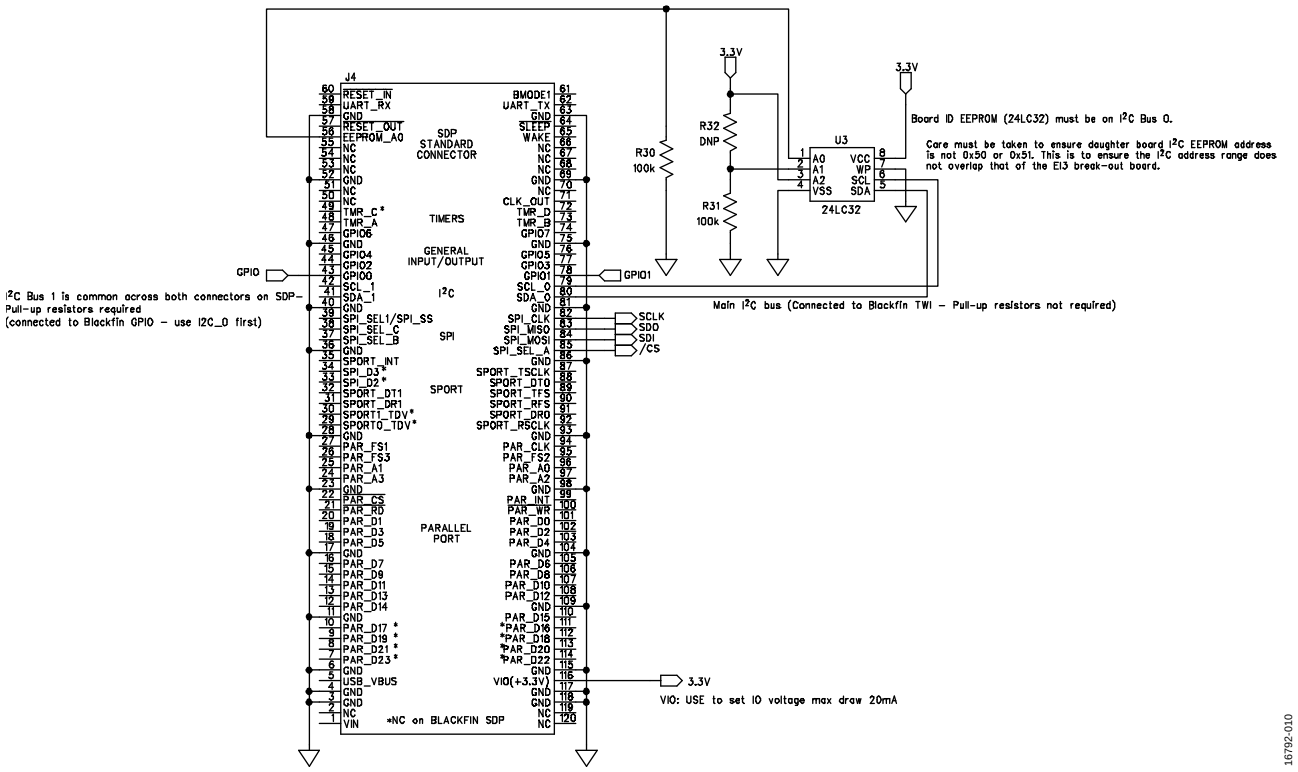

Figure 10. EVAL-ADGS1408SDZ—SDP Connector

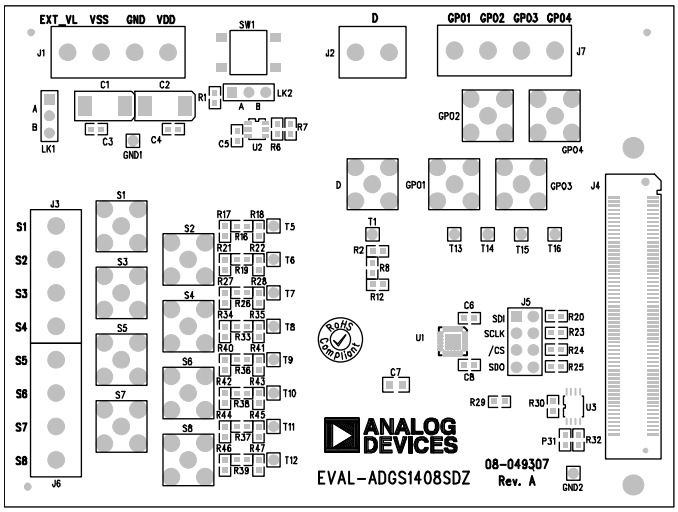

Figure 11. EVAL-ADGS1408SDZ Silk Screen

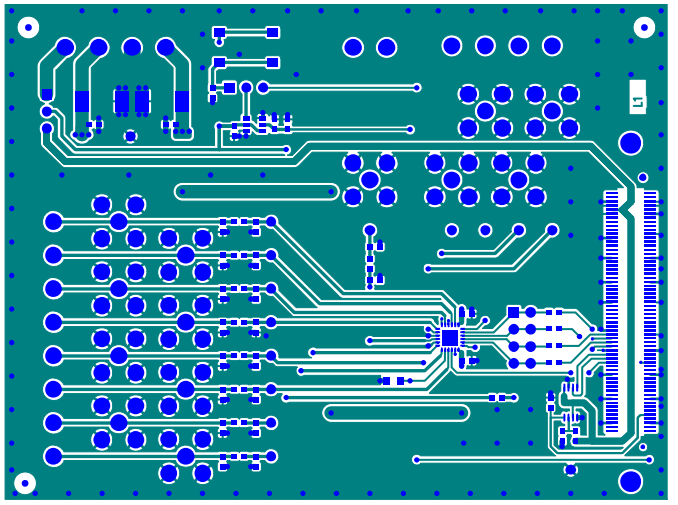

Figure 12. EVAL-ADGS1408SDZ Top Layer

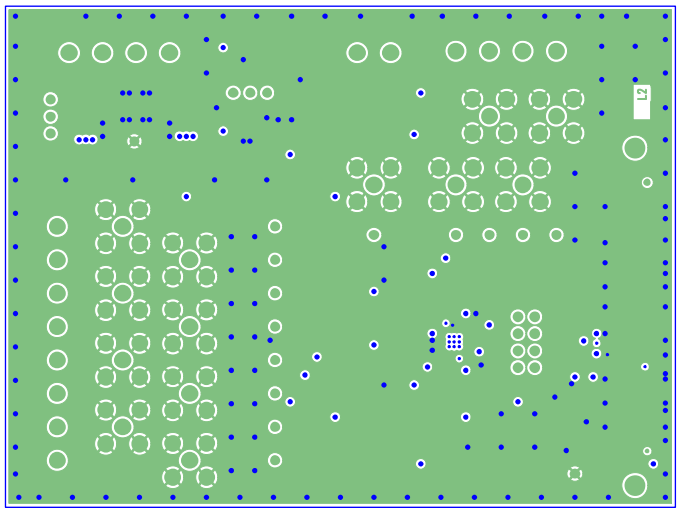

Figure 13. EVAL-ADGS1408SDZ Layer 2

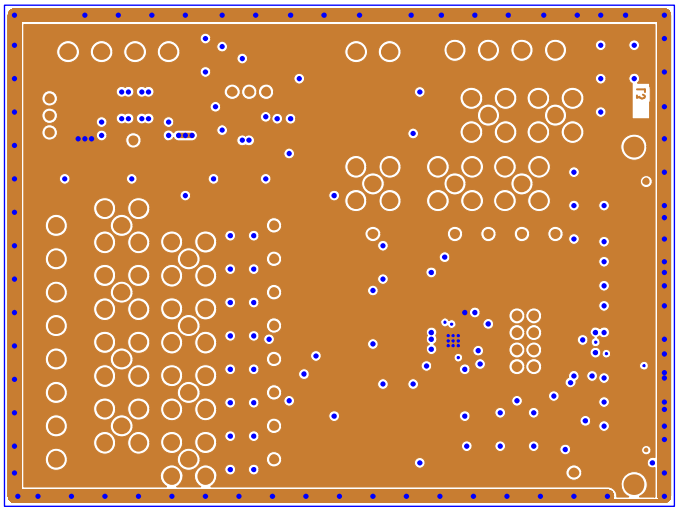

Figure 14. EVAL-ADGS1408SDZ Layer 3

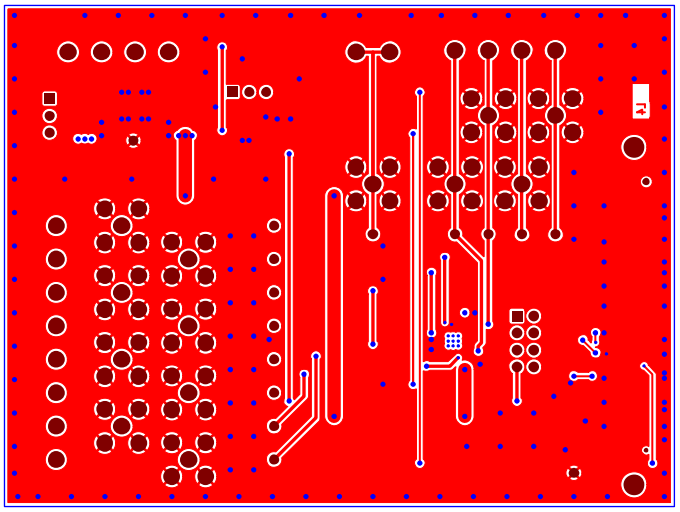

Figure 15. EVAL-ADGS1408SDZ Bottom Layer

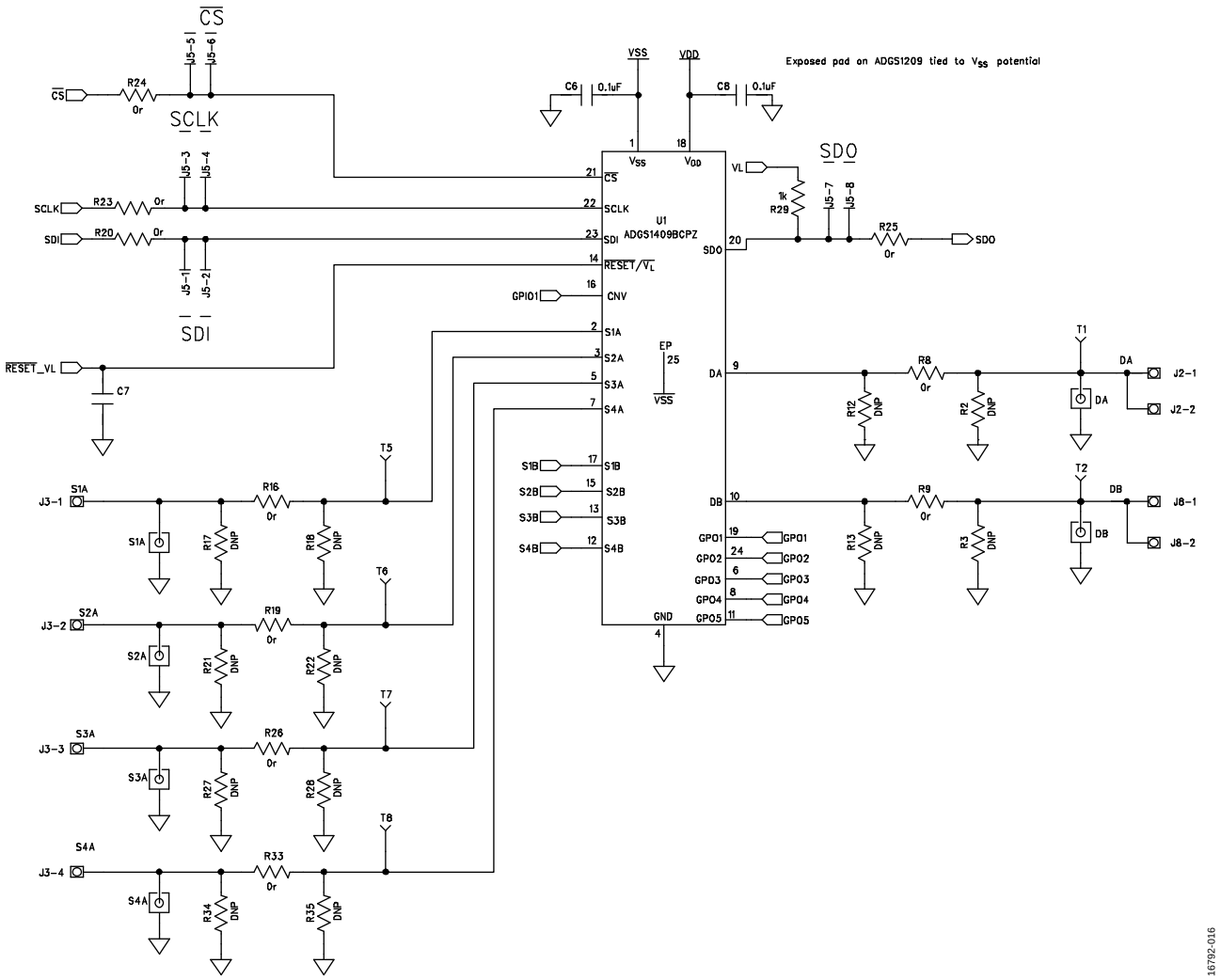

Figure 16. EVAL-ADGS1409SDZ—Main Device

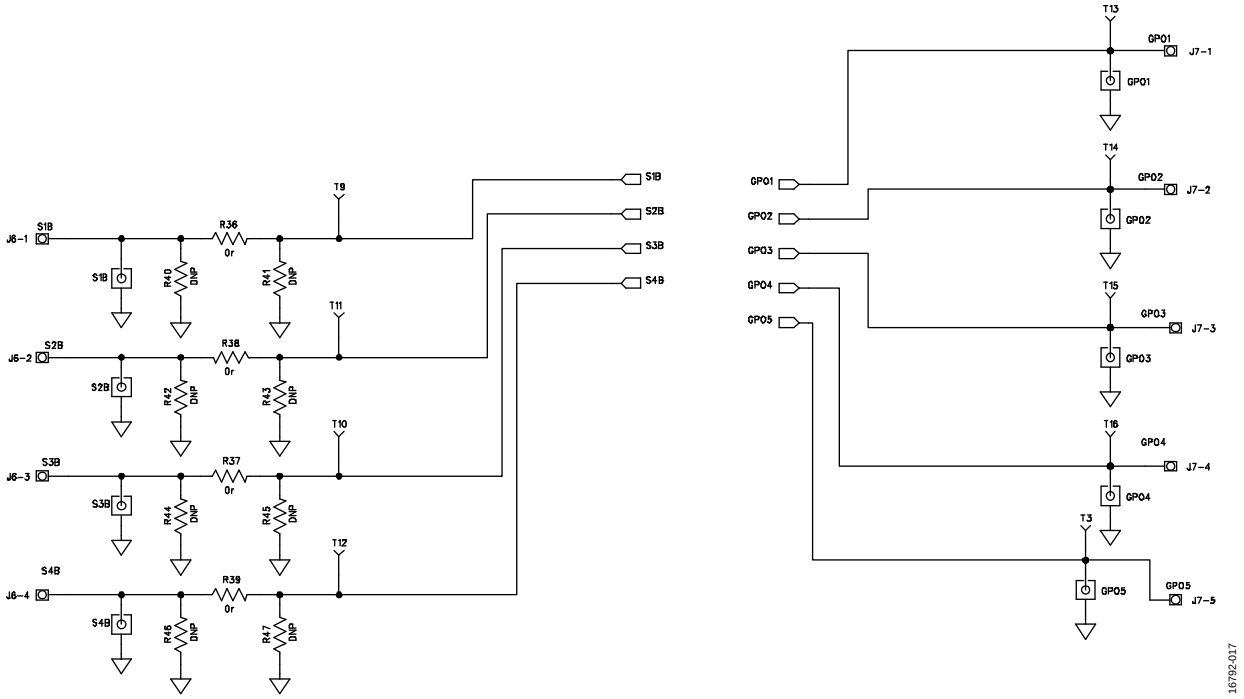

Figure 17. EVAL-ADGS1409SDZ—Main Device, Continued

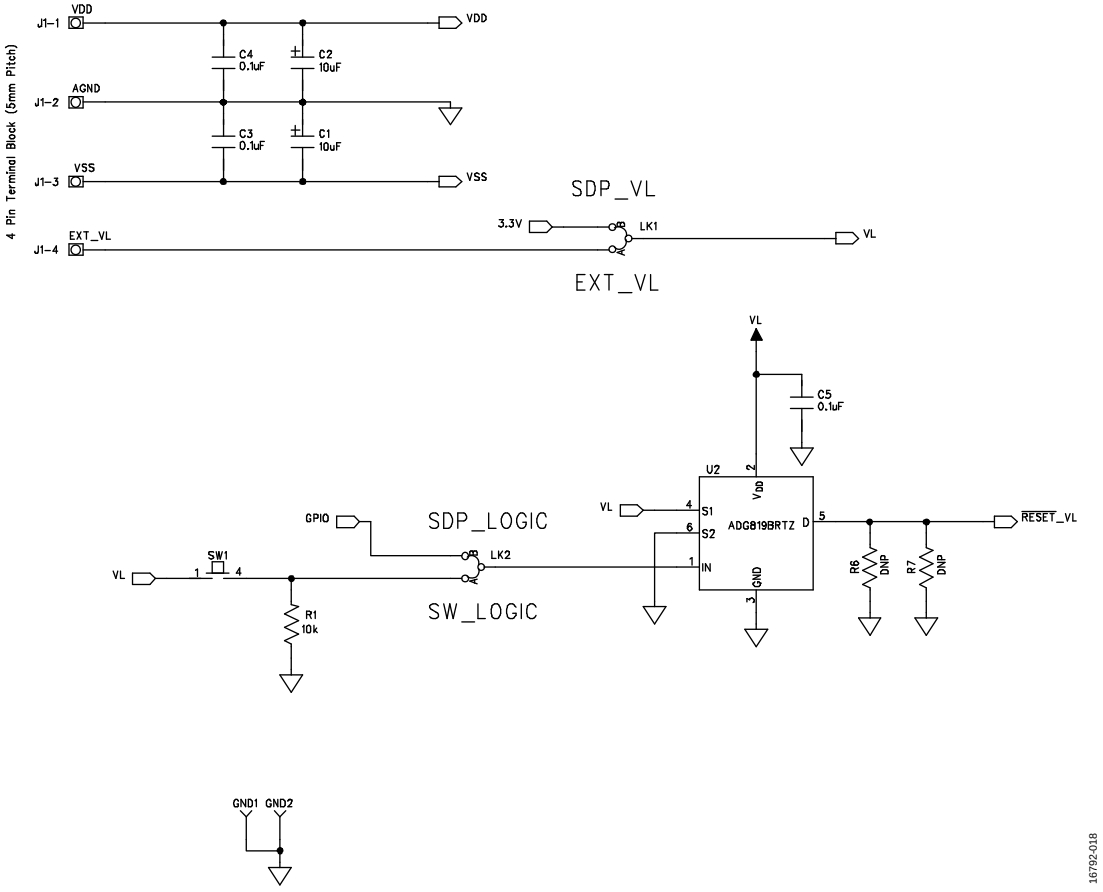

Figure 18. EVAL-ADGS1409SDZ—Power and Hardware Reset

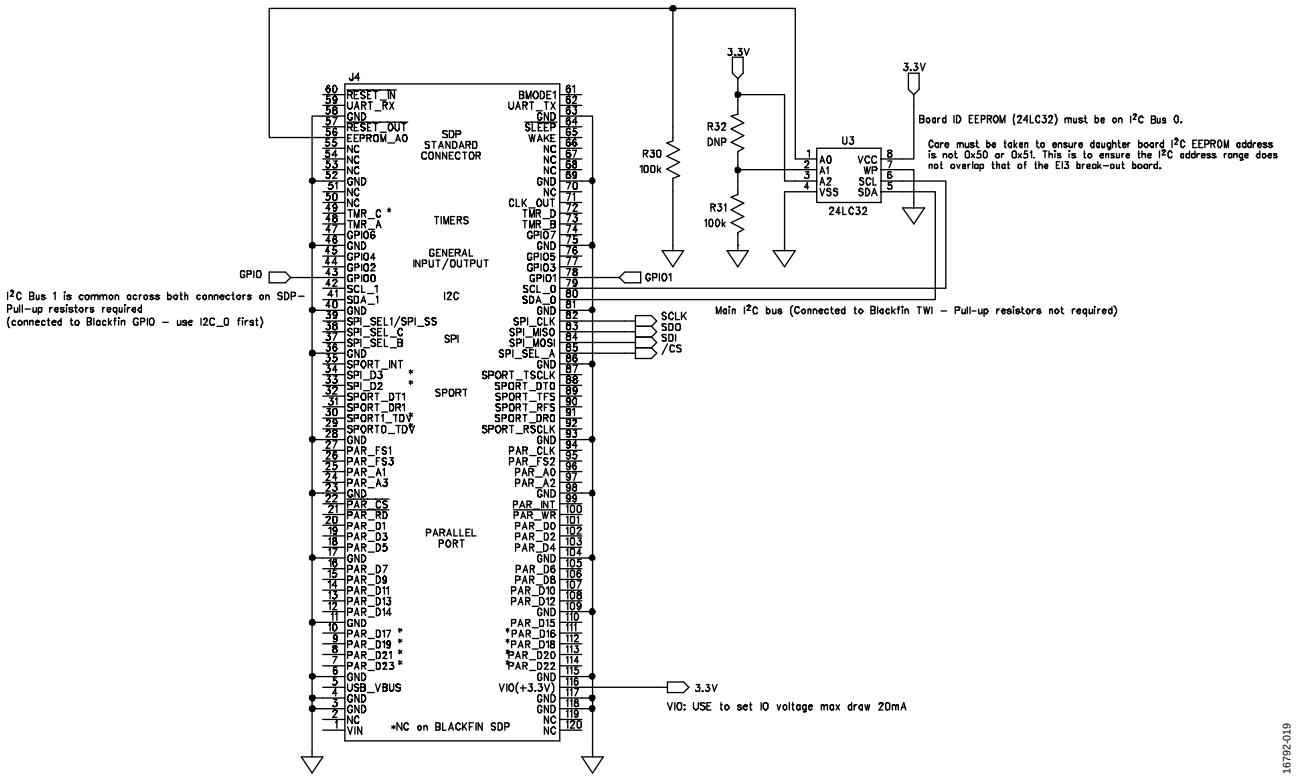

Figure 19. EVAL-ADGS1409SDZ—SDP Connector

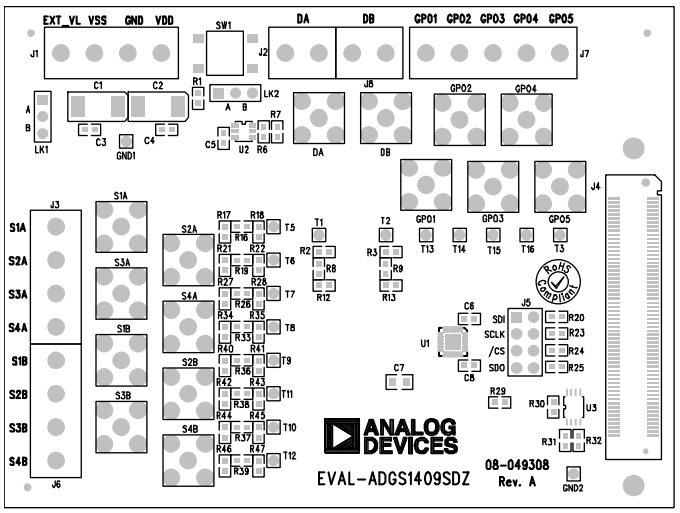

Figure 20. EVAL-ADGS1409SDZ Silk Screen

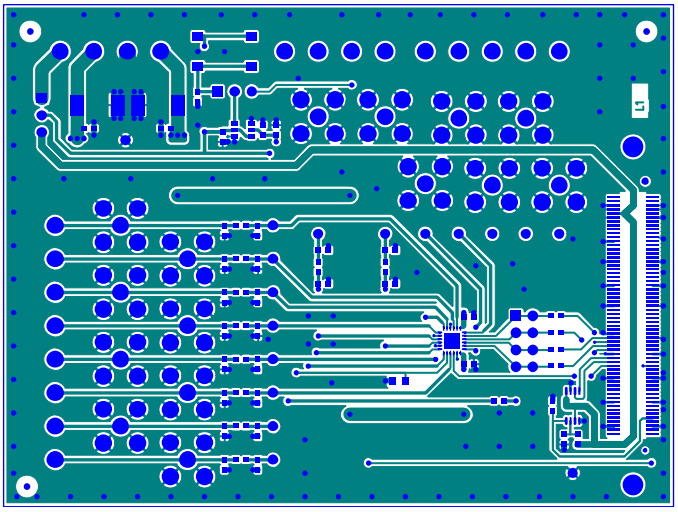

Figure 21. EVAL-ADGS1409SDZ Top Layer

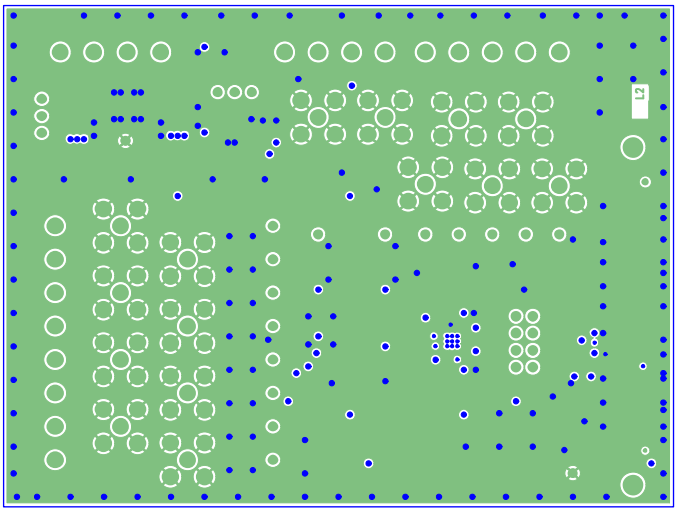

Figure 22. EVAL-ADGS1409SDZ Layer 2

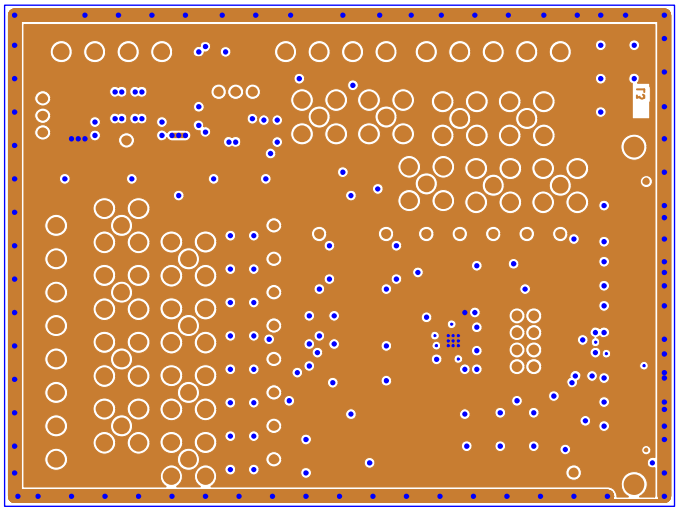

Figure 23. EVAL-ADGS1409SDZ Layer 3

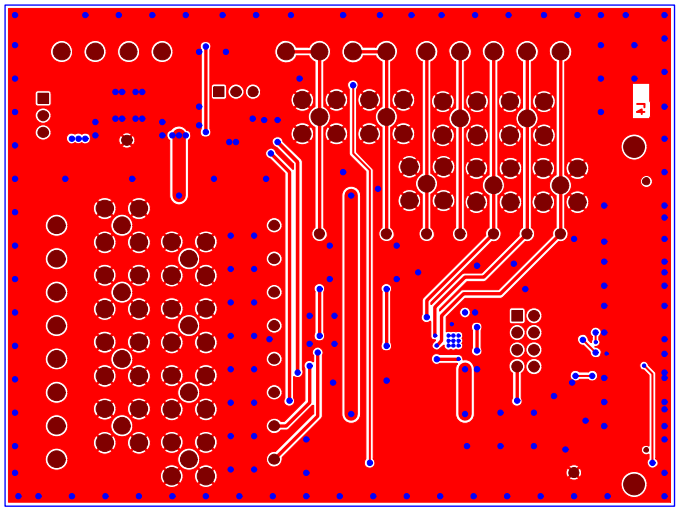

Figure 24. EVAL-ADGS1409SDZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description
C1 to C2	50 V tantalum capacitors, 10 µF, D size
C3 to C6, C8	50 V, X7R multilayer ceramic capacitors, 0.1 µF, 0603
C7	Capacitor, 10 µF, 0805, 16 V
D or DA, DB	Not placed
S1 to S8 or S1A to S4A, S1B to S4B	Not placed
T1, T2, T5 to T16	Red test points
GND1, GND2	Black test points
J1 to J3, J6 to J8	4-pin terminal blocks, 5 mm pitch
J4	120-way connector, 0.6 mm pitch
J5	Through hole, header, 4 × 2, 2.54 mm
LK1, LK2	3-pin single inline (SIL) headers and shorting link
R2, R3, R6, R7, R12, R13, R17, R18, R21, R22, R27, R28, R32, R34, R35, R40 to R47	Not placed
R8, R9, R16, R19, R20, R23 to R26, R33, R36 to R39	Resistors, 0 Ω, 0603, 1%
R1	Resistor, 10 kΩ, 0.063 W, 1%, 0603
R29	Resistor, 1 kΩ, 0.063 W, 1%, 0603
R30, R31	Resistor, 100 kΩ, 0.063 W, 1%, 0603
SW1	Surface-mount device (SMD) push button switch
U1	ADGS1408/ADGS1409, SPI interface, 4 Ω R_{ON}, ±15 V/+12 V/±5 V, 1.8 V logic control, 8:1/dual 4:1 muxes
U2	ADG819, 1.8 V to 5.5 V, 2:1 multiplexer and SPDT switch
U3	24LC32A-I/MS, 32 kbit, I^2C serial EEPROM