19-2234; Rev 1; 11/02

MAXIM

ECL/PECL Phase-Frequency Detectors

General Description

The MAX9382/MAX9383 are high-speed PECL/ECL phase-frequency detectors designed for use in high-bandwidth phase-locked loop (PLL) applications. The devices compare a single-ended reference (R) and a VCO (V) input and produce pulse streams on differential up (U) and down (D) outputs. When integrated, the difference of the output pulse streams provides a control voltage proportional to input phase or frequency difference. Guaranteed minimum short pulse duration completely eliminates minimum phase difference requirements during the lock condition, maximizing loop jitter performance.

The MAX9382/MAX9383 feature low propagation and reset delay, making them ideal for high-frequency clock synchronization use. The MAX9382 uses 100K logic levels, has a supply voltage range of V_{CC} - V_{EE} = 4.2V to 5.5V, and is pin compatible with Motorola's MCK12140. The MAX9383 uses 10H logic levels with a supply voltage range of V_{CC} - V_{EE} = 4.75V to 5.5V and is pin compatible with the MCH12140.

The MAX9382/MAX9383 are available in industry-standard 8-pin SO and space-saving 8-pin µMAX packages.

Applications

Precision Clock Distribution

Central Office

DSLAM

DLC

Base Station

ATE

Features

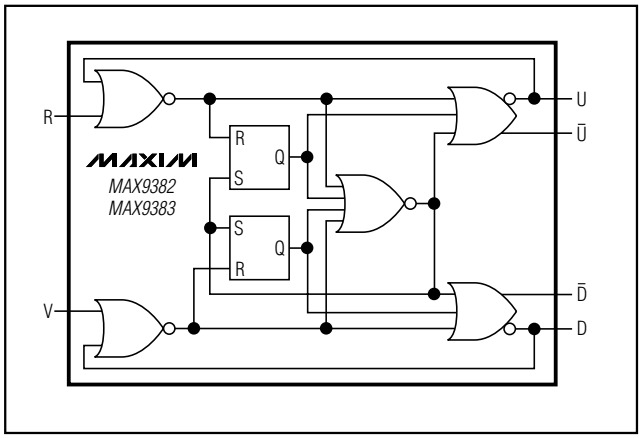
- **Guaranteed Minimum Pulse Width Eliminates Dead Band**
- **450MHz Typical Bandwidth with up to ±π Phase Detection**
- **75kΩ Internal Input Pulldown Resistors**
- **44mA Typical Supply Current**
- **±2kV ESD Protection (Human Body Model)**
- **Pin Compatible with MCK12140 and MCH12140**
- **Available in 8-Pin µMAX and SO Packages**

Ordering Information

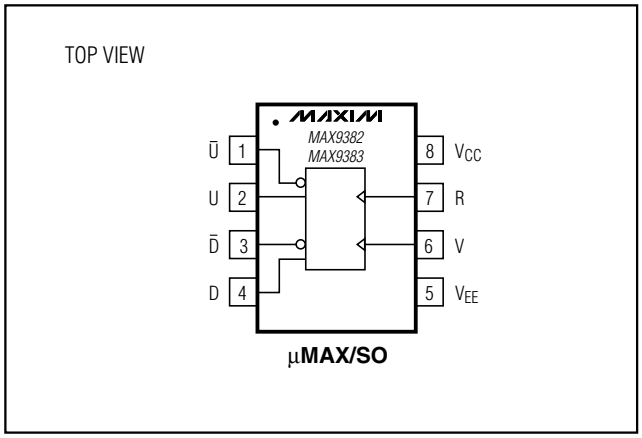
PART	TEMP RANGE	PIN-PACKAGE
MAX9382EUA*	-40°C to +85°C	8 µMAX
MAX9382ESA	-40°C to +85°C	8 SO
MAX9383EUA*	-40°C to +85°C	8 µMAX
MAX9383ESA	-40°C to +85°C	8 SO

**Future product—contact factory for availability.*

Functional Diagram



Pin Configuration



ECL/PECL Phase-Frequency Detectors

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} .....+6.0V
Inputs (R, V).....(V_{CC}) to (V_{EE} - 0.3V)
Continuous Output Current.....50mA
Surge Output Current.....100mA
Junction-to-Ambient Thermal Resistance in Still Air*
8-Pin µMAX.....+221°C/W
8-Pin SO.....+170°C/W
Junction-to-Ambient Thermal Resistance with*
500LFPM Airflow
8-Pin µMAX.....+155°C/W
8-Pin SO.....+99°C/W
Junction-to-Case Thermal Resistance
8-Pin µMAX.....+39°C/W
8-Pin SO.....+40°C/W
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
ESD Protection
Human Body Model (R, V, U, $\overline{U}$, D, $\overline{D}$).....±2kV
Soldering Temperature (10s)..... +300°C

*Ratings are for single-layer board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAX9382 DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 4.2V to 5.5V. Outputs loaded with 50Ω ±1% to V_{CC} - 2V, unless otherwise noted. Typical values at V_{CC} - V_{EE} = 4.5V.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUTS (R, V)												
Input High Voltage	V_{IH}		V_{CC} - 1.165		V_{CC} - 0.880	V_{CC} - 1.165		V_{CC} - 0.880	V_{CC} - 1.165		V_{CC} - 0.880	V
Input Low Voltage	V_{IL}		V_{CC} - 1.810		V_{CC} - 1.475	V_{CC} - 1.810		V_{CC} - 1. 475	V_{CC} - 1.810		V_{CC} - 1.475	V
Input High Current	I_{IH}	$V_{IN} = V_{IHMAX}$			150			150			150	µA
Input Low Current	I_{IL}	$V_{IN} = V_{ILMIN}$	0.5			0.5			0.5			µA
OUTPUTS (U, $\overline{U}$, D, $\overline{D}$)												
Single-Ended Output High Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	V_{CC} - 1.085	V_{CC} - 0.990	V_{CC} - 0.880	V_{CC} - 1.035	V_{CC} - 0.960	V_{CC} - 0.880	V_{CC} - 1.035	V_{CC} - 0.940	V_{CC} - 0.880	V
Single-Ended Output Low Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	V_{CC} - 1.890	V_{CC} - 1.810	V_{CC} - 1.555	V_{CC} - 1.850	V_{CC} - 1.770	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.730	V_{CC} - 1.600	V
Differential Output Voltage	V_{OH} - V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	585	820		585	810		585	800		mV
POWER SUPPLY												
Supply Current	I_{EE}	(Note 4)		43	56		44	56		45	58	mA

MAX9383 DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 4.75V to 5.5V. Outputs loaded with 50Ω ±1% to V_{CC} - 2V, unless otherwise noted. Typical values at V_{CC} - V_{EE} = 5.2V.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUTS (R, V)												
Input High Voltage	V_{IH}		V_{CC} - 1.230		V_{CC} - 0.890	V_{CC} - 1.130		V_{CC} - 0.810	V_{CC} - 1.060		V_{CC} - 0.720	V
Input Low Voltage	V_{IL}		V_{CC} - 1.950		V_{CC} - 1.500	V_{CC} - 1.950		V_{CC} - 1. 480	V_{CC} - 1.950		V_{CC} - 1.480	V
Input High Current	I_{IH}	V_{IN} = V_{IHMAX}			150			150			150	µA
Input Low Current	I_{IL}	V_{IN} = V_{ILMIN}	0.5			0.5			0.5			µA
OUTPUTS (U, $\overline{U}$, D, $\overline{D}$)												
Single-Ended Output High Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	V_{CC} - 1.115	V_{CC} - 1.010	V_{CC} - 0.890	V_{CC} - 0.980	V_{CC} - 0.924	V_{CC} - 0.810	V_{CC} - 0.945	V_{CC} - 0.900	V_{CC} - 0.720	V
Single-Ended Output Low Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	V_{CC} - 1.990	V_{CC} - 1.832	V_{CC} - 1.650	V_{CC} - 1.950	V_{CC} - 1.740	V_{CC} - 1.630	V_{CC} - 1.950	V_{CC} - 1.700	V_{CC} - 1.595	V
Differential Output Voltage	V_{OH} - V_{OL}	V_{IN} = V_{IH} or V_{IL}	650	822		650	817		650	803		mV
POWER SUPPLY												
Supply Current	I_{EE}	(Note 4)		37	52		38	52		39	52	mA

MAX9382/MAX9383 AC ELECTRICAL CHARACTERISTICS

(Over specified DC input parameters, f = 100MHz, outputs loaded with 50Ω ±1% to V_{CC} - 2V, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
R Input to U Output Delay	t_{PRU}	Figure 1	575	650	750	590	660	780	635	720	830	ps
V Input to D Output Delay	t_{PVD}	Figure 1	575	650	750	590	660	780	635	720	830	ps
R Input to D Output Delay	t_{PRD}	Figure 1	945	1120	1320	960	1110	1360	1005	1150	1360	ps
V Input to U Output Delay	t_{PVU}	Figure 1	945	1120	1320	960	1110	1360	1005	1150	1360	ps
Minimum Pulse Duration	t_{Pmin}	Figure 1	370	470		370	450		370	430		ps

MAX9382/MAX9383 AC ELECTRICAL CHARACTERISTICS (continued)

(Over specified DC input parameters, f = 100MHz, outputs loaded with 50Ω ±1% to V_{CC} - 2V, unless otherwise noted.) (Note 5)

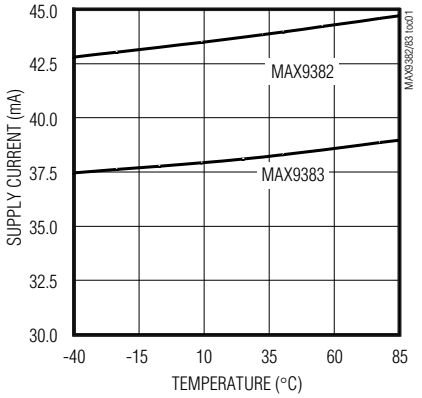
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Operating Frequency	f_{MAX}	±π usable phase difference range	400	450		400	450		400	450		MHz
Phase Offset		V_{IN} = 200MHz, 50% duty cycle (Note 6)		30	70		28	60		28	60	ps
Added Random Jitter	t_{RJ}	V_{IN} = 400MHz, 50% duty cycle (Note 7)		0.2	1.0		0.2	1.0		0.2	1.0	ps (RMS)
Output Rise/ Fall Time	t_R, t_F	20% to 80%, Figure 2	80		160	100		180	110		190	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +85°C. DC limits are guaranteed by design and characterization over the full operating temperature range.
Note 4: All pins open except V_{CC} and V_{EE}.
Note 5: Guaranteed by design and characterization. Limits are set to ±6 sigma.
Note 6: Phase offset is defined as the difference in propagation delay timing between the two input paths. It is measured between the U and D outputs at the differential crosspoint with a rising edge simultaneously applied at the R and V inputs.
Note 7: Device jitter added to the input signal.

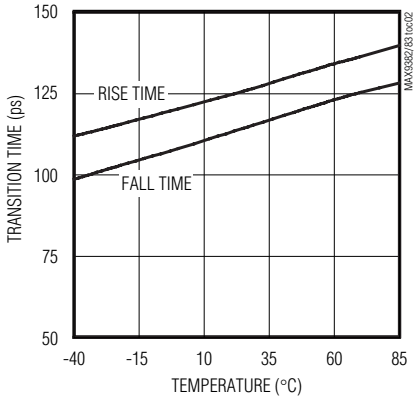
Typical Operating Characteristics

(V_{CC} - V_{EE} = +4.5V (MAX9382) or V_{CC} - V_{EE} = +5.2V (MAX9383), V_{IH} = V_{CC} - 1.00V, V_{IL} = V_{CC} - 1.60V, f_R = f_V = 100MHz, outputs loaded with 50Ω to V_{CC} - 2V, T_A = +25°C, unless otherwise noted.)

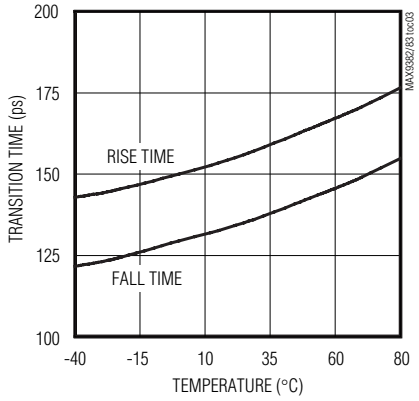
SUPPLY CURRENT vs. TEMPERATURE



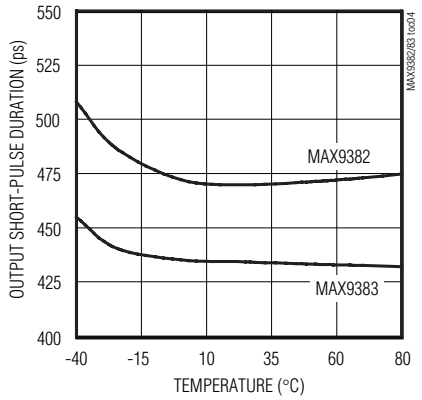
MAX9382 TRANSITION TIME vs. TEMPERATURE



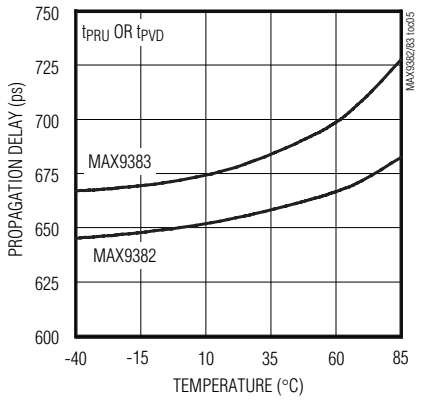
MAX9383 TRANSITION TIME vs. TEMPERATURE



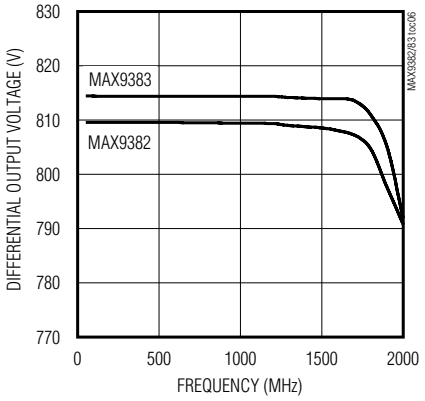
OUTPUT SHORT-PULSE DURATION vs. TEMPERATURE



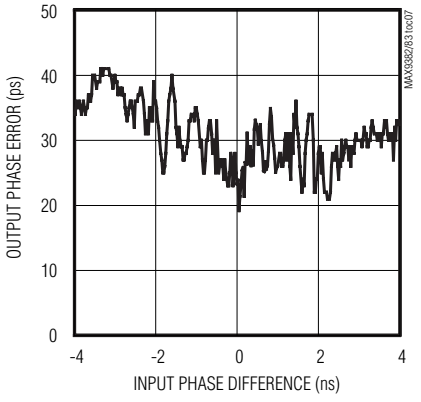
PROPAGATION DELAY vs. TEMPERATURE



DIFFERENTIAL OUTPUT VOLTAGE vs. FREQUENCY



OUTPUT PHASE ERROR vs. INPUT PHASE DIFFERENCE



ECL/PECL Phase-Frequency Detectors

Pin Description

PIN	NAME	FUNCTION
1	$\overline{U}$	Inverting Up Output. Pulse stream is generated at this pin when $f_R > f_V$ or V lags R in phase. Terminate with 50Ω resistor to V_{CC} - 2V or equivalent.
2	U	Noninverting Up Output. Pulse stream is generated at this pin when $f_R > f_V$ or V lags R in phase. Terminate with 50Ω resistor to V_{CC} - 2V or equivalent.
3	$\overline{D}$	Inverting Down Output. Pulse stream is generated at this pin when $f_V > f_R$ or R lags V in phase. Terminate with 50Ω resistor to V_{CC} - 2V or equivalent.
4	D	Noninverting Down Output. Pulse stream is generated at this pin when $f_V > f_R$ or R lags V in phase. Terminate with 50Ω resistor to V_{CC} - 2V or equivalent.
5	V_{EE}	Negative Supply
6	V	Single-Ended VCO Input
7	R	Single-Ended Reference Input
8	V_{CC}	Positive Supply. Bypass from V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Detailed Description

The MAX9382/MAX9383 are high-speed phase or frequency detectors. The MAX9382 is compatible with 100K logic and has a power-supply range of V_{CC} - V_{EE} = 4.2V to 5.5V. The MAX9383 is compatible with 10H logic with a power-supply range of V_{CC} - V_{EE} = 4.75V to 5.5V. Both devices are specified to function from -40°C to +85°C.

Each device is symmetrical; the R and V input functions may be swapped, together with the U and D output functions, and the inputs and outputs relabeled. Because of this device symmetry, a necessary condition for correct phase measurement operation is that the $\overline{U}$ and $\overline{D}$ outputs must both be high (state 0 condition) when the rising edge of the leading input is received. This condition is automatically generated when the two inputs are at different frequencies.

Phase Detection

The MAX9382/MAX9383 are intended for use in high-bandwidth PLL applications. These devices compare a single-ended VCO input (V) to a single-ended reference input (R) to determine the phase or frequency relationship between V and R. The device differential outputs U, $\overline{U}$ and D, $\overline{D}$ provide pulse trains with duty cycle proportional to the phase or frequency difference between R and V. These outputs are the up and down signals required to control the system VCO. Figure 1 shows typical waveforms when V leads R and V lags R. Subtracting and integrating these two outputs provide the necessary VCO control signal. Figure 3 shows the device transfer function obtained. The detector can detect phase differences up to ±2π. The application frequency and the characteristics of the device internal reset circuits determine the usable input phase difference range.

Frequency Detection

Figure 4 is the state diagram for the MAX9382/MAX9383. With the two inputs at the same frequency, and input R leading input V, the device toggles between states 0 and 2. Similarly, if input R lags input V, the device toggles between states 0 and 1. With the two inputs at different frequencies, the output becomes a function of the frequency difference. The normalized ideal transfer function is given by:

$$V_{OUT\_AVE} = 1 - \frac{f_R}{2f_V} \text{ for } f_V > f_R$$

and

$$V_{OUT\_AVE} = 1 - \frac{f_V}{2f_R} \text{ for } f_R > f_V$$

Output Pulses

When inputs R and V are at the same phase and frequency, outputs U, $\overline{U}$ and D, $\overline{D}$ produce a stream of minimum duration pulses that occur at the rising edges of the input waveforms. This is the lock condition. If either input starts to lead the other in phase, the width of pulses on the corresponding output (U for R input, D for V input) increases in proportion to the phase difference. In a PLL implementation, these outputs direct the

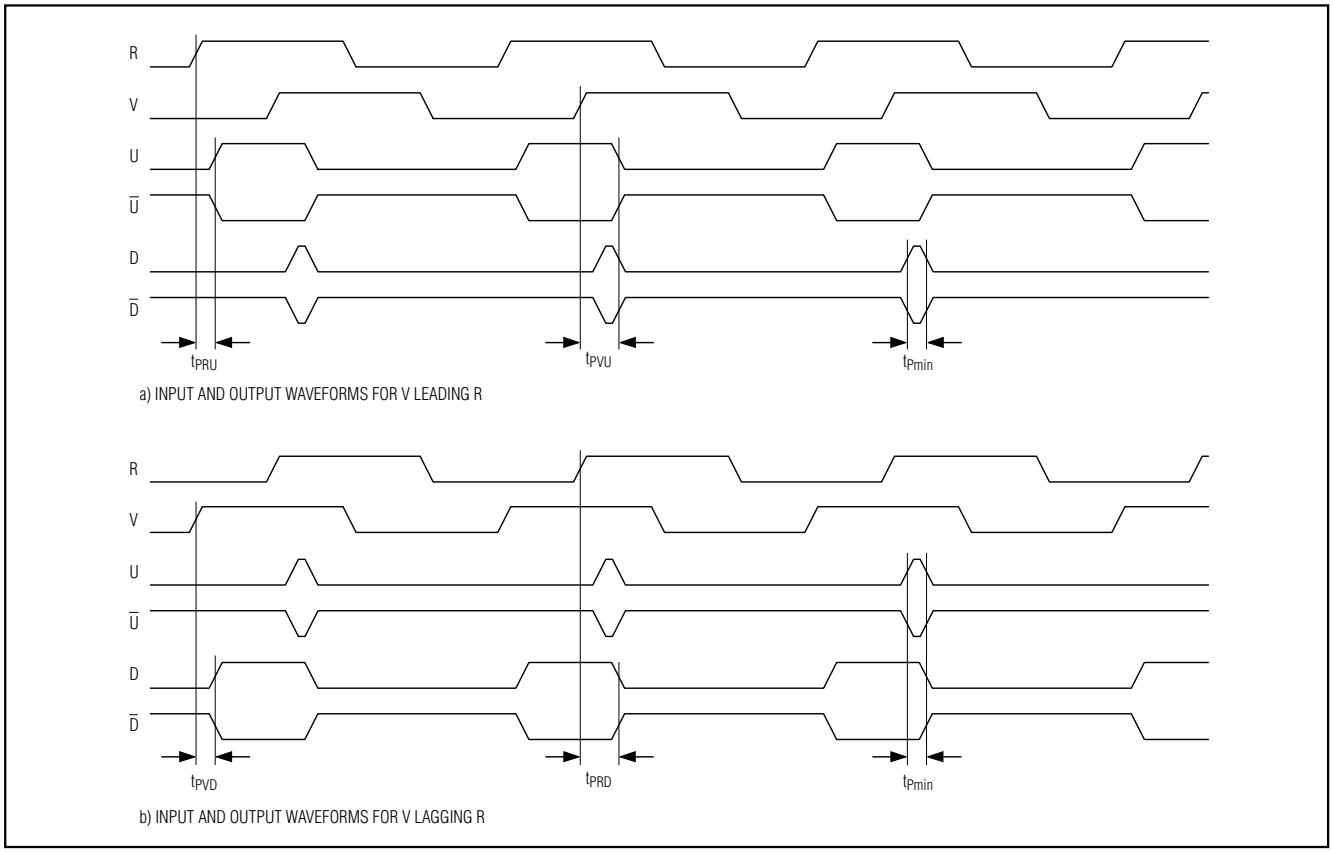


Figure 1. Typical Waveforms when $f_R = f_V$

system VCO to increase or decrease frequency to maintain the lock condition.

The minimum output pulse duration is an important parameter for the design of the signal processing functions, which follow the phase detector. When controlling a charge-pump integrator, a detector can produce a dead-zone characteristic at the lock condition if the minimum pulse width is too short. MAX9382/MAX9383 eliminate this dead-zone characteristic, and the resulting phase offset at lock, by providing a well-defined minimum output pulse width.

Applications Information

The MAX9382/MAX9383 input and output levels are defined to be relative to the positive supply voltage. In ECL systems, the positive supply voltage is conventionally chosen to be system ground. This arrangement produces the best noise immunity, since ground is normally a system-wide reference voltage. Operate the devices with V_{CC} connected to ground and V_{EE} connected to a negative supply for ECL systems. With

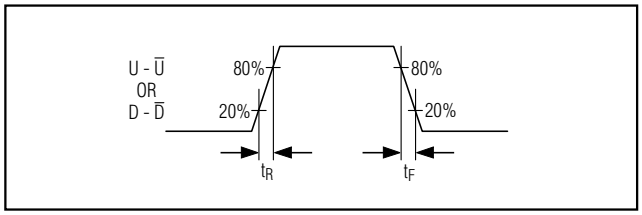


Figure 2. Output Transition Times

PECL systems, connect V_{CC} to a positive supply and V_{EE} to ground.

Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize the performance and noise immunity of ECL devices. This is particularly true of a PECL system where the power-supply voltage is used as a reference. Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel and as close to the device as possible, with the 0.01µF capaci-

ECL/PECL Phase-Frequency Detectors

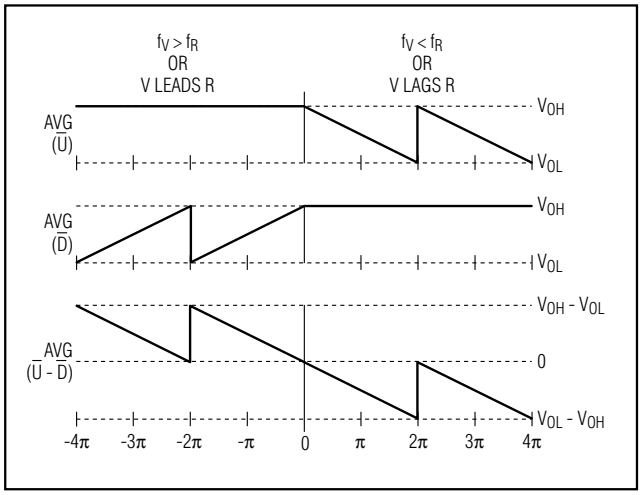


Figure 3. Average Output Voltage vs. Phase Difference

tor closest to the device pins. Use multiple parallel vias for ground plane connection to minimize inductance.

Circuit Board Traces

Input and output trace characteristics affect the performance of ECL/PECL devices. Connect each of the detector's inputs and outputs to a 50Ω characteristic impedance trace. Avoid impedance discontinuities, maintain the distance between differential traces, avoid sharp corners, and keep the electrical length of the differential traces matched. This maximizes common-mode noise rejection and reduces signal skew. Trace vias cause impedance discontinuities, so keep the number of vias in the 50Ω traces to a minimum. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables.

Output Termination

Terminate outputs through 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if the U output of the MAX9382 or MAX9383 is connected to a single-ended input, terminate both the U and $\overline{U}$ outputs.

Chip Information

TRANSISTOR COUNT: 706

PROCESS: Bipolar

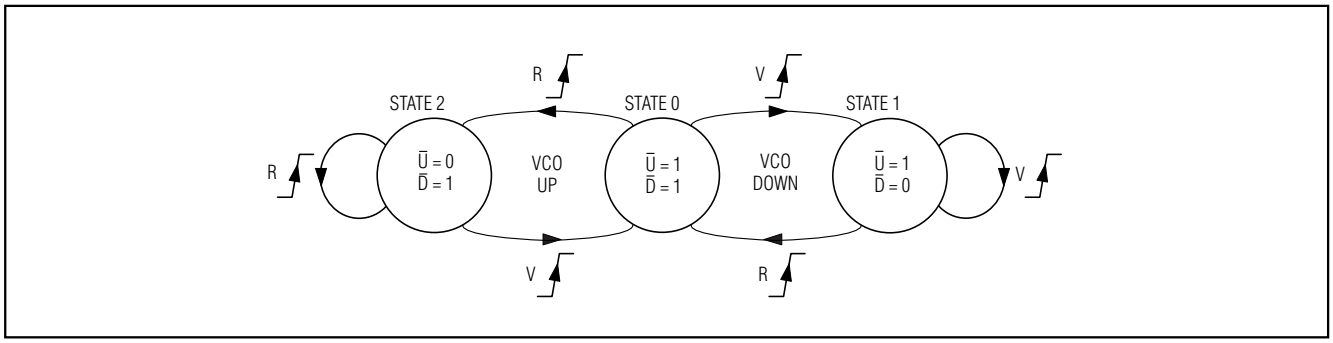
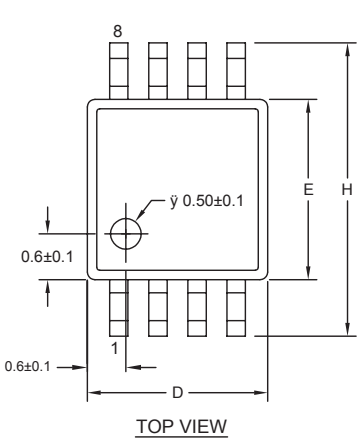


Figure 4. MAX9382/MAX9383 State Diagram

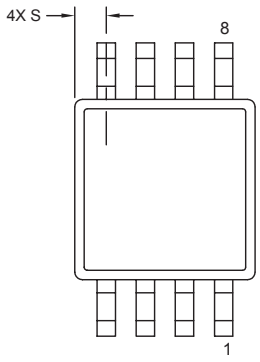
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS

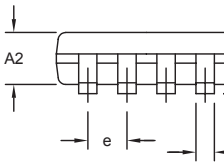


TOP VIEW

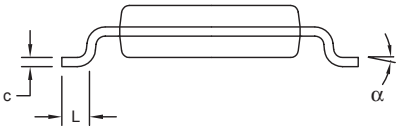


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1

ECL/PECL Phase-Frequency Detectors

Package Information (continued)

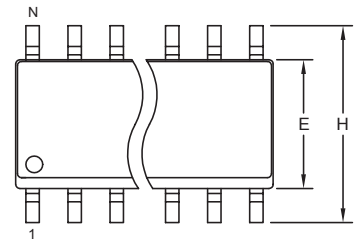
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

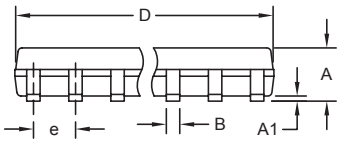
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

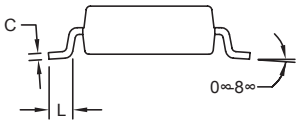
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

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