# 8 A Integrated Synchronous Buck Converter

# NCP3237

The NCP3237 is a single−phase synchronous buck converter that integrates power MOSFETs to provide a high−efficiency and compact−footprint power management solution. This device is able to deliver up to 8 A output current over a wide output voltage range from 0.6 V to 12 V (up to 80% of $V_{IN}$). The NCP3237 offers a fixed frequency regulator ideally suited for noise sensitive systems.

### Features

- $V_{IN}$ = 4.5 V ~ 16 V
- $V_{OUT}$ = 0.6 V ~ 0.80*$V_{IN}$ and up to 12 V
- Integrated Power MOSFETs
- Up to 8 A Output Current
- Integrated 5 V LDO
- Programmable Switching Frequency from 300 kHz to 1.2 MHz
- Forced CCM
- Both High−side and Low−side OCP Operation
- Hiccup Over−Current Protection
- Hiccup Over−Voltage and Under−Voltage Protection
- Recoverable Thermal Shutdown Protection
- 3.5 mm x 3.5 mm, QFN18 Package
- Safe Startup into Pre−biased Output Voltage
- This is a Pb−Free Device

### Typical Application

- Base Station Radio Units
- Point of Load
- Telecom and Networking
- Server and Storage System

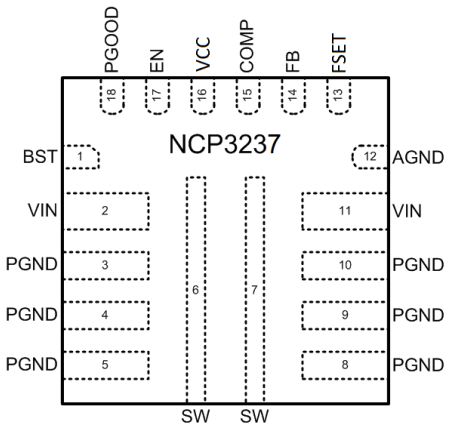
**MARKING DIAGRAM**

**QFN18 3.5x3.5, 0.5P**
**CASE 485FR**


| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**PINOUT DIAGRAM**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP3237MNTXG | QFN18 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

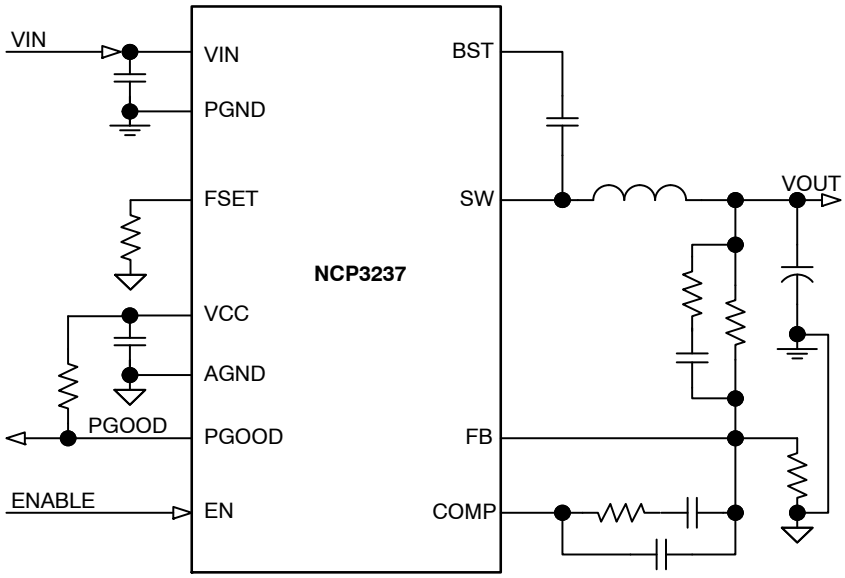



**Figure 1. Typical Application Circuit**

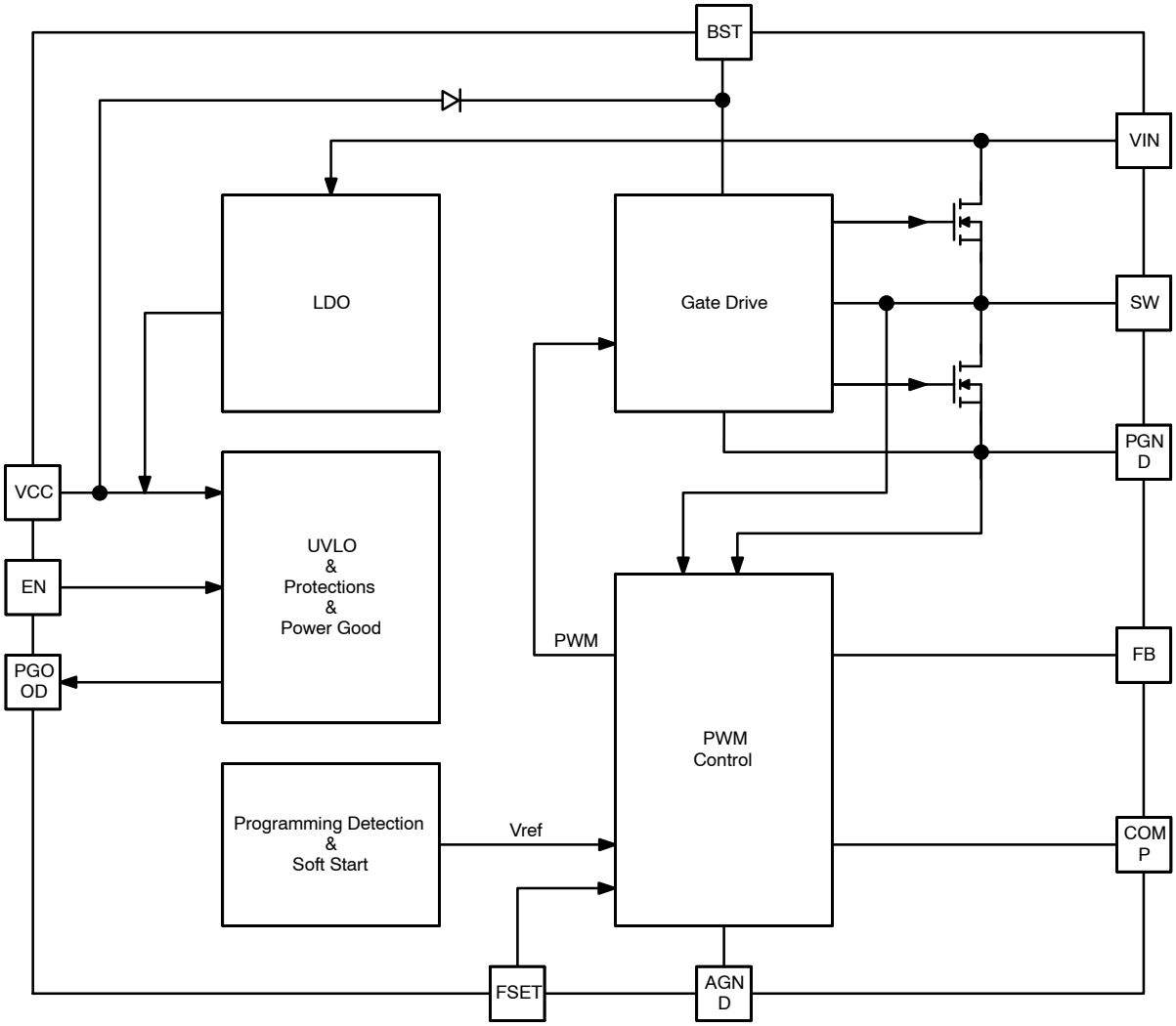



**Figure 2. Functional Block Diagram**

## PIN DESCRIPTION

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | BST | Power Bidirectional | **Bootstrap**. Provides bootstrap voltage for the high−side gate driver. A 0.1 μF ~ 1 μF ceramic capacitor is required from this pin to SW. |
| 2, 11 | VIN | Power Input | **Power Supply Input**. Power supply input pin of the device, which is connected to drain of internal high−side power MOSFET. Ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to this pin. |
| 3, 4, 5, 8, 9, 10 | PGND | Power Ground | **Power Ground**. These pins are the power supply ground pins of the device, which are connected to source of internal low−side power MOSFET. |
| 6, 7 | SW | Power Output | **Switching Node**. Pins to be connected to an external inductor. These pins are interconnection between internal high−side MOSFET and low−side MOSFET. |
| 12 | AGND | Analog Ground | **Analog Ground**. Signal reference ground for the IC. Must be connected to the power ground. |
| 13 | FSET | Analog Input | **Frequency Option**. A resistor from this pin to AGND programs switching frequency. |
| 14 | FB | Analog Input | **Feedback**. Inverting input to error amplifier. |
| 15 | COMP | Analog Output | **Compensation**. Output pin of error amplifier. |
| 16 | VCC | Analog Power | **Voltage Supply of Controller**. Power supply input pin of control circuits. A 4.7 μF or larger ceramic capacitor bypasses this input to AGND. This capacitor should be placed as close as possible to this pin. |
| 17 | EN | Logic Input | **Enable**. Logic high enables the device and logic low shuts down the device. |
| 18 | PGOOD | Logic Output | **Power Good**. Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window. |

## MAXIMUM RATINGS

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power Supply Voltage to PGND | $V_{IN}$ | −0.3 | 17 | V |
| Switch Node to PGND | $V_{SW}$ | −0.3<br>−3 (<10ns) | 17<br>22 (<10ns) | V |
| Analog Supply Voltage to GND | $V_{CC}$ | −0.3 | 6.0 | V |
| BST to PGND | BST_PGND | −0.3 | 22<br>28 (<10ns) | V |
| BST to SW | BST_SW | −0.3 | 6.0 | V |
| FB to AGND | FB | −0.3 | 6.0 | V |
| AGND to PGND | | −0.3 | 0.3 | V |
| Exposed Pad to PGND | | −0.3 | 0.3 | V |
| Other Pins | | −0.3 | $V_{CC}$+0.3 | V |
| Operating Junction Temperature Range | $T_J$ | −40 | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −40 | 150 | °C |
| Storage Temperature Range | $T_{STG}$ | −55 | 150 | °C |
| Thermal Characterization Parameter, Junction to Top Case (Note 1) | $R_{\Psi JC}$ | 2 | | °C/W |
| Thermal Resistance Junction to Bottom Case/Leads (Note 1) | $R_{\theta JC}$ | 3.3 | | °C/W |
| Thermal Resistance Junction to Ambient (Note 1) | $R_{\theta JA}$ | 31 | | °C/W |
| Power Dissipation at $T_A$ = 25°C (Note 2) | $P_D$ | 4 | | W |
| ESD Capability, Human Body Model per JESD22−A114 | $ESD_{HBM}$ | 2 | | kV |
| ESD Capability, Charged Device Model per JESD22−C101 | $ESD_{CDM}$ | 1 | | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The thermal resistance values are dependent of the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4−layer FR−4 PCB board, which has two, 1−ounce copper internal power and ground planes and 2−ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors etc.)
2. The maximum power dissipation (PD) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout. The reference data is obtained based on $T_{JMAX}$ = 150°C and $R_{\theta JA}$ = 31°C/W.

## RECOMMENDED OPERATING RANGE

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | 4.5 | 16 | V |
| Output Voltage | $V_{OUT}$ | 0.6 | 12 | V |
| Output Current, Continuous | $I_{OUT}$ | 0 | 8 | A |
| Junction Temperature (Note 3) | $T_J$ | −40 | 130 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Device specifications tested and characterized for 150°C operation with the Tsd function disabled.

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = 12V, typical values are referenced to $T_J$ = 25°C, Min and Max values are referenced to $T_J$ = −40°C to 150°C. unless otherwise noted.)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE MONITOR** | | | | | | |
| VCC Under−Voltage (UVLO) Threshold | VCC falling | $V_{CCUV}$ | 3.7 | 3.88 | | V |
| VCC OK Threshold | VCC rising | $V_{CCOK}$ | | 4.15 | 4.3 | V |
| VCC UVLO Hysteresis | | $V_{CCHYS}$ | | 269 | | mV |
| **SUPPLY CURRENT** | | | | | | |
| $V_{IN}$ Quiescent Supply Current | EN high, $V_{FB}$ = 600 mV, Non−switching | $I_{QIN}$ | | 6.1 | 9.5 | mA |
| $V_{IN}$ Shutdown Current | EN low | $I_{SD\_IN}$ | | 65 | 115 | μA |
| **VCC** | | | | | | |
| Output Voltage | 6V < VIN < 16V, IVCC = 20mA, EN High (Note 4) | $V_{CC}$ | 4.85 | 5.0 | 5.15 | V |
| Load Regulation | 6V < VIN < 16V, IVCC = 5mA to 50mA, EN High (Note 4) | $V_{CC\_LOR}$ | −3.0 | | 3.0 | % |
| Dropout Voltage | VIN = 5V, IVCC = 50mA, EN High (Note 4) | $V_{DC\_VCC}$ | | 260 | | mV |
| Effective Capacitance of VCC Bypass Capacitor | FSW < 600 kHz | $C_{LDO\_EFF}$ | 680 | | | nF |
| | FSW ≥ 600 kHz | | 840 | | | |
| **ENABLE** | | | | | | |
| EN High Threshold | Normal Operation | $V_{H\_EN}$ | 1.6 | | | V |
| EN Low Threshold | Shutdown | $V_{L\_EN}$ | | | 1.2 | V |
| EN Input Impedance | Resistance from EN pin to AGND | $R_{EN}$ | | 1.5 | | MΩ |
| **SOFT START** | | | | | | |
| System Reset Time | From EN High to BST Refresh (Note 5) | $T_{RST}$ | | 0.8 | | ms |
| BST Refresh Time | | $T_{BST}$ | | 10 | | μs |
| Soft Start Slew Rate | Refer to Internal VREF From Beginning of SS until PGOOD Asserts | $SR_{SS}$ | 0.55 | 0.6 | 0.68 | mV/μs |
| **PGOOD** | | | | | | |
| PGOOD Startup Delay | Measured from end of Soft Start to PGOOD Assertion (Note 5) | $T_{d\_PGOOD}$ | | 100 | | μs |
| PGOOD Shutdown Delay | Measured from EN to PGOOD de−assertion | | | 1 | | μs |
| PGOOD Low Voltage | $I_{PGOOD}$ = −4 mA | $V_{I\_PGOOD}$ | | | 0.3 | V |
| PGOOD Leakage Current | PGOOD = 5 V | $I_{lkg\_PGOOD}$ | | | 1.0 | μA |
| **SWITCHING FREQUENCY** | | | | | | |
| Switching Frequency in CCM | 1% 40.2 kΩ Resistor from FSET Pin to AGND | $F_{SW}$ | 495 | 550 | 605 | kHz |
| **VOLTAGE REGULATION** | | | | | | |
| Regulated Feedback Voltage | EN = High 0°C to 85°C<br>−40°C to 150°C | $V_{FB}$ | 595<br>594 | 600<br>600 | 605<br>606 | mV |

**ELECTRICAL CHARACTERISTICS** (continued)
($V_{IN}$ = 12V, typical values are referenced to $T_J$ = 25°C, Min and Max values are referenced to $T_J$ = –40°C to 150°C. unless otherwise noted.)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **PWM MODULATION** | | | | | | |
| PWM Ramp Amplitude | (Note 5) | $V_{RAMP}$ | | $V_{IN}$/8 | | V |
| Minimum On Time | (Note 5) | $T_{on\_min}$ | | 50 | 68 | ns |
| Minimum Off Time, absolute | (Note 5) (Note 6) | $T_{off\_min}$ | | 160 | 200 | ns |
| **VOLTAGE ERROR AMPLIFIER** | | | | | | |
| Open–Loop DC Gain | (Note 5) | $GAIN_{EA}$ | 94 | 100 | | dB |
| Unity Gain Bandwidth | (Note 5) | $GBW_{EA}$ | 11 | 14 | | MHz |
| Slew Rate | (Note 5) | $SR_{COMP}$ | 9 | 15 | | V/μs |
| COMP Voltage Swing | $I_{COMP}$(source) = 2 mA | $V_{maxCOMP}$ | 2.6 | 3 | | V |
| | $I_{COMP}$(sink) = 2 mA | $V_{minCOMP}$ | | 0.75 | 0.89 | |
| FB Bias Current | $V_{FB}$ = 0.6 V | $I_{FB}$ | –100 | | 100 | nA |
| COMP Max Sourcing | $V_{FB}$ = 0.5 V | $I_{COMP(source)}$ | 18 | | | mA |
| COMP Max Sinking | $V_{FB}$ = 0.7 V | $I_{COMP(sinking)}$ | 10 | | | mA |
| **HIGH–SIDE MOSFET** | | | | | | |
| Drain–to–Source ON Resistance | BST – SW = 5 V, $T_A$ = $T_J$ = 25°C | $R_{ON\_H}$ | | 10.5 | | mΩ |
| **LOW–SIDE MOSFET** | | | | | | |
| Drain–to–Source ON Resistance | $V_{CC}$ = 5 V, $T_A$ = $T_J$ = 25°C | $R_{ON\_L}$ | | 5.2 | | mΩ |
| **PROTECTIONS** | | | | | | |
| Over Current Threshold | High–side Current Limit | $I_{LMT\_HS}$ | 11 | 13 | 16 | A |
| | Low–side Current Limit | $I_{LMT\_LS}$ | 10 | 12 | 15 | |
| Negative Over Current Threshold | Low–side negative current limit | $I_{LMT\_LS\_NEG}$ | | –6 | –10 | A |
| Under Voltage Protection (UVP) Threshold | Voltage from FB to GND | $V_{UVTH}$ | | 350 | | mV |
| Under Voltage Protection (UVP) Hysteresis | | $V_{UVHYS}$ | | 20 | | mV |
| Under Voltage Protection (UVP) Debounce Time | | $t_{D\_UVTH}$ | | 2 | | μs |
| Over Voltage Protection (OVP) Threshold | Voltage from FB to GND | $V_{OVTH}$ | | 750 | | mV |
| Over Voltage Protection (OVP) Hysteresis | | $V_{OVHYS}$ | | 30 | | mV |
| Over Voltage Protection (OVP) Debounce Time | | $t_{D\_OVTH}$ | | 1 | | μs |
| Thermal Shutdown (TSD) Threshold | (Note 5) | $T_{sd}$ | | 133 | | °C |
| Recovery Temperature Threshold | (Note 5) | $T_{rec}$ | | 116 | | °C |
| **BOOTSTRAP** | | | | | | |
| On Resistance of Rectifier Switch | $V_{VCC}$ = 5 V, Id = 2 mA, $T_A$ = $T_J$ = 25°C | $R_{BST}$ | | 40 | | Ω |
| Rectifier Switch Leakage Current | | $I_{lkgBST}$ | | | 1.1 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Not for external usage
5. Guaranteed by Design and/or Characterization. Not Production Tested
6. For most applications, the observed off–time will be over–ridden by the 80% duty cycle limit.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 12 V, $V_{OUT}$ = 1.8 V, Fsw = 550 kHz, L = 1 μH (TDK, SPM6550T−1R0M100A), $C_{OUT}$ = 4x 47 μF + 0.1 μF, $T_A$ = 25°C, unless otherwise indicated.

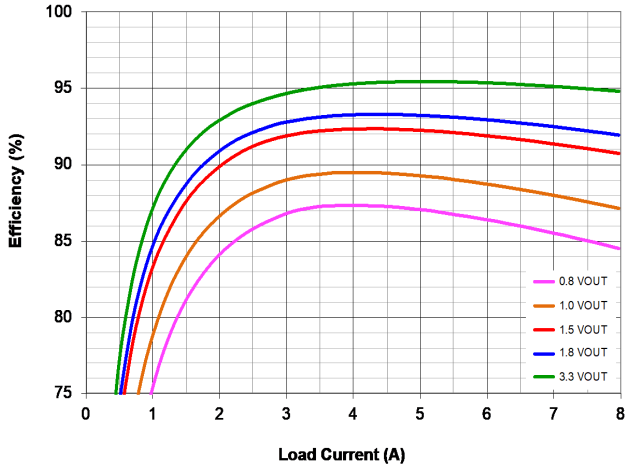



**Figure 3. Efficiency vs. Load Current and Output Voltage**

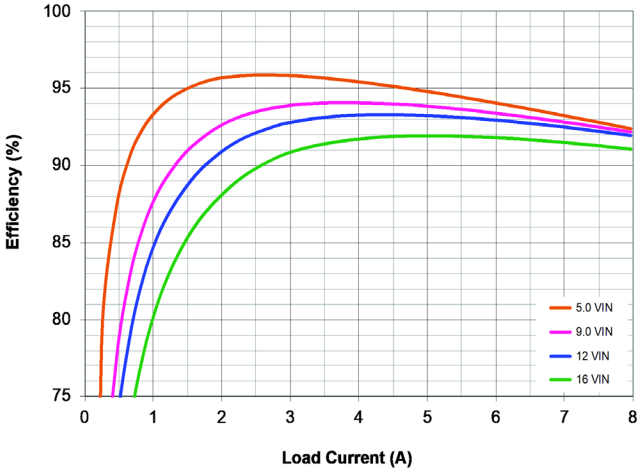



**Figure 4. Efficiency vs. Load Current and Input Voltage**

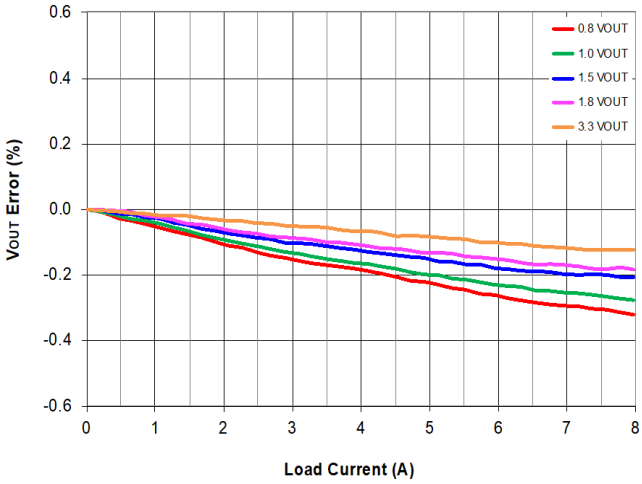



**Figure 5. Load Regulation**

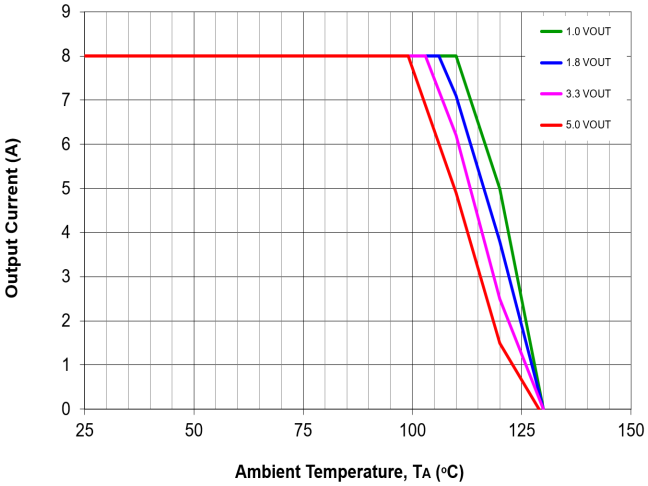



**Figure 6. Thermal Safe Operating Area, No Airflow, PCB: 2 oz. Cu**

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 12 V, $V_{OUT}$ = 1.8 V, Fsw = 550 kHz, L = 1 μH (TDK, SPM6550T−1R0M100A), $C_{OUT}$ = 4x 47 μF + 0.1 μF, $T_A$ = 25°C, unless otherwise indicated.

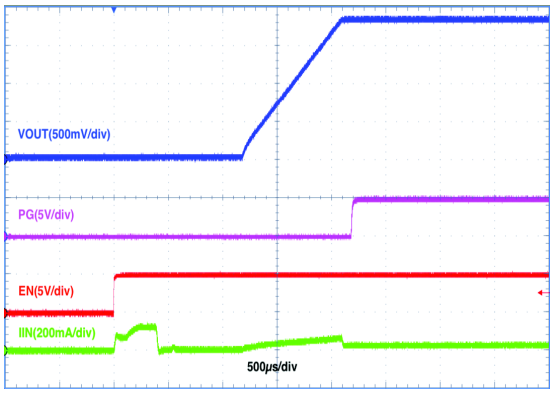



**Figure 7. Start−up, No Load**

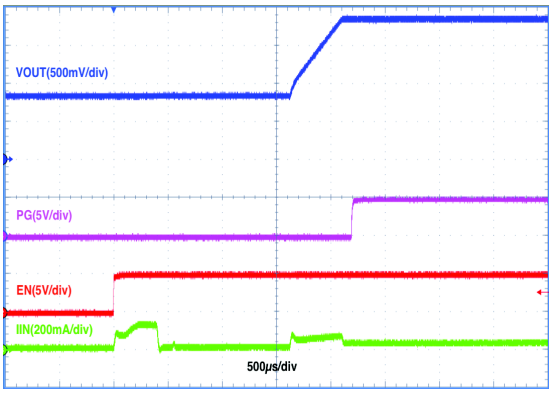



**Figure 8. Start−up With 50% Pre−bias**

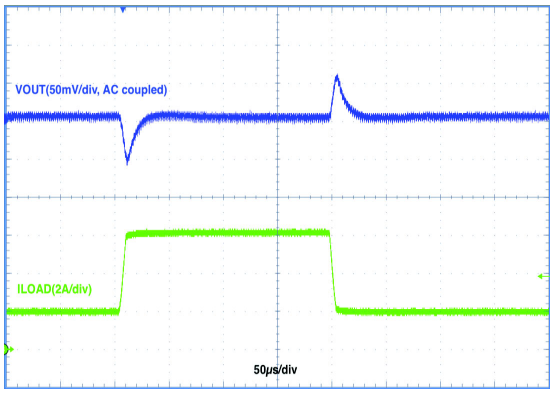



**Figure 9. Load Transient, 2 A <−> 6 A, Slew Rate = 1 A/μs**

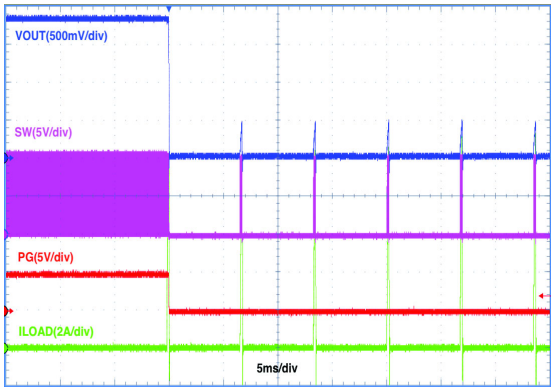



**Figure 10. Over Current Protection, Hiccup Mode**

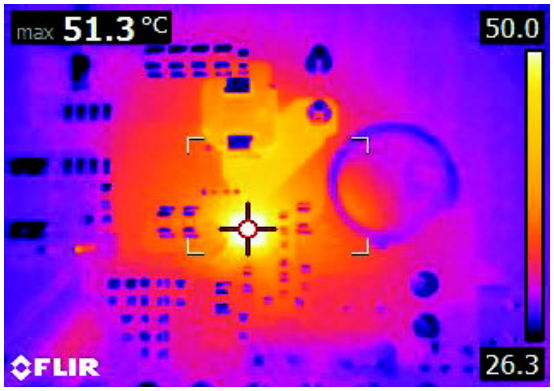



**Figure 11. Thermal Image, No Airflow, $I_{OUT}$ = 8 A, PCB: 2 oz. Cu**

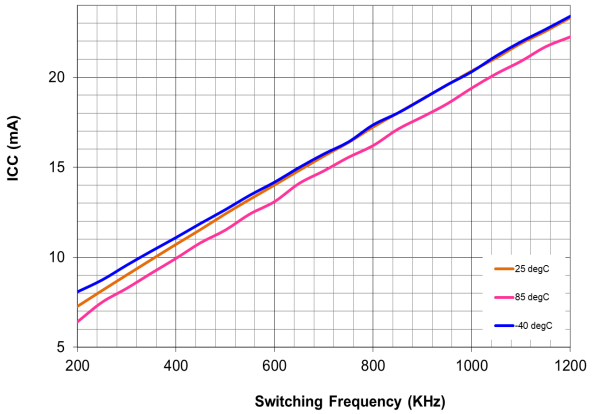



**Figure 12. $I_{CC}$ vs. Switching Frequency and Ambient Temperature**

## DETAILED DESCRIPTION

### General

NCP3237 is a single−phase synchronous buck converter with two integrated N−type power MOSFETs to provide a high−efficiency and compact−footprint power management solution. The device is able to deliver up to 8A output current over a wide output voltage range from 0.6 V to 0.8 × VIN. It has a wide input voltage range from 4.5 V to 16 V.

The NCP3237 features include resistor adjustable frequency input to optimize the output filter size, an enable and power good indicator for sequencing and an internal soft−start function during the initial power up. These devices offer safe start up into a pre−biased output condition and offer multiple protection features including cycle−by−cycle high side and low side over−current limiting, output over−voltage protection (OVP), under voltage protection (UVP) and thermal shutdown protection (TSD). During over−current, over−voltage and under−voltage conditions, these devices enter hiccup protection.

### Operation

NCP3237 operates in forced CCM. In forced CCM, the high−side FET is ON during the on−time and the low−side FET is ON during the entire off−time. The switching is synchronized to an internal clock thus the switching frequency is fixed.

### Reference Voltage

The NCP3237 incorporates an internal reference that allows output voltage to be as low as 0.6 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

### Oscillator Ramp

The ramp waveform is a saw tooth formed at the PWM frequency with a peak−to−peak amplitude of VIN/8, offset from AGND by typically 1.0 V. The PWM duty cycle is limited to a typical 80%, allowing the bootstrap capacitor to charge during each cycle.

### Soft Start

The NCP3237 incorporates a soft start function. The output starts to ramp up following a system reset period ($T_{RST}$) after the device is enabled. Please see Figure 13 for the timing of the soft start. The device is able to start up smoothly with an output pre−biased voltage up to the target VOUT level.

### Under−Voltage Lockout (UVLO)

UVLO engages when $V_{CC}$ falls below $V_{CCUV}$ and the device shuts down. Once $V_{CC}$ rises above $V_{CCOK}$, a soft−start is initiated following BST refresh cycles ($T_{BST}$).

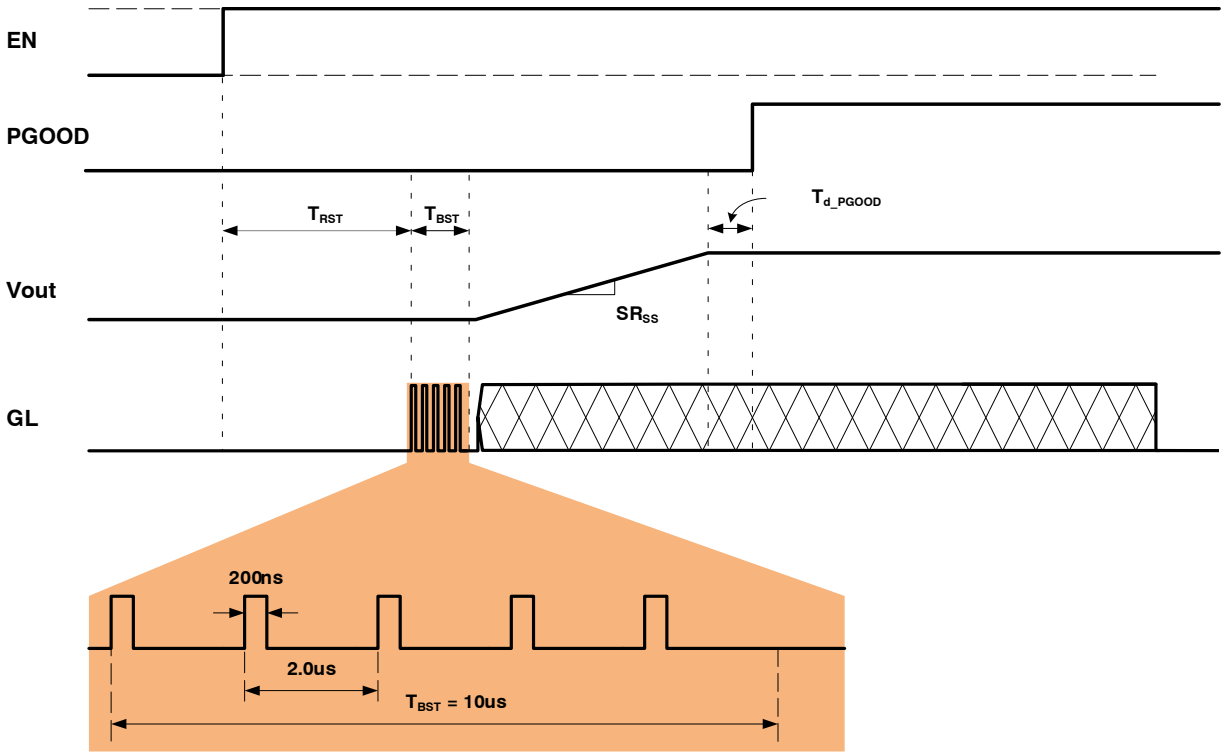



**Figure 13. Timing Diagram of Soft Start**

### High−side MOSFET Over−Current Protection (HSOCP)

The NCP3237 protects the converter from high−side MOSFET over currents by employing a cycle−by−cycle peak current limit. The high−side MOSFET current is monitored by differential voltage sensing between VIN pin and SW pin, and compared with the internal OCP limit value $I_{LMT\_HS}$. If it reaches the $I_{LMT\_HS}$ level on any given clock cycle, the cycle terminates to prevent the current from increasing any further.

If HSOCP occurs for more than 3 consecutive switching cycles, the device shuts down and enters hiccup mode. To prevent nuisance trips, the internal HSOCP counter adds 2 for a HSOCP event, and subtracts 1 for every normal switching cycle (not LSOCP cycles). The counter resets when it counts up to 6 and the device shuts down. Upon shut down, the high side switch is held off, while the low side switch remains on until a ZCD is detected. This is to prevent the switching node going very negative which can cause malfunction. PGOOD is pulled low upon ZCD detection.

The device implements a 6 soft−start cycle hiccup time−out after PGOOD goes low. After the time−out, it implements BST refresh cycles before a normal soft−start attempt. Please see Figure 14 for the timing diagram.

The device may enter into under voltage protection before OCP hiccup happens if the output voltage drops down very fast.

HSOCP detection starts from the beginning of soft−start, and ends in shutdown and idle time of hiccup mode.

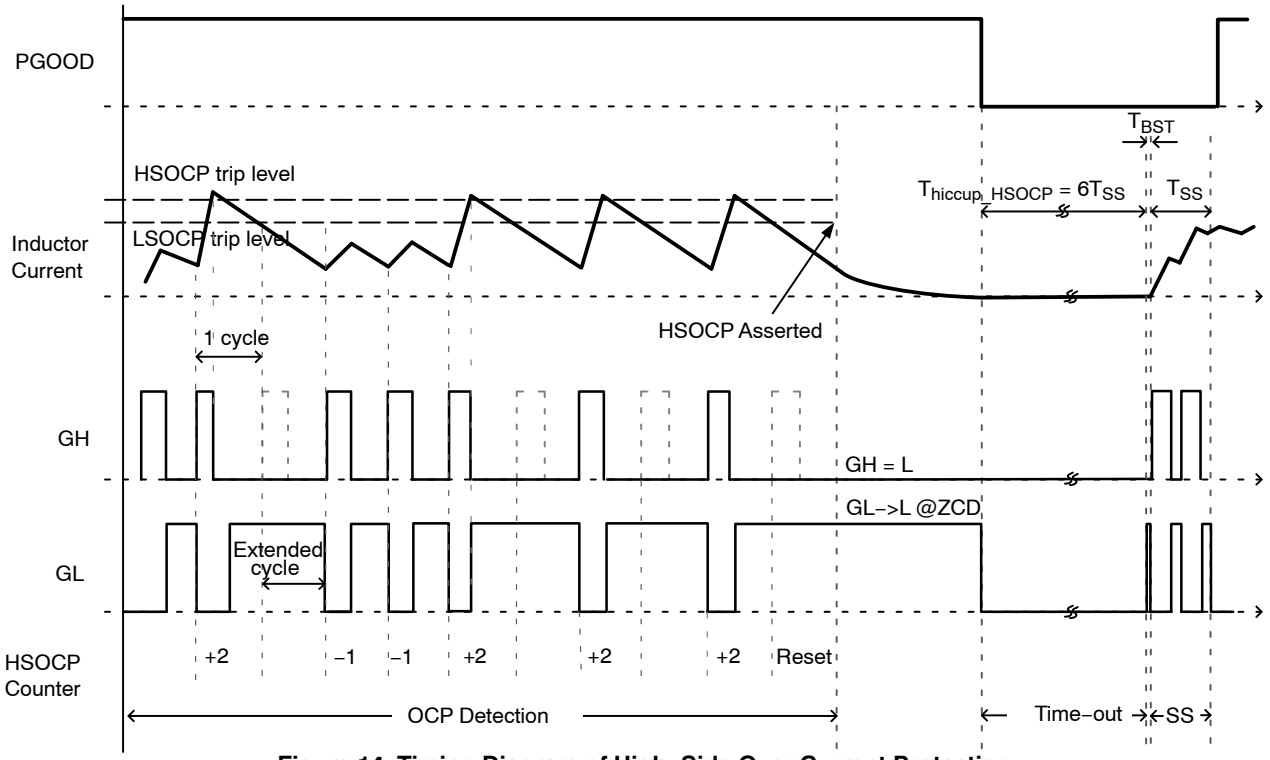



**Figure 14. Timing Diagram of High−Side Over Current Protection**

### Low−side MOSFET Over−Current Protection (LSOCP)

The NCP3237 protects the converter from low−side MOSFET over current utilizing a cycle−by−cycle current limit. The low−side MOSFET current is monitored by voltage sensing between SW pin and PGND pin, and compared with the internal OCP limit value $I_{LMT\_LS}$. If it is higher than $I_{LMT\_LS}$ level on any given clock cycle, the high−side MOSFET will not be turned on and the low−side MOSFET stays on for the next switching cycle. The high−side MOSFET is turned on again only when the low−side current is below the OCP limit value during the previous switching cycle.

If LSOCP occurs for more than 4 consecutive switching cycles, the device shuts down and enters hiccup mode. To prevent nuisance trips, the internal LSOCP counter adds 2 for a LSOCP event, and subtracts 1 for every normal switching cycle (not extended cycles). The counter resets when it counts up to 8 and the device shuts down. Upon shut down, the high side switch keeps off all the time, while the low side switch keeps on until a ZCD is detected. This is to prevent the switching node going very negative which can cause malfunction. PGOOD is pulled low upon ZCD detection.

The device implements a 4 soft−start cycle time−out after PGOOD goes low. After the time−out, it implements BST refresh cycles before a normal soft−start attempt. Please see Figure 15 for the timing diagram.

The device may enter into under voltage protection before OCP hiccup happens if the output voltage drops down very fast.

LSOCP detection starts from the beginning of the soft start time, and ends in shutdown and idle time of hiccup mode.

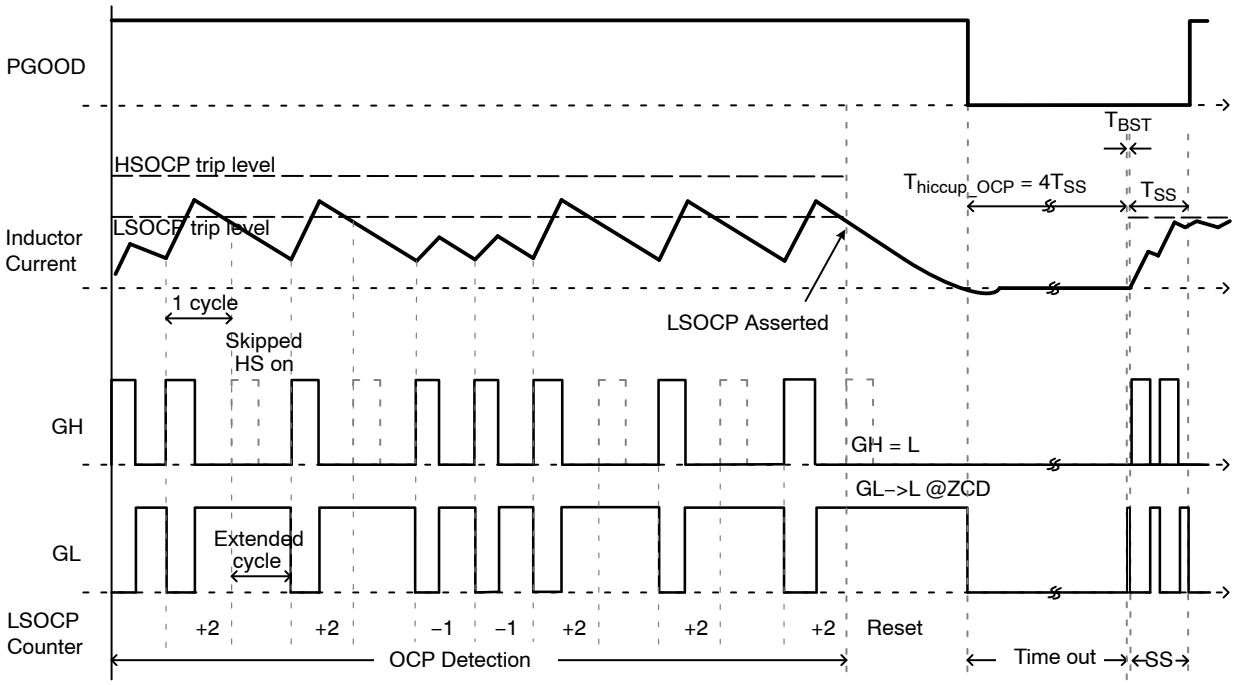



**Figure 15. Timing Diagram of Low−Side Over Current Protection**

### Under Voltage Protection (UVP)

NCP3237 monitors the FB voltage to detect a UVP event. A UVP is asserted once FB voltage drops below $V_{UVTH}$ for more than UVP debounce time ($t_{D\_UVTH}$). When UVP is asserted, it turns off the high side FET, and keep the low−side FET on until a ZCD is detected. PGOOD is pulled low upon ZCD detection. It implements a 5 soft−start cycle time−out from when PGOOD goes low. After the time−out, it implements BST refresh cycles before a normal soft−start attempt. Please see Figure 16 for the timing diagram.

UVP detection starts when PGOOD delay $T_{d\_PGOOD}$ is expired right after a soft start, and ends in shutdown and idle time of hiccup mode.

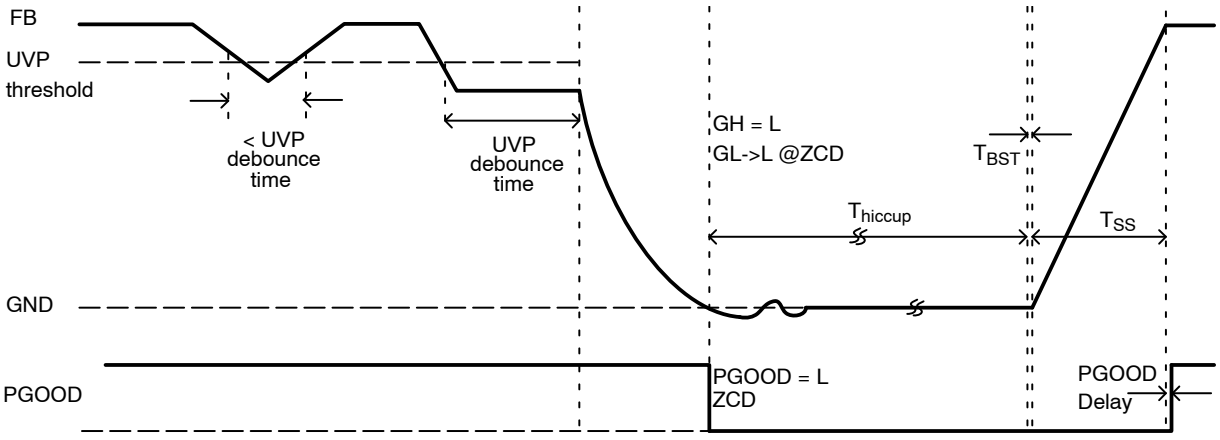



**Figure 16. Timing Diagram of Non−latched Under Voltage Protection**

### Over Voltage Protection (OVP)

During normal operation the output voltage is monitored at the FB pin. If FB voltage exceeds the OVP threshold ($V_{OVTH}$)for more than $t_{D\_OVTH}$, OVP is triggered and PGOOD is pulled low. In the meanwhile, the high−side MOSFET is latched off and the low−side MOSFET is turned on. After the OVP trips, the DAC immediately goes down to zero. The low−side MOSFET current would become negative during OVP. If the low−side negative current limit is exceeded, the low−side MOSFET is turned off immediately. In this scenario, both MOSFETs are off. After negative over current protection trips, the low−side MOSFET turns off and stays off for at least 640 ns. If the OVP is still not cleared, the low−side MOSFET will turn on again. The OVP threshold is set to a fixed value of Vovth.

After the OVP gets asserted, NCP3237 implements an 8 normal soft−start cycle time−out. Then it is followed by BST refresh cycles before a normal soft−start attempt. Please see Figure 17 for the timing diagram.

OVP detection starts from the beginning of the soft start and ends in shutdown and idle time of hiccup mode.

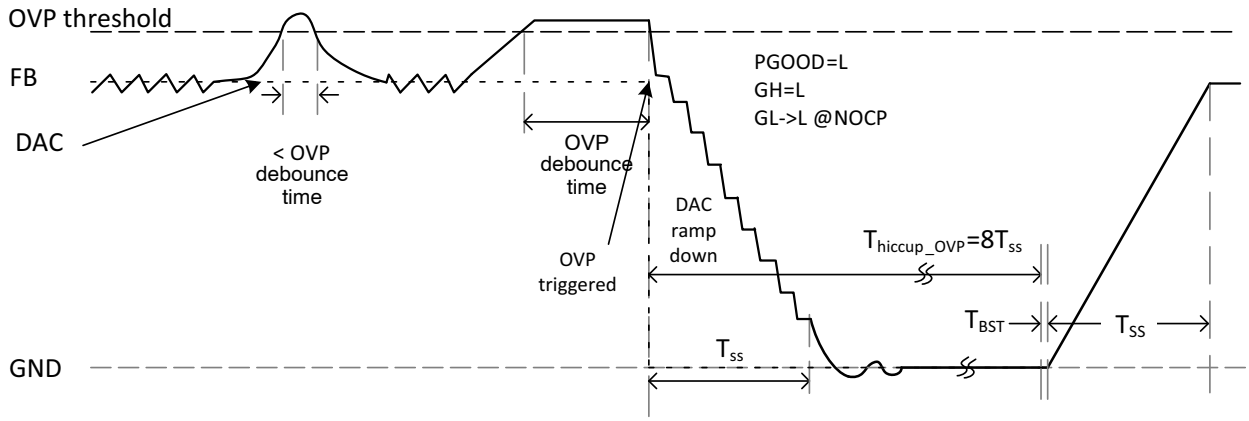



**Figure 17. Function of Non Latch−Off Over Voltage Protection**

### Thermal Shutdown (TSD)

The NCP3237 has an internal thermal shutdown protection to protect the device from overheating in an extreme case that the die temperature exceeds Tsd. TSD detection starts from the beginning of soft−start. Once the thermal protection is triggered, the whole chip shuts down. If the temperature drops below Trec, the system automatically recovers and a normal soft−start sequence follows.

### Power Good Monitor (PGOOD)

The NCP3237 provides a window comparator to monitor the voltage at FB pin. The open−drain PG goes high when the device is operating in a normal operating condition (no UVLO, UVP, OVP, OCP or TSD faults). Connect a pull up resistor to VCC for simplicity or to an external voltage to interfacing to another logic rail such as 3.3 V. When a fault occurs, PGOOD goes low. Choose a pull up to limit the sink current to 4 mA. During soft start, PGOOD stays low until the feedback voltage is within the specified range for about 100 μs. The PGOOD pin de−asserts as the EN pin pulled low for 1 μs. For an under−voltage event on VCC, PGOOD goes low immediately.

### Switching Frequency

The NCP3237 provides programmable switching frequency in the range of 300 kHz to 1.2 MHz. The switching frequency can be programmed through the resistor from the FSET pin to AGND. The switching frequency is calculated by:

$$F_{SW} = \left(\frac{40\ k\Omega}{R_{FSET}}\right) \cdot 550\ kHz$$

The default switching frequency is set at 550 kHz typical with a 40.2 kΩ resistor. 1% resistors are recommended to be used.

### External VCC Supply

The NCP3237 can operate with an external voltage supply to the VCC pin in place of the internal LDO. When operating with $V_{IN}$ > 5 V, a constant voltage greater than 5.15 V (recommended 5.2 V) must be supplied to the VCC pin to override the internal LDO output. To prevent forward biasing the LDO body diode, $V_{IN}$ must be always greater than the external VCC.

## LAYOUT GUIDELINES

### Electrical Layout Considerations

Good electrical layout is a key to ensure proper operation, high efficiency, and noise reduction.

- **Power Paths**: Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- **Power Supply Decoupling**: The device should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low−ESL MLCC is placed very close to VIN and PGND pins.
- **VCC Decoupling**: Place decoupling caps as close as possible to VCC pin. The filter resistor at VCC pin should be not higher than 4.7 Ω to prevent large voltage drop.
- **Output Decoupling**: The output capacitors should be as close as possible to the load. If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
- **Switching Node**: SW node should be a copper pour, but compact because it is also a noise source.
- **Bootstrap**: The bootstrap cap and an option resistor need to be very close and directly connected between pin 17 (BST) and pin 16 (SW).
- **Ground**: It would be good to have separated ground planes for PGND and AGND and connect the AGND planes to the exposed pad GND through vias.
- **Voltage Sense**: Route a “quiet” path for the output voltage sense. AGND could be used as a remote ground sense when differential sense is preferred.
- **Compensation Network**: The compensation network should be close to the NCP3237. Keep FB trace short to minimize it capacitance to ground.

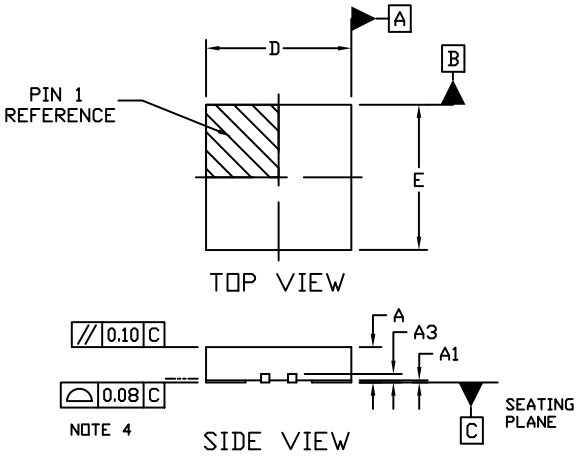
### Thermal Layout Considerations

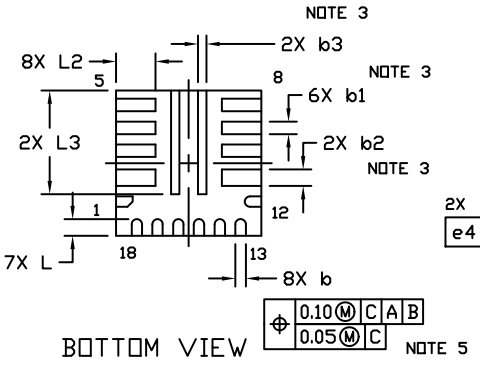
Good thermal layout helps high power dissipation from a small−form factor VR with reduced temperature rise.

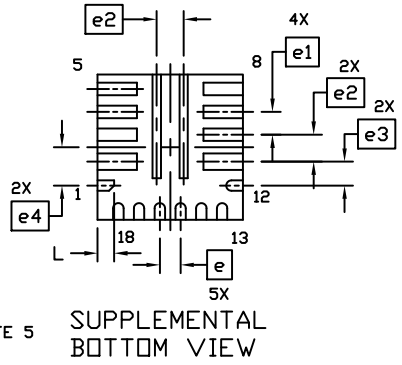
- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

**QFN18 3.5x3.5, 0.5P**
CASE 485FR
ISSUE O

DATE 28 MAR 2018



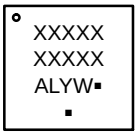




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO ALL OF THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE TERMINALS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM.. | MAX. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.20 | 0.25 | 0.30 |
| b1 | 0.25 | 0.30 | 0.35 |
| b2 | 0.35 | 0.40 | 0.45 |
| b3 | 0.15 | 0.20 | 0.25 |
| D | 3.40 | 3.50 | 3.60 |
| E | 3.40 | 3.50 | 3.60 |
| e | 0.50 BSC | | |
| e1 | 0.55 BSC | | |
| e2 | 0.65 BSC | | |
| e3 | 0.575 BSC | | |
| e4 | 0.925 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| L2 | 0.85 | 0.95 | 1.05 |
| L3 | 2.40 | 2.50 | 2.60 |

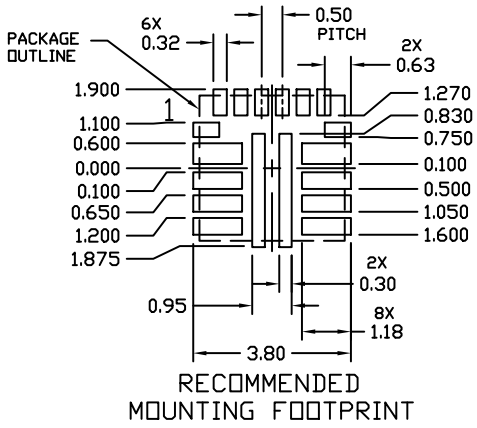
**GENERIC MARKING DIAGRAM***




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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