International
IOR Rectifier

IRSM808-105MH

Half-Bridge IPM for Small Appliance Motor Drive Applications

μIPM™

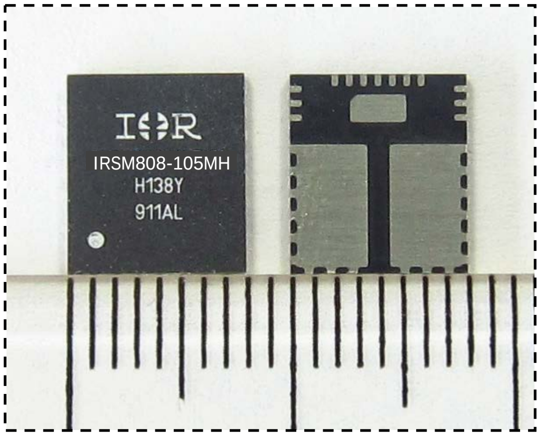
10A, 500V

Description

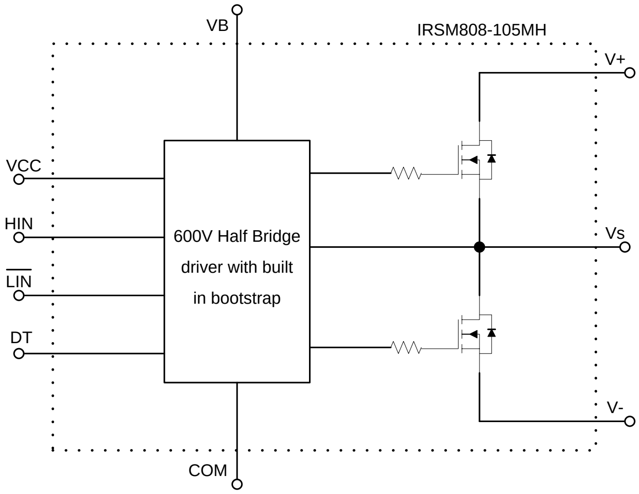
IRSM808-105MH is a 10A, 500V half-bridge module designed for advanced appliance motor drive applications such as energy efficient fans and pumps. IR's technology offers an extremely compact, high performance half-bridge topology in an isolated package. This advanced IPM offers a combination of IR's low $R_{DS(on)}$ Trench FREDFET technology and the industry benchmark half-bridge high voltage, rugged driver in a small PQFN package. At only 8x9mm and featuring integrated bootstrap functionality, the compact footprint of this surface-mount package makes it suitable for applications that are space-constrained. IRSM808-105MH functions without a heat sink.

Features

- Integrated gate drivers and bootstrap functionality
- Suitable for sinusoidal modulation applications
- Low $R_{DS(on)}$ Trench FREDFET
- Under-voltage lockout for both channels
- Matched propagation delay for all channels
- Optimized dV/dt for loss and EMI trade offs
- 3.3V input logic compatible
- Active high HIN and active low LIN
- Motor Power range 80-200W
- Isolation 1500V_{RMS} min
- ROHS compliant



Internal Electrical Schematic



Ordering Information

Orderable Part Number	Package Type	Form	Quantity
IRSM808-105MH	PQFN 8x9mm	Tray	1300
IRSM808-105MHTR	PQFN 8x9mm	Tape and Reel	2000

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested at manufacturing. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance rating is measured under board mounted and still air conditions.

Symbol	Description	Min	Max	Unit
BV_{DSS}	MOSFET Blocking Voltage	---	500	V
I_O	Output DC Current per MOSFET @ T_C=25°C	---	10	A
P_d	Power dissipation per MOSFET @ T_C =100°C	---	55	W
T_J (MOSFET & IC)	Maximum Operating Junction Temperature	---	150	°C
T_L	Lead temperature (soldering 30 seconds)	---	260	°C
T_S	Storage Temperature Range	-40	150	°C
V_B	High side floating supply voltage	-0.3	VS + 20	V
V_S	High side floating supply offset voltage	VB - 20	VB +0.3	V
V_{CC}	Low Side fixed supply voltage	-0.3	20	V
V_{IN}	Logic input voltage LIN, HIN	-0.3	VCC+0.3	V
V_{ISO}	Isolation voltage (1min) (Note2)	---	1500	V_{RMS}

Note1: Calculated based on maximum junction temperature. Bond wires current limit is 3.5A. Note2: Characterized, not tested at manufacturing

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units	Conditions
V^+	Positive DC Bus Input Voltage	---	---	400	V	
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	(Note 3)	---	400	V	
$V_{B1,2,3}$	High Side Floating Supply Voltage	V_S+12	---	V_S+20	V	
V_{CC}	Low Side and Logic Supply Voltage	13.5	---	16.5	V	
V_{IN}	Logic Input Voltage	COM	---	V_{CC}	V	
F_p	PWM Carrier Frequency	---	---	20	kHz	

For proper operation the module should be used within the recommended conditions. All voltages are absolute referenced to COM. The V_S offset is tested with all supplies biased at 15V differential.
Note 3: Logic operational for V_s from COM-8V to COM+500V. Logic state held for V_s from COM-8V to COM-V_{BS}.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS})=15V, T_J=25ºC, unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to COM

Symbol	Description	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	---	---	V	T_J=25°C, I_{LK}=3mA
I_{LKH}	Leakage Current of High Side FET's in Parallel	---	15	---	µA	T_J=25°C, V_{DS}=500V
I_{LKL}	Leakage Current of Low Side FET's in Parallel Plus Gate Drive IC	---	20	---	µA	T_J=25°C, V_{DS}=500V
$R_{DS(ON)}$	Drain to Source ON Resistance	---	0.58	0.8	Ω	T_J=25°C, V_{CC}=10V, Id = 6A
		---	1.60	---		T_J=150°C, V_{CC}=10V, Id = 6A (Note 4)
V_{SD}	Diode Forward Voltage	---	0.85	1.0	V	T_J=25°C, V_{CC}=10V, Id = 6A
$V_{HIN/LIN}$	Logic "1" input voltage for HIN & "0" for LIN	2.2	---	---	V	
$V_{HIN/LIN}$	Logic "0" input voltage for HIN & "1" for LIN	---	---	0.8	V	
V_{CCUV+}, V_{BSUV+}	V_{CC} and V_{BS} Supply Under-Voltage, Positive Going Threshold	8	8.9	9.8	V	
V_{CCUV-}, V_{BSUV-}	V_{CC} and V_{BS} supply Under-Voltage, Negative Going Threshold	7.4	8.2	9.0	V	
V_{CCUVH}, V_{BSUVH}	V_{CC} and V_{BS} Supply Under-Voltage Lock-Out Hysteresis	---	0.7	---	V	
I_{QBS}	Quiescent V_{BS} Supply Current V_{IN}=0V	---	45	70	µA	
I_{QCC}	Quiescent V_{CC} Supply Current V_{IN}=0V	---	1100	3000	µA	
I_{HIN+}	Input Bias Current V_{IN}=4V	---	5	20	µA	
I_{LIN-}	Input Bias Current V_{IN}=0V	---	1	2	µA	
R_{BR}	Internal Bootstrap Equivalent Resistor Value	---	200	---	Ω	T_J=25°C

Note 4: Characterized, not tested at manufacturing

MOSFET Avalanche Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
EAS	Single Pulse Avalanche Energy	---	216	---	mJ	T_J=25°C, L=3mH, VDD=100V, IAS=12A, TO-220 package.

Dynamic Electrical Characteristics

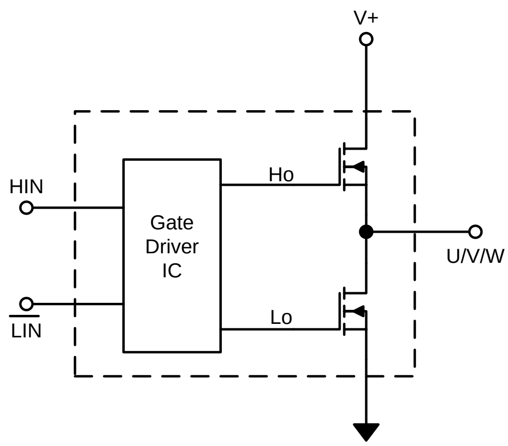
V_{BIAS} (V_{CC}, V_{BS})=15V, TJ=25ºC, unless otherwise specified. Driver only timing unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
T_{ON}	Input to Output Propagation Turn-On Delay Time	---	0.8	1.3	µs	I_D=1mA, V^+=50V
T_{OFF}	Input to Output Propagation Turn-Off Delay Time	---	0.8	1.3	µs	Gate Driver; V_{LIN}=0 & V_{HIN}=5V with no external deadtime
DT	Built-in Deadtime	0.9	1.3	---	µs	
$T_{FIL,IN}$	Input Filter Time (HIN, LIN)	---	300	---	ns	

Thermal and Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
$R_{th(J-B)}$	Thermal resistance, junction to mounting pad, each MOSFET	---	0.9	---	°C/W	Standard reflow-solder process
$R_{th(J-A)}$	Thermal resistance, junction to ambient, each MOSFET	---	40	---	°C/W	Mounted on 13.2cm2 of two-layer FR4 with 36 vias

Input-Output Logic Level Table



HIN	LIN	U,V,W
HI	HI	V+
LO	LO	0
HI	LO	* *
LO	HI	*

* V+ if motor current is flowing into VS, 0 if current is flowing out of VS into the motor winding
** Anti Shoot-through protection active (both HO and LO are OFF)

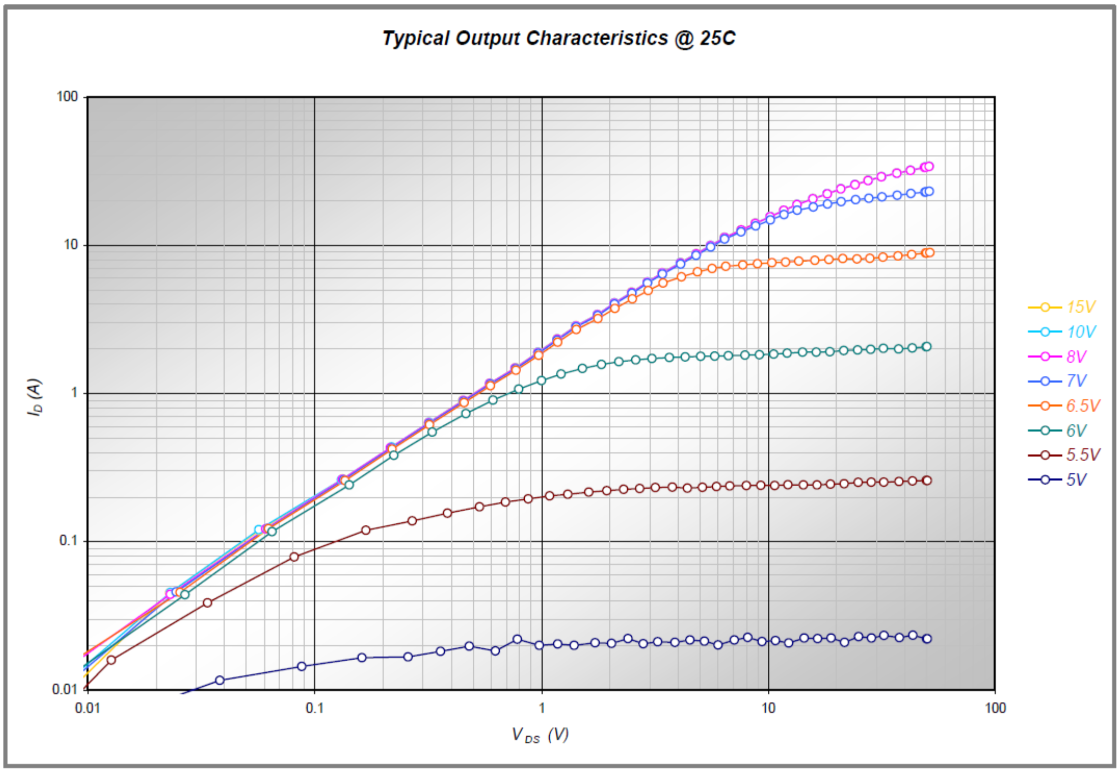


Figure 1 – MOS typical output characteristics at 25°C

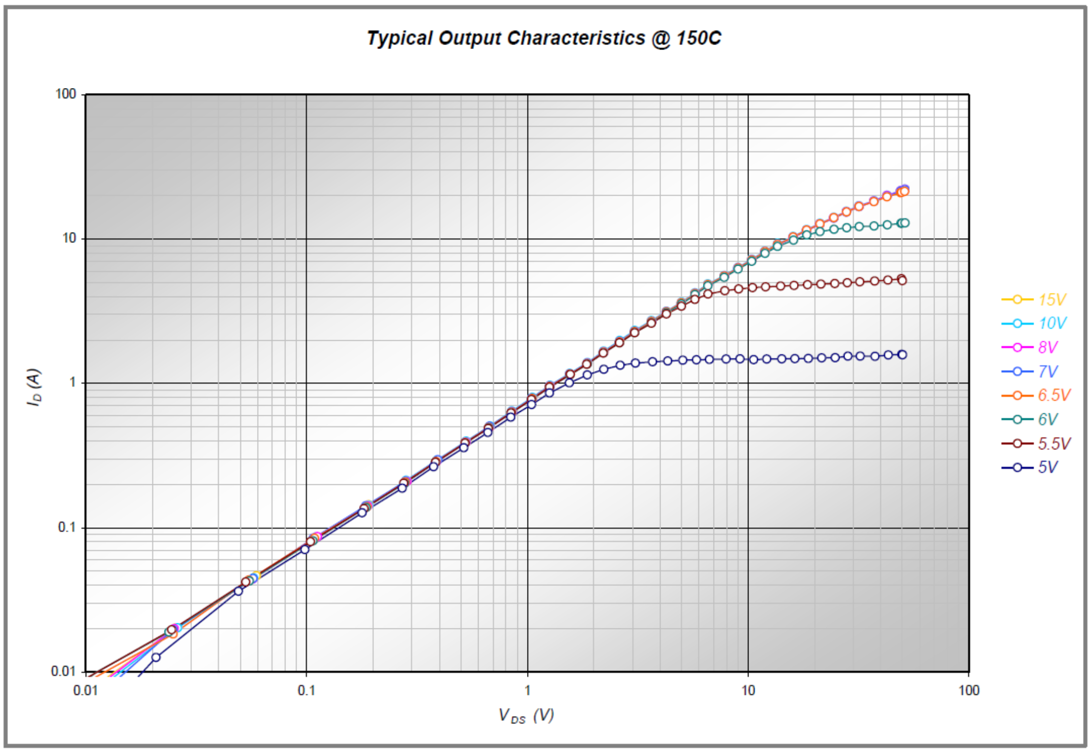


Figure 2 – MOS typical output characteristics at 25°C

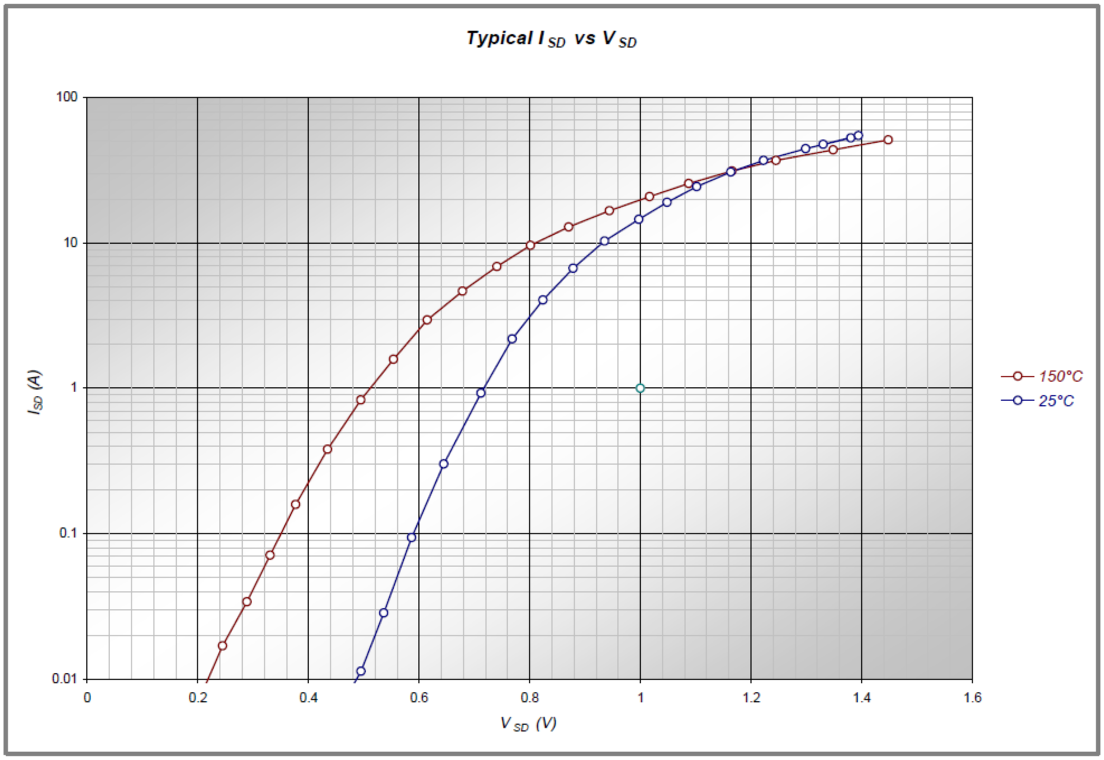


Figure 3 – MOS body diode typical characteristics at 25°C and 150°C

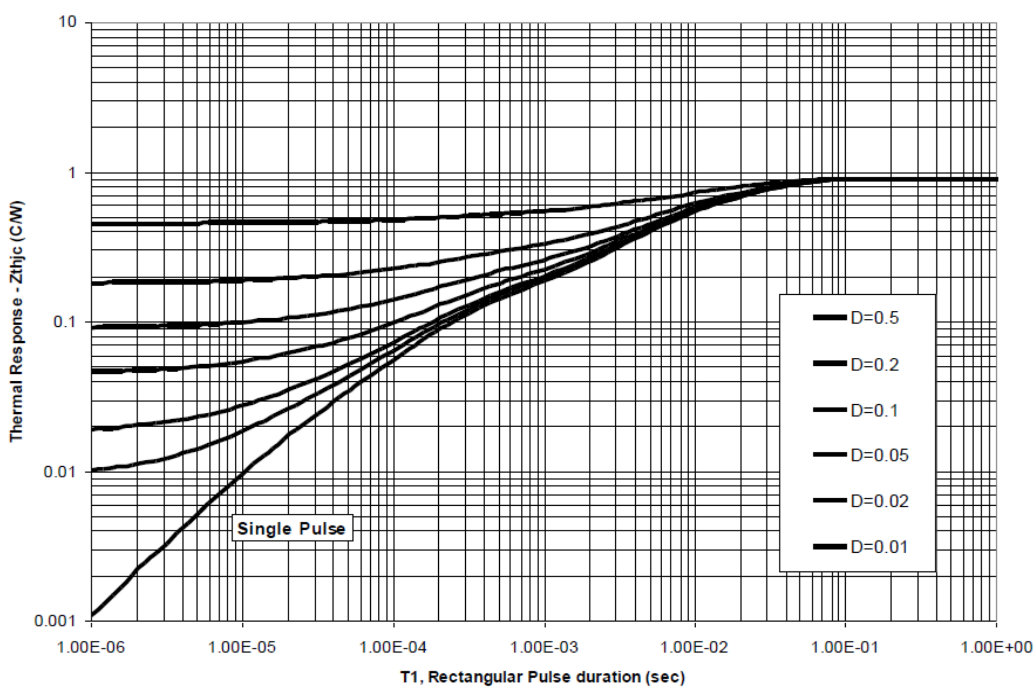


Figure 4 – module top surface typical thermal impedance

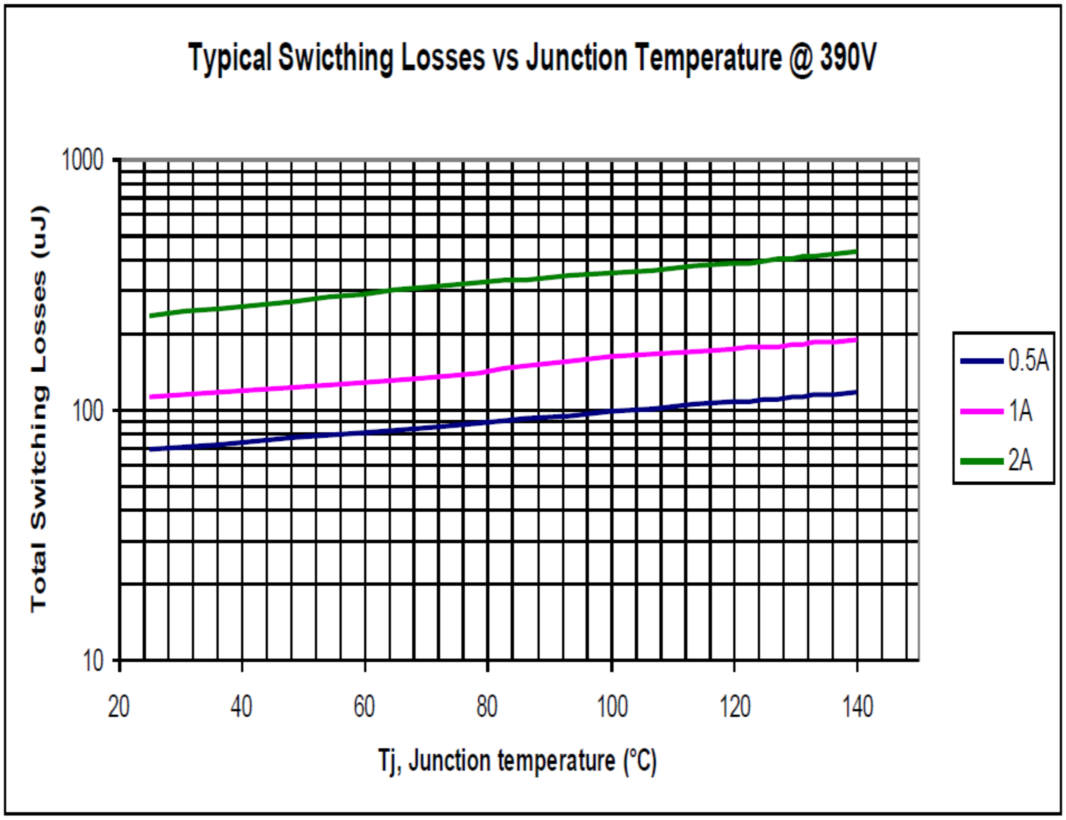


Figure 5 – Typical switching losses at 390V

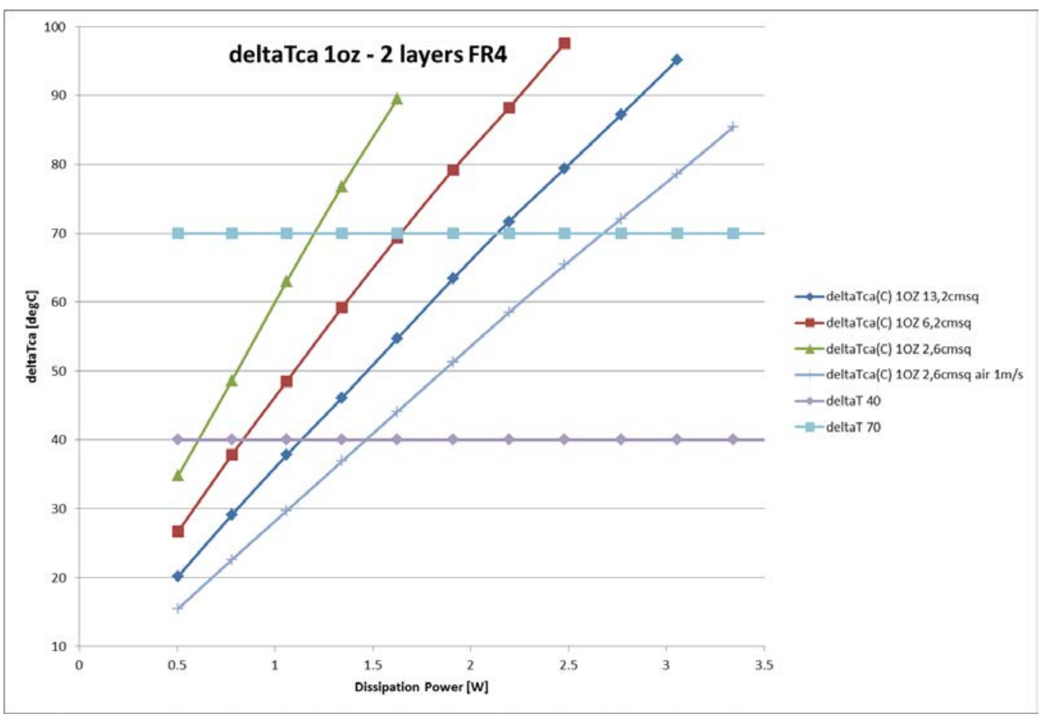


Figure 6 – typical delta temperature between case (no heat-sink) and ambient with 1oz FR4 vs. power dissipation in the module

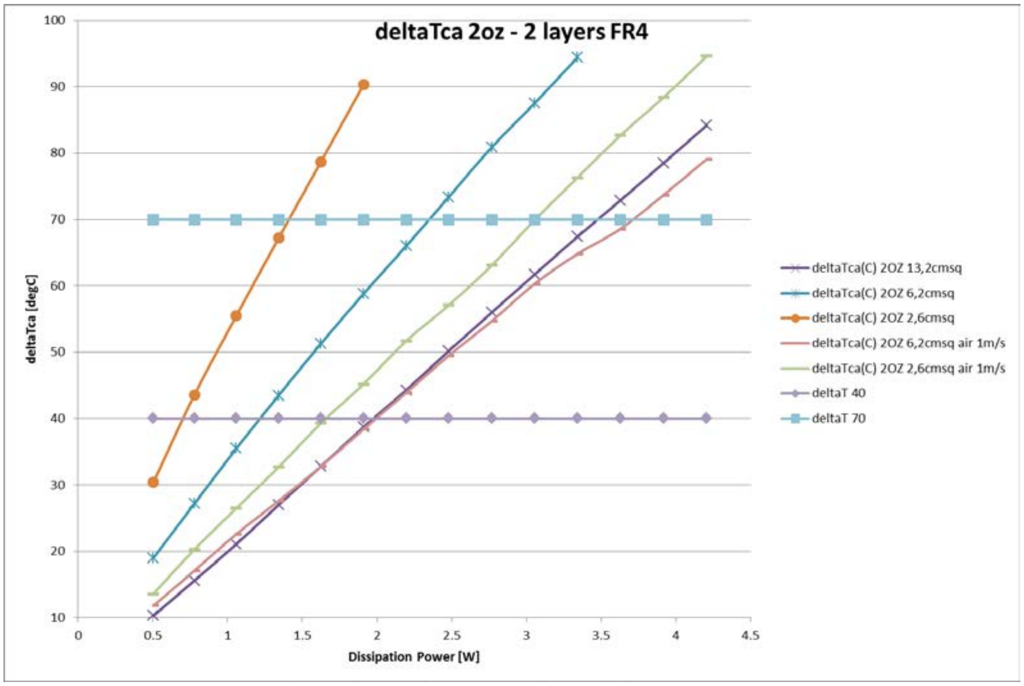


Figure 7 – typical delta temperature between case (no heat-sink) and ambient with 2oz FR4 vs. power dissipation in the module

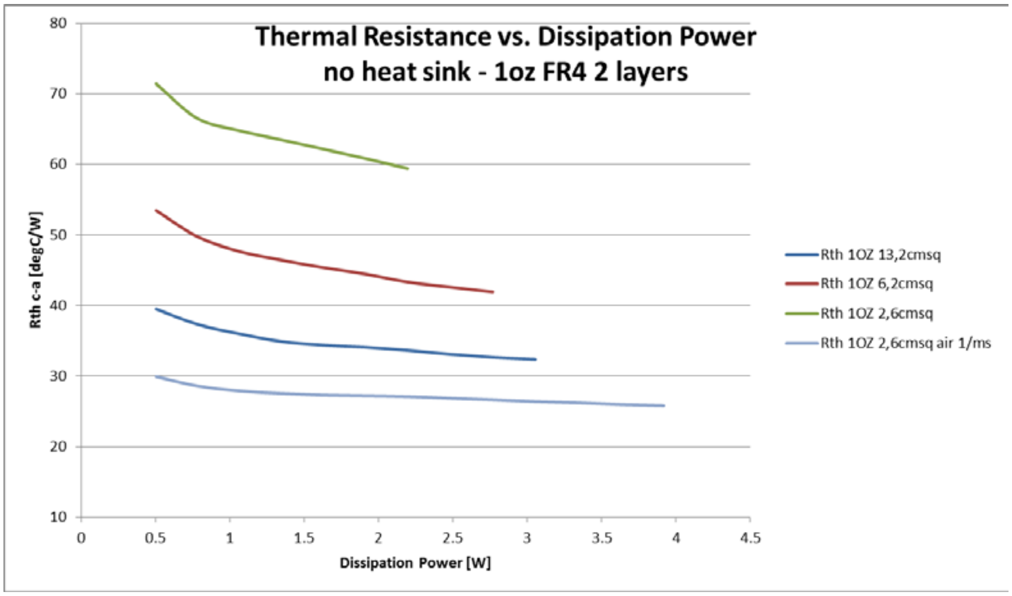


Figure 8 – Typical thermal resistance vs. power dissipation in the module (no heat sink) with 1oz FR4

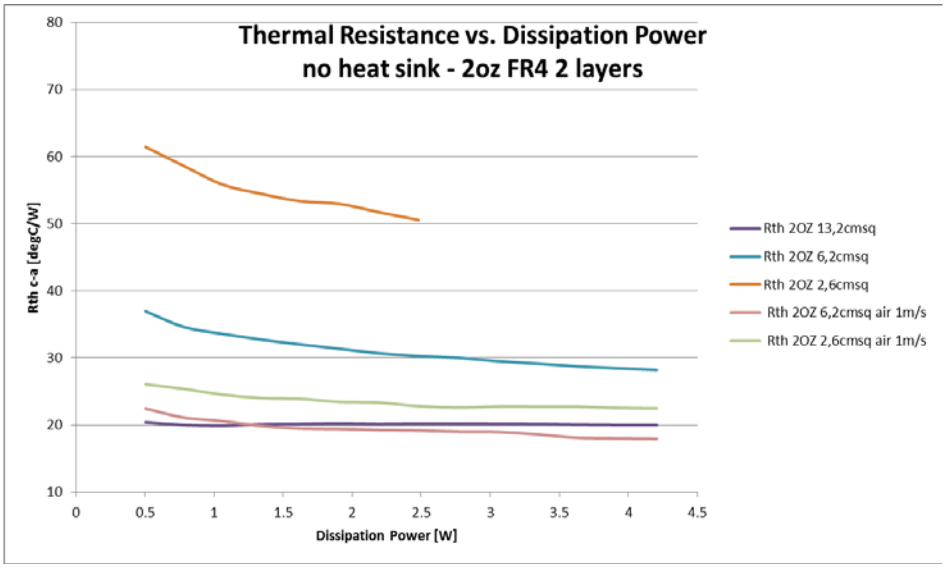


Figure 9 – Typical thermal resistance vs. power dissipation in the module (no heat sink) with 2oz FR4

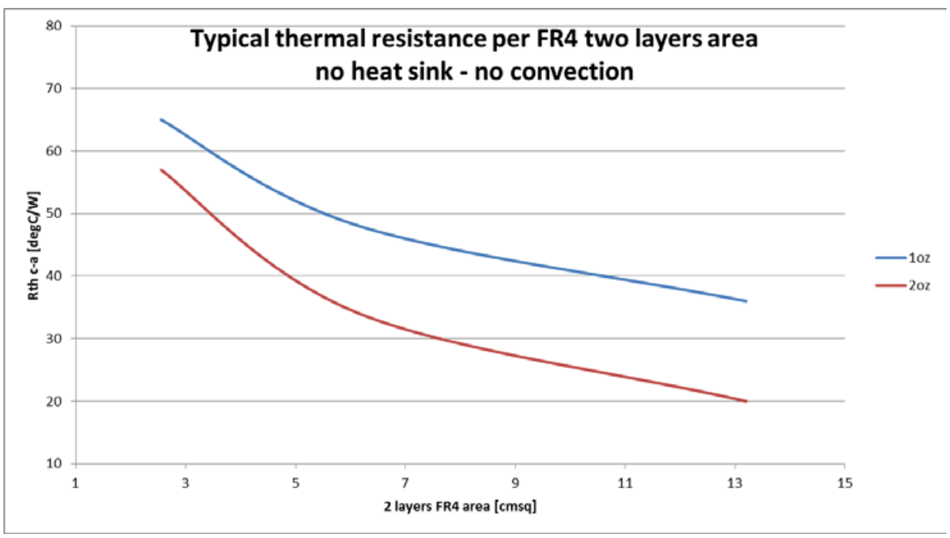


Figure 10 – Typical thermal resistance vs. area per module (no heat sink) with two layers FR4

Qualification†

Qualification Level		Industrial†† (per JEDEC JESD 47)
Moisture Sensitivity Level		MSL3††† (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 1C (per JEDEC standard ANSI/ESDA/JEDEC JS-001)
	Machine Model	Class A (per EIA/JEDEC standard JESD22-A115)
RoHS Compliant		Yes

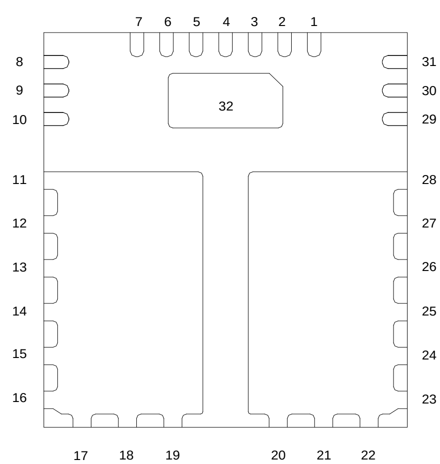
† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

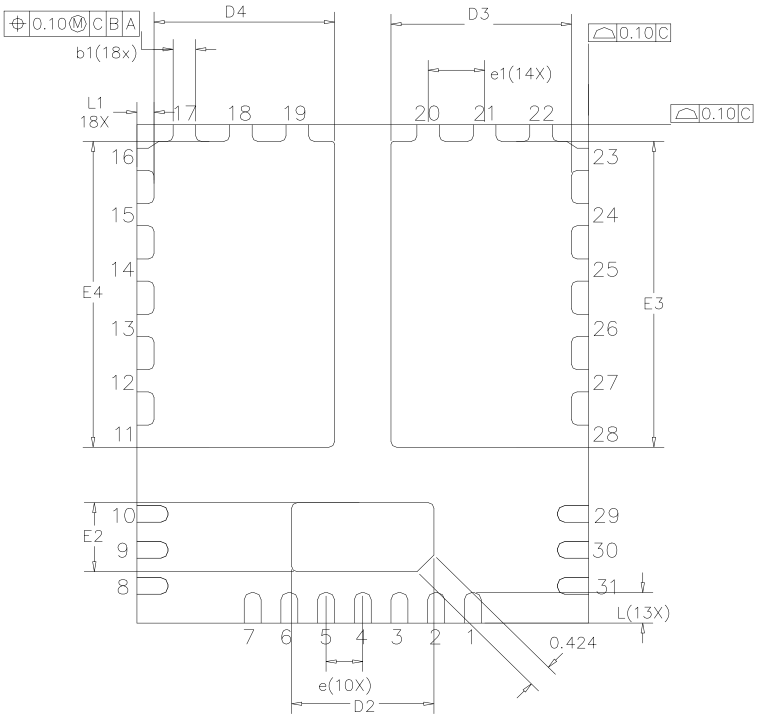
Module Pin-Out Description

Pin	Name	Description
1, 4, 7, 32	COM	Low Side Gate Drive Return
2	VCC	15V Gate Drive Supply
3	HIN	Logic Input for High Side (Active High)
5	$\overline{\text{LIN}}$	Logic Input for Low Side (Active Low)
6	DT	Dead time
8, 9, 10	V-	Low Side Source Connection
11 – 19	VS	Phase Output
20 – 28	V+	DC Bus
29 – 30	VS	Phase Output (-ve Bootstrap Cap Connection)
31	VB	High Side Floating Supply (+ve Bootstrap Cap Connection)



Exposed pad (Pin 32) has to be connected to COM for better electrical performance

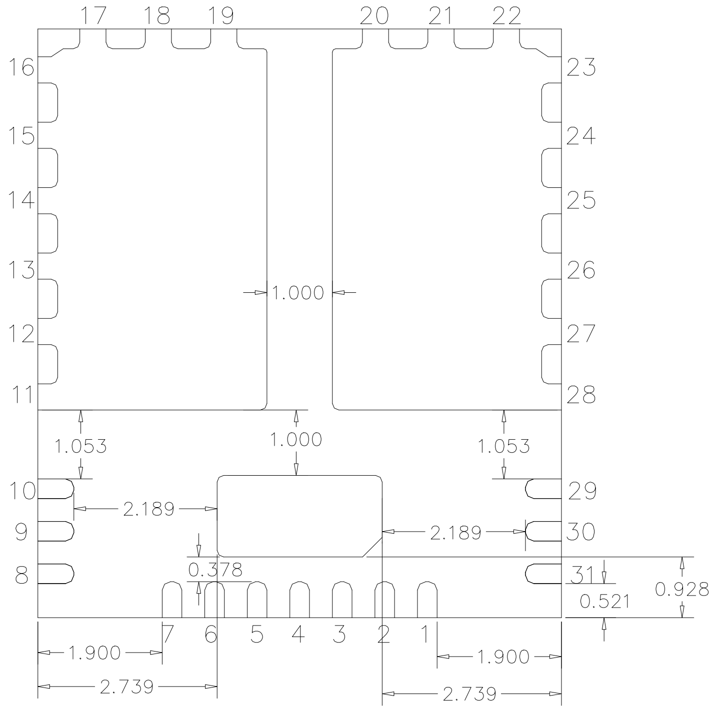
Package Outline IRSM808-105MH (Bottom View), 1 of 2



SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN.	NOM.	MAX.
A	0.800	0.900	1.000
A1	0.000	–	0.050
A3	0.203 REF.		
b	0.250	0.300	0.350
b1	0.350	0.400	0.450
D	7.900	8.000	8.100
E	8.900	9.000	9.100
D2	2.472	2.522	2.572
E2	1.197	1.247	1.297
D3	3.147	3.197	3.247
E3	5.472	5.522	5.572
D4	3.147	3.197	3.247
E4	5.472	5.522	5.572
e	0.650 BSC		
e1	1.000 BSC		
e2	1.403 BSC		
e3	2.318 BSC		
L	0.500	0.550	0.600
L1	0.253	0.303	0.353

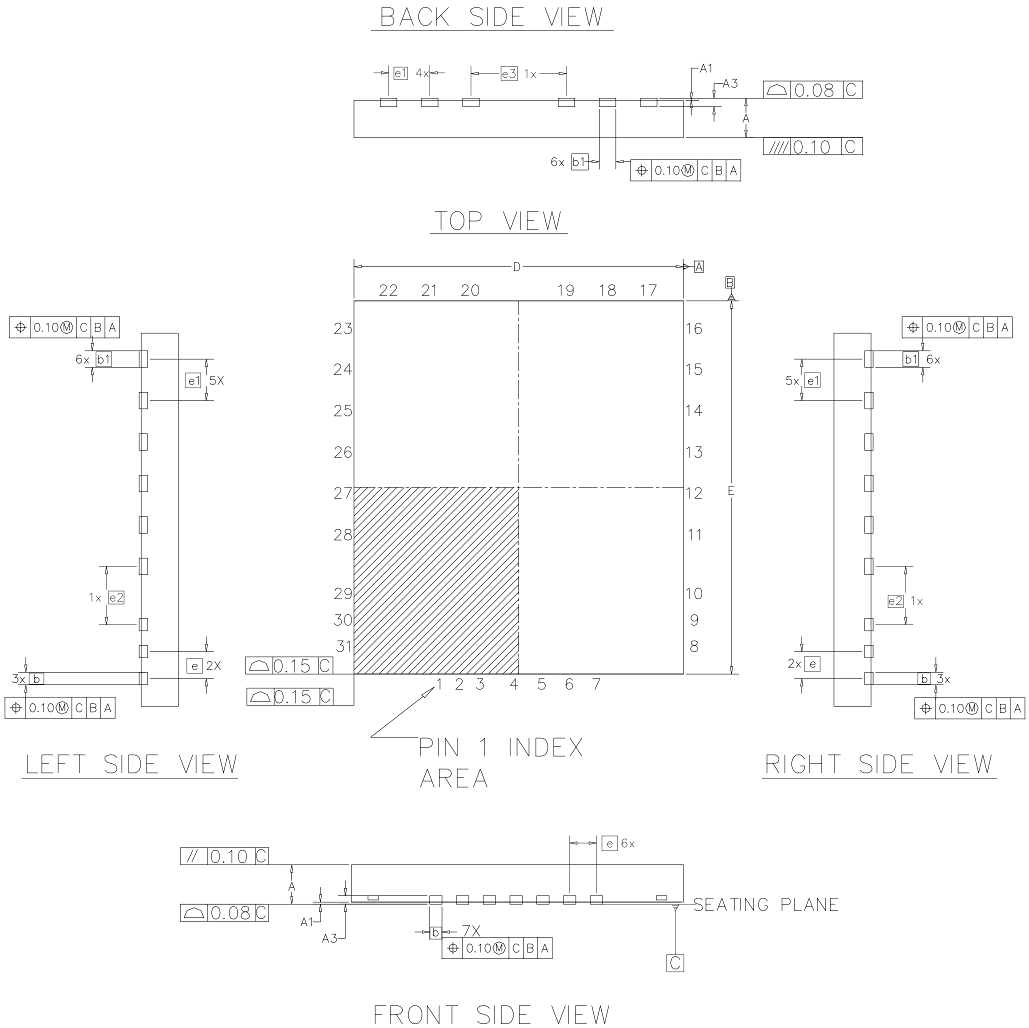
Dimensions in mm

Package Outline IRSM808-105MH (Bottom View), 2 of 2



Dimensions in mm

Package Outline IRSM808-105MH (Top & Side View)



SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN.	NOM.	MAX.
A	0.800	0.900	1.000
A1	0.000		0.050
A3	0.203 REF.		
b	0.250	0.300	0.350
b1	0.350	0.400	0.450
D	7.900	8.000	8.100
E	8.900	9.000	9.100
D2	2.472	2.522	2.572

E2	1.197	1.247	1.297
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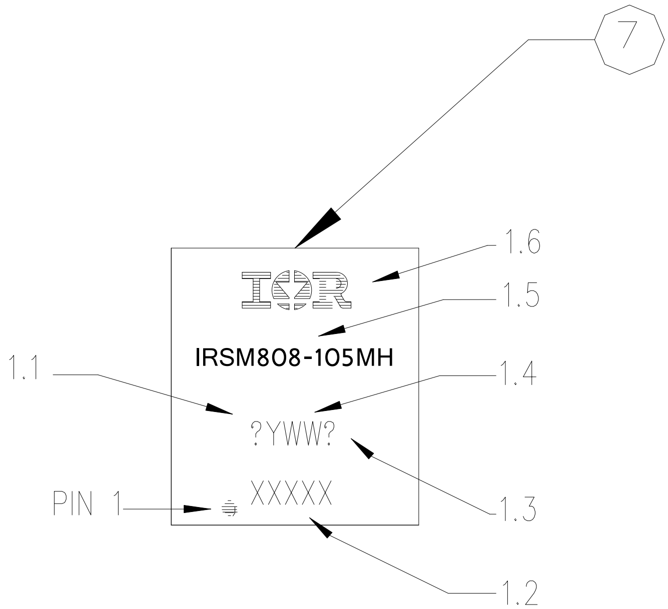
E3	5.472	5.522	5.572
D4	3.147	3.197	3.247
E4	5.472	5.522	5.572
e	0.650 BSC		
e1	1.000 BSC		
e2	1.403 BSC		
e3	2.318 BSC		
L	0.500	0.550	0.600
L1	0.253	0.303	0.353

Dimensions in mm

Top Marking



TOP MARKING

NOTES, MARKING:
1.1) SITE CODE: X
1.2) LAST 4 CHARACTER OF SPN/NANA CODE: XXXX
1.3) LEADFREE INDICATOR: P
1.4) DATE CODE: YWW
1.5) PART NUMBER: IRSM607-105MH
1.6) IR LOGO
1.7) MEDIUM:
1.7.1) TOP:LASER
1.7.2) BOTTOM: NONE

Typical Application Connection IRS808-105MH

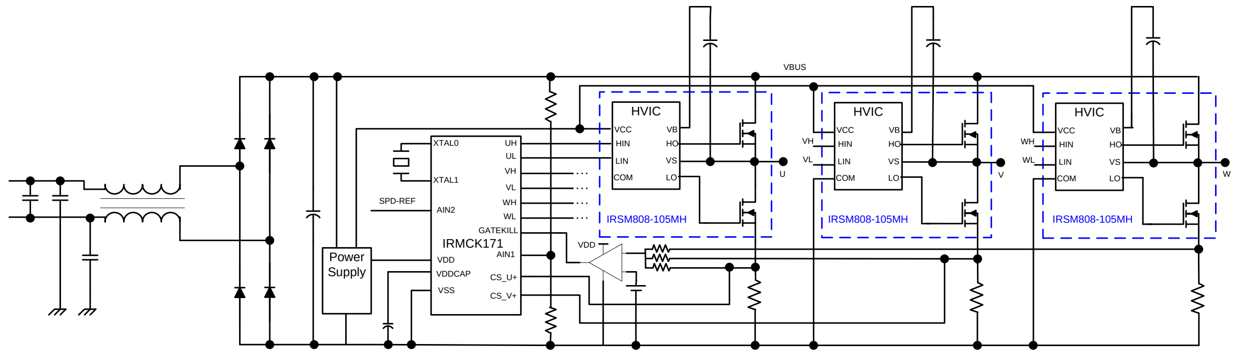


Figure 1: Typical Application Connection

1. Bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. In order to provide a good decoupling between VCC-VSS abd VB-VS terminals, the capaciotrs shown connected at these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1uF, are recommended.
3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR Design tip DT04-4 or application note AN-1044.

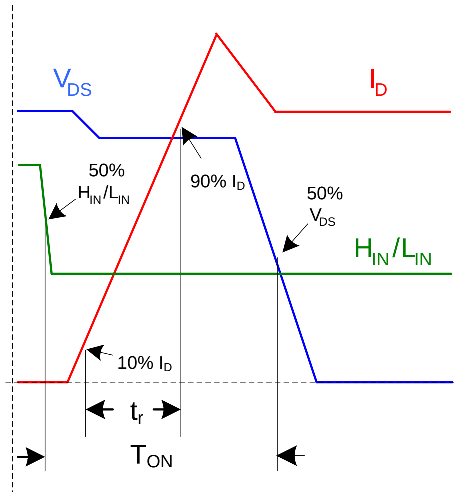


Figure 3a. Input to Output propagation turn-on delay time.

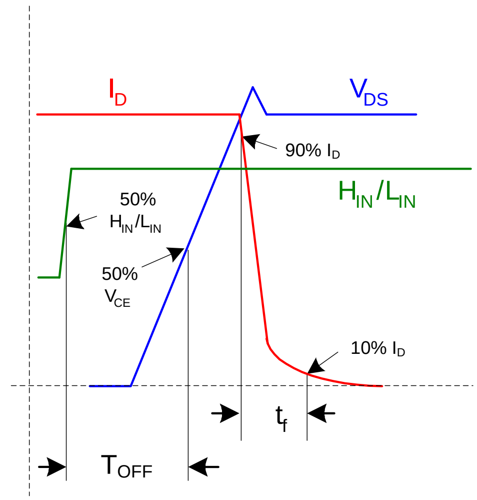


Figure 3b. Input to Output propagation turn-off delay time.

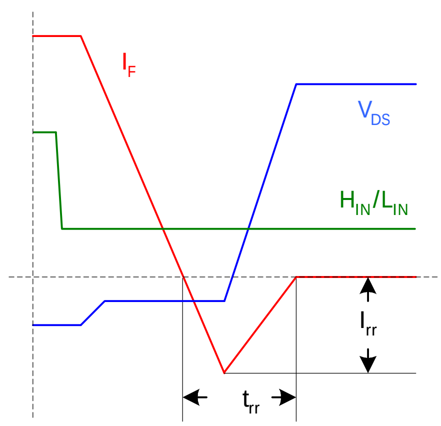


Figure 3c. Diode Reverse Recovery

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

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