

# Analog Multiplexers / Demultiplexers with LSTTL Compatible Inputs

## High-Performance Silicon-Gate CMOS



ON Semiconductor®

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### MC74HCT4051A, MC74HCT4052A, MC74HCT4053A

The MC74HCT4051A, MC74HCT4052A and MC74HCT4053A utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from  $V_{CC}$  to  $V_{EE}$ ).

The HCT4051A, HCT4052A and HCT4053A are identical in pinout to the metal-gate MC14051AB, MC14052AB and MC14053AB. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS and LSTTL outputs.

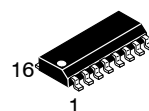
These devices have been designed so that the ON resistance ( $R_{on}$ ) is more linear over input voltage than  $R_{on}$  of metal-gate CMOS analog switches.

For a multiplexer/demultiplexer with injection current protection, see HC4851A and HCT4851A.

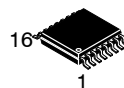
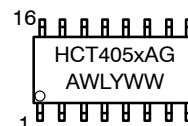
#### Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- In Compliance with the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: HCT4051A – 184 FETs or 46 Equivalent Gates  
HCT4052A – 168 FETs or 42 Equivalent Gates  
HCT4053A – 156 FETs or 39 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

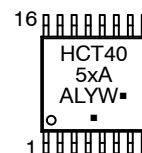
#### MARKING DIAGRAMS



SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



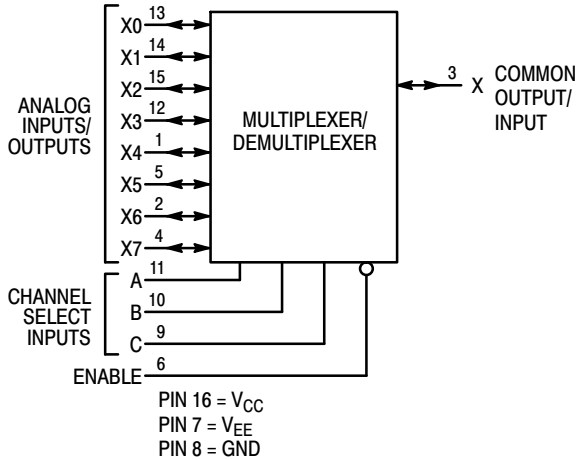
x = 1, 2, 3  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

# MC74HCT4051A, MC74HCT4052A, MC74HCT4053A

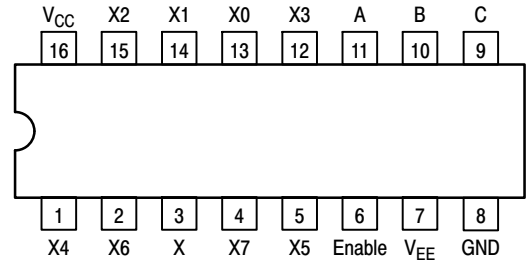


**Figure 1. Logic Diagram – MC74HCT4051A Single-Pole, 8-Position Plus Common Off**

**FUNCTION TABLE – MC74HCT4051A**

Control Inputs		ON Channels		
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

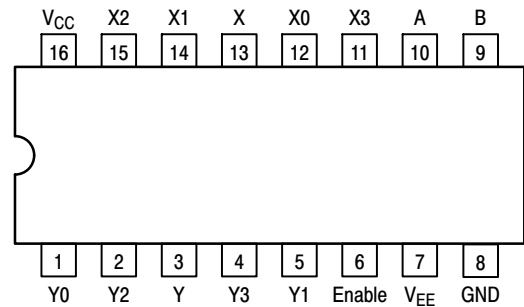


**Figure 2. Pinout: MC74HCT4051A (Top View)**

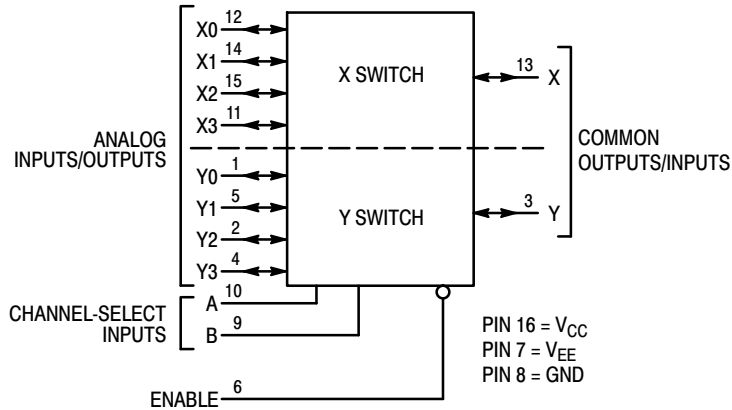
**FUNCTION TABLE – MC74HCT4052A**

Control Inputs		ON Channels	
Enable	Select		
	B	A	
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care



**Figure 4. Pinout: MC74HCT4052A (Top View)**



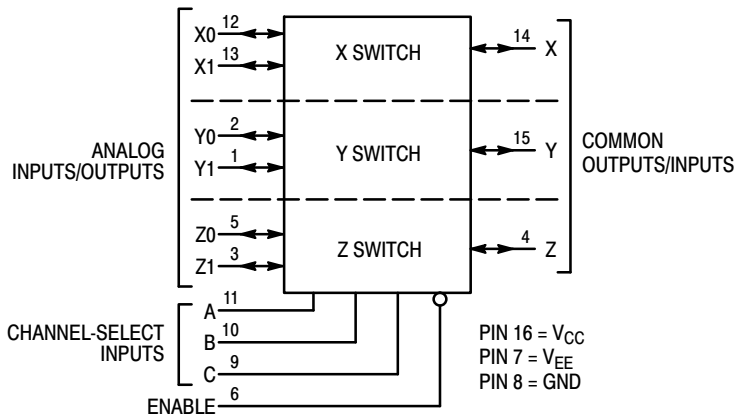
**Figure 3. Logic Diagram – MC74HCT4052A Double-Pole, 4-Position Plus Common Off**

# MC74HCT4051A, MC74HCT4052A, MC74HCT4053A

FUNCTION TABLE – MC74HCT4053A

Control Inputs				ON Channels		
Enable	Select					
	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care



NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

Figure 5. Logic Diagram – MC74HCT4053A Triple Single-Pole, Double-Position Plus Common Off

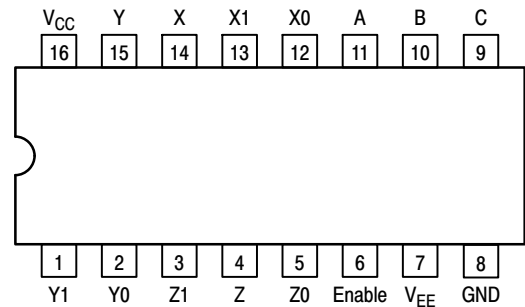


Figure 6. Pinout: MC74HCT4053A (Top View)

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND) (Referenced to $V_{EE}$ )	-0.5 to +7.0 -0.5 to +14.0	V
$V_{EE}$	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +5.0	V
$V_{IS}$	Analog Input Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
$V_{in}$	Digital Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I	DC Current, Into or Out of Any Pin	$\pm 25$	mA
$P_D$	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature Range	-65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating – SOIC Package: - 7 mW/°C from 65°C to 125°C  
TSSOP Package: - 6.1 mW/°C from 65°C to 125°C

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND) (Referenced to $V_{EE}$ )	2.0 2.0	6.0 12.0	V	
$V_{EE}$	Negative DC Supply Voltage, Output (Referenced to GND)	-6.0	GND	V	
$V_{IS}$	Analog Input Voltage	$V_{EE}$	$V_{CC}$	V	
$V_{in}$	Digital Input Voltage (Referenced to GND)	GND	$V_{CC}$	V	
$V_{IO}^*$	Static or Dynamic Voltage Across Switch		1.2	V	
$T_A$	Operating Temperature Range, All Package Types	-55	+125	°C	
$t_r, t_f$	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 0 0 0	1000 600 500 400	ns

\*For voltage drops across switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND) $V_{EE} = \text{GND}$ , Except Where Noted

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit	
				-55 to 25°C	≤85°C	≤125°C		
$V_{IH}$	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	4.5 to 5.5	2.0	2.0	2.0	V	
$V_{IL}$	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	4.5 to 5.5	0.8	0.8	0.8	V	
$I_{in}$	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0\text{ V}$	6.0	±0.1	±1.0	±1.0	μA	
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{IO} = 0\text{ V}$	$V_{EE} = \text{GND}$	6.0	1	10	20	μA
			$V_{EE} = -6.0$	6.0	4	40	80	

## DC CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	$V_{CC}$	$V_{EE}$	Guaranteed Limit			Unit			
					-55 to 25°C	≤85°C	≤125°C				
$R_{on}$	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IS} = V_{CC}$ to $V_{EE}$ ; $I_S \leq 2.0\text{ mA}$ (Figures 7, 8)	4.5	0.0	190	240	280	Ω			
			4.5	-4.5	120	150	170				
		6.0	-6.0	100	125	140					
		4.5	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IS} = V_{CC}$ or $V_{EE}$ (Endpoints); $I_S \leq 2.0\text{ mA}$ (Figures 7, 8)	0.0	150	190	230				
-4.5	100			125	140						
6.0			-6.0	80	100	115					
			$\Delta R_{on}$	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IS} = 1/2 (V_{CC} - V_{EE})$ ; $I_S \leq 2.0\text{ mA}$	4.5	0.0	30	35	40	Ω
						4.5	-4.5	12	15	18	
6.0	-6.0	10				12	14				
$I_{off}$	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IO} = V_{CC} - V_{EE}$ ; Switch Off (Figure 9)	5.0	-5.0	0.1	0.5	1.0	μA			
			Maximum Off-Channel Leakage Current, Common Channel	HCT4051A HCT4052A HCT4053A	$V_{in} = V_{IL}$ or $V_{IH}$ ; $V_{IO} = V_{CC} - V_{EE}$ ; Switch Off (Figure 10)	5.0	-5.0		0.2	2.0	4.0
	5.0	-5.0				0.1	1.0		2.0		
	5.0	-5.0				0.1	1.0		2.0		
$I_{on}$	Maximum On-Channel Leakage Current, Channel-to-Channel	HCT4051A HCT4052A HCT4053A	$V_{in} = V_{IL}$ or $V_{IH}$ ; Switch-to-Switch = $V_{CC} - V_{EE}$ ; (Figure 11)	5.0	-5.0	0.2	2.0	4.0	μA		
				5.0	-5.0	0.1	1.0	2.0			
				5.0	-5.0	0.1	1.0	2.0			
				5.0	-5.0	0.1	1.0	2.0			

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## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 15)	2.0	270	320	350	ns
		3.0	90	110	125	
		4.5	59	79	85	
		6.0	45	65	75	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figure 16)	2.0	40	60	70	ns
		3.0	25	30	32	
		4.5	12	15	18	
		6.0	10	13	15	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 17)	2.0	160	200	220	ns
		3.0	70	95	110	
		4.5	48	63	76	
		6.0	39	55	63	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Enable to Analog Output (Figure 17)	2.0	245	315	345	ns
		3.0	115	145	155	
		4.5	49	69	83	
		6.0	39	58	67	
C <sub>in</sub>	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
C <sub>I/O</sub>	Maximum Capacitance (All Switches Off)	Analog I/O	35	35	35	pF
		Common O/I: HCT4051A	130	130	130	
		HCT4052A	80	80	80	
		HCT4053A	50	50	50	
	Feed-through		1.0	1.0	1.0	

C <sub>PD</sub>	Power Dissipation Capacitance (Figure 19)*	HCT4051A HCT4052A HCT4053A	Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V			pF
			45			
			80			
			45			

\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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## ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V <sub>CC</sub> V	V <sub>EE</sub> V	Limit*			Unit
					25°C			
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 12)	f <sub>in</sub> = 1 MHz Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub> ; Increase f <sub>in</sub> Frequency Until dB Meter Reads -3 dB; R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25	'51	'52	'53	MHz
			4.50	-4.50	80	95	120	
			6.00	-6.00	80	95	120	
-	Off-Channel Feed-through Isolation (Figure 13)	f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF	2.25	-2.25	-50			dB
			4.50	-4.50	-50			
			6.00	-6.00	-50			
-	Feedthrough Noise. Channel-Select Input to Common I/O (Figure 14)	V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns); Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A; Enable = GND R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF	2.25	-2.25	25			mV <sub>PP</sub>
			4.50	-4.50	105			
			6.00	-6.00	135			
-	Crosstalk Between Any Two Switches (Figure 18) (Test does not apply to HCT4051A)	f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF	2.25	-2.25	-50			dB
			4.50	-4.50	-50			
			6.00	-6.00	-50			
-	Crosstalk Between Any Two Switches (Figure 18) (Test does not apply to HCT4051A)	f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	2.25	-2.25	-40			dB
			4.50	-4.50	-40			
			6.00	-6.00	-40			
THD	Total Harmonic Distortion (Figure 20)	f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF THD = THD <sub>measured</sub> - THD <sub>source</sub> V <sub>IS</sub> = 4.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 8.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 11.0 V <sub>PP</sub> sine wave	2.25	-2.25	0.10			%
			4.50	-4.50	0.08			
			6.00	-6.00	0.05			

\*Limits not tested. Determined by design and verified by qualification.

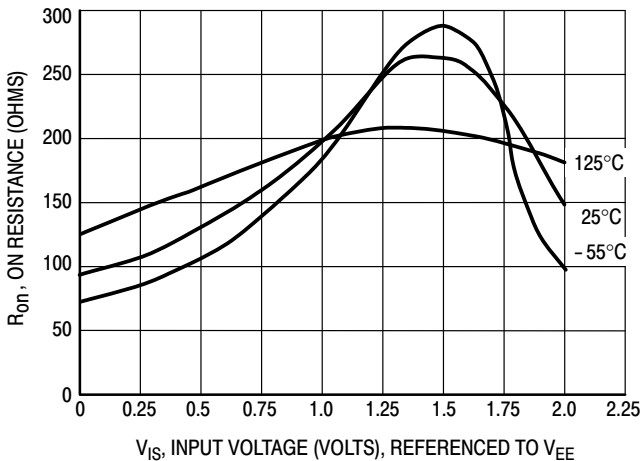


Figure 7a. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 2.0 V

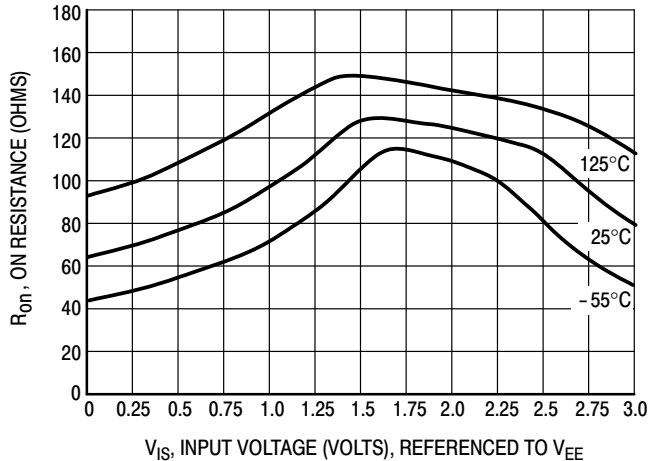


Figure 7b. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 3.0 V

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Figure 7c. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5 \text{ V}$



Figure 7d. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0 \text{ V}$

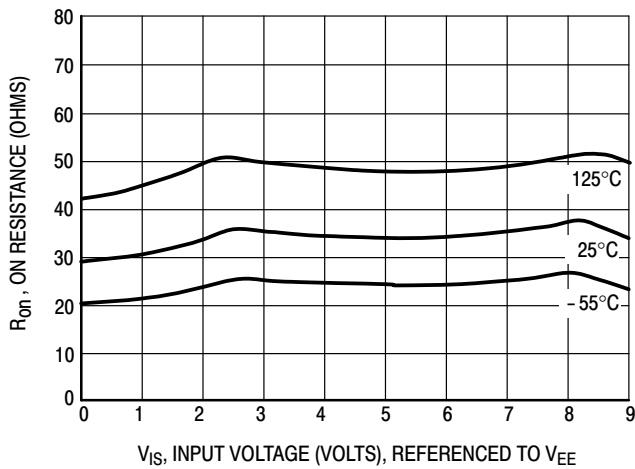


Figure 7e. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0 \text{ V}$

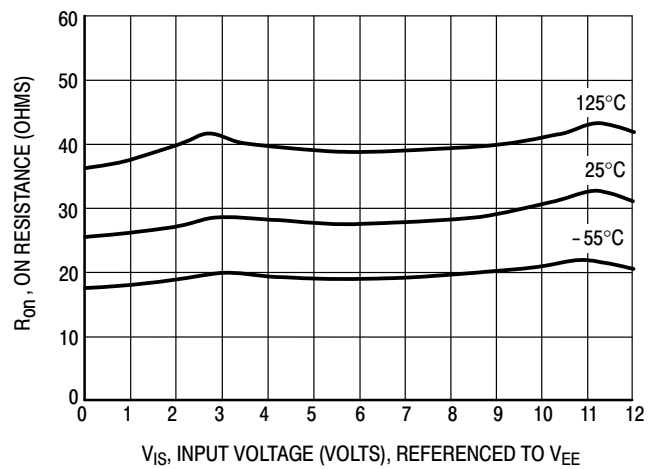


Figure 7f. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0 \text{ V}$

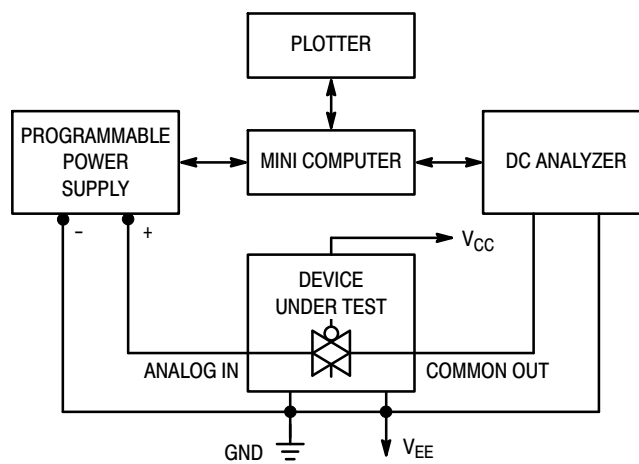
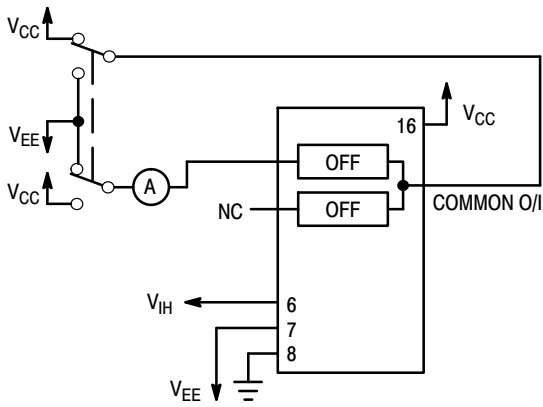


Figure 8. On Resistance Test Set-Up

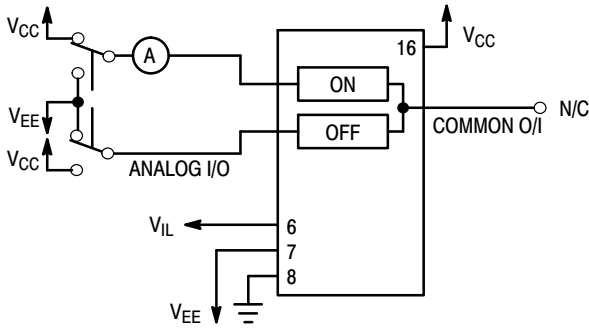
# MC74HCT4051A, MC74HCT4052A, MC74HCT4053A



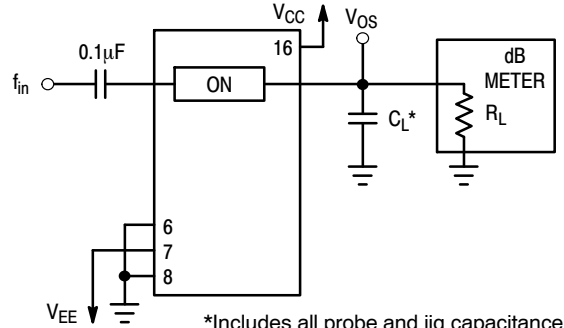
**Figure 9. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up**



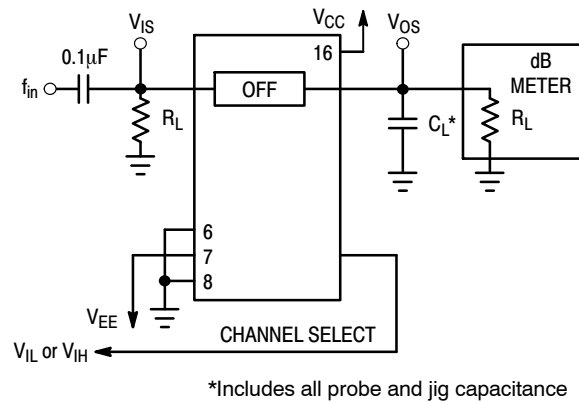
**Figure 10. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up**



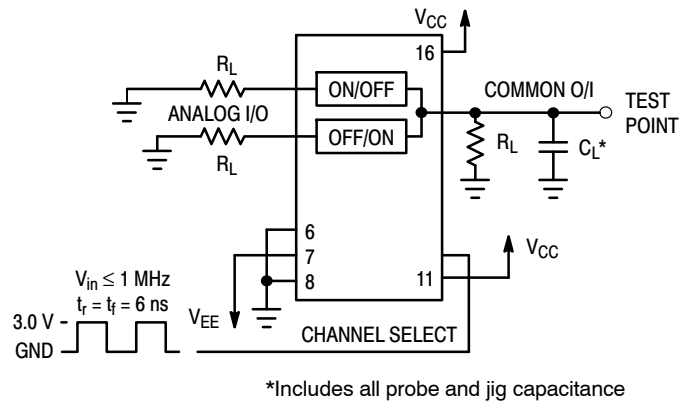
**Figure 11. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up**



**Figure 12. Maximum On Channel Bandwidth, Test Set-Up**



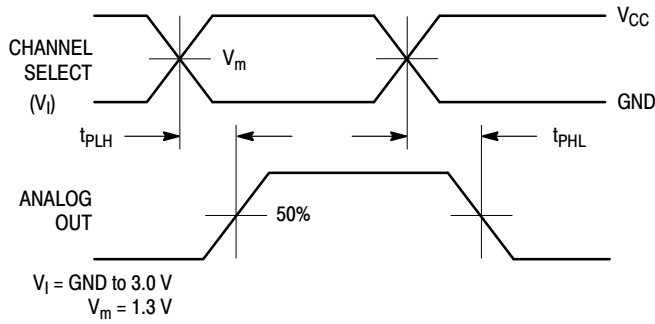
**Figure 13. Off Channel Feedthrough Isolation, Test Set-Up**



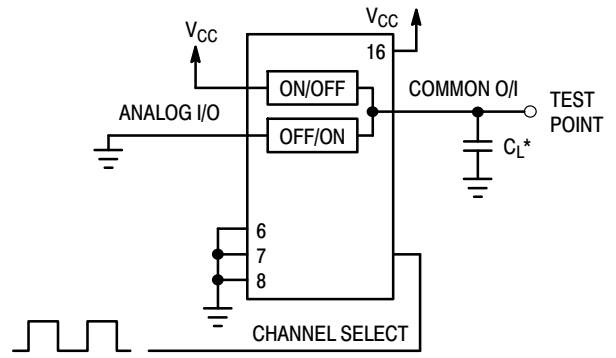
**Figure 14. Feedthrough Noise, Channel Select to Common Out, Test Set-Up**



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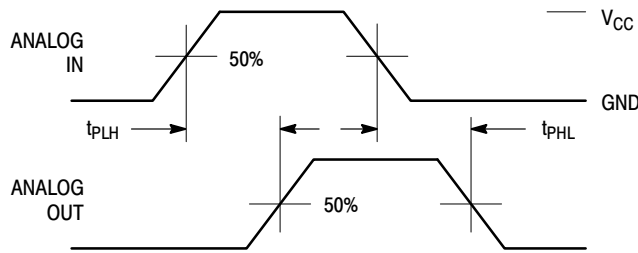


**Figure 15a. Propagation Delays, Channel Select to Analog Out**

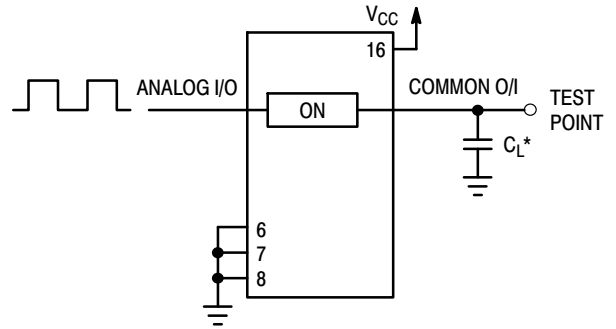


\*Includes all probe and jig capacitance

**Figure 15b. Propagation Delay, Test Set-Up Channel Select to Analog Out**

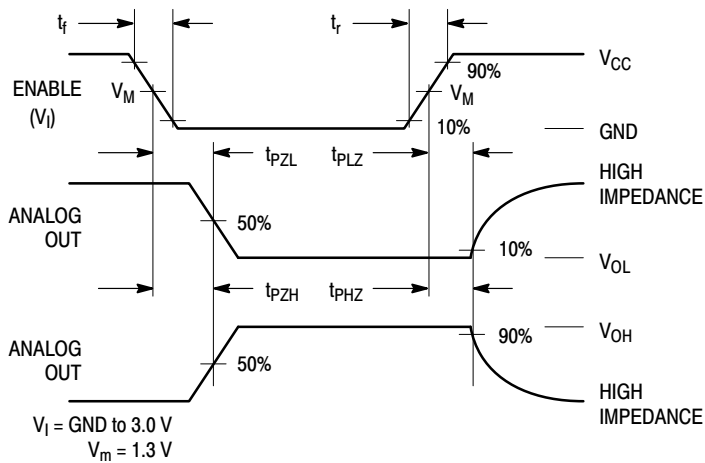


**Figure 16a. Propagation Delays, Analog In to Analog Out**

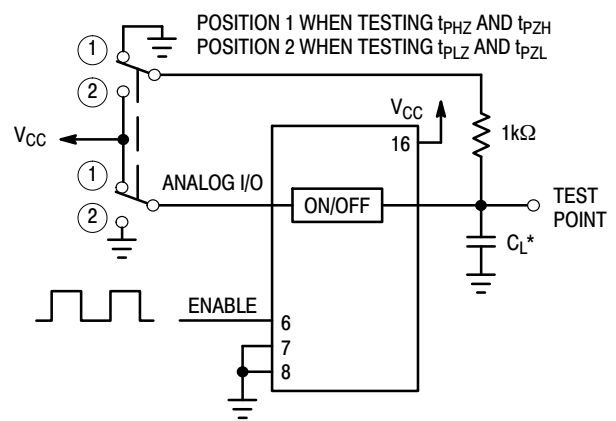


\*Includes all probe and jig capacitance

**Figure 16b. Propagation Delay, Test Set-Up Analog In to Analog Out**

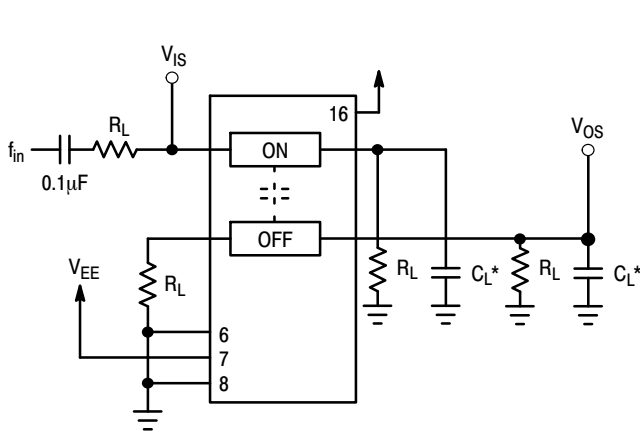


**Figure 17a. Propagation Delays, Enable to Analog Out**



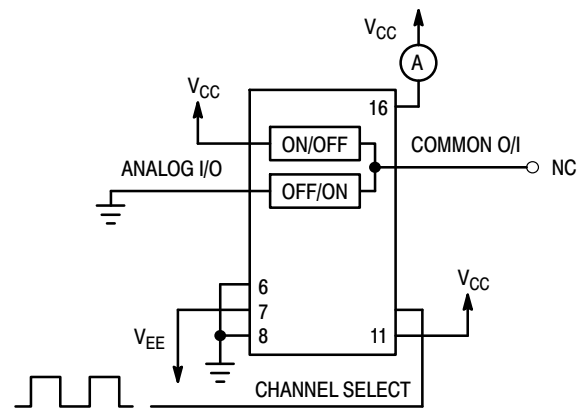
**Figure 17b. Propagation Delay, Test Set-Up Enable to Analog Out**

## MC74HCT4051A, MC74HCT4052A, MC74HCT4053A

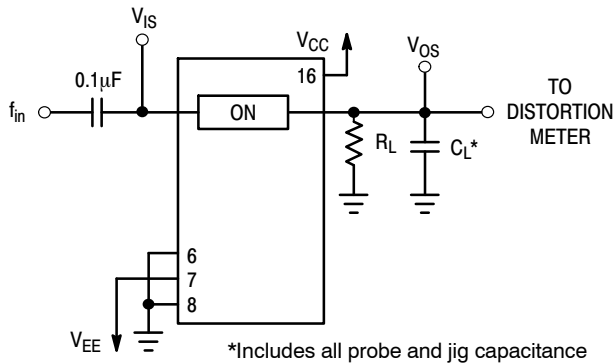


\*Includes all probe and jig capacitance

**Figure 18. Crosstalk Between Any Two Switches, Test Set-Up**

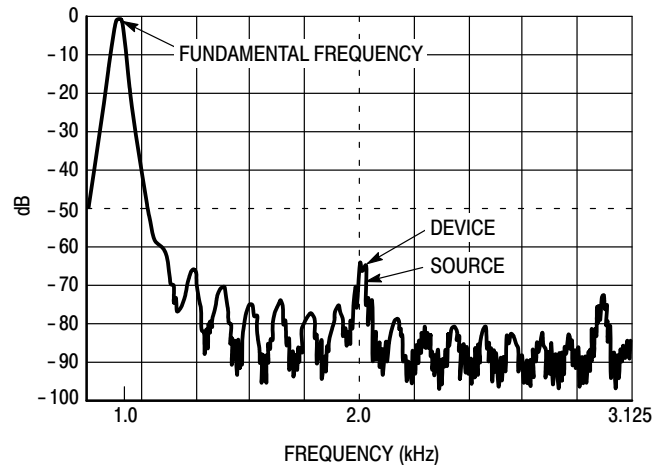


**Figure 19. Power Dissipation Capacitance, Test Set-Up**



\*Includes all probe and jig capacitance

**Figure 20a. Total Harmonic Distortion, Test Set-Up**



**Figure 20b. Plot, Harmonic Distortion**

### APPLICATIONS INFORMATION

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In this example, the difference between  $V_{CC}$  and  $V_{EE}$  is ten volts. Therefore, using the configuration of Figure 21, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor helps minimize crosstalk and feed-through noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ V} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ V} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ V} \\ &\text{and } V_{EE} \leq \text{GND} \end{aligned}$$

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external Germanium or Schottky diodes ( $D_x$ ) are recommended as shown in Figure 22. These diodes should be able to absorb the maximum anticipated current surges during clipping.

# MC74HCT4051A, MC74HCT4052A, MC74HCT4053A

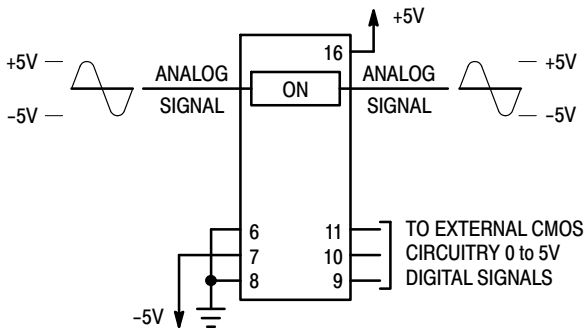
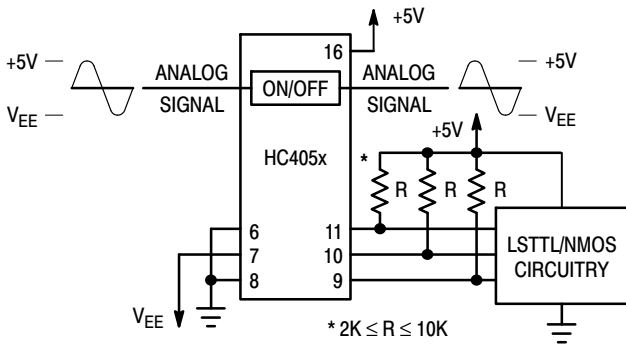


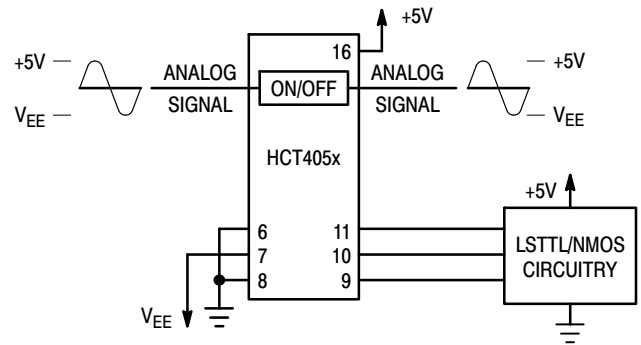
Figure 21. Application Example



Figure 22. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors with a HC Device



b. Using HCT Interface

Figure 23. Interfacing LSTTL/NMOS to CMOS Inputs

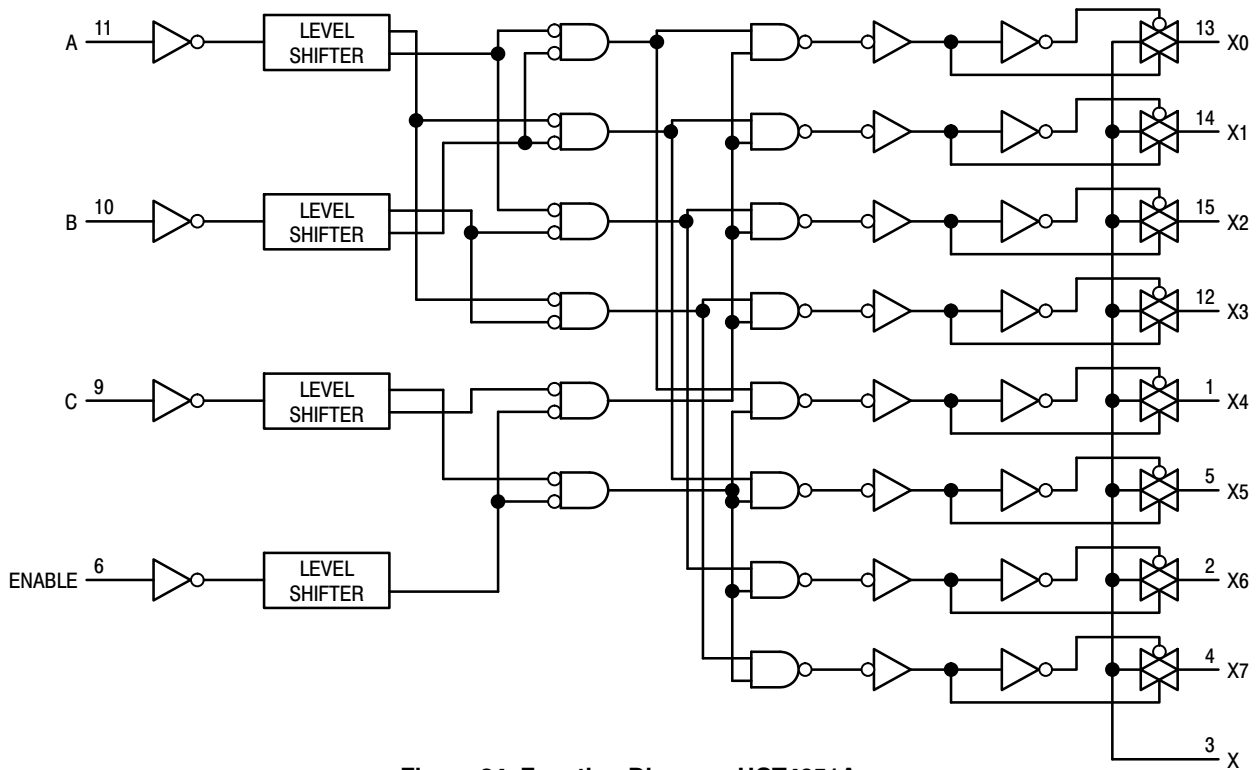
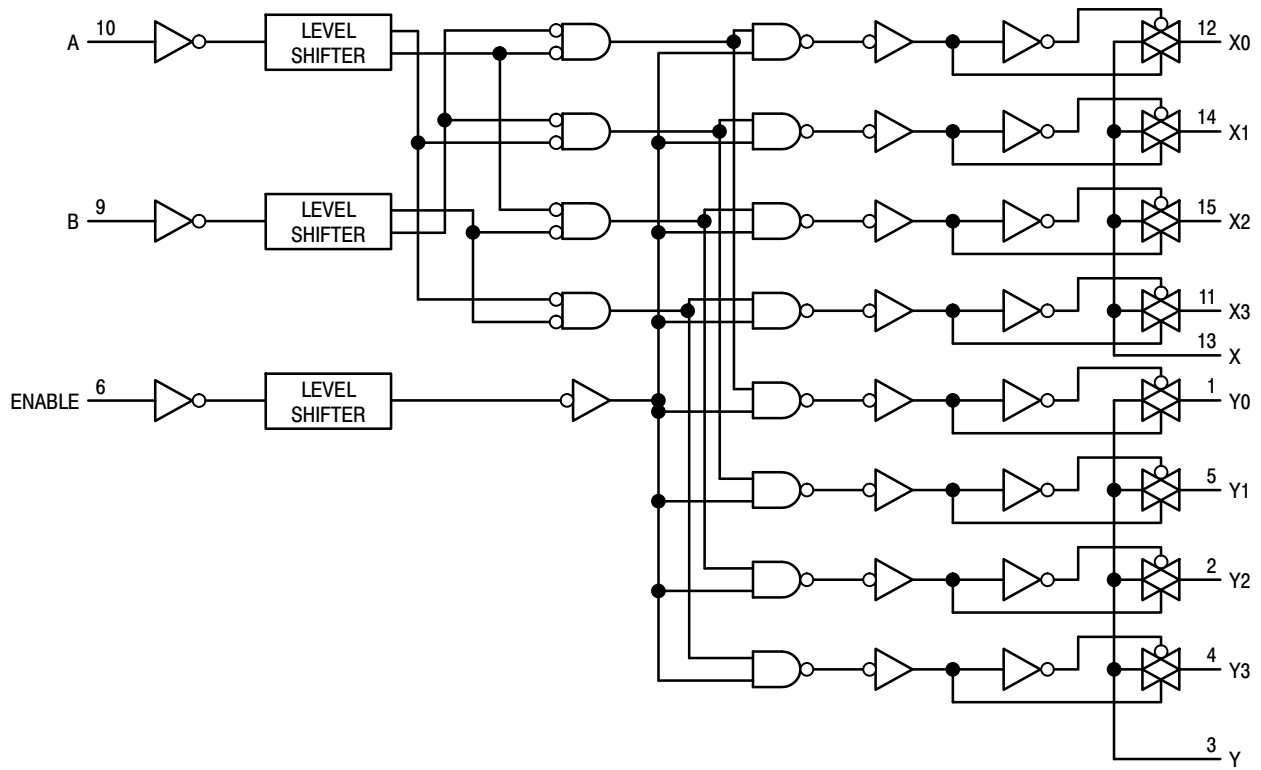
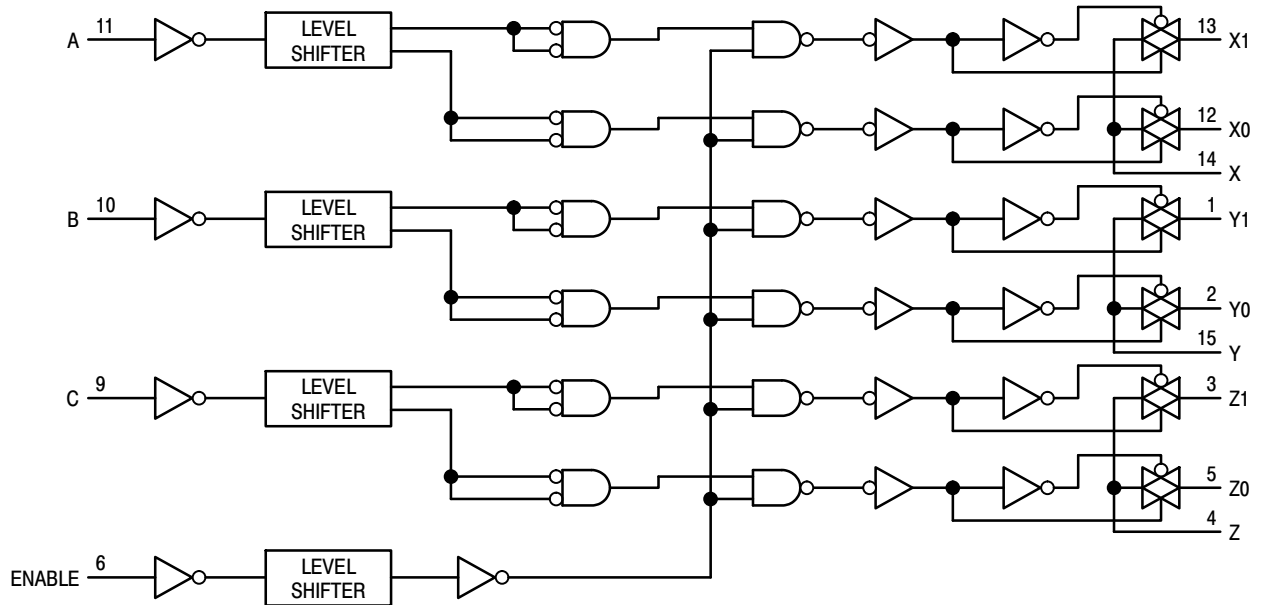


Figure 24. Function Diagram, HCT4051A

**MC74HCT4051A, MC74HCT4052A, MC74HCT4053A**



**Figure 26. Function Diagram, HCT4052A**



**Figure 25. Function Diagram, HCT4053A**

## MC74HCT4051A, MC74HCT4052A, MC74HCT4053A

### ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT4051ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HCT4051ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC74HCT4051ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
M74HCT4051ADTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLV74HCT4051ADTR2G*	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
MC74HCT4052ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
M74HCT4052ADTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
MC74HCT4053ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
M74HCT4053ADTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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