# ASNT8172-KMF
2V Driver with Asynchronous Finite Impulse Response Filter

- DC to $10GHz$ 9-tap finite impulse response filter (FIR)

- One differential digital CML input port

- One differential analog output port

- 6-bit tap gain and tap peaking controls

- 3-bit additional gain control for initial FIR calibration using a tap replica

- 4-bit output buffer gain and 6-bit output buffer peaking controls

- 3-wire SPI for loading all control values

- Three positive power supplies

- Maximum power consumption: 1.24W
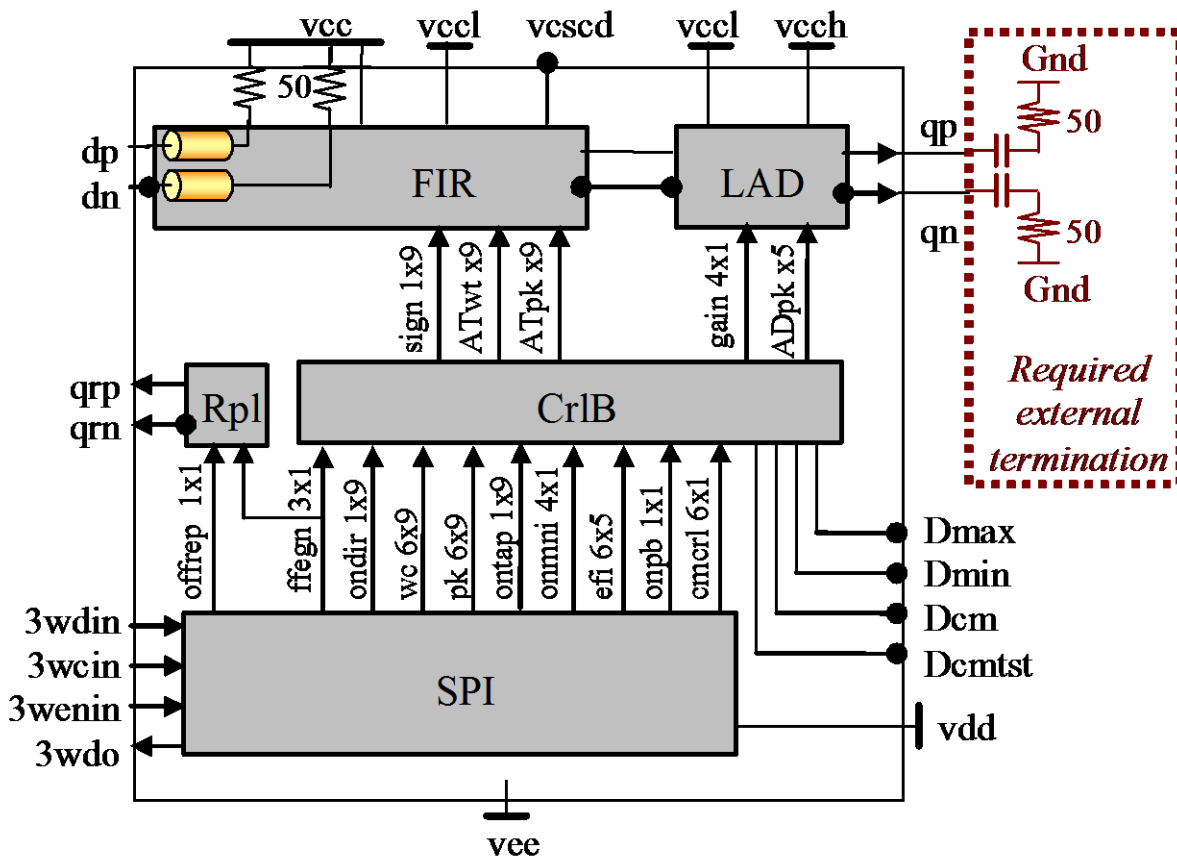
- Custom CQFP 64-pin package
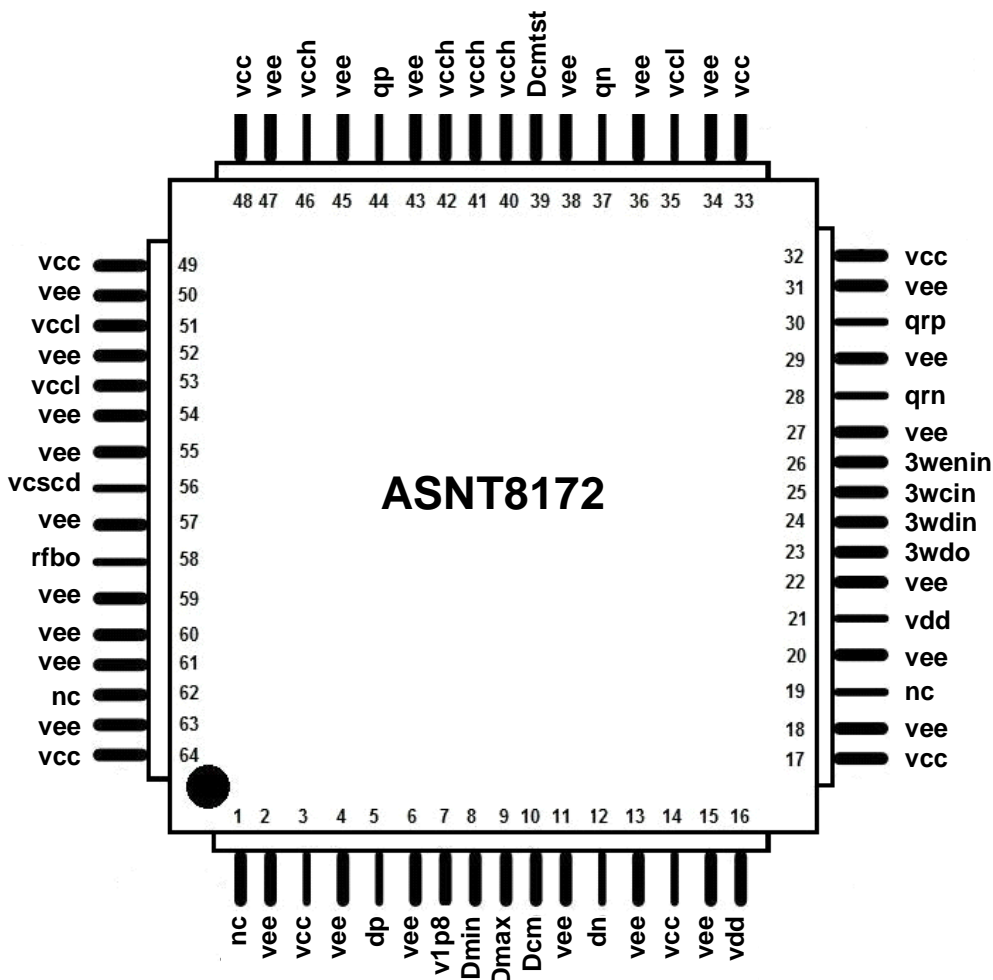
DESCRIPTION

Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 is a differential driver with an externally controlled 9-tap pre-emphasis. It receives a high-speed binary data signal through its differential input port dp/dn. The FIR block processes the input signal in accordance with nine pre-defined filter coefficients to perform the pre-emphasis operation. The resulting analog signal is amplified by a linear amplifier-driver LAD, and delivered to the output linear differential port outp/outn that operates in ECL-type mode and requires external $50 Ohm$ AC terminations. If DC terminations are desired, a special external resistor network should be designed.

All chip functions are controlled through a 3-wire serial-to-parallel interface (SPI) that operates in combination with an internal control block CrlB.

The chip includes a 1-tap replica Rpl that can be independently enabled and used for initial gain calibration as described below.

FIR

The FIR block includes 8 dual transmission lines for direct and inverted input data signals with a single-ended impedance of $50 Ohm$ and matching internal terminations to vcc at their ends. Signals from all 9 nodes are processed by tap buffers to deliver 9 delayed copies of the differential input signal with controlled signs and weights to a summation point. The signs and weights are defined by internal binary signals sign and analog signals ATwt respectively. In addition, frequency response (peaking) of each tap can be adjusted using internal

analog signals ATpk. The weight of any tap #X can be reduced to exact 0 by a 1-bit digital signal ontapX="0", or can be controlled normally with ontapX="1" as described below in CrlB.

FIR requires initial calibration after which it delivers an optimal signal to its output. The calibration is performed using a replica block (Rpl) that is described below.

LAD

LAD amplifies the analog signal from FIR, and delivers it to the differential output port outp/outn. This port operates in ECL-type mode as a current source/sink and requires external $50 Ohm$ AC terminations. A DC termination scheme is also possible but requires an external resistor network.

The gain and frequency response (peaking) of LAD can be adjusted using internal 4-bit binary signal gain, and six analog signals ADpk respectively. The LAD's internal buffer with the gain adjust functionality includes a cascode stage for better performance. The reference voltage for the cascode stage can be monitored and adjusted through a control port vcscd to achieve the best output signal.

CrlB

This control block converts binary signals from SPI into binary, and analog control signals delivered to FIR, LAD, and Rpl.

There are 45 input binary signals to CrlB from SPI, 10 output binary signals, and 23 output analog signals from CrlB. Their logic relations are detailed in Table 1.

Table 1. Control Signals

Output	To	Bits	Signals	Input 1	Bits	Operation	Input 2	Bits	Operation	Input 3	Bits
signX	FIR	1	9	ondirX	1						
ATwtX	FIR	-	9	wcX	6	**AND**	ontapX	1	**AND**	ffegn	3
ATpkX	FIR	-	9	pkX	6	**AND**	ontapX	1	**AND**	ffegn	3
gain	LAD	4	1	onmni	4	**AND**	onpb	1			
ADpkX	LAD	-	5	efi	6						
Internal DAC threshold adjustment				cmcrl	6						

The value of ondirX="1" corresponds to a positive gain of tap #X. The minimum value of wcX=0 corresponds to a tap #X gain close to 0. The exact 0 gain value for the tap #X is achieved in case of ontapX="0". The maximum value of wcX=63 corresponds to the nominal gain of tap #X specified in ELECTRICAL CHARACTERISTICS. The initial calibration of this nominal gain should be performed as described in Rpl. The maximum value of pkX=63 corresponds to maximum bandwidth (and peaking) in the tap #X.

The minimum value of onmni=0 corresponds to a LAD gain close to 0. The exact 0 gain value for LAD is achieved in case of onpb="0". The maximum value of onmni=7 corresponds to the highest gain of LAD. The optimal value of LAD gain depends on the fabrication process variations, and should be defined by the nominal output swing specified in ELECTRICAL CHARACTERISTICS. The maximum value of efi=63 corresponds to maximum bandwidth (and peaking) in LAD.

LAD also provides signals to 4 external analog ports for monitoring of its internal DAC operation as shown in Table 2.

Table 2. DAC Monitoring Signals

Output signal	Function	Input signal
Dmax	Maximum DAC output signal	Constant 111111 DAC input
Dmin	Minimum DAC output signal	Constant 000000 DAC input
Dcm	DAC threshold	cmcrl
Dcmtst	DAC threshold before downshift	cmcrl

The values of Dmax and Dmin must be within the ranges specified in ELECTRICAL CHARACTERISTICS. The value of Dcm should be equal to (Dmux+Dmin)/2. Dcm is a downshifted copy of Dcmtst, and both values can be adjusted by a 6-bit signal cmcrl delivered through SPI. This adjustment of internal DAC thresholds is required for the correct generation of internal differential control signals.

Rpl

The tap replica Rpl can be used for initial tap gain calibration to ensure the optimal maximum data signal swing at the FIR output over process variations.

Rpl is an exact copy of one tap operating at its maximum weight. In the optimal state, it should generate a predefined DC voltage difference between its outputs qrp and qrn. This difference may be adjusted using the 3-bit binary signal ffegn. The same signal is used to adjust the ATwtX and ATpkX analog signals applied to actual taps as shown in Table 1. Rpl is used for initial calibration only, and can be completely disabled by the binary signal offrep="1".

SPI

3-wire SPI operates in slave mode and accepts three CMOS signals: 3wenin (SSn), 3wcin (SCLK), and 3wdin (MOSI) as described in ELECTRICAL CHARACTERISTICS. Additional CMOS data output 3wdo (MISO) is provided for control purposes.

SPI converts 25 input serial bytes into 45 parallel binary control signals delivered to CrlB, and one binary signal to Rpl. The input package description is presented in Table 3.

Table 3. Control Bytes

Byte No.	Signal 1 Name	Bit #	Signal 2 Name	Bit#	Signal 3 Name	Bit#	Byte No.	Signal 1 Name	Bit #	Signal 2 Name	Bit#	Signal 3 Name	Bit#
1	ontap1	7	ondir1	6	wc1	5-0	14	pk7	7-2	*empty*	1	*empty*	0
2	pk1	7-2	*empty*	1	*empty*	0	15	ontap8	7	ondir8	6	wc8	5-0
3	ontap2	7	ondir2	6	wc2	5-0	16	pk8	7-2	*empty*	1	*empty*	0
4	pk2	7-2	*empty*	1	*empty*	0	17	ontap9	7	ondir9	6	wc9	5-0
5	ontap3	7	ondir3	6	wc3	5-0	18	pk9	7-2	*empty*	1	*empty*	0
6	pk3	7-2	*empty*	1	*empty*	0	19	efi0	7-2	*empty*	1	*empty*	0
7	ontap4	7	ondir4	6	wc4	5-0	20	efi1	7-2	*empty*	1	*empty*	0
8	pk4	7-2	*empty*	1	*empty*	0	21	efi2	7-2	*empty*	1	*empty*	0
9	ontap5	7	ondir5	6	wc5	5-0	22	efi3	7-2	*empty*	1	*empty*	0
10	pk5	7-2	*empty*	1	*empty*	0	23	efi4	7-2	*empty*	1	*empty*	0
11	ontap6	7	ondir6	6	wc6	5-0	24	cmcrl	7-2	offrep	1	*empty*	0
12	pk6	7-2	*empty*	1	*empty*	0	25	ffegn	7-5	onpb	4	onmni	3-0
13	ontap7	7	ondir7	6	wc7	5-0							

The bytes are delivered starting from 1 to 25 and bits within a byte are delivered starting from MSB. Bit#7 is the MSB of a byte as shown in Fig. 2. Internal registers are updated at a rising edge of 3wenin.
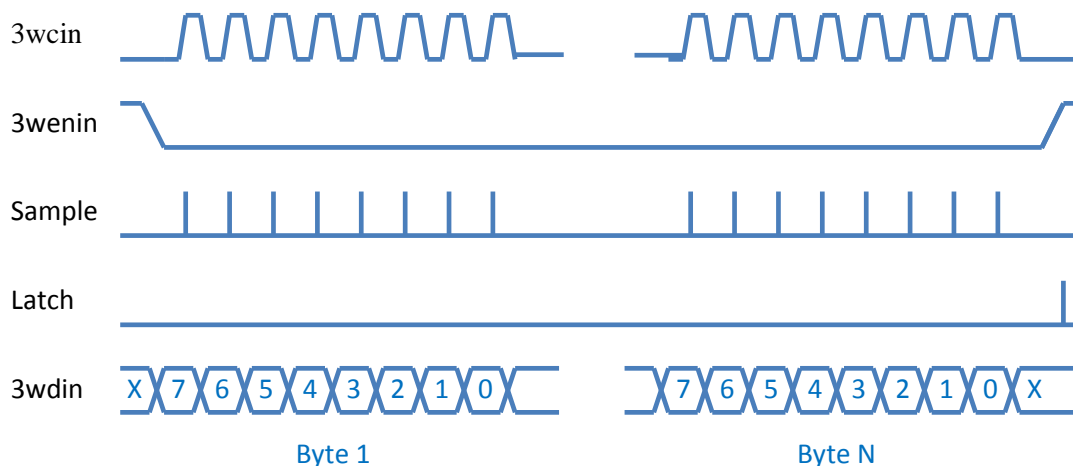

Fig. 2. SPI Operation

The FIR block is designed in such a way that it requires normalization of tap gains. Assuming that wc$_{MAX}$ equals 63 (or 111111 in binary code), the tap weight control binary signals wcX supplied to the SPI should be softly normalized to satisfy the equation $\sum_{i=1}^{9} |wc(i)| \leq wc_{MAX}$.

POWER SUPPLY CONFIGURATION

The IC requires four positive external power supplies. The first supply vcc is used for the data input terminations, and to power all high-speed digital circuitry and reference sources. The second supply vccl powers the internal analog circuitry. The third supply vcch is used for the output analog driver. The digital supply vdd is used for the internal CMOS circuits of the SPI.

All supplies are positive in relation to the internal common node vee=0.0*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltages (vcc, vccl, vcch, vdd)		3.0, 4.0, 8.0, 1.5	*V*
Power Consumption		1.5	*W*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			Description
Name	**No.**	**Type**	
High-Speed I/Os			
dp	5	CML-type input	Differential high-speed data inputs with internal SE $50Ohm$ terminations to vcc
dn	12		
qp	44	ECL-type output	Differential high-speed data outputs; require external SE $50Ohm$ AC terminations
qn	37		
Low-Speed I/Os			
3wenin	26	$1.2V$ CMOS input	Enable input signal SSn for 3-wire interface
3wcin	25		Clock input signal SCLK for 3-wire interface
3wdin	24		Data input signal MOSI for 3-wire interface
3wdo	23	$1.2V$ CMOS output	Data output signal MISO for 3-wire interface
Analog Control Voltages			
v1p8	7	Internal voltage generator output	Internal voltage source of vee+$1.8V$
vcscd	56		Internal voltage source of vcch-$4.0V$
rfbo	58		Internal voltage reference node
Analog Control Nodes (for DMM measurements only!)			
Dmin	8	Analog DC output	DAC minimum output indicator
Dmax	9		DAC maximum output indicator
Dcm	10		DAC common-mode output indicator
Dcmtst	39		DAC control output with internal $12.4Ohm$ termination to vcc
qrp	30		Replica differential data outputs with internal SE $42Ohm$ terminations to vccl
qrn	28		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vee	External ground	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 50, 52, 54, 55, 57, 59, 60, 61, 63
vcc	Positive power supply (HS digital part)	3, 14, 17, 32, 33, 48, 49, 64
vccl	Positive power supply (analog part)	35, 51, 53
vcch	Positive power supply (output driver)	40-42, 46
vdd	Positive power supply (digital control part)	16, 21
nc	not connected pins	1, 19, 62

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc		2.6		*V*	High-speed digital supply
vccl		3.5		*V*	Analog supply
vcch		7.5		*V*	Analog supply
vdd		1.2		*V*	CMOS digital supply
vee		0.0		*V*	External ground
*I*vcc		43		*mA*	
*I*vccl		40		*mA*	
*I*vcch		132		*mA*	
Power consumption		1.24		*W*	
Junction temperature	-25	50	125	*°C*	
FIR Parameters					
No. of Taps		9			
Delay between Taps		11		*ps*	
Voltage gain		3.5		*dB*	From chip input to FIR output, can be verified by Rpl measurements
High Speed Input Data (dp/dn)					
Data Rate	DC		20	*Gb/s*	
Swing		220		*mV*	Differential or SE, p-p
S11		TBD		*dB*	
CM Voltage Level		vcc		*V*	Must match for both inputs
Analog Output Data (qp/qn)					
Bandwidth	DC		10	*GHz*	
Swing		1200		*mV*	on each SE output
S22		TBD		*dB*	
CM Voltage Level		2.4		*V*	
DC Control Voltages					
v1p8	vee+1.85		vee+1.75	*V*	
vcscd	vcch-4.1		vcch-3.9	*V*	
qrp-qrn		330		*mV*	with optimal ffegn
Dmax	vcc-0.9		vcc-0.7	*V*	Should be always
Dmin	vcc-1.3		vcc-1.1	*V*	Dmax-Dmin=0.4±0.05
Dcm	vcc-1.1		vcc-0.9	*V*	Should be Dcm=(Dmux+Dmin)/2
Dcmtst	vcc-0.25		vcc-0.15	*V*	
3-Wire Interface Ports					
Clock frequency			6	*MHz*	
Low logic level		0		*V*	
High logic level		1.2		*V*	

ADSANTEC

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

Ultra High-Speed Mixed Signal ASICs

PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the **vee** plain, which is ground for a positive supply.

The part's identification label is ASNT8172-KMF. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

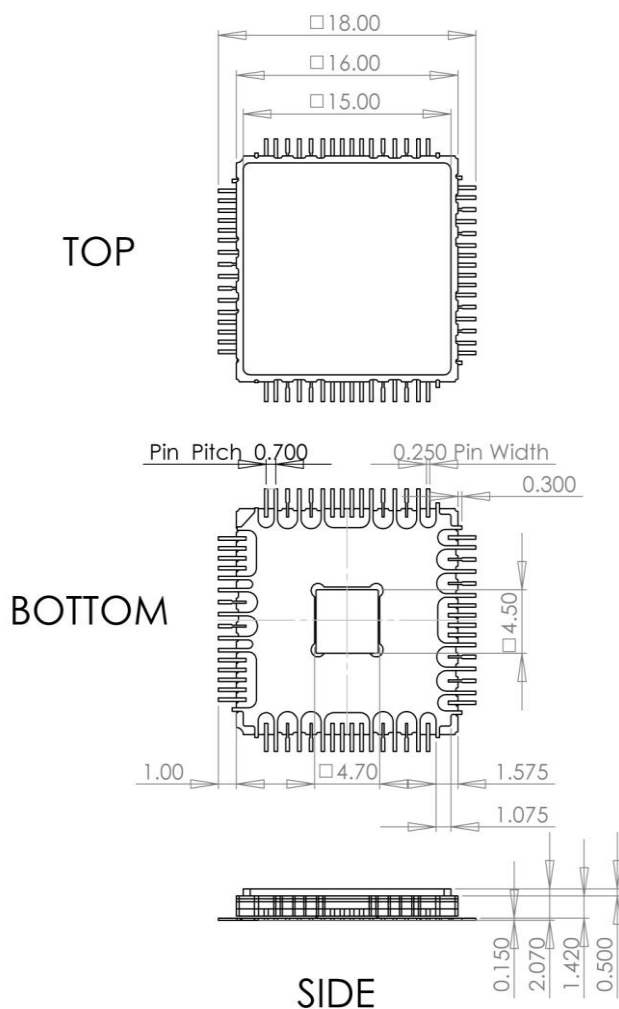*Fig. 3. CQFP 64-Pin Package Drawing (All Dimensions in mm)*

REVISION HISTORY

Revision	Date	Changes
1.2.2	05-2020	Updated Package Information
1.1.2	07-2019	Updated Letterhead
1.1.1	08-2017	Corrected terminal functions section Corrected electrical characteristics section Corrected package information section
1.0.1	05-2017	Initial Release